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(19) **United States**
(12) **Reissued Patent**
Mizuno et al.

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(45) **Date of Reissued Patent: Feb. 18, 2003**

(54) **MANUFACTURING METHOD OR AN EXPOSING METHOD FOR A SEMICONDUCTOR DEVICE OR A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND A MASK USED THEREFOR**

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(73) Assignees: **Hitachi, Ltd.**, Tokyo (JP); **Hitachi VLSI Engineering Corp.**, Kodaira (JP)

(21) Appl. No.: **09/544,634**

(22) Filed: **Apr. 6, 2000**

Related U.S. Patent Documents

Reissue of:
(64) Patent No.: **5,736,300**
Issued: **Apr. 7, 1998**
Appl. No.: **08/694,263**
Filed: **Aug. 8, 1996**

U.S. Applications:
(63) Continuation of application No. 08/443,431, filed on May 18, 1995, now Pat. No. 5,578,422, which is a continuation of application No. 07/912,511, filed on Jul. 13, 1992, now Pat. No. 5,436,095.

(30) **Foreign Application Priority Data**

Jul. 13, 1991 (JP) 3-170946

(51) **Int. Cl.**[7] **G03C 5/00**
(52) **U.S. Cl.** **430/313**; 430/311; 430/315
(58) **Field of Search** 430/311, 313, 430/315

(56) **References Cited**

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Primary Examiner—S. Rosasco
(74) *Attorney, Agent, or Firm*—Antonelli, Terry, Stout & Kraus, LLP

(57) **ABSTRACT**

One object of the present invention is to provide the reduced projection exposure method which enables the exposure of various and fine patterns in manufacturing process of semiconductor devices or semiconductor integrated circuit devices. Structure of the present invention to attain the above object is to carry out the reduced projection exposure using a phase shift mask provided with a prescribed correction pattern on the end of the mask pattern domain of a constant mode or the boundary of the mask pattern domain of plural modes. According to this structure, as the end effects etc. are canceled by the correction pattern, the various and fine patterns can be exposed.

34 Claims, 47 Drawing Sheets

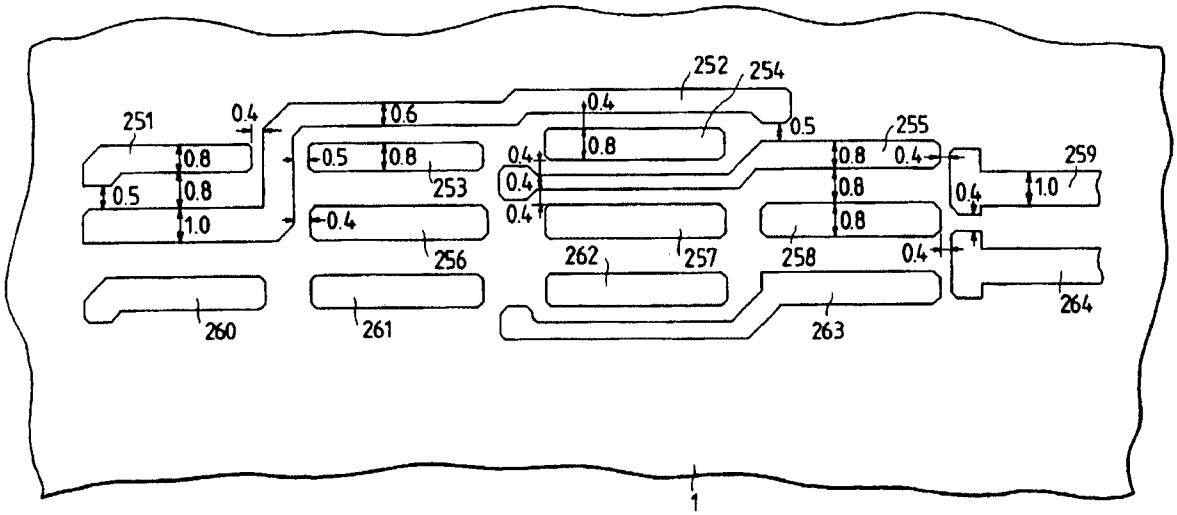


FIG. 1

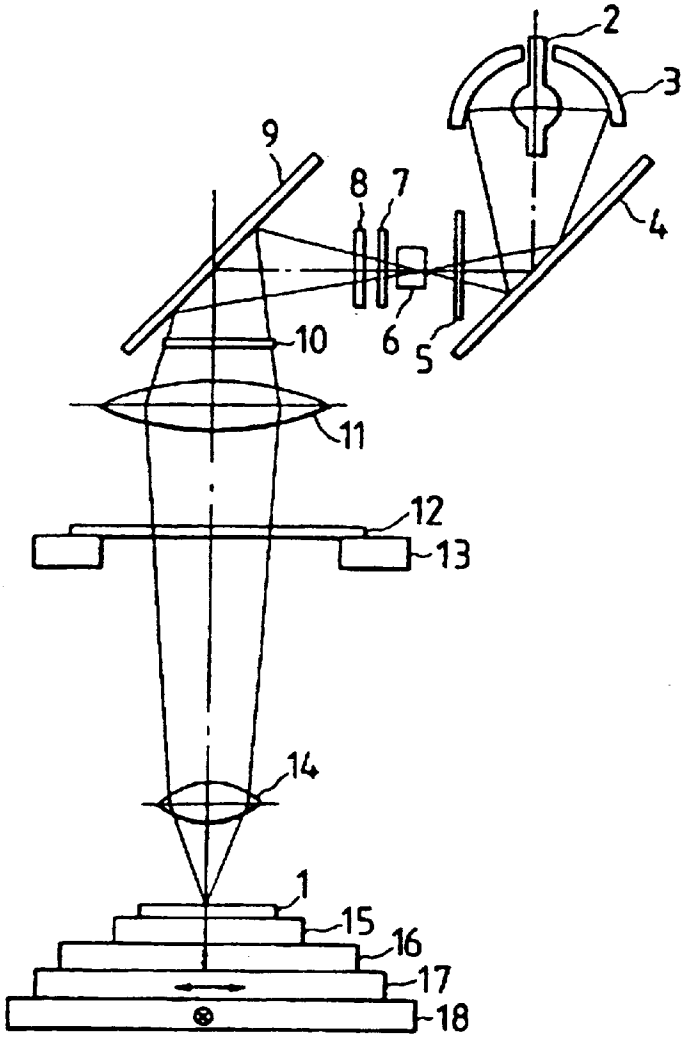


FIG. 2

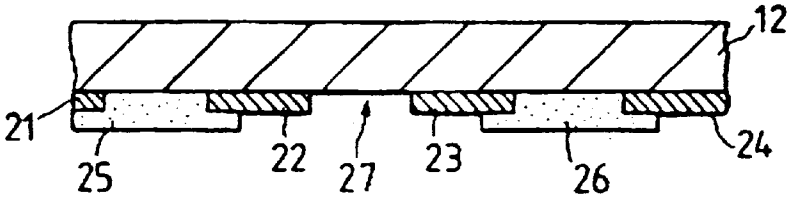


FIG. 3

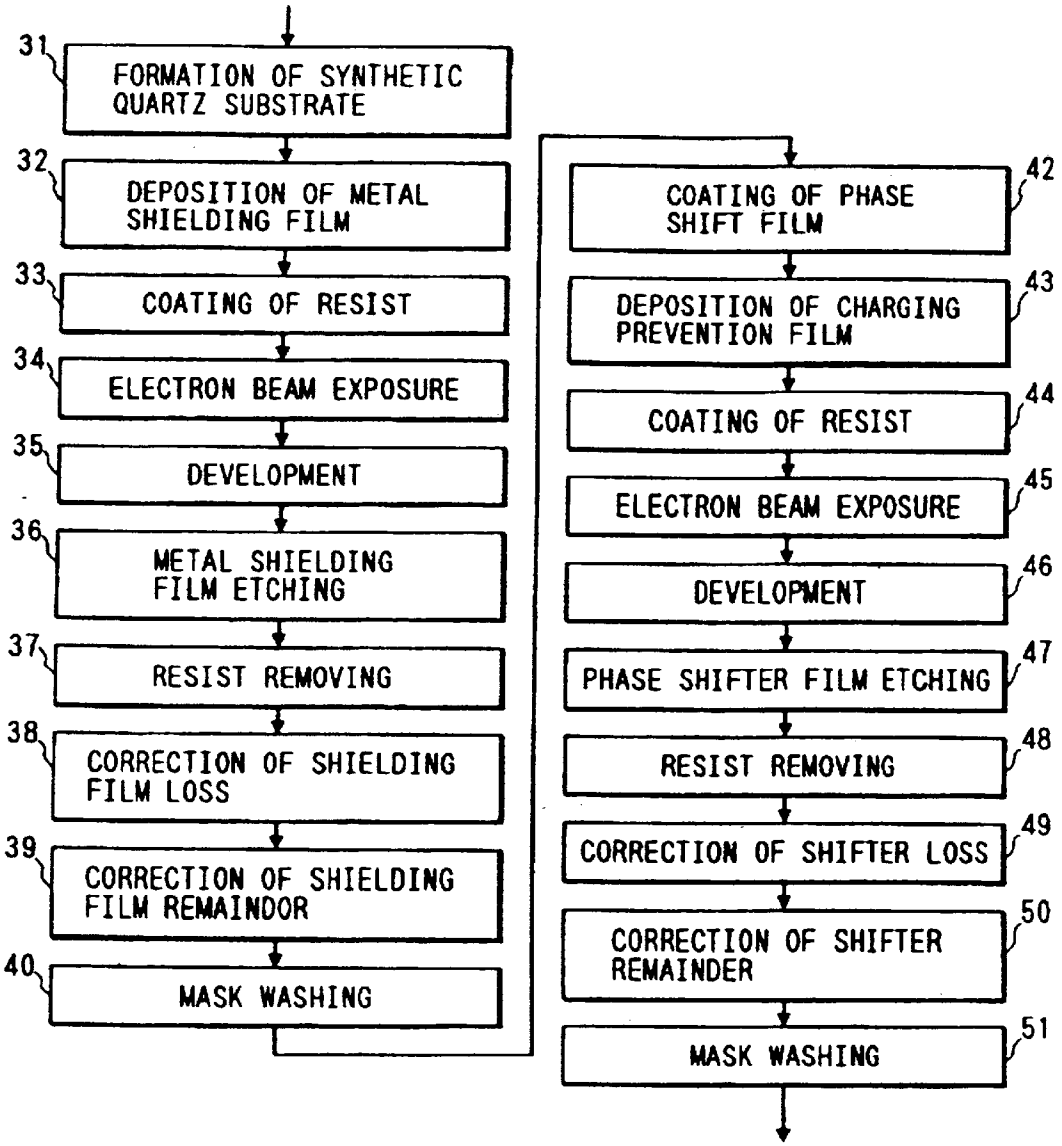

31
FORMATION OF SYNTHETIC QUARTZ SUBSTRATE
32
DEPOSITION OF METAL SHIELDING FILM
33
COATING OF RESIST
34
ELECTRON BEAM EXPOSURE
35
DEVELOPMENT
36
METAL SHIELDING FILM ETCHING
37
RESIST REMOVING
38
CORRECTION OF SHIELDING FILM LOSS
39
CORRECTION OF SHIELDING FILM REMAINDOR
40
MASK WASHING
42
COATING OF PHASE SHIFT FILM
43
DEPOSITION OF CHARGING PREVENTION FILM
44
COATING OF RESIST
45
ELECTRON BEAM EXPOSURE
46
DEVELOPMENT
47
PHASE SHIFTER FILM ETCHING
48
RESIST REMOVING
49
CORRECTION OF SHIFTER LOSS
50
CORRECTION OF SHIFTER REMAINDER
51
MASK WASHING

FIG. 4

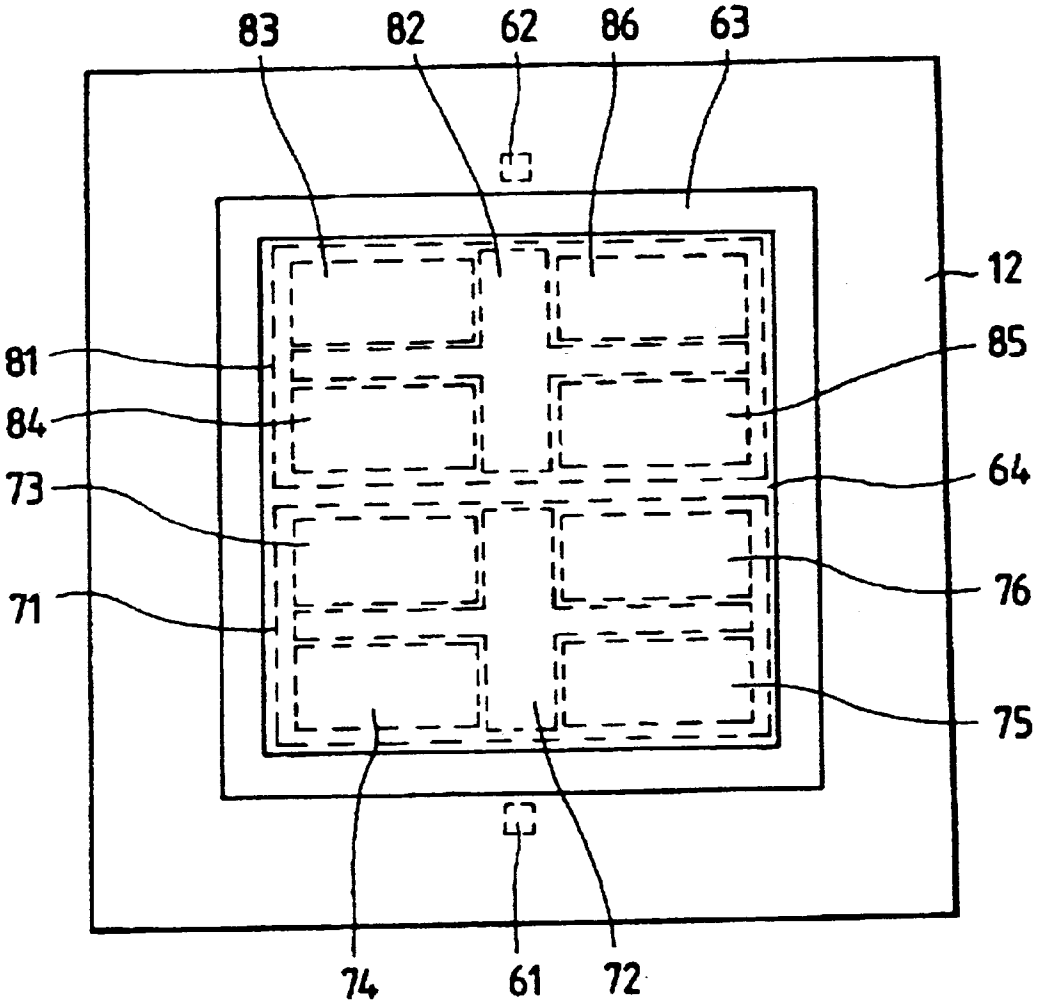


FIG. 6

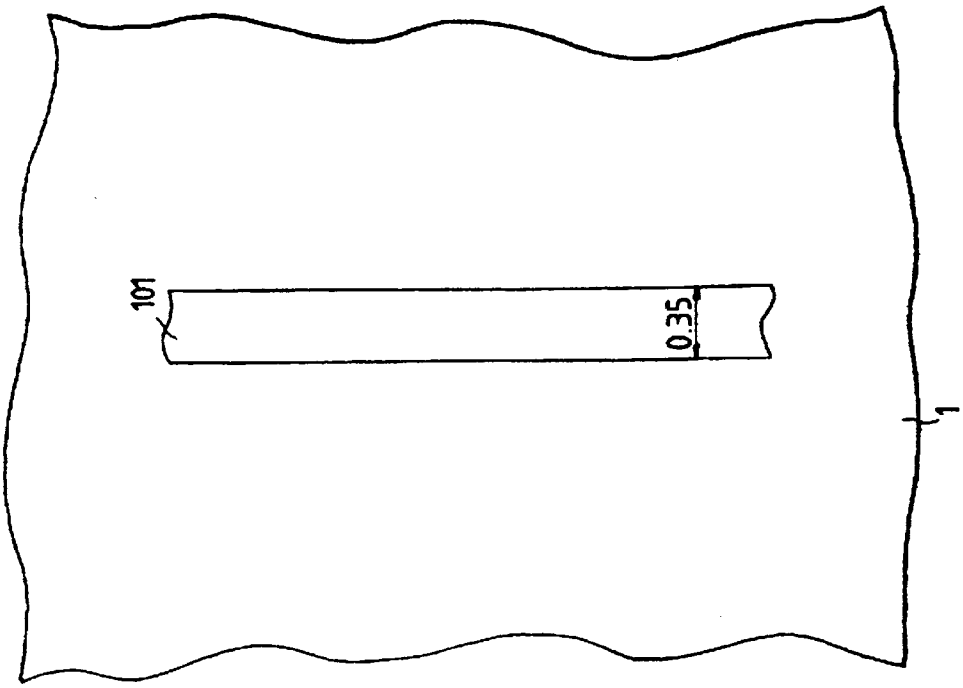


FIG. 5

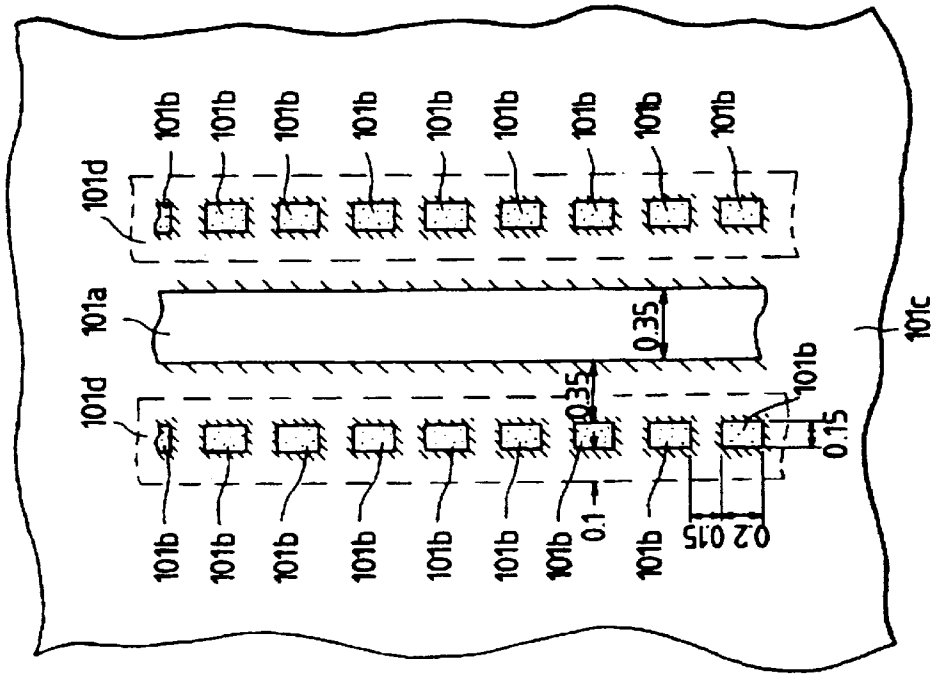
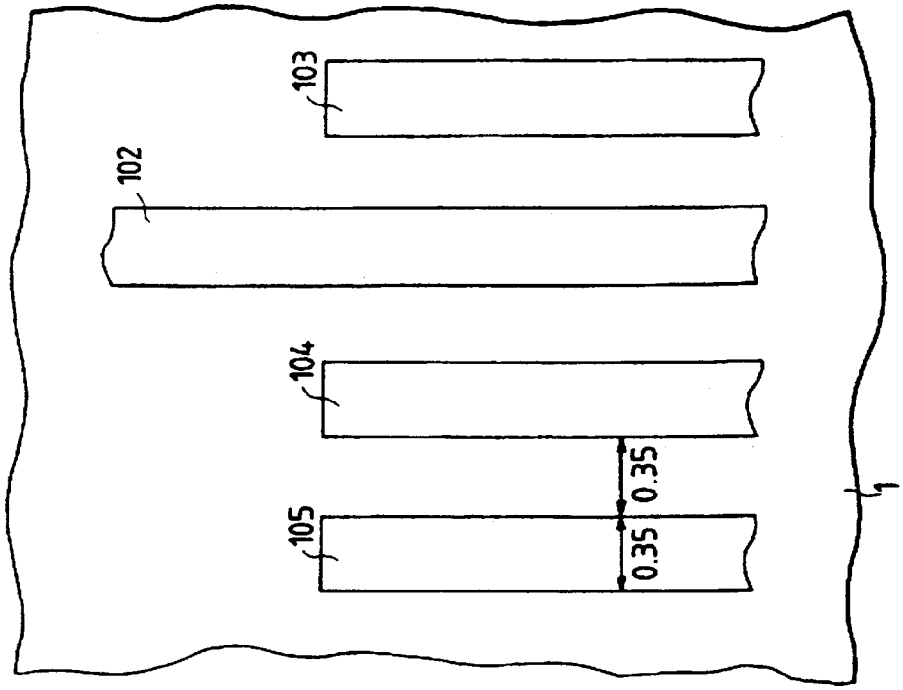


FIG. 8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102
104
105
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0.35
1

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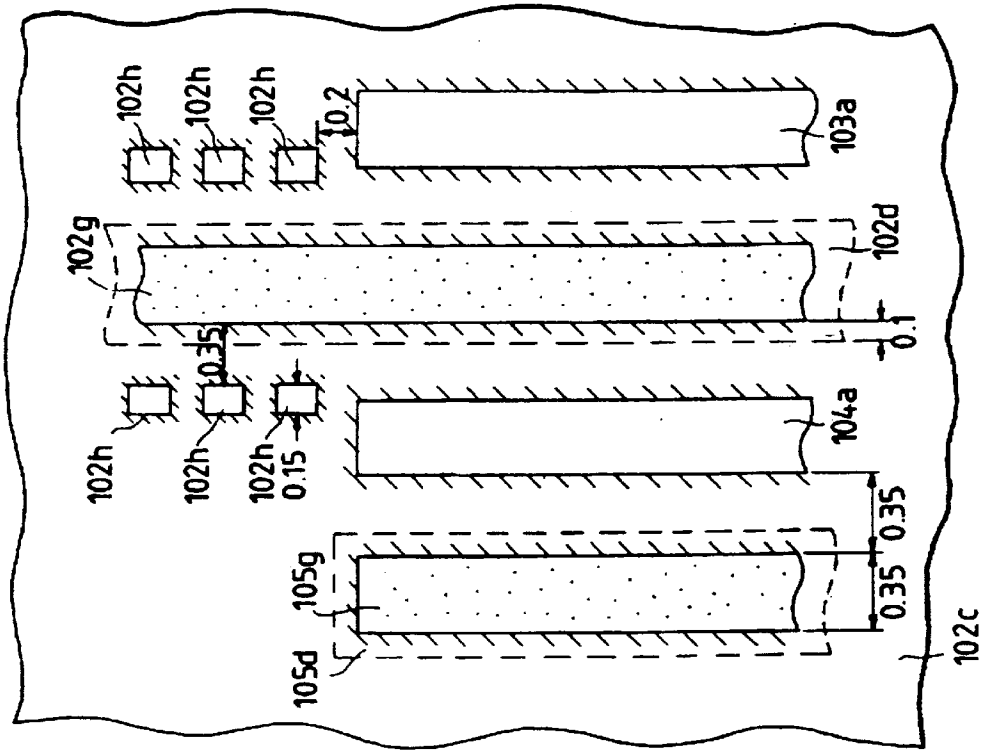
102h
102h
102h
0.2
103a
102g
102d
0.1
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102h
102h
102h
0.15
104a
0.35
105g
0.35
105d
102c

FIG. 10

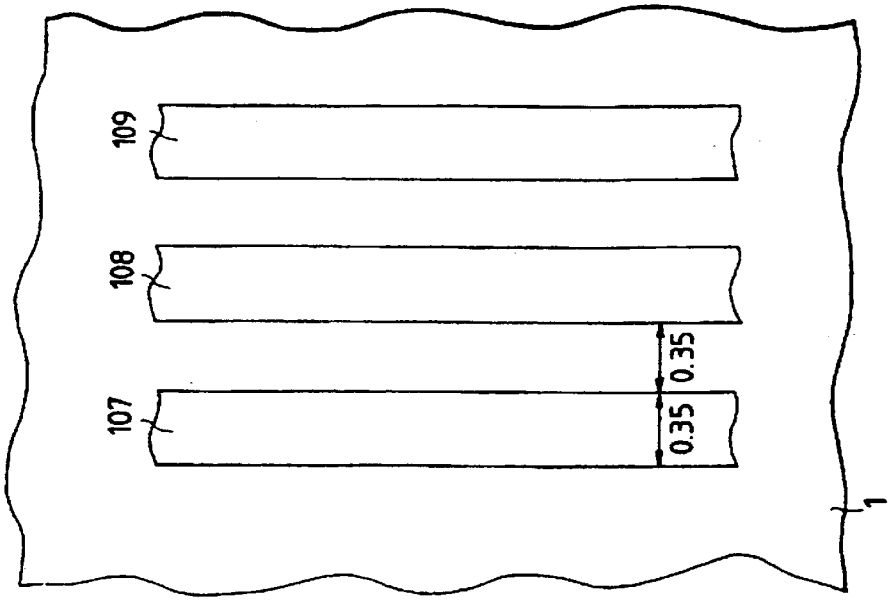


FIG. 9

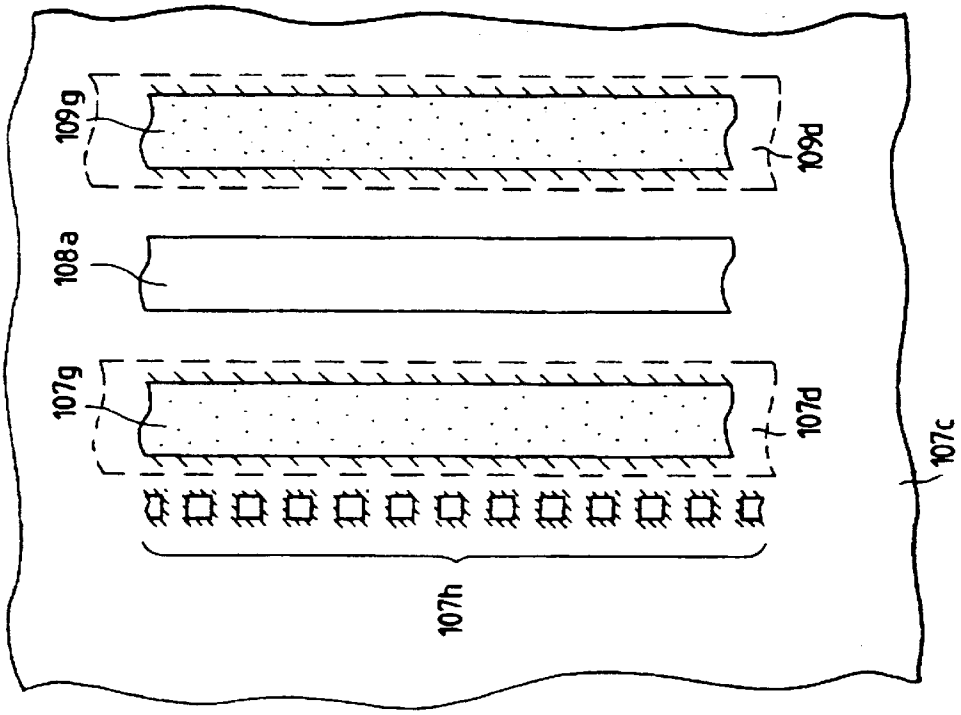


FIG. 12

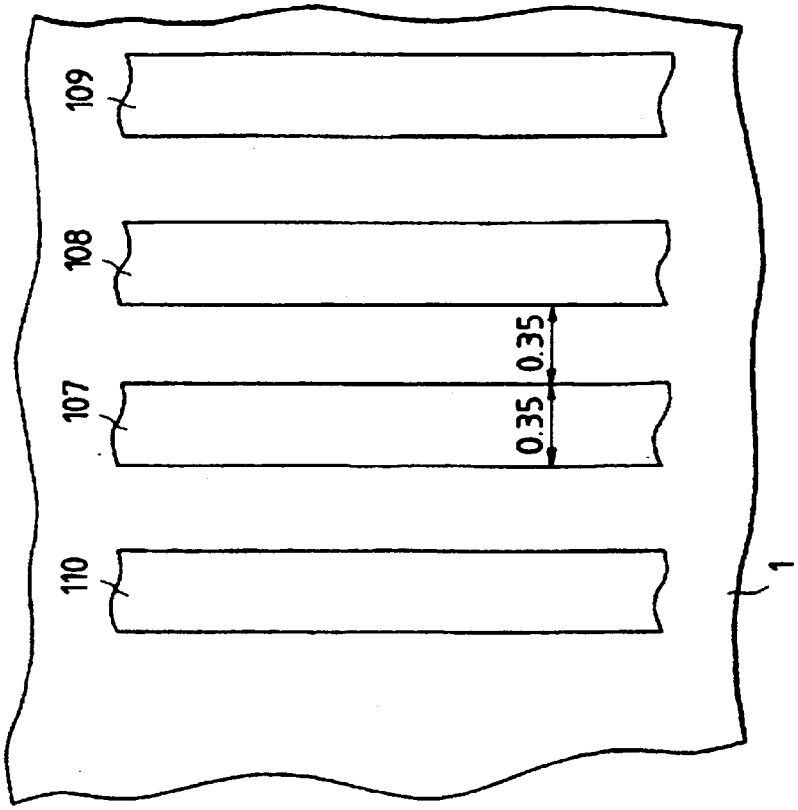

109
108
107
110
0.35
0.35
1

FIG. 11

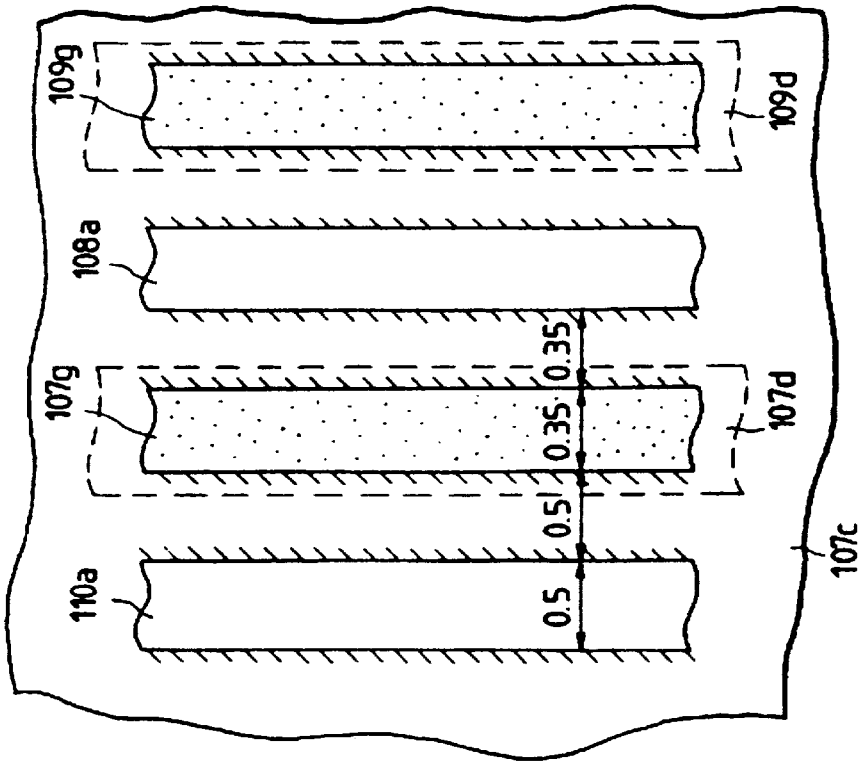
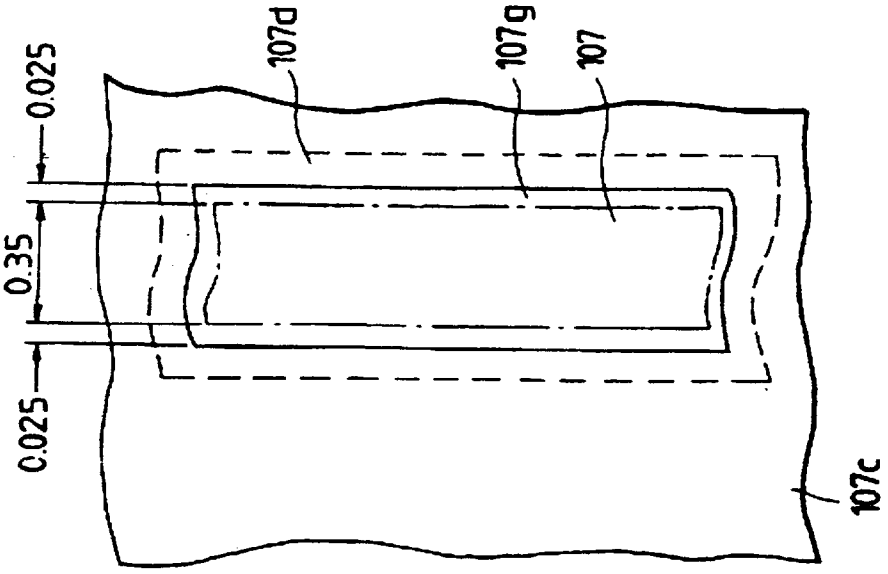

109g
108a
107g
110a
0.5
0.5
0.35
0.35
109d
107d
107c

FIG. 14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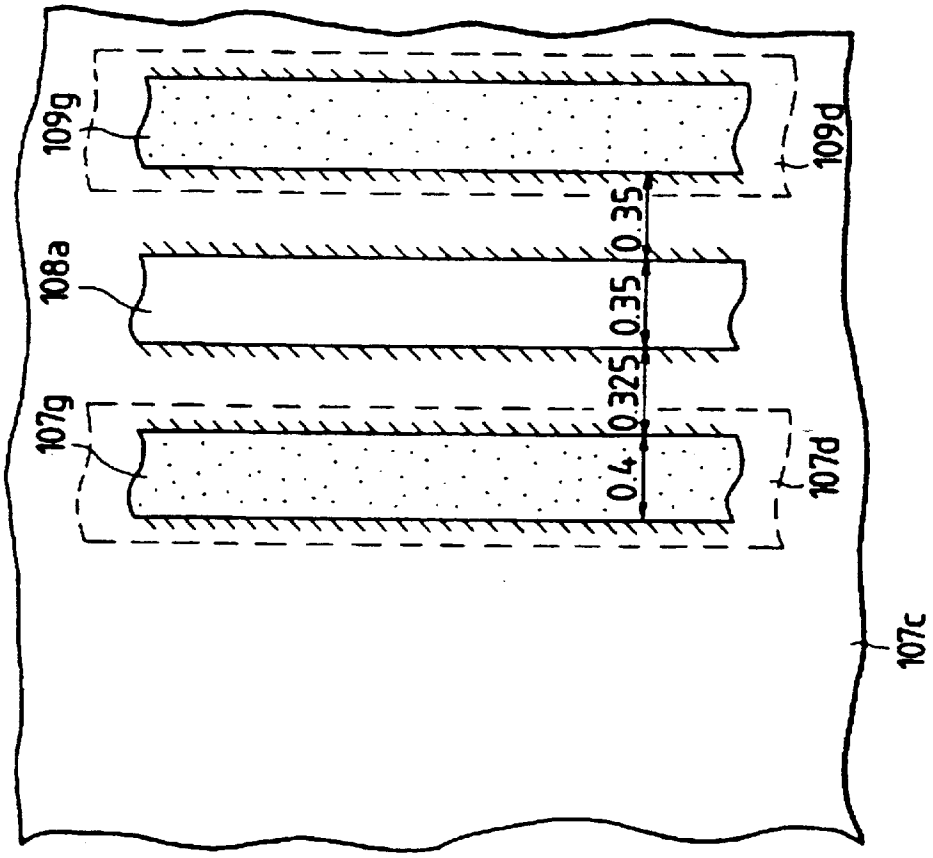
0.35
0.025
107d
107g
107
107c

FIG. 13


109g
108a
107g
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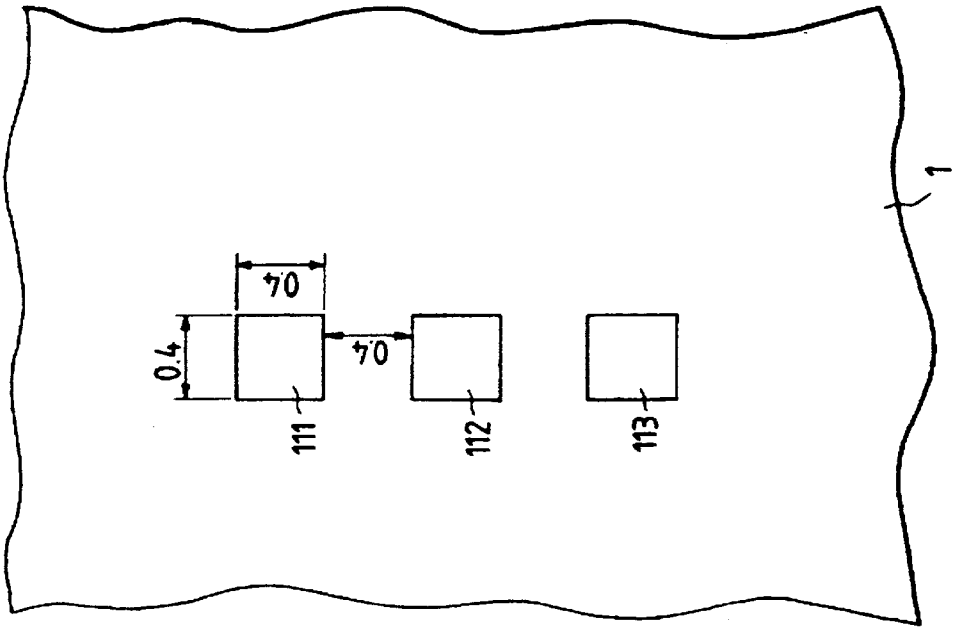
0.35
0.325
0.4
109d
107d
107c

FIG. 16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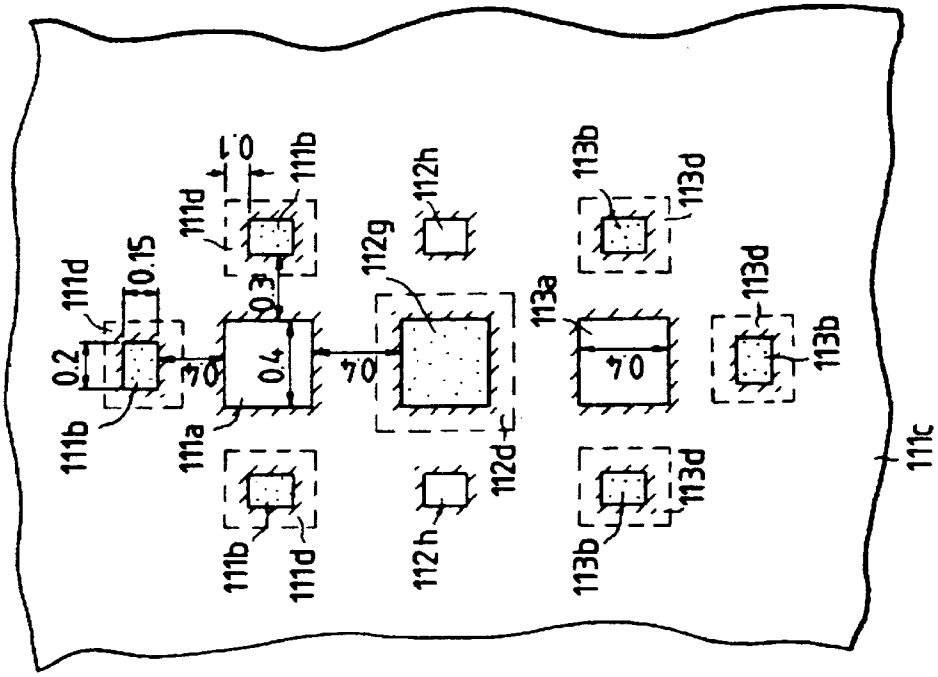
70
70
111
112
113
1

FIG. 15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111b
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111a
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111d
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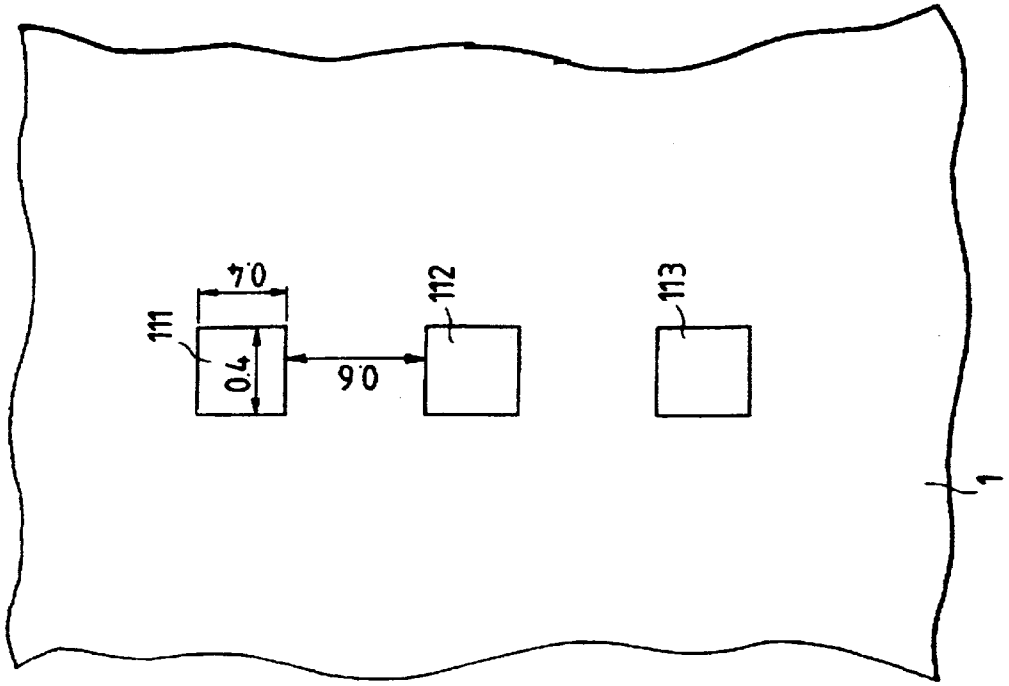
112d
112h
113a
70
113b
113d
113d
113b
113b
113d
111c

FIG. 18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0.7
0.6
112
113
1

FIG. 17

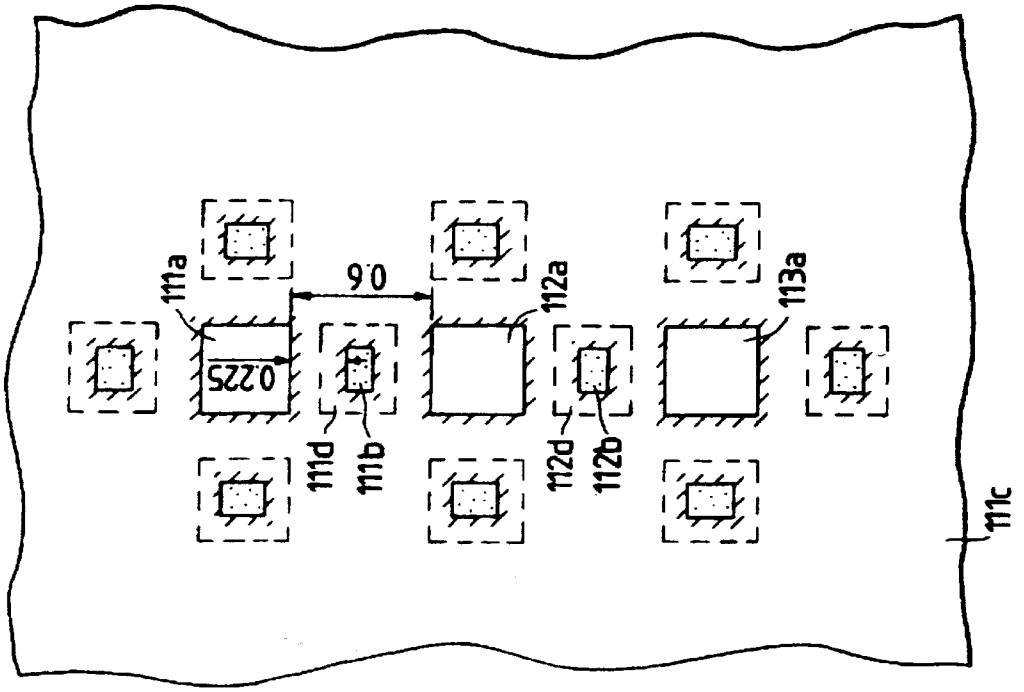

111a
0.225
0.6
111d
111b
112a
112d
112b
113a
111c

FIG. 20

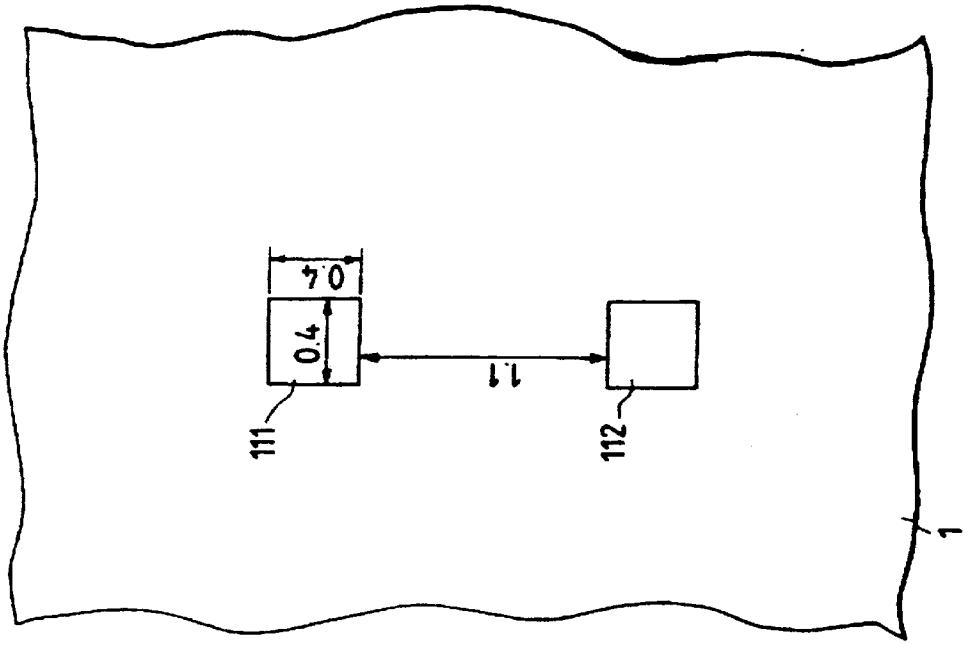


FIG. 19

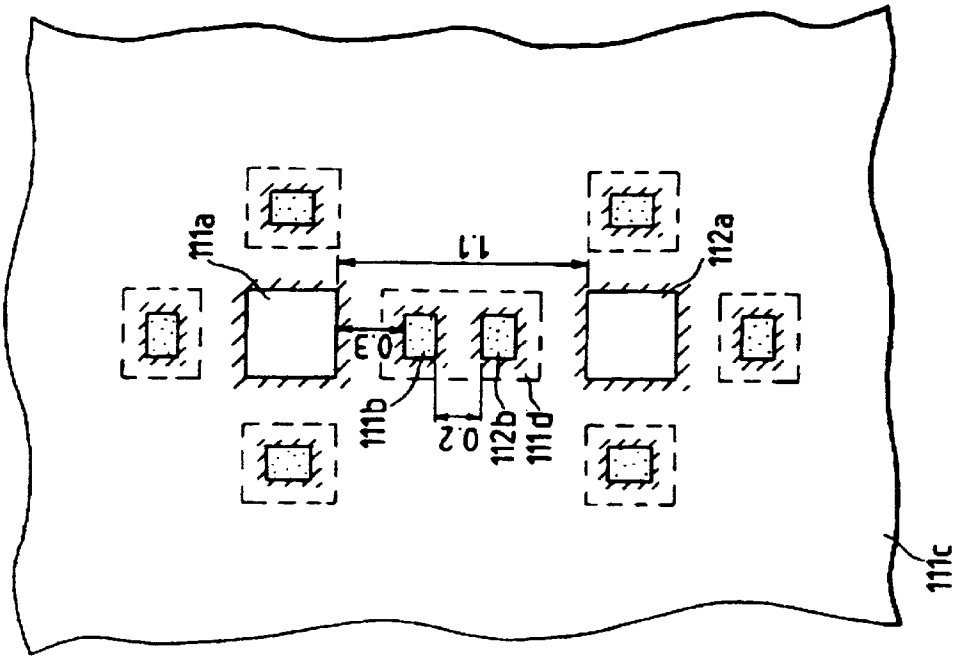


FIG. 22

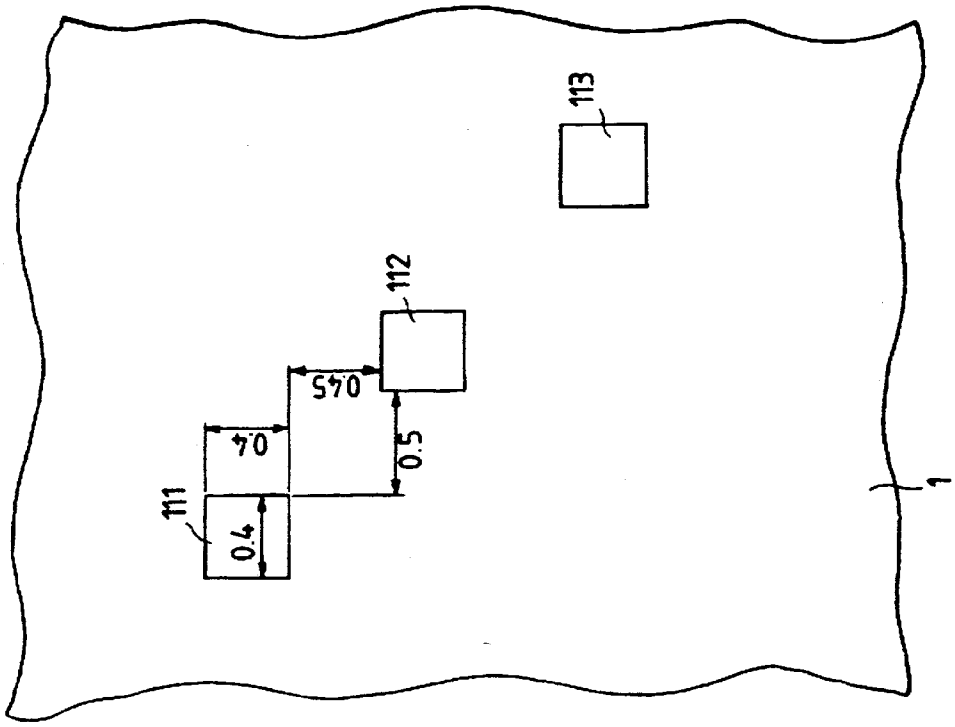
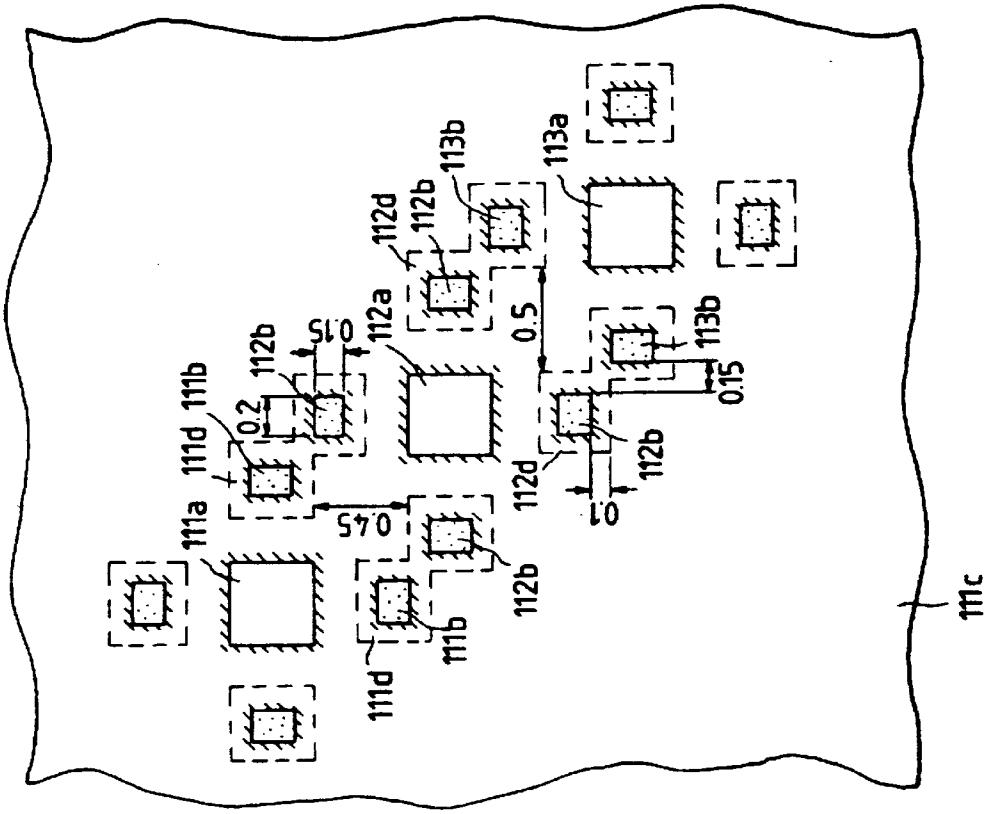

111
0.4
0.4
0.45
0.5
112
113
1

FIG. 21


111a
111d
111b
0.2
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112a
112d
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112d
112b
0.1
112b
111d
111b
111c

FIG. 24

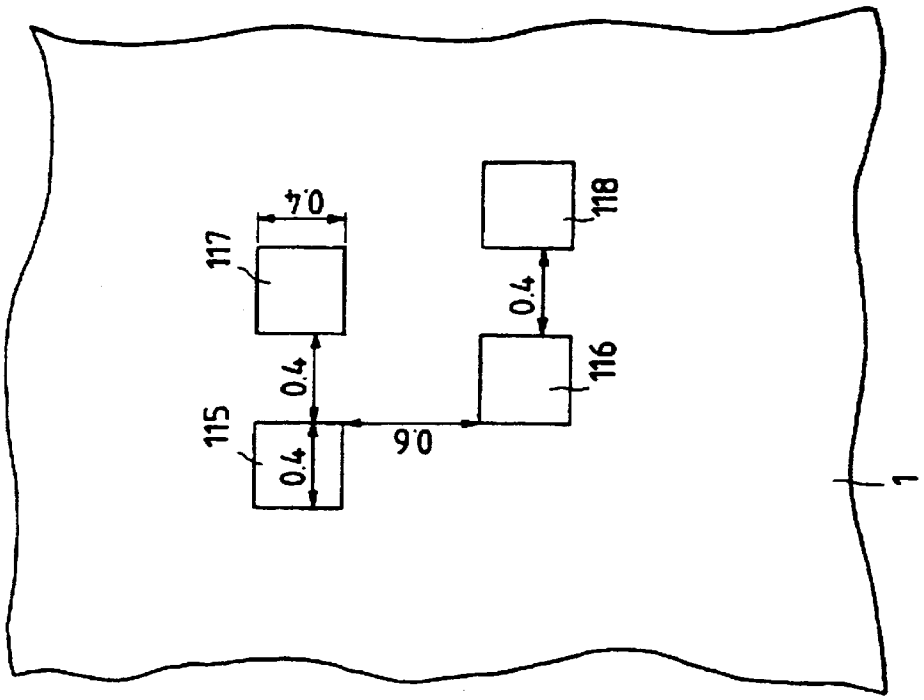

0.4
117
0.4
115
0.4
9.0
0.4
116
118
1

FIG. 23

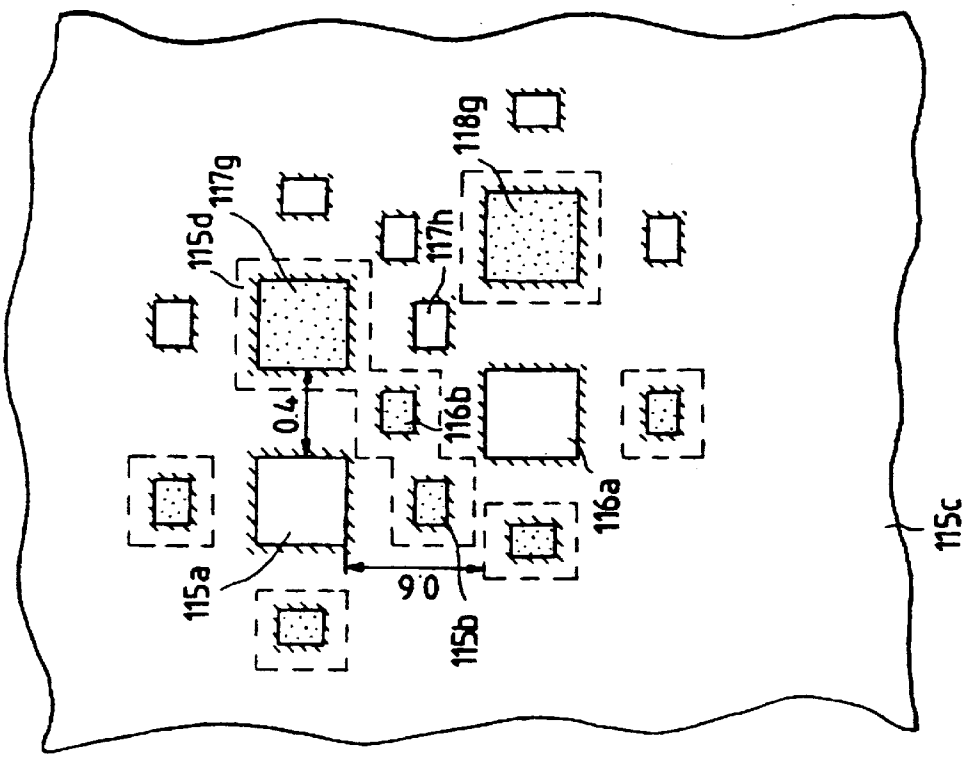
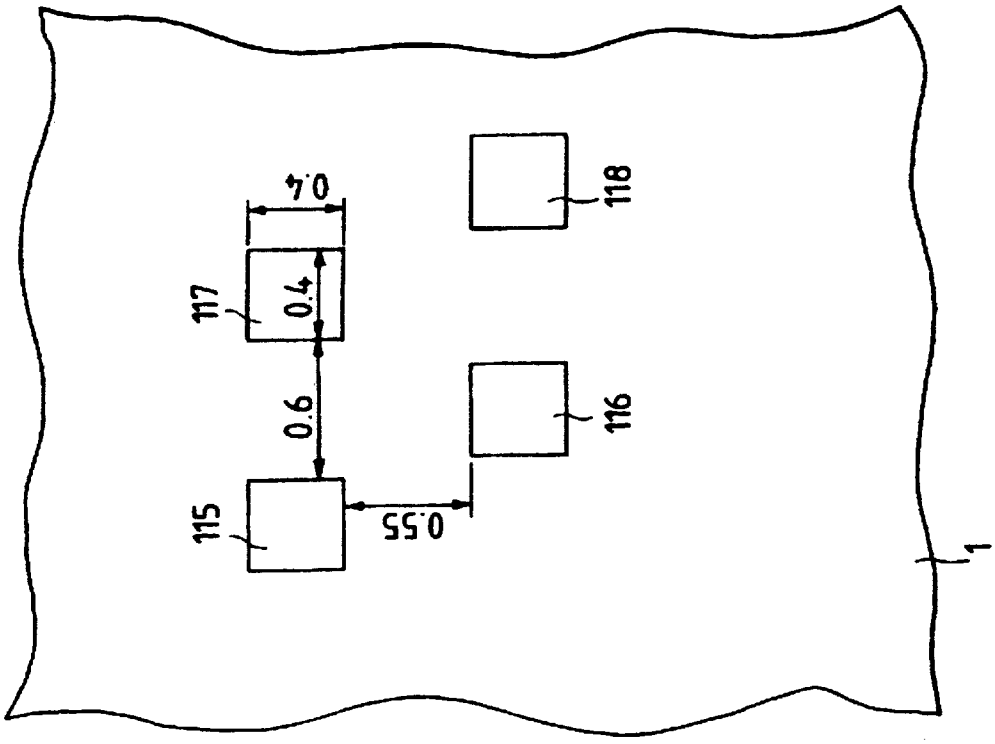

115d
117g
0.4
115a
9.0
115b
117h
116b
118g
116a
115c

FIG. 26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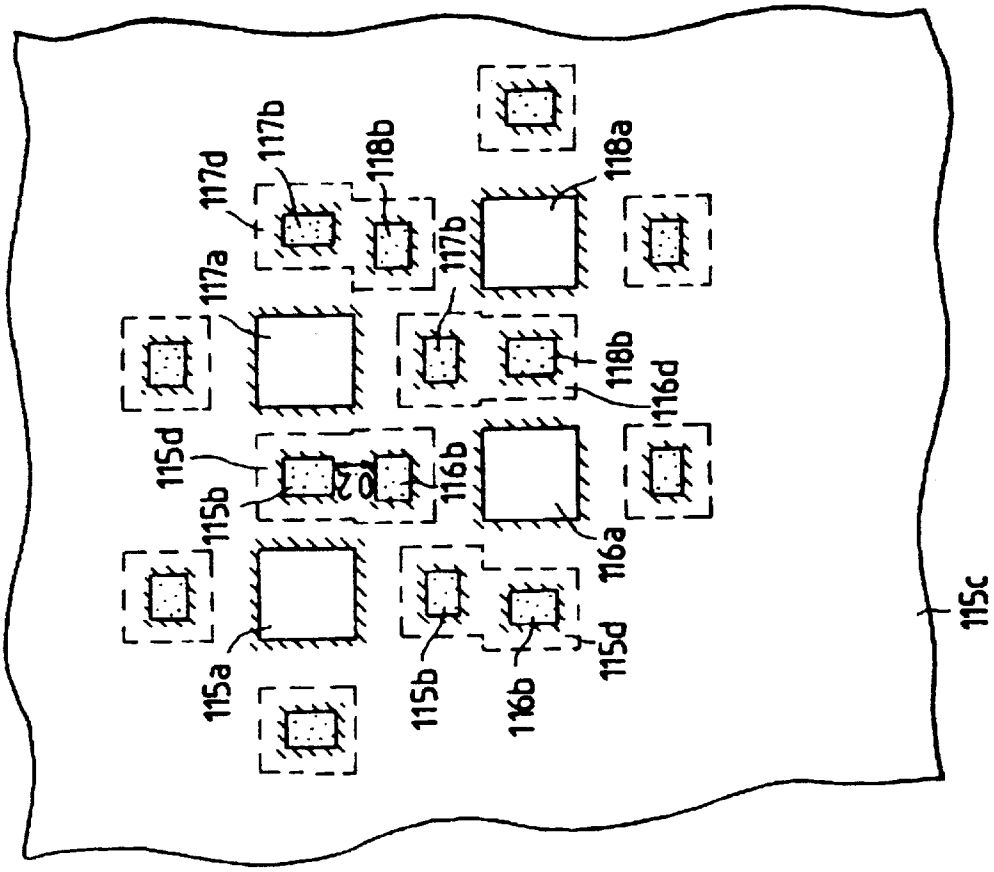
117
118
116
0.6
0.4
0.4
0.55
1

FIG. 25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115b
115d
117a
117d
117b
118b
118a
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116a
116d
115c

FIG. 27

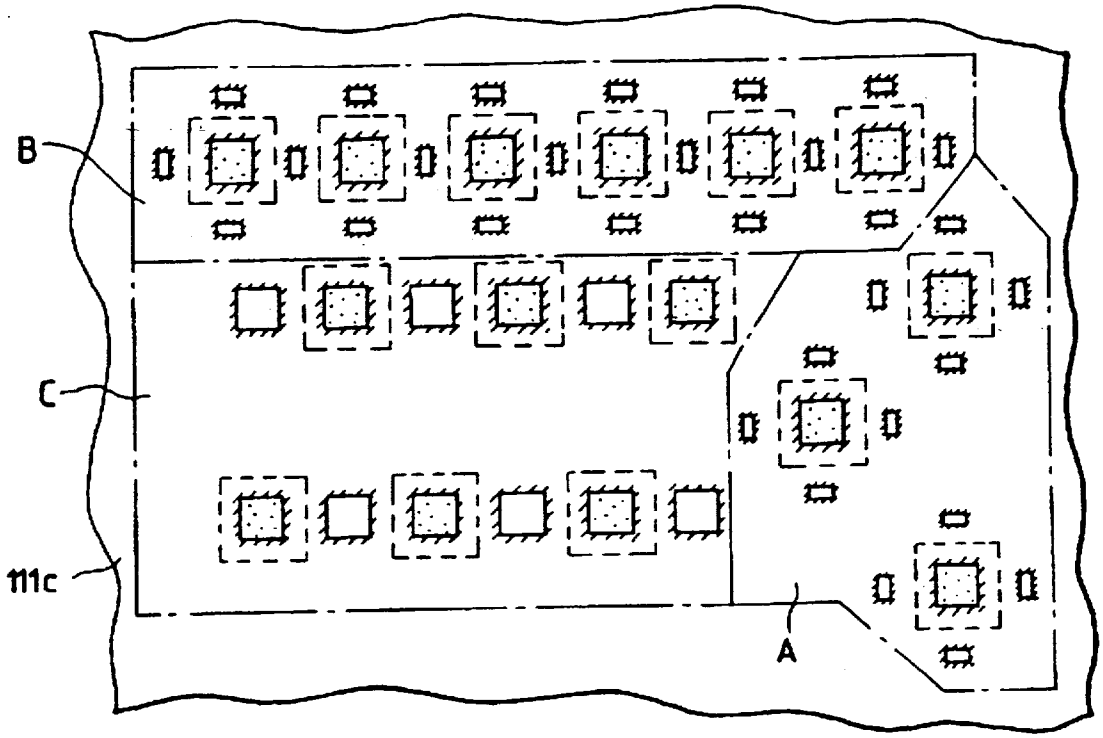


FIG. 28

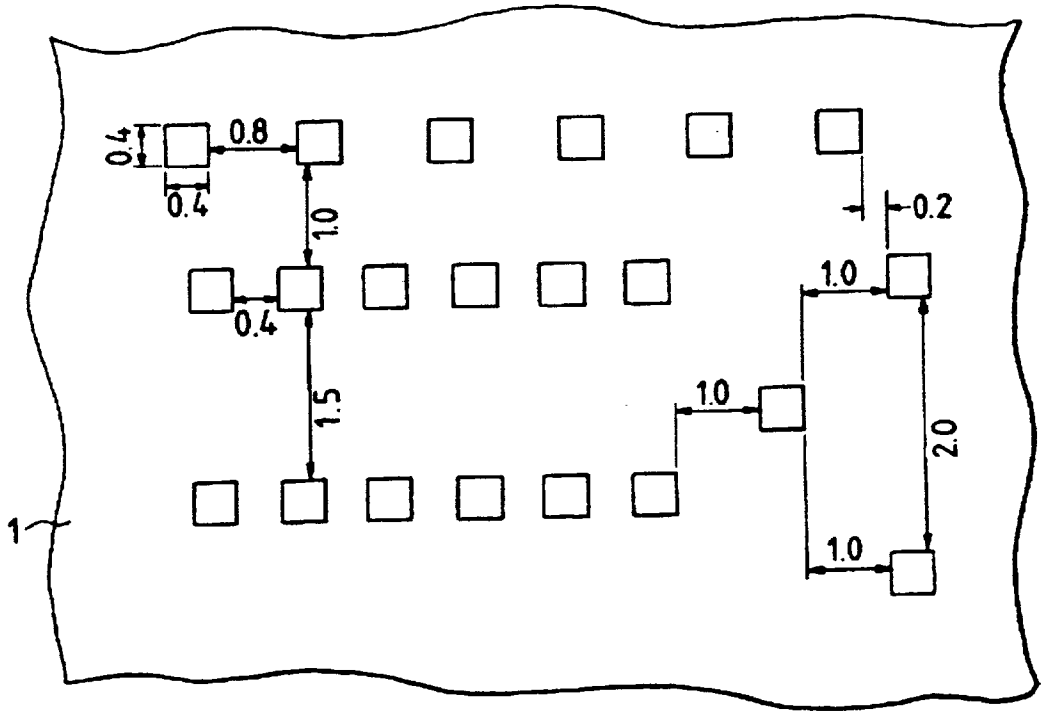


FIG. 29

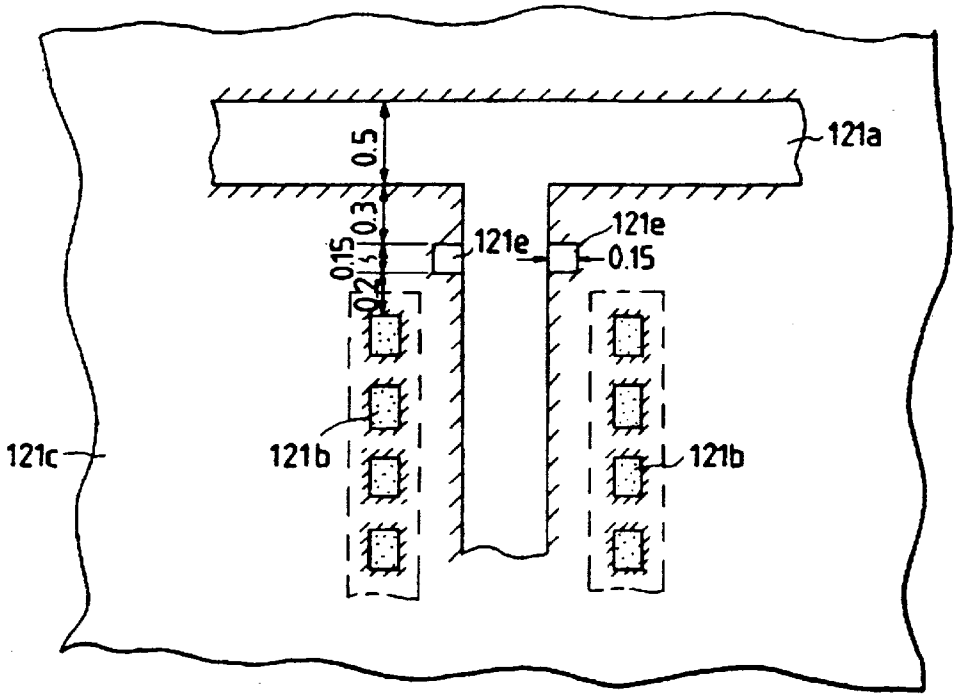


FIG. 30

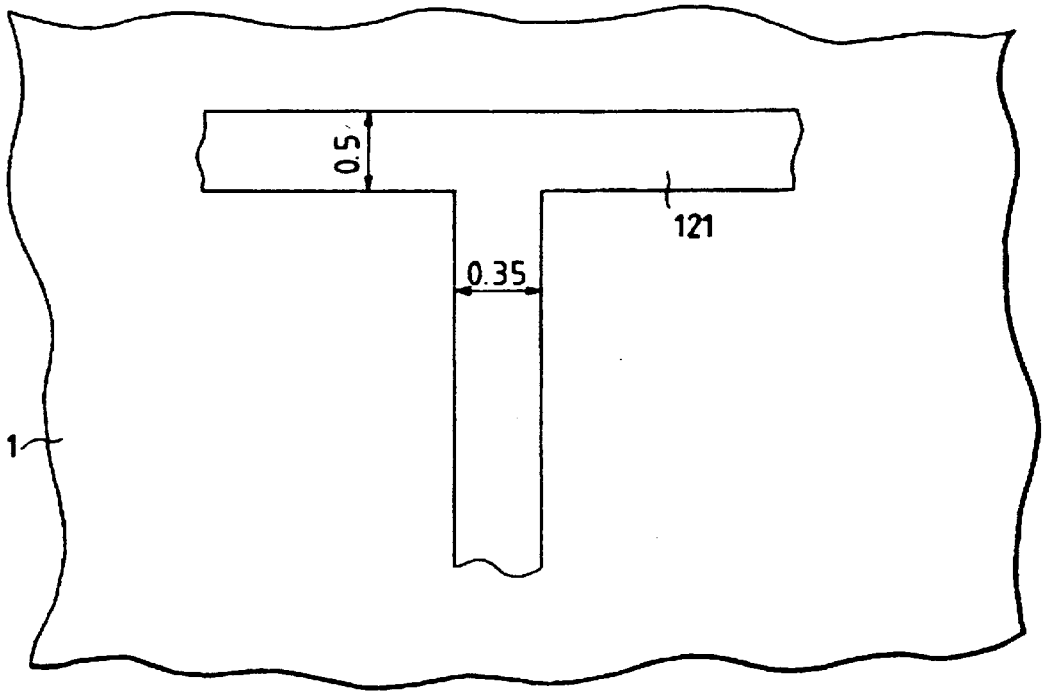
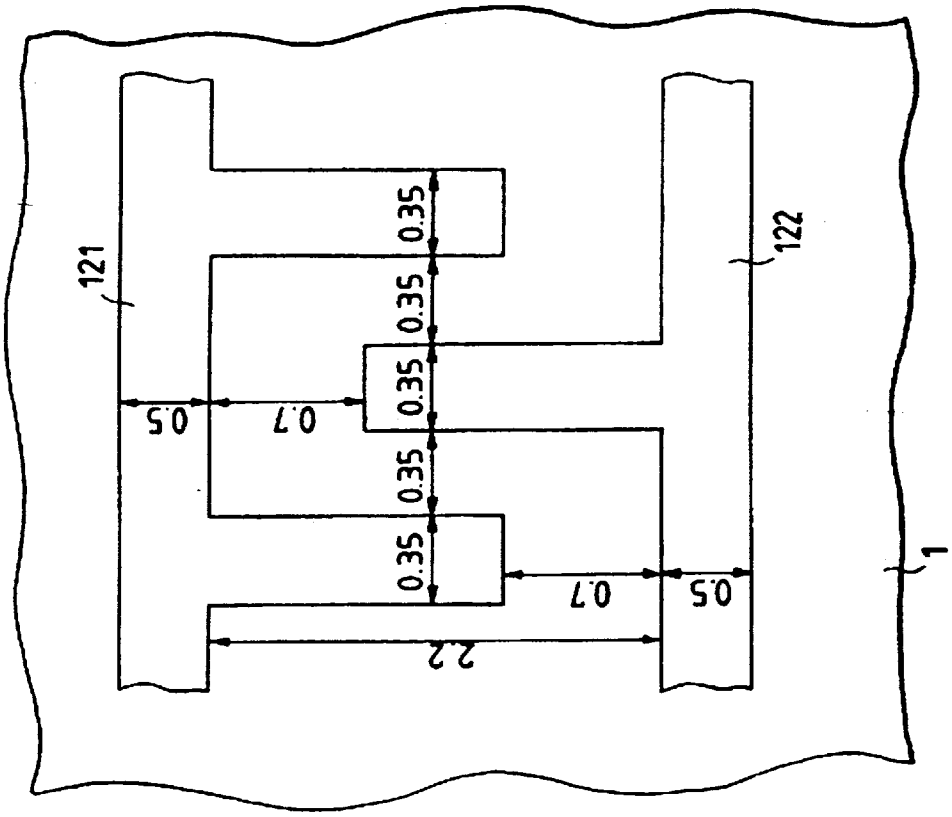


FIG. 32


121
122
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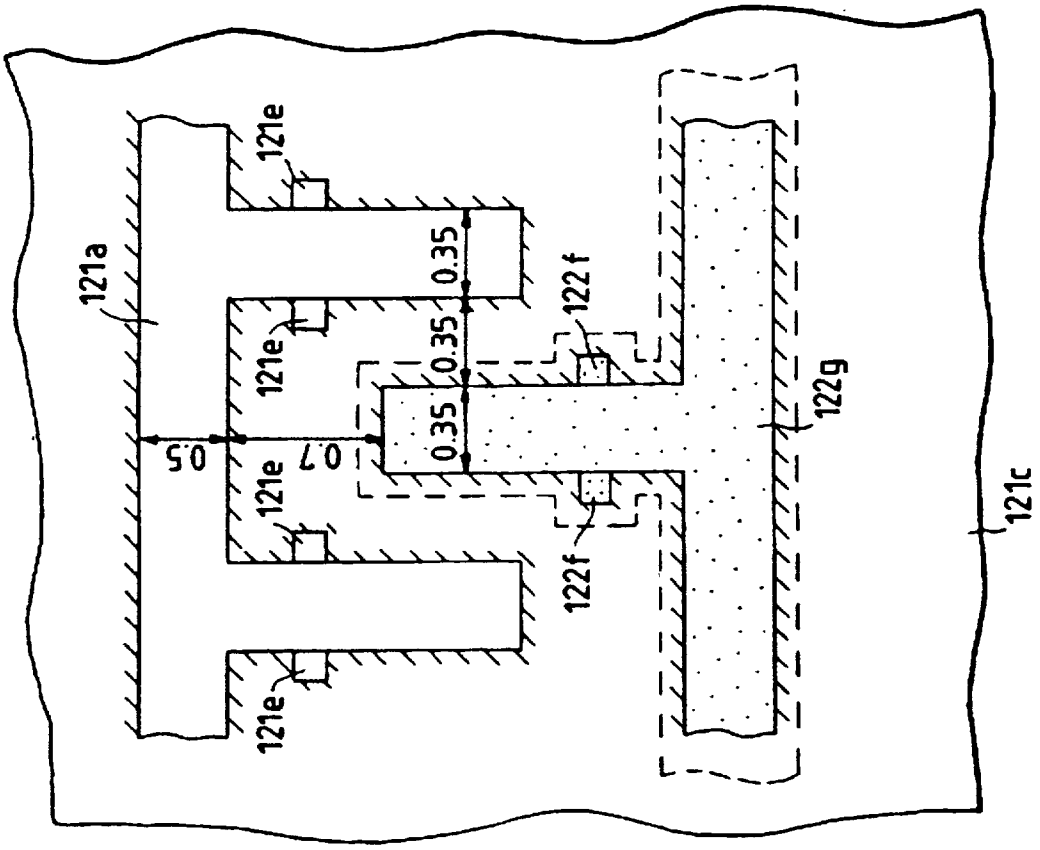
0.7
0.7
0.5
2.2
1

FIG. 31


121a
121e
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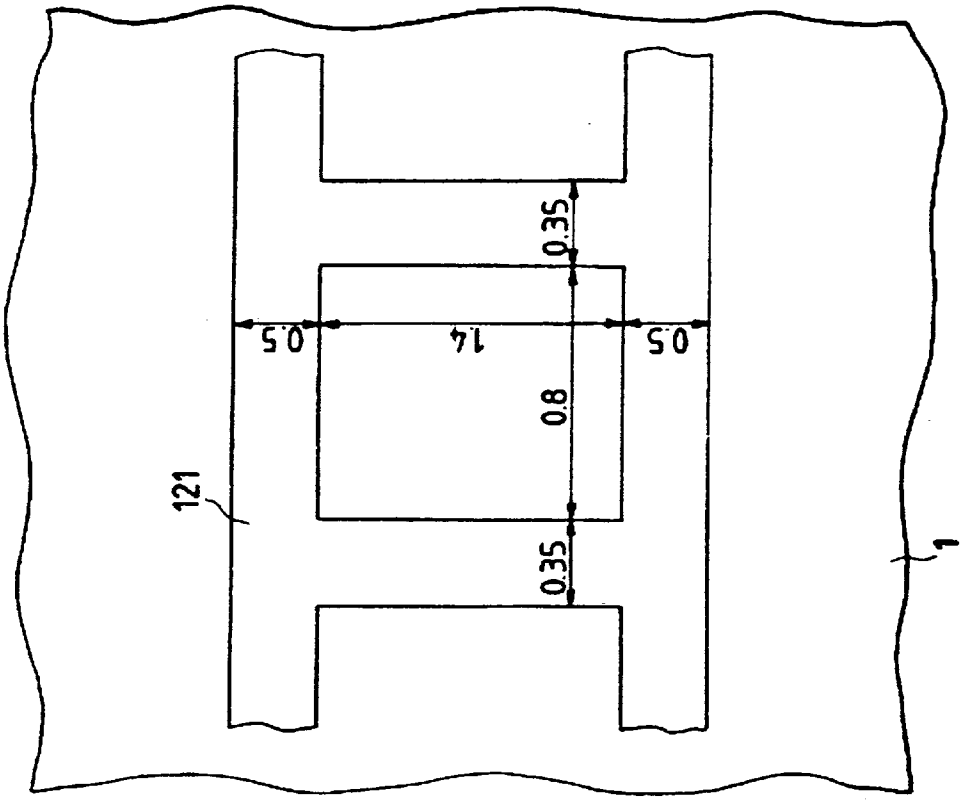
122f
122f
122g
121c

FIG. 34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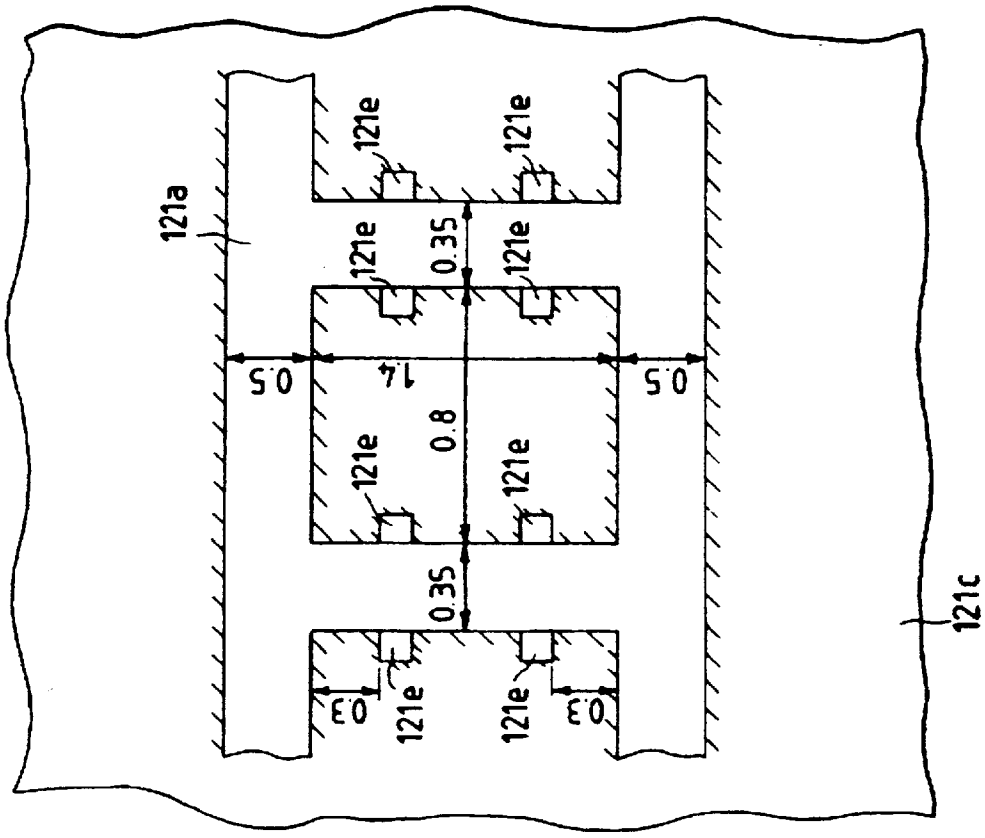
0.5
1

FIG. 33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0.3
0.3
121c

FIG. 35

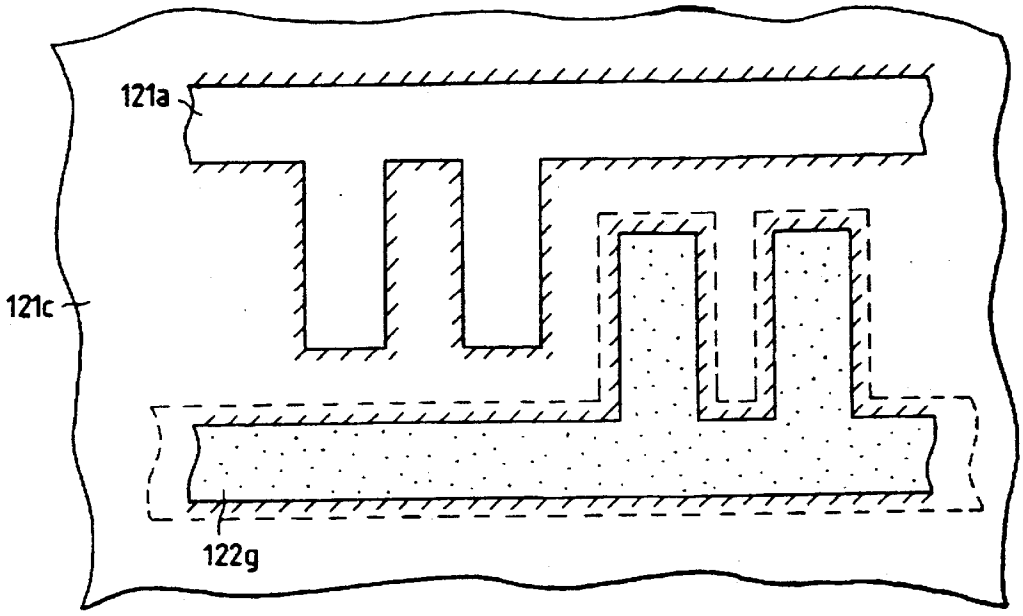


FIG. 36

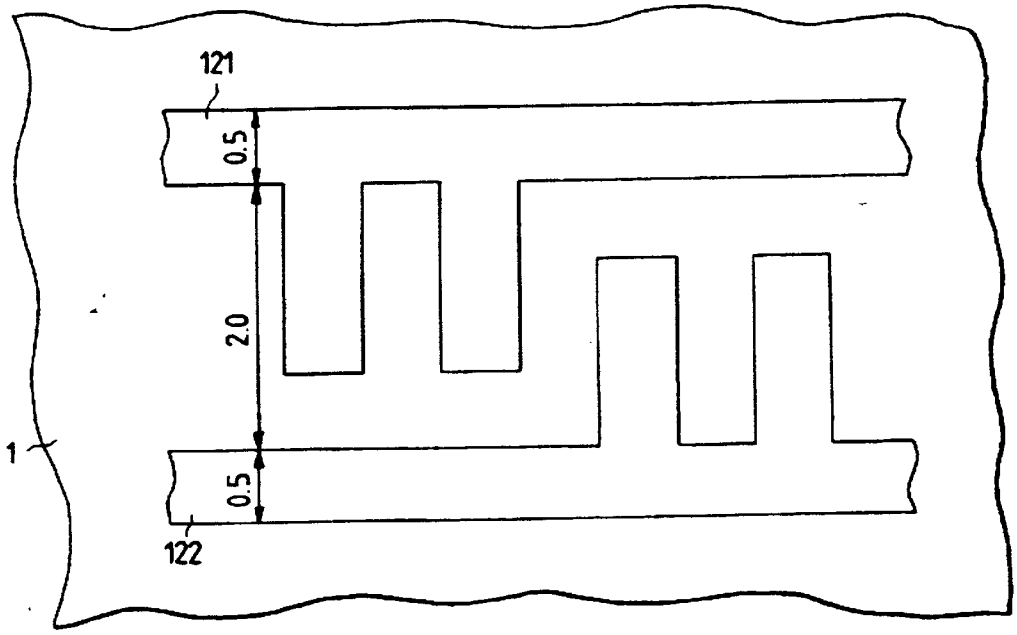


FIG. 37

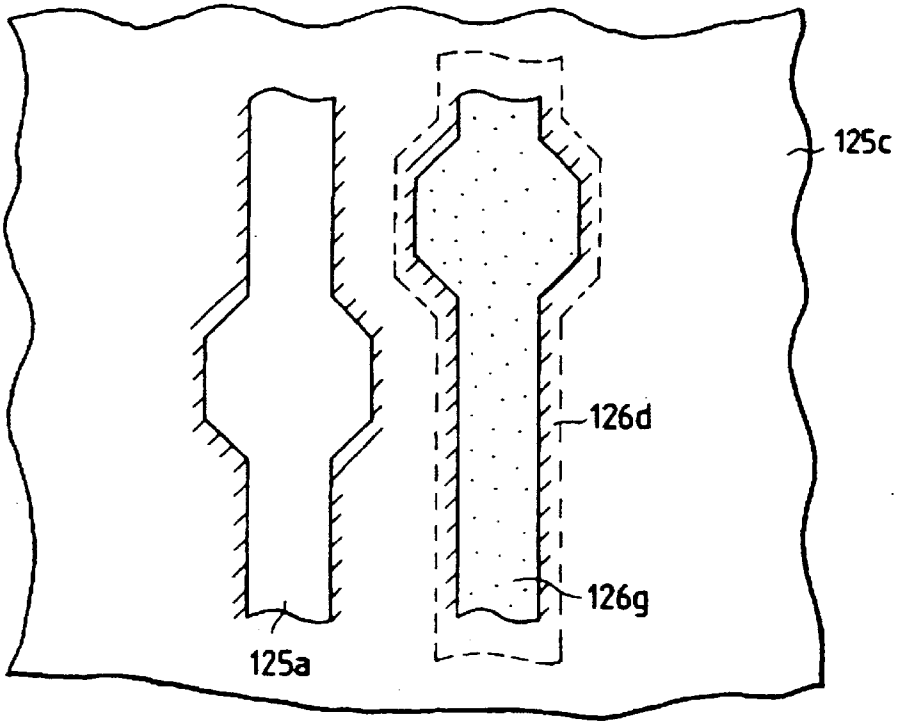


FIG. 38

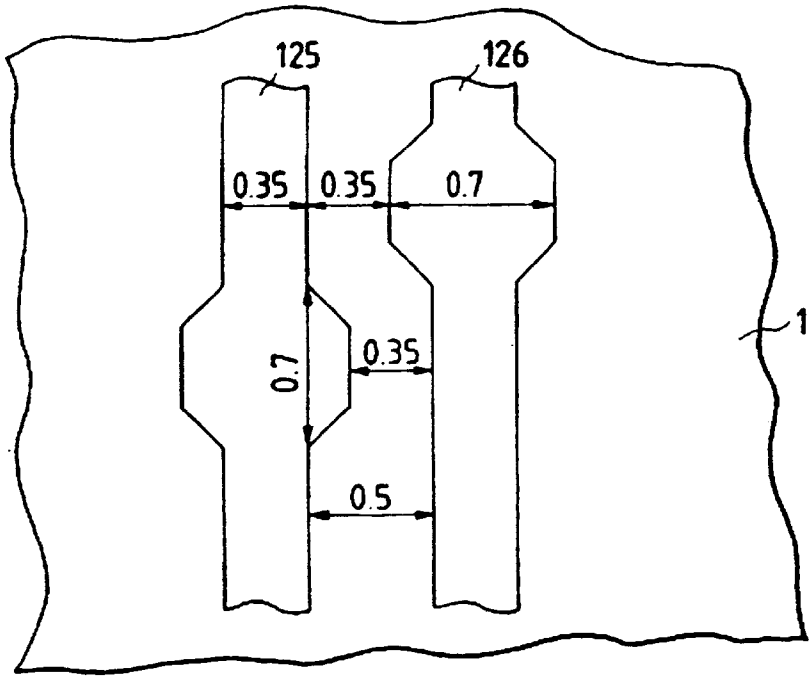
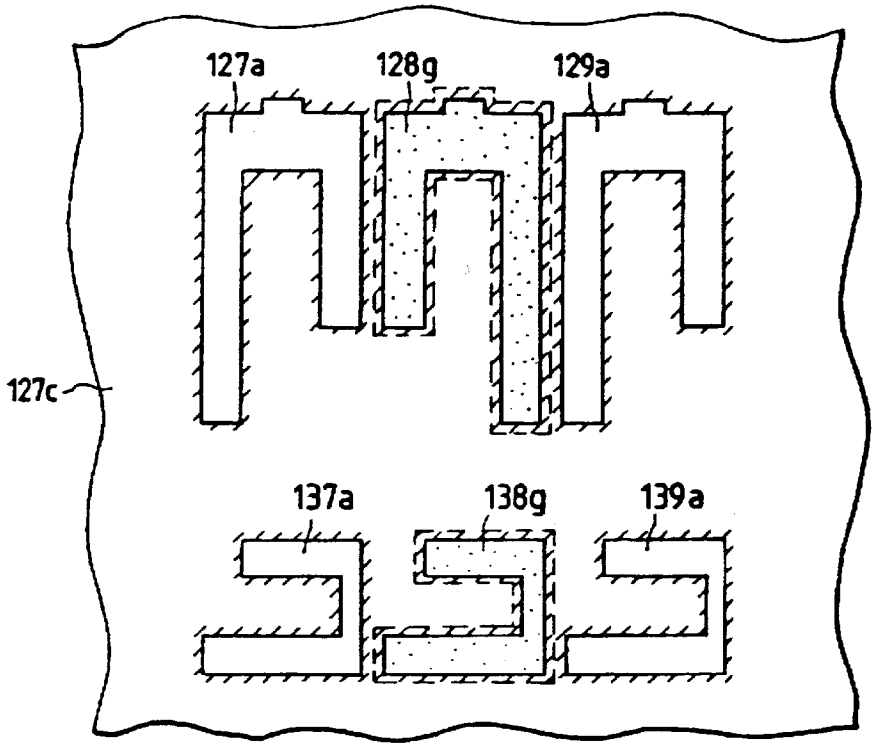


FIG. 39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128g
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138g
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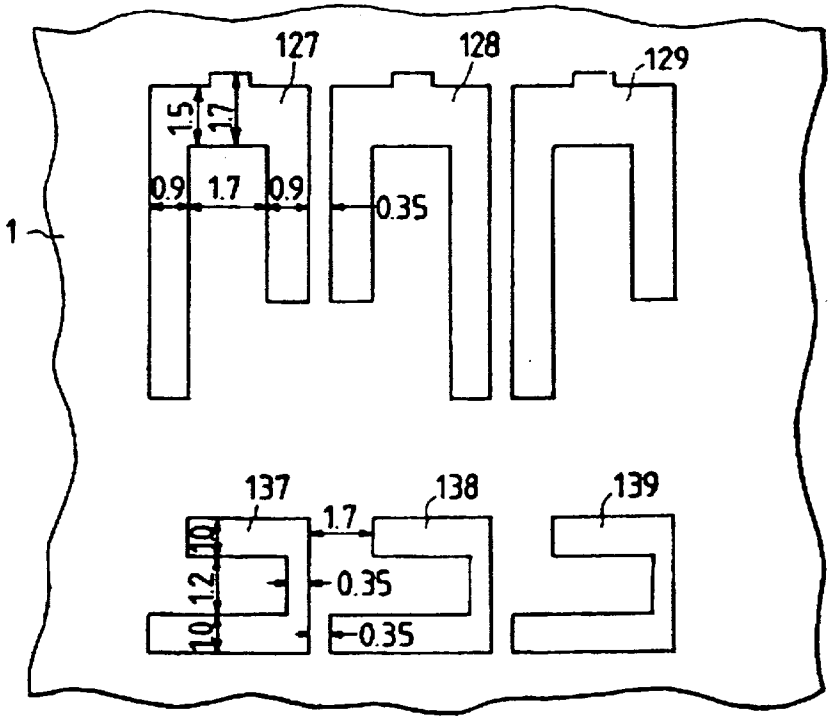
FIG. 40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1.0
0.35
0.35

FIG. 42

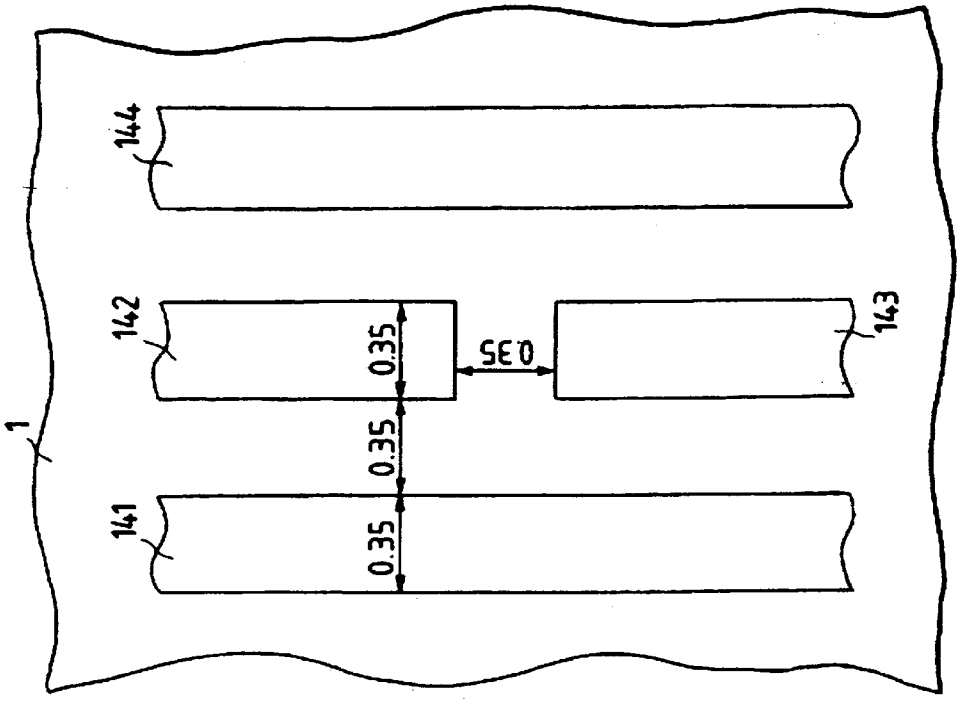

1
141
142
143
144
0.35
0.35
0.35
0.35

FIG. 41

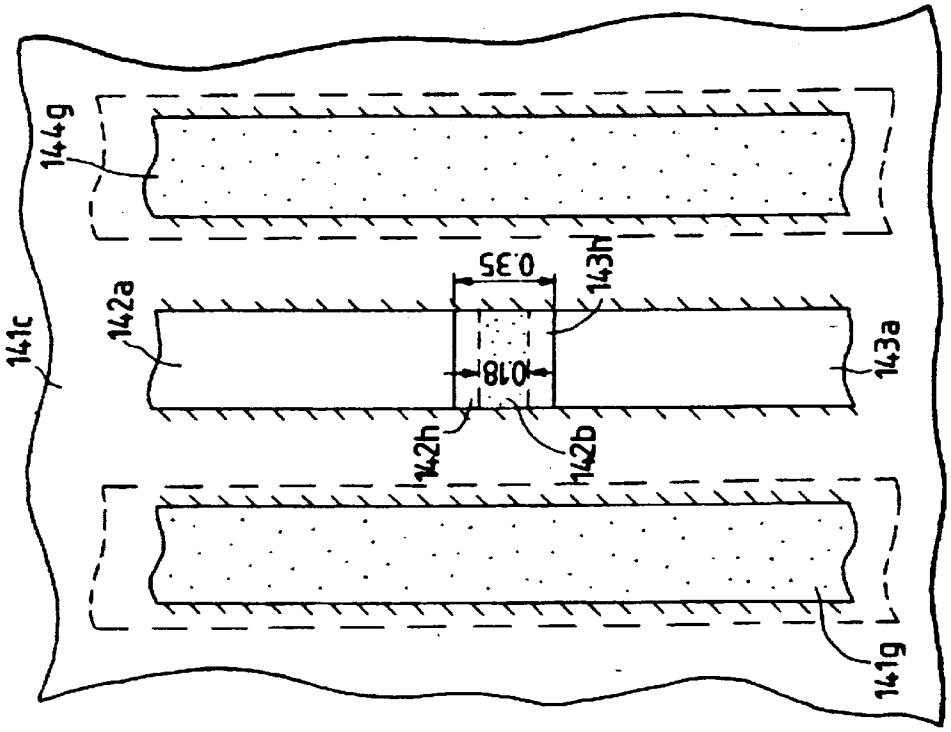

141c
142a
143a
144g
141g
142h
142b
143h
0.18
0.35

FIG. 43

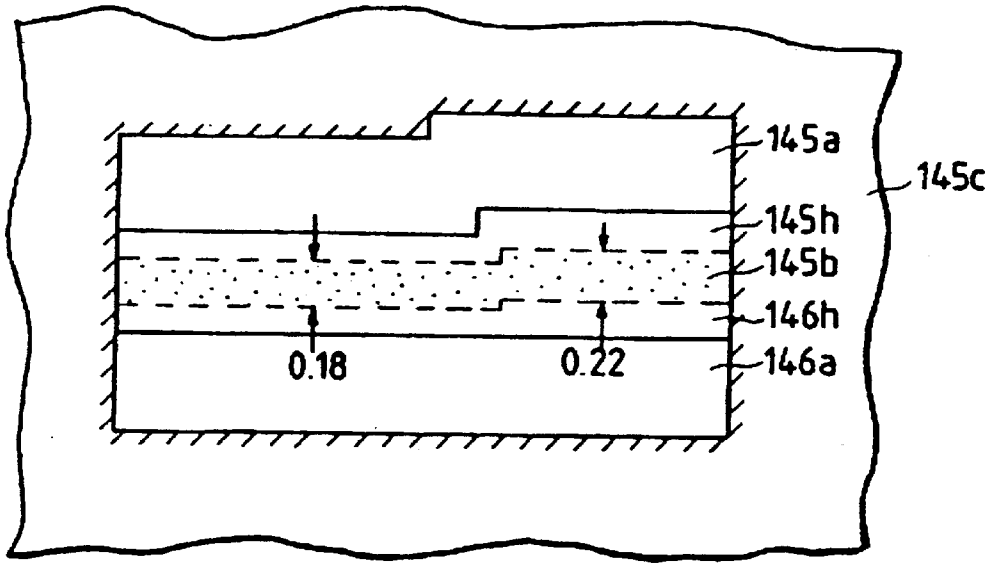

145a
145c
145h
145b
146h
0.18
0.22
146a

FIG. 44

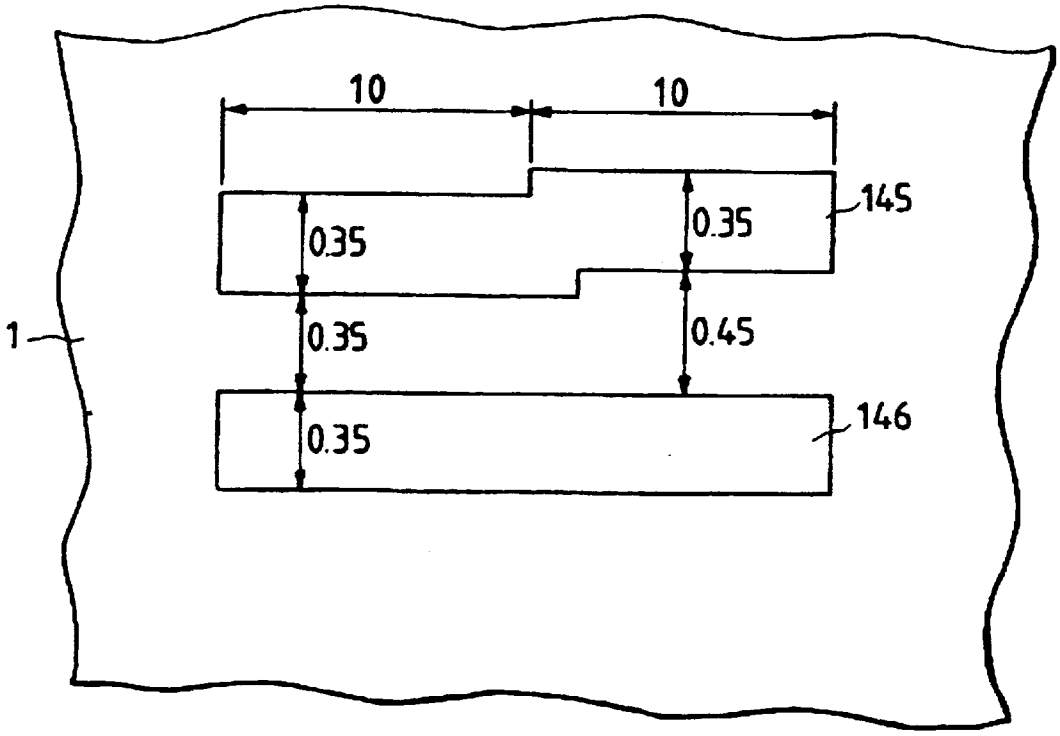

10
10
145
0.35
0.35
1
0.35
0.45
146
0.35

FIG. 45

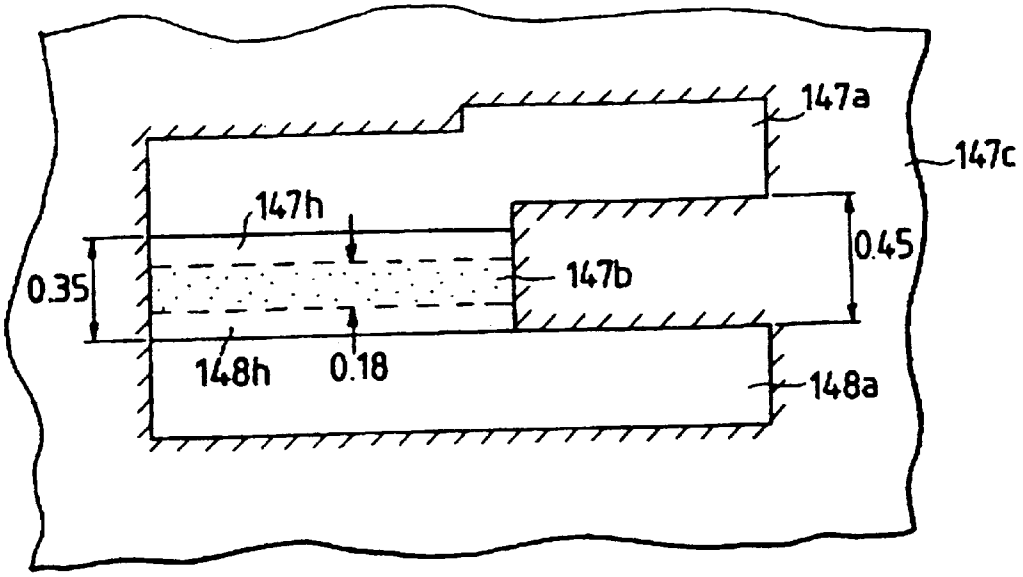

147a
147c
147h
0.45
0.35
147b
148h
0.18
148a

FIG. 46

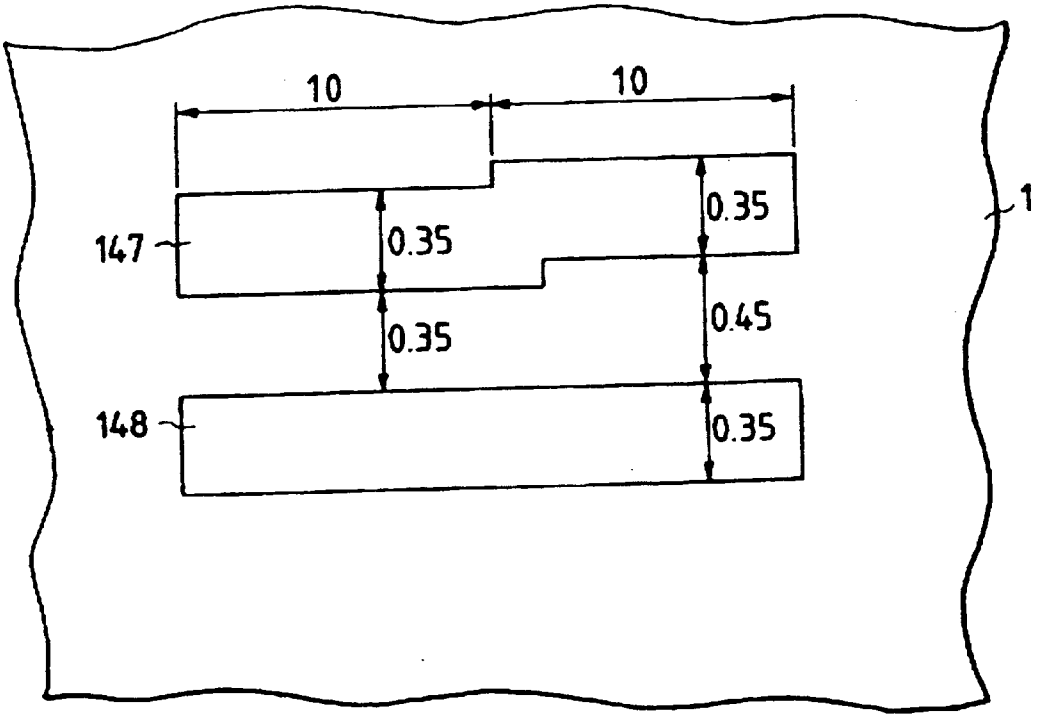

10
10
1
147
0.35
0.35
0.35
0.45
148
0.35

FIG. 47

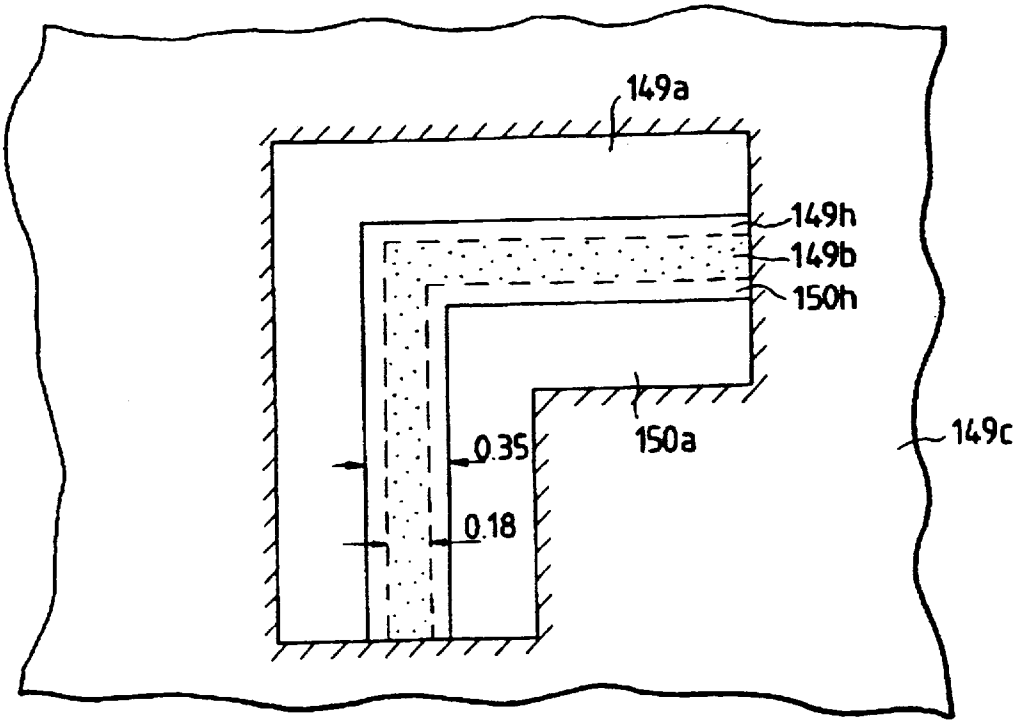


FIG. 48

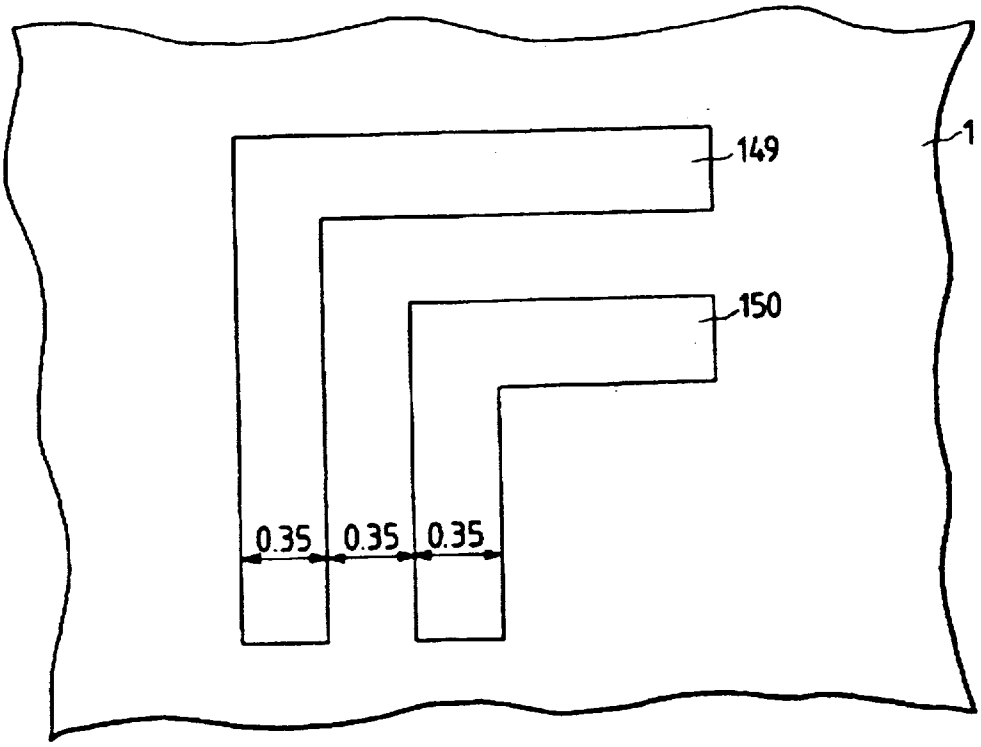


FIG. 49

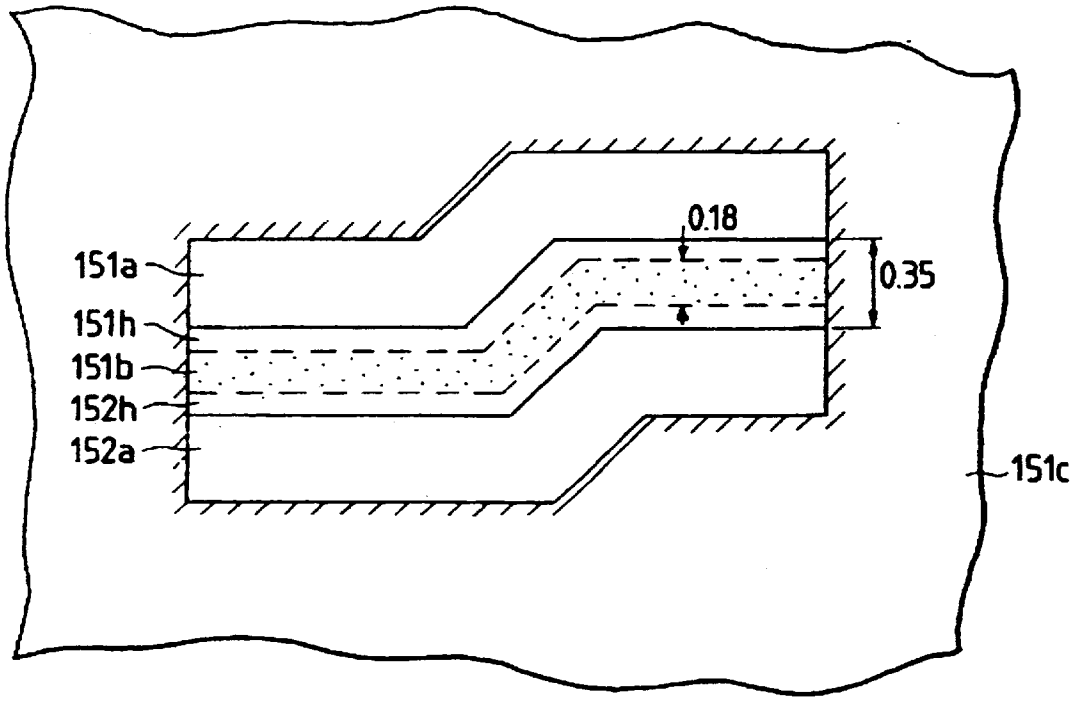


FIG. 50

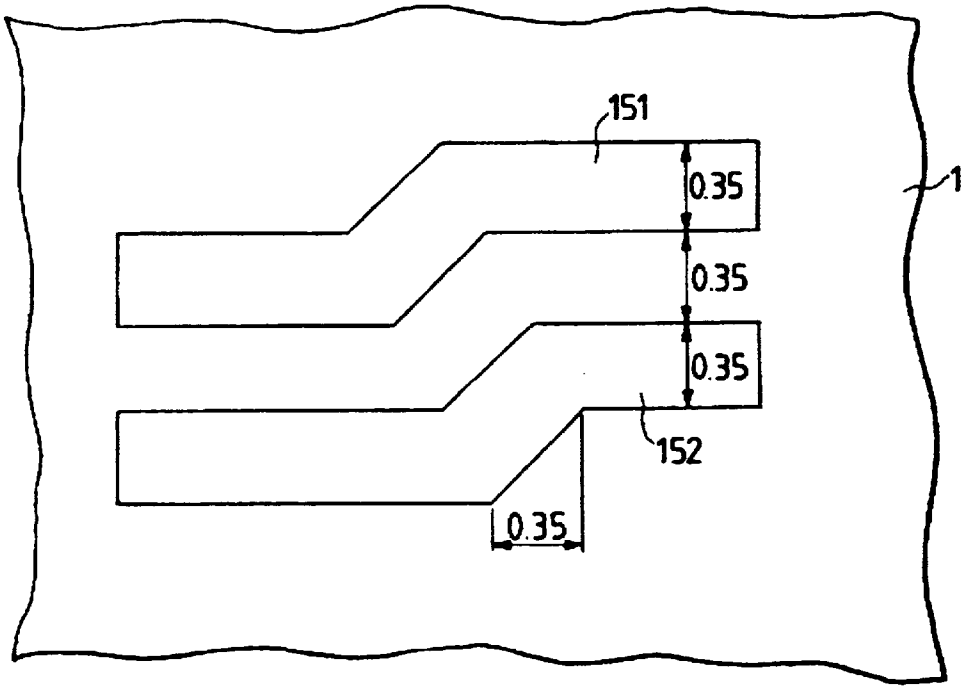


FIG. 51

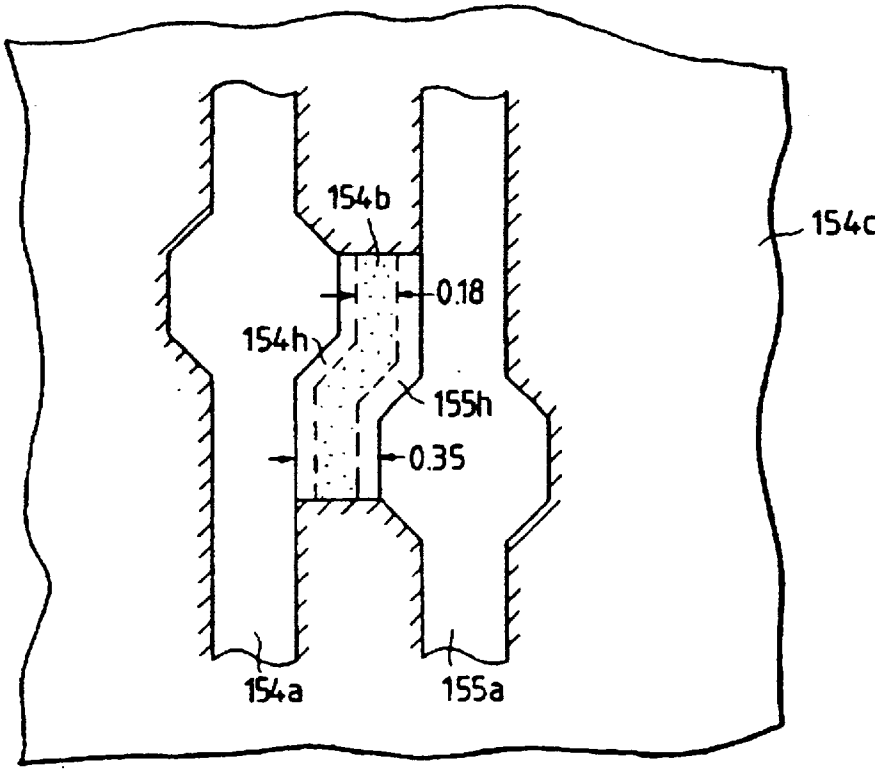

154b
154c
0.18
154h
155h
0.35
154a
155a

FIG. 52

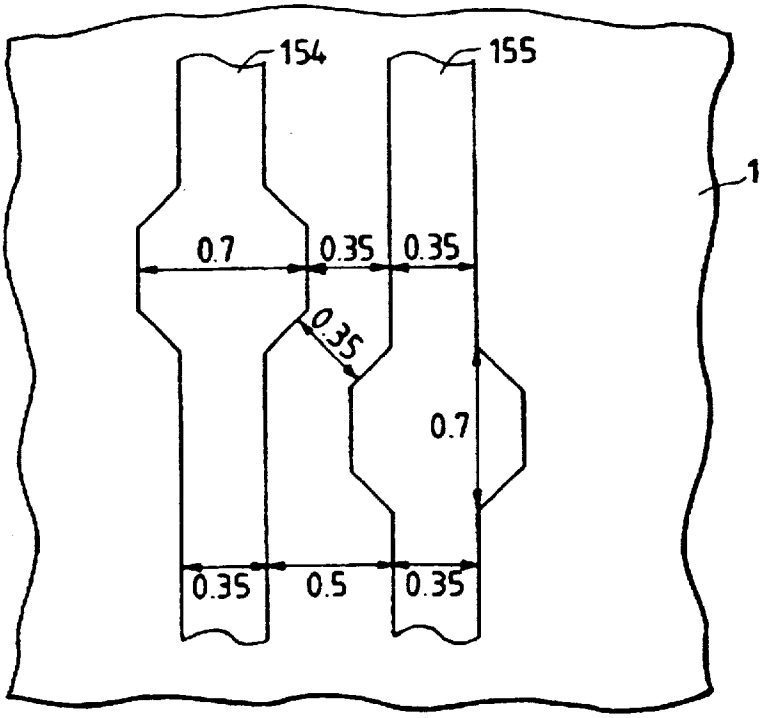

154
155
1
0.7
0.35
0.35
0.35
0.7
0.35
0.5
0.35

FIG. 53

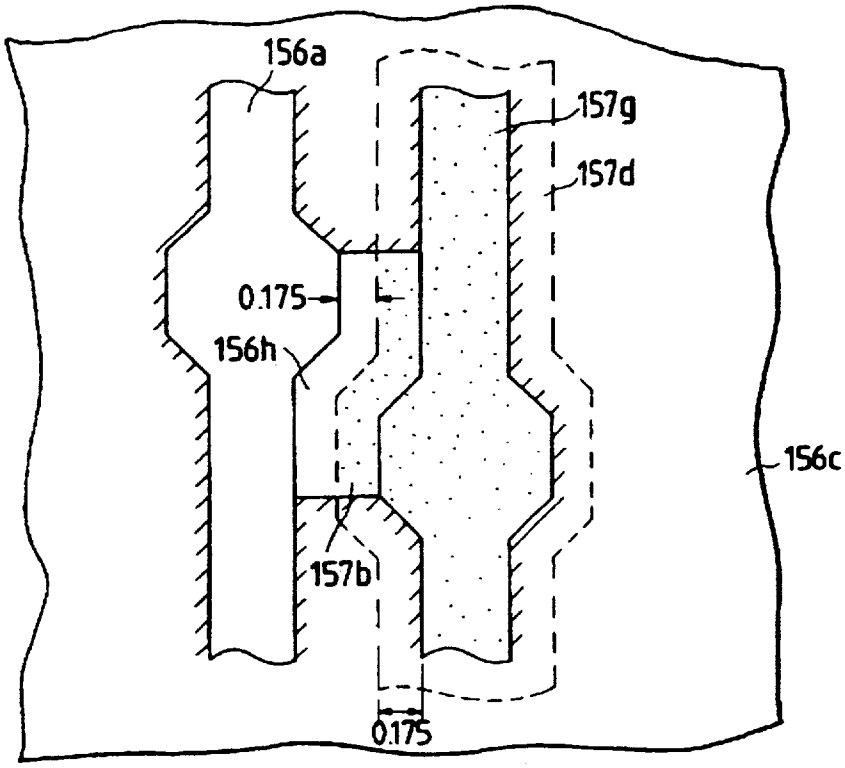

156a
157g
157d
0.175
156h
156c
157b
0.175

FIG. 54

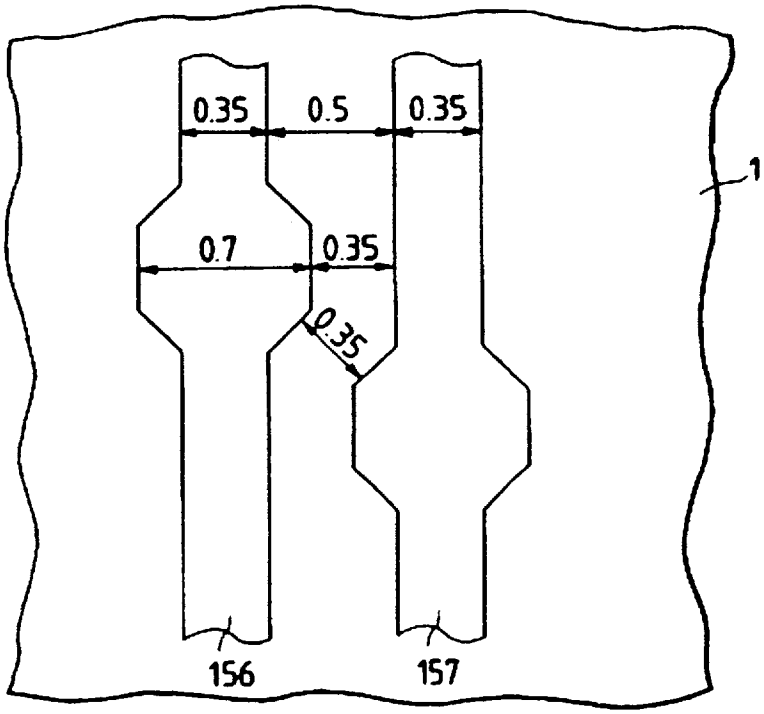

0.35
0.5
0.35
1
0.7
0.35
0.35
156
157

FIG. 55

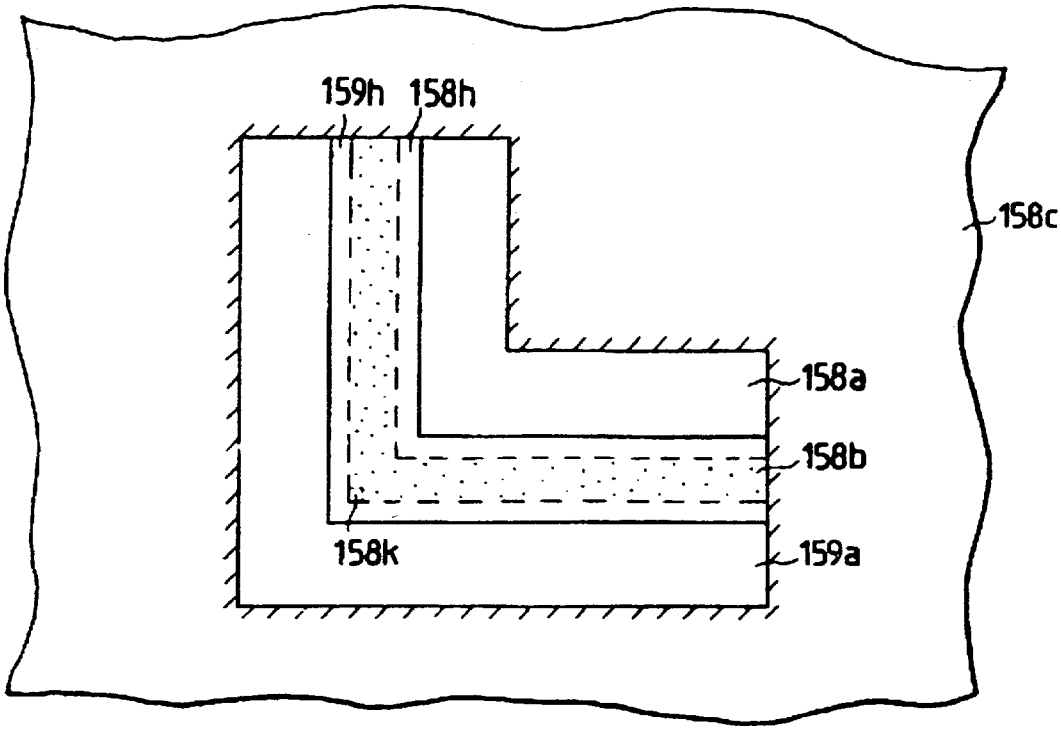


FIG. 56

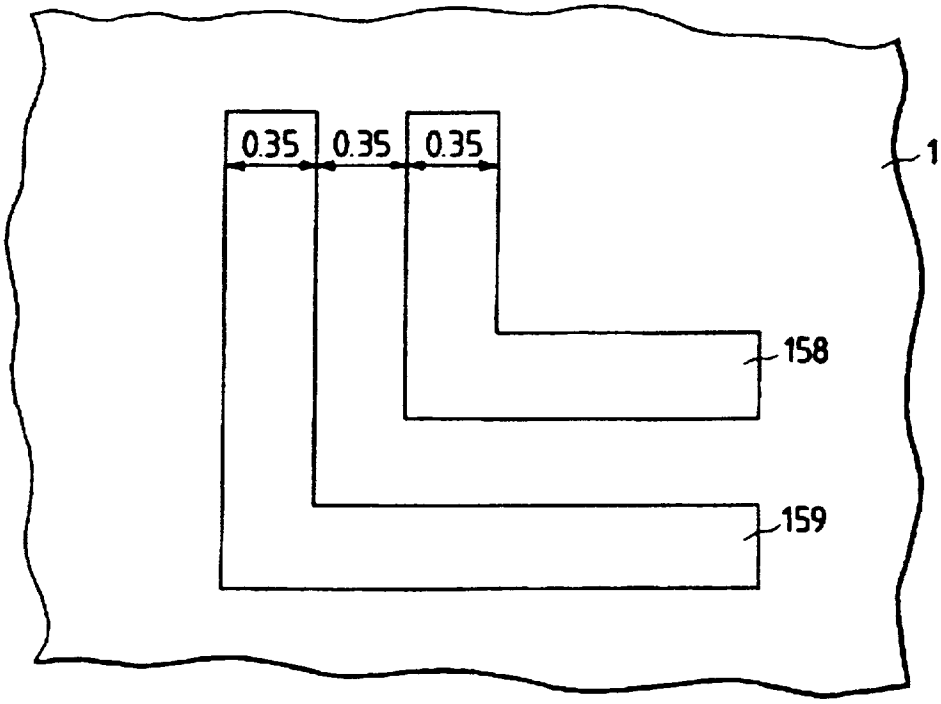


FIG. 57

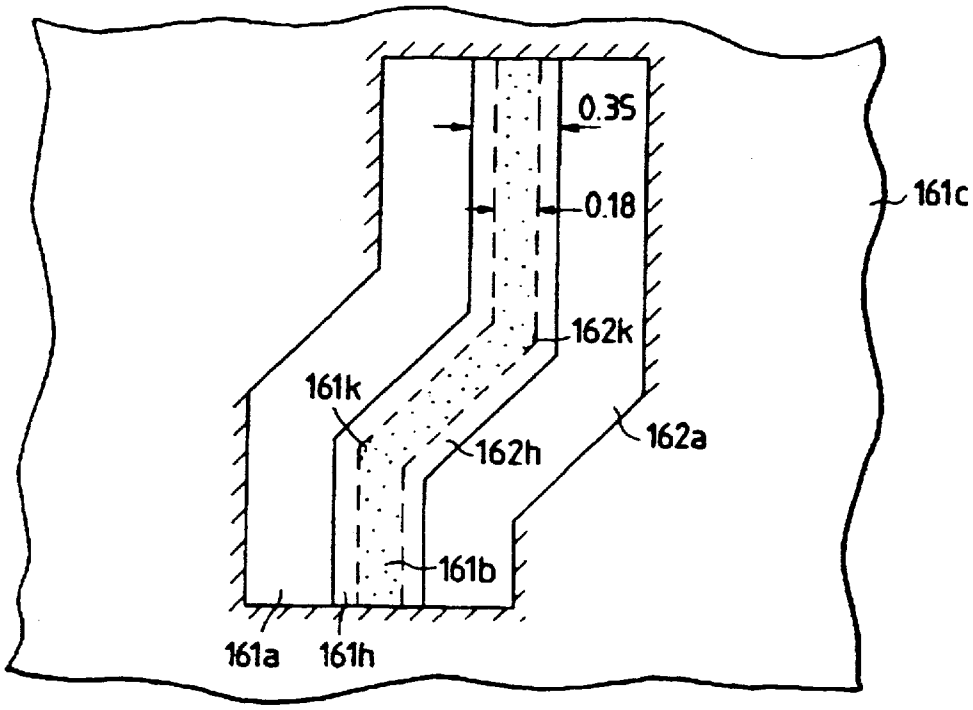

0.35
0.18
161c
162k
161k
162h
162a
161b
161a
161h

FIG. 58

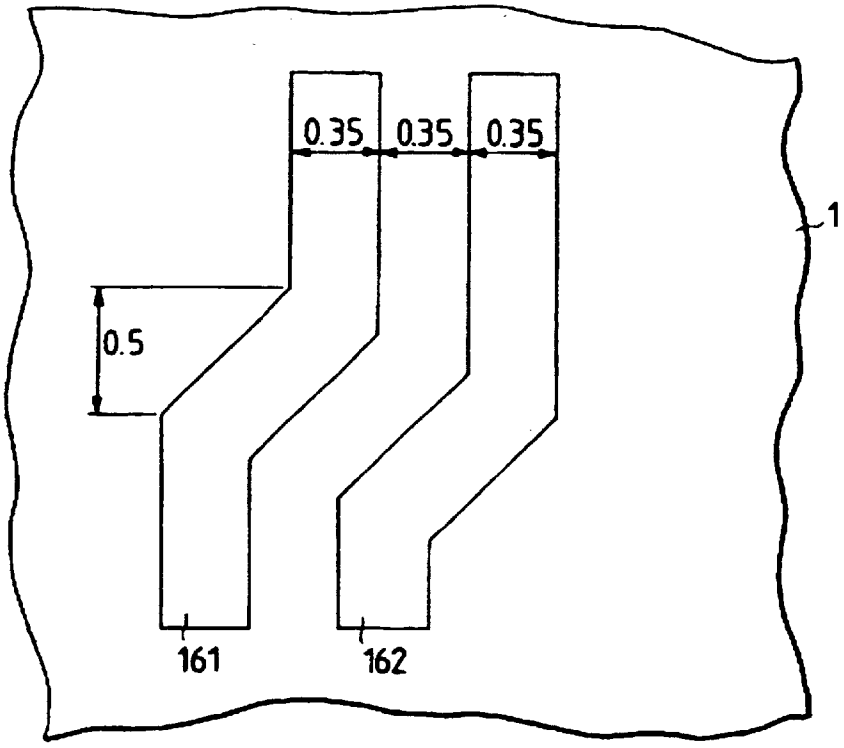

0.35
0.35
0.35
1
0.5
161
162

FIG. 59

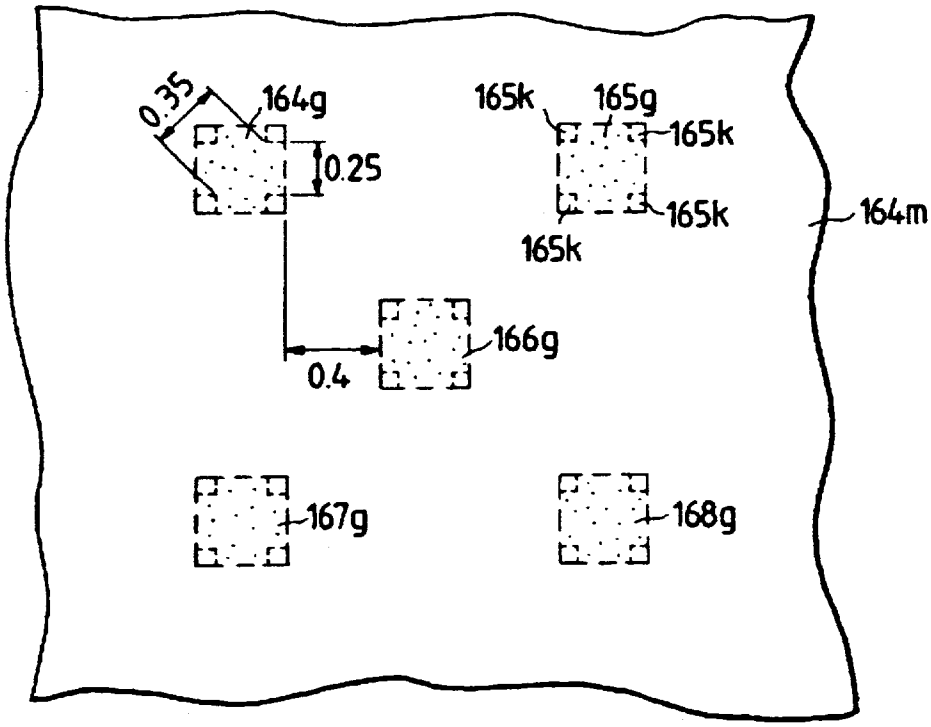

0.35
164g
0.25
165k
165g
165k
165k
165k
164m
166g
0.4
167g
168g

FIG. 60

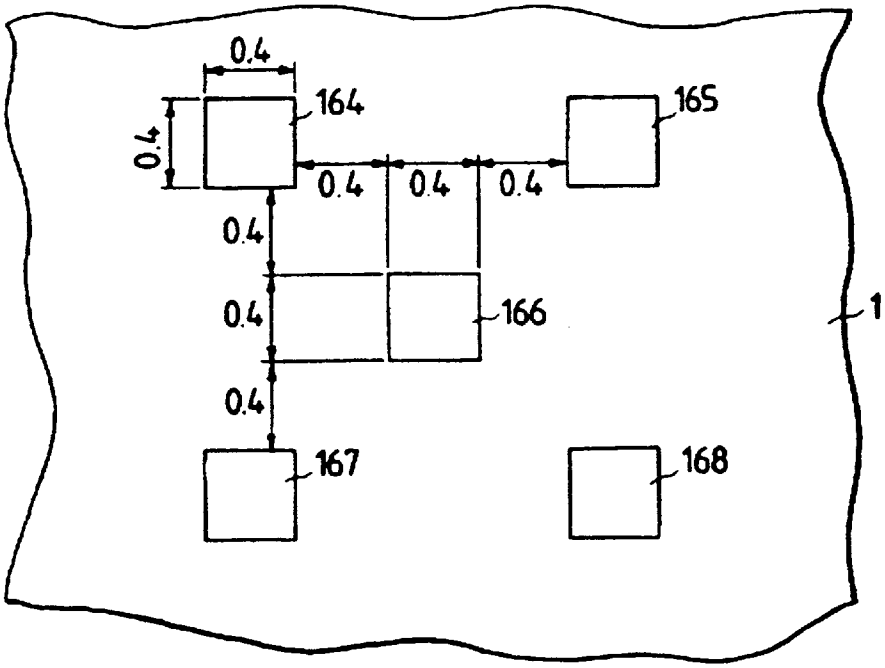

0.4
164
165
0.4
0.4
0.4
0.4
0.4
0.4
166
1
0.4
167
168

FIG. 61

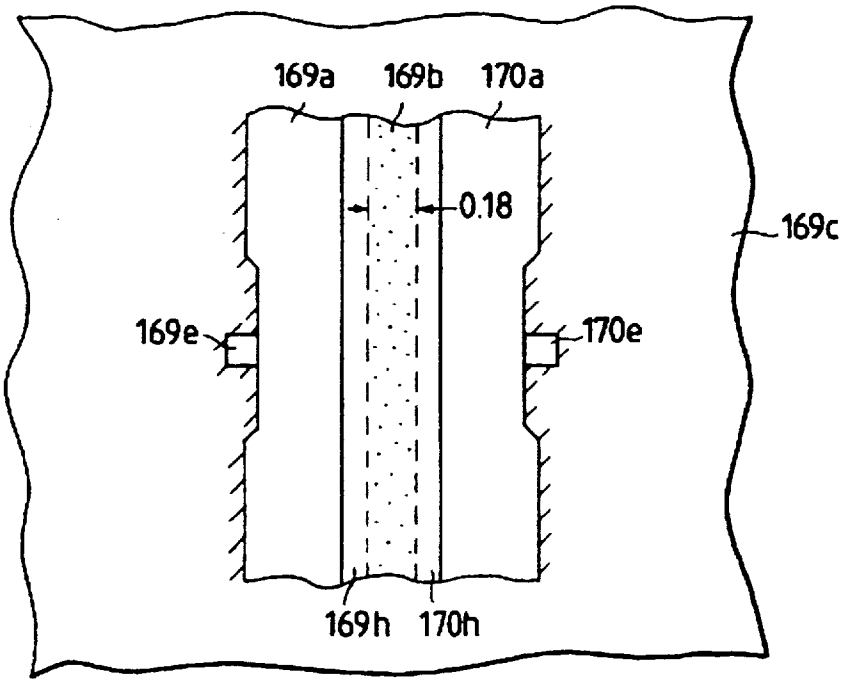

169a
169b
170a
0.18
169c
169e
170e
169h
170h

FIG. 62

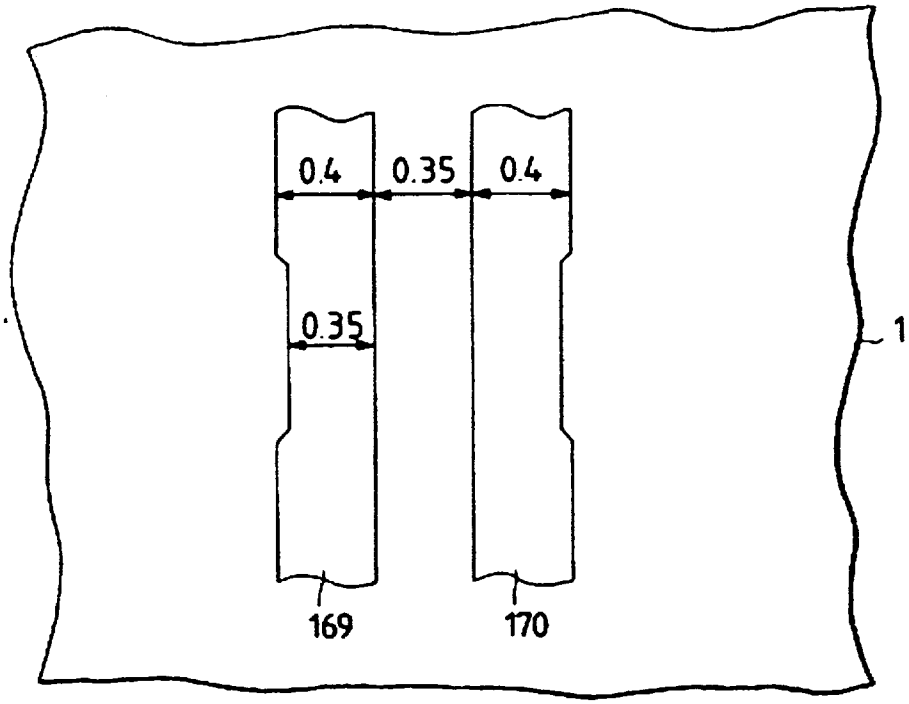

0.4
0.35
0.4
0.35
1
169
170

FIG. 63

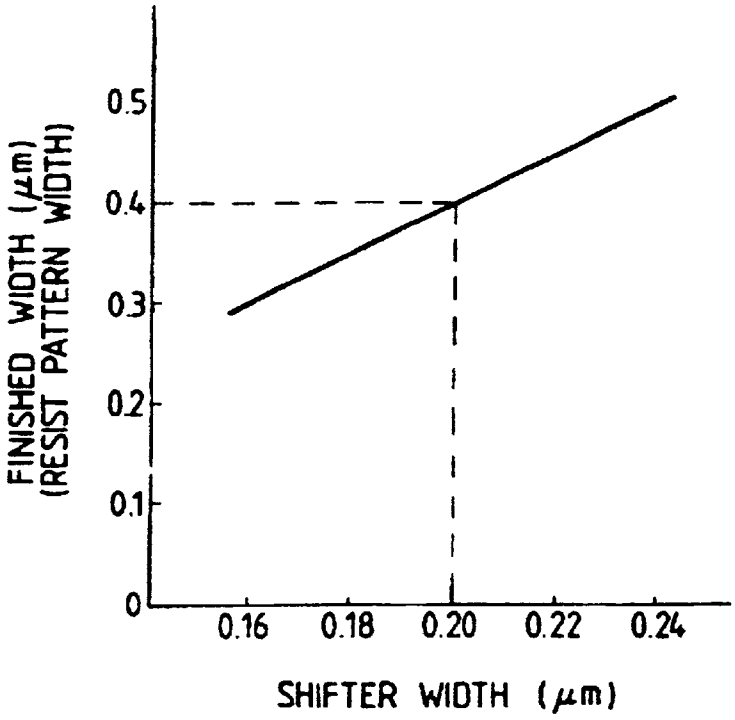

FINISHED WIDTH (μm)
(RESIST PATTERN WIDTH)
0.5
0.4
0.3
0.2
0.1
0
0.16
0.18
0.20
0.22
0.24
SHIFTER WIDTH (μm)

FIG. 64

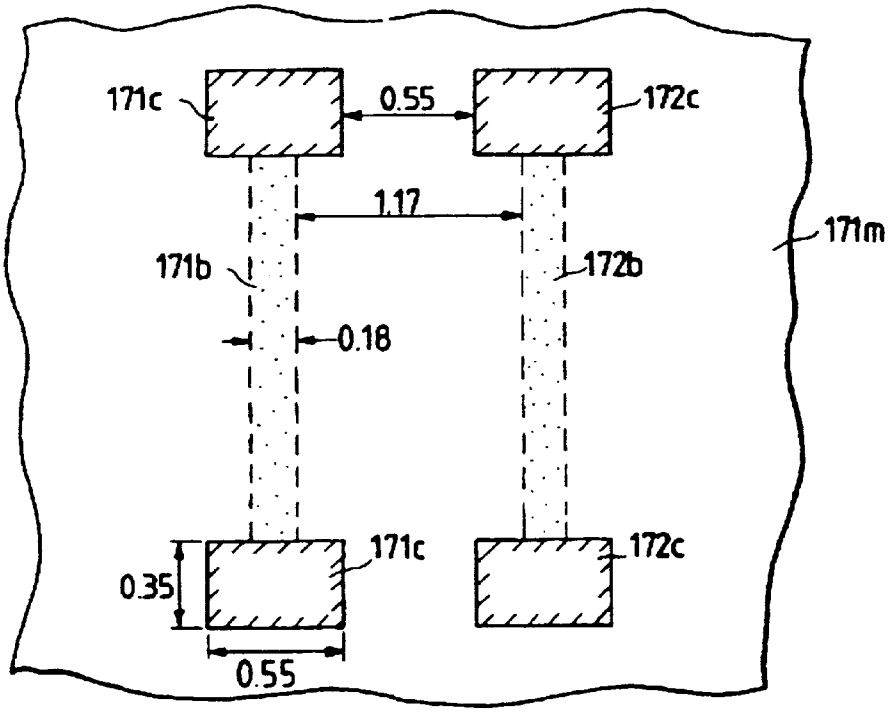

171c
0.55
172c
1.17
171m
171b
172b
0.18
171c
172c
0.35
0.55

FIG. 65

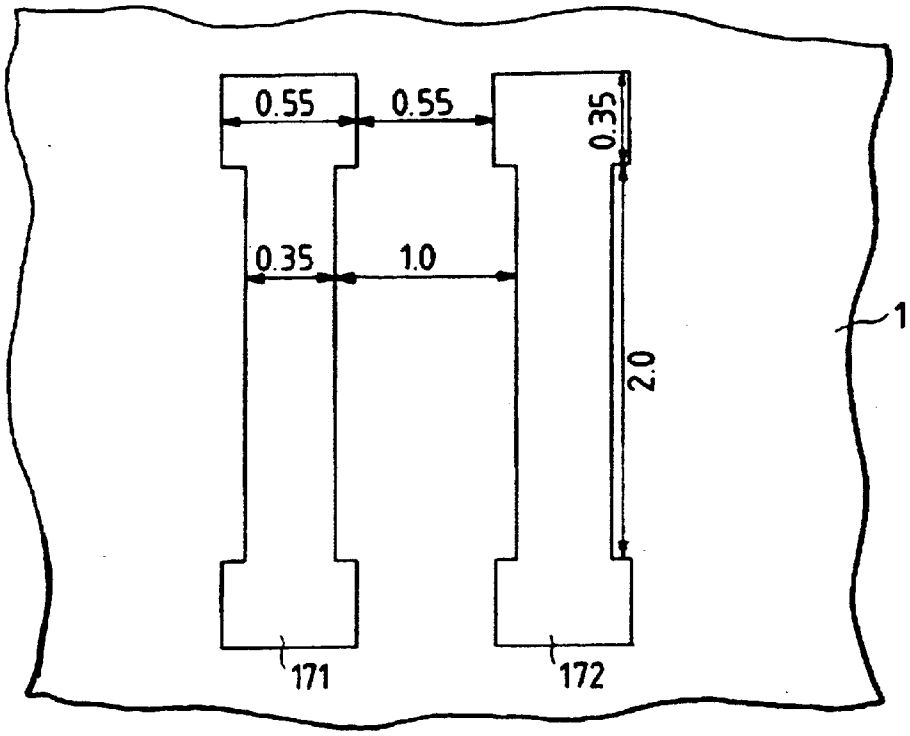

0.55
0.55
0.35
0.35
1.0
2.0
1
171
172

FIG. 66

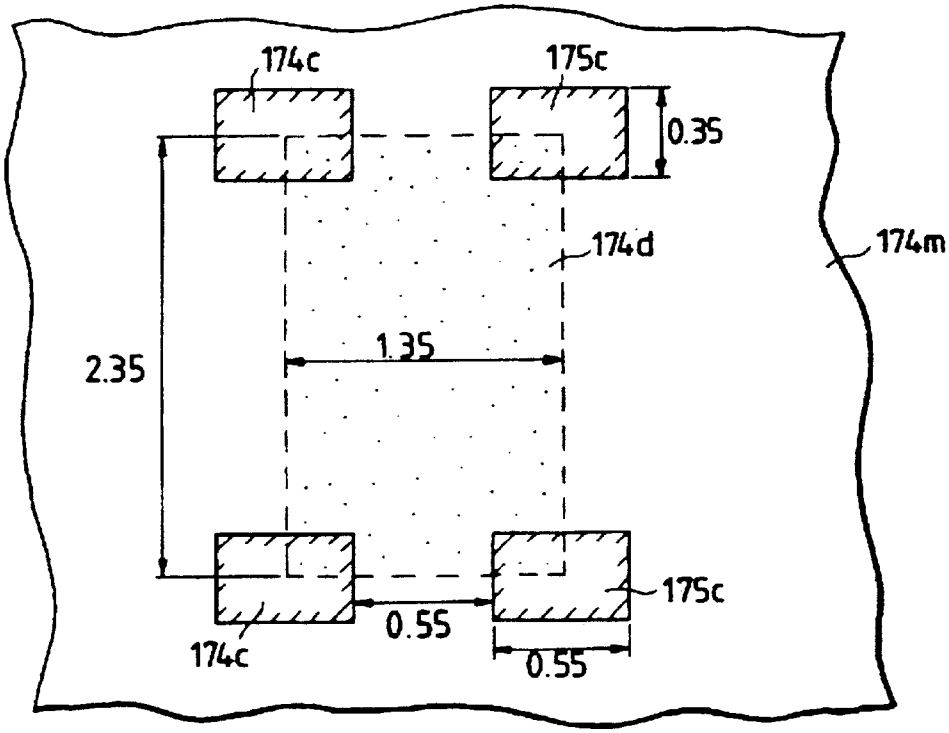

174c
175c
0.35
174d
174m
2.35
1.35
175c
0.55
174c
0.55

FIG. 67

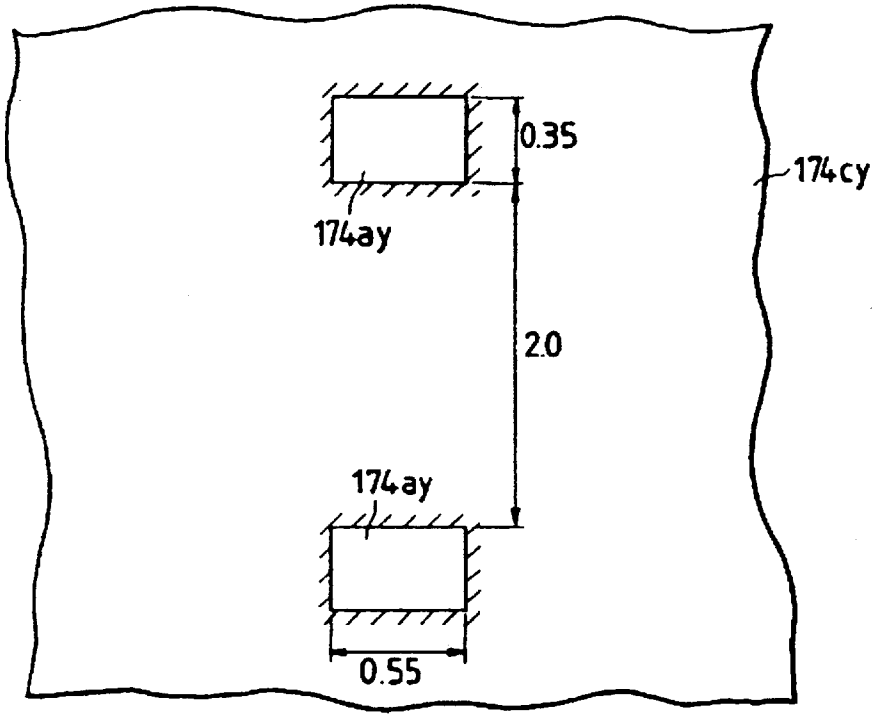


FIG. 68

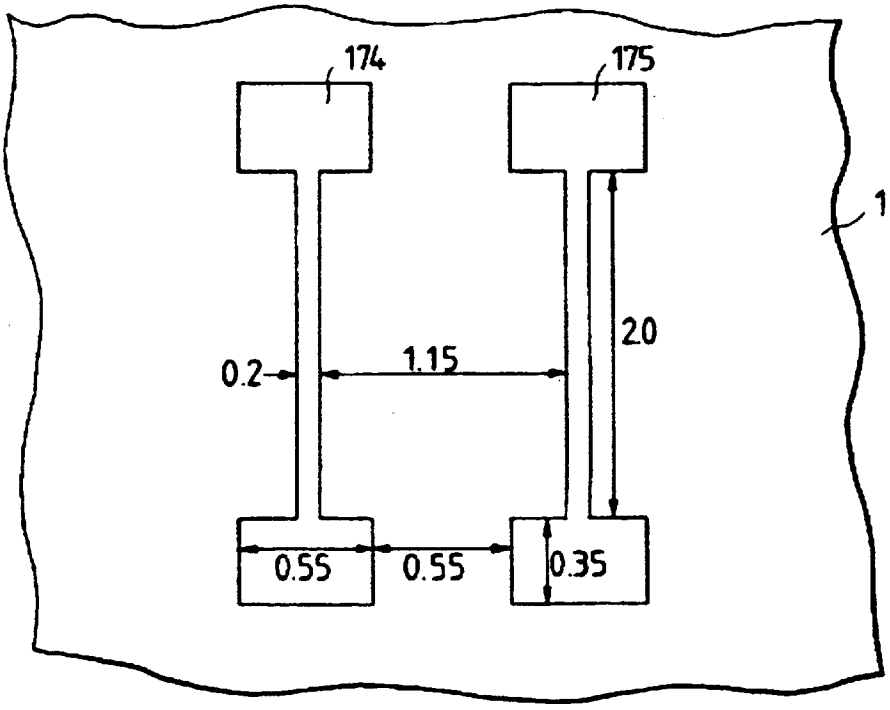


FIG. 69

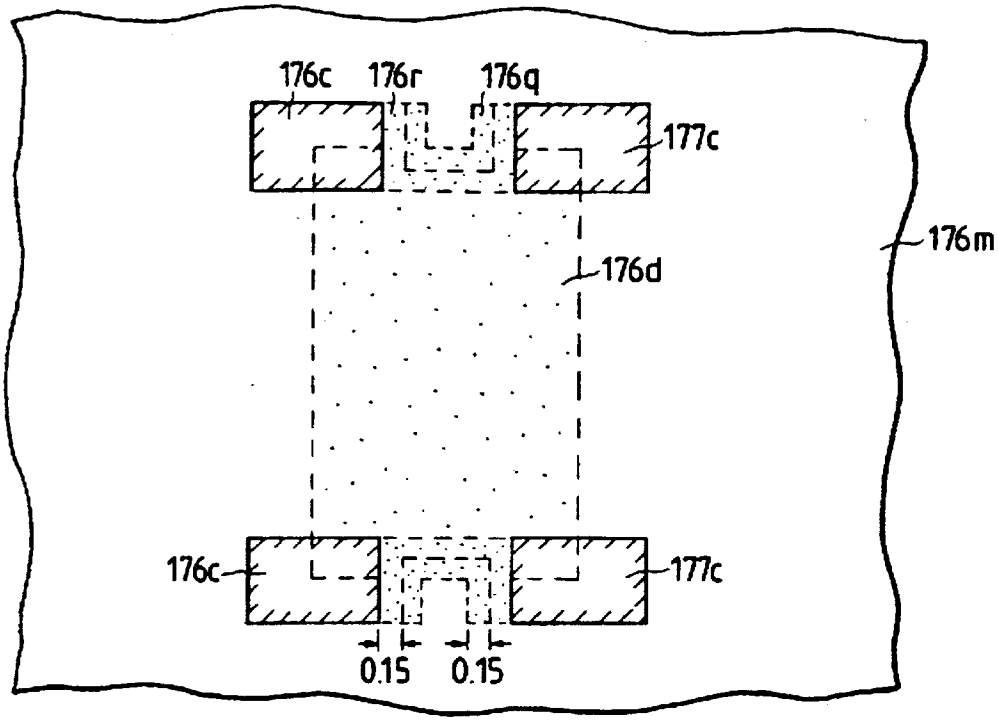


FIG. 70

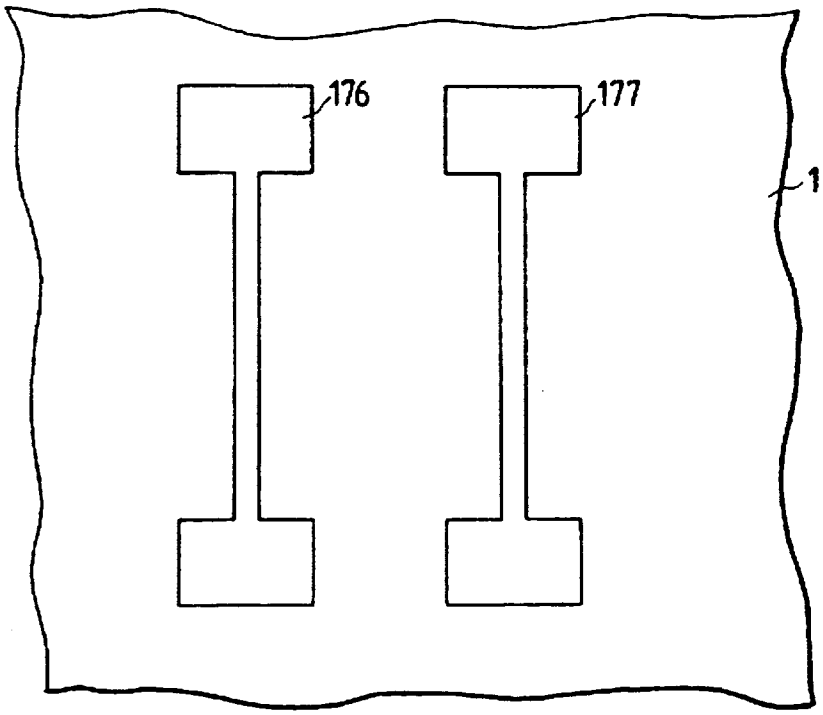


FIG. 71

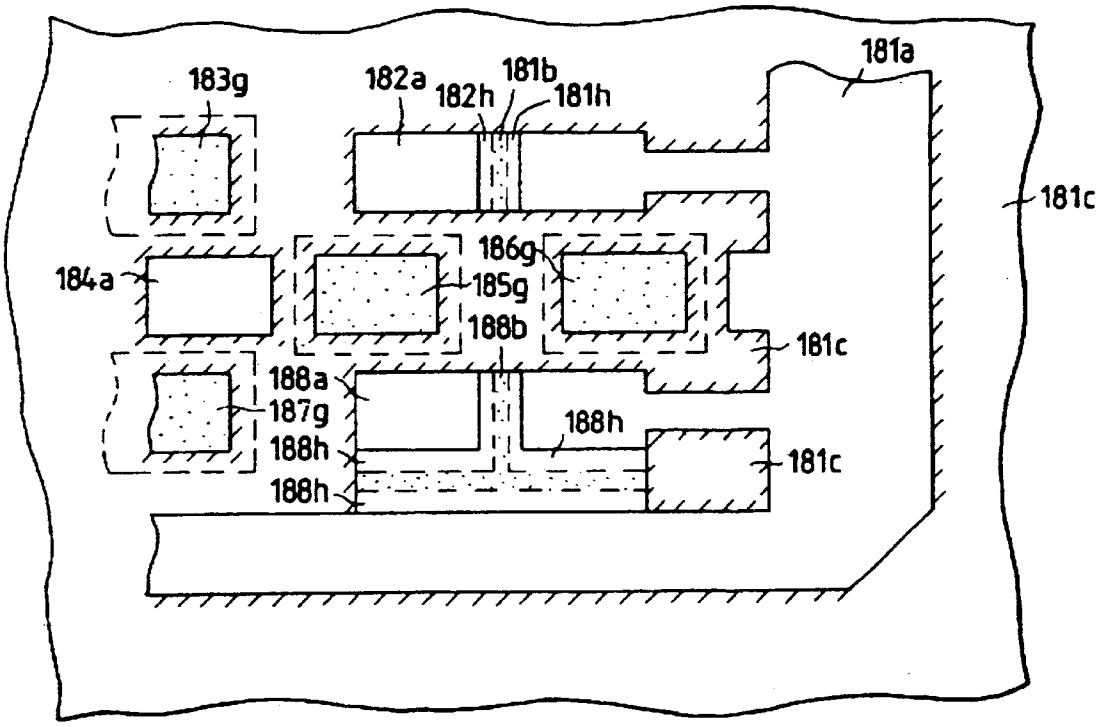

183g
182a
182h
181b
181h
181a
181c
184a
186g
185g
188b
181c
188a
187g
188h
188h
188h
181c

FIG. 72

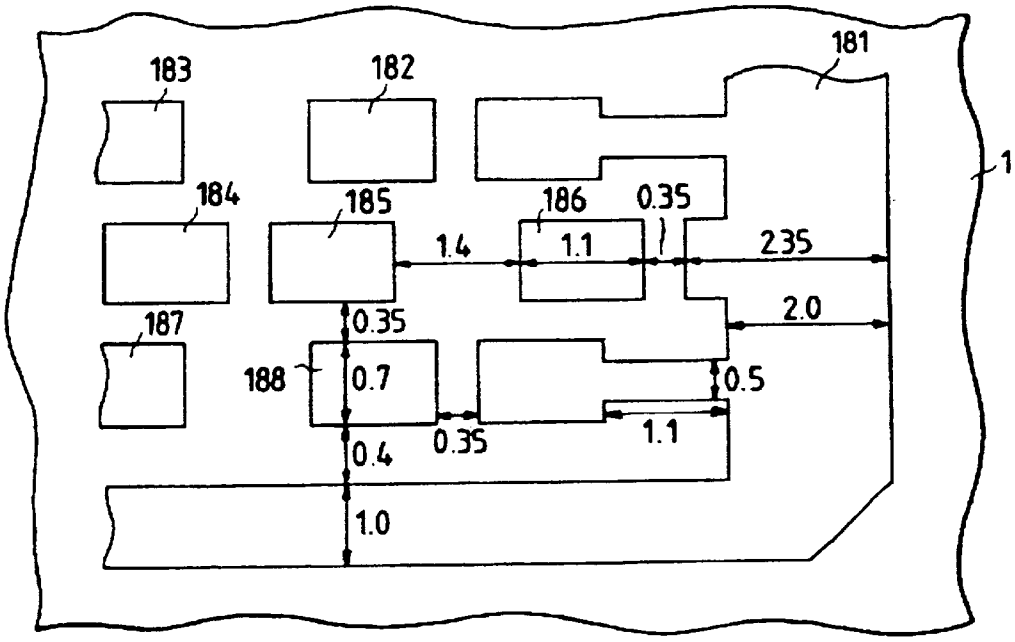

183
182
181
1
184
185
186
0.35
1.4
1.1
2.35
2.0
187
0.35
188
0.7
0.5
0.35
1.1
0.4
1.0

FIG. 73

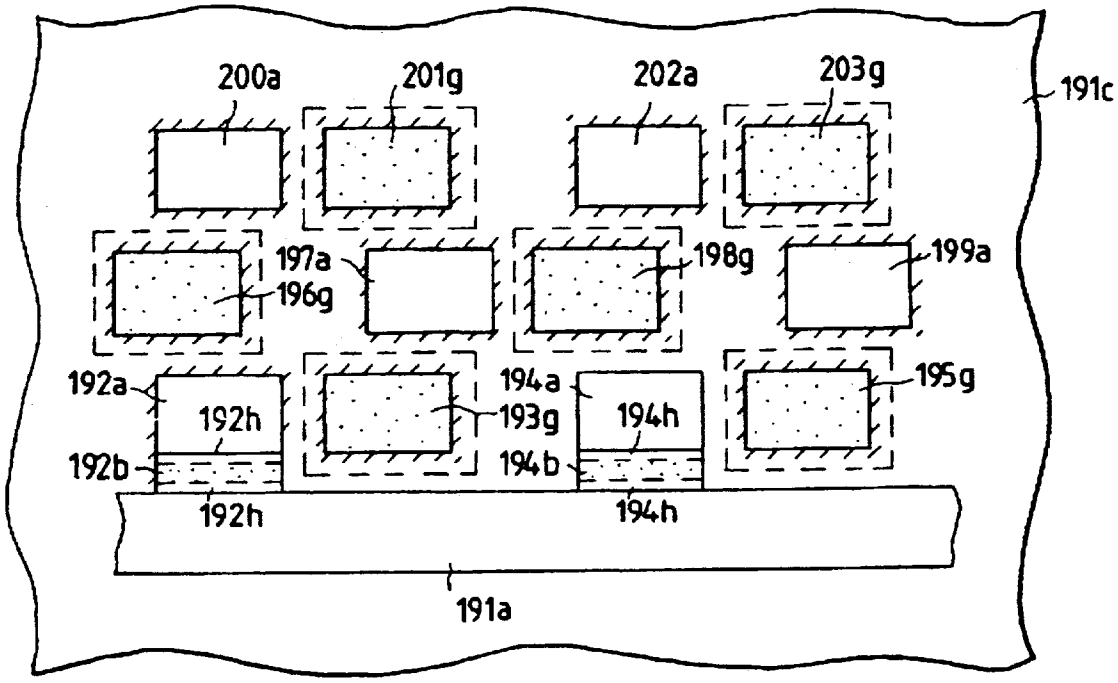

200a
201g
202a
203g
191c
197a
196g
198g
199a
192a
192h
193g
194a
194h
195g
192b
194b
192h
194h
191a

FIG. 74

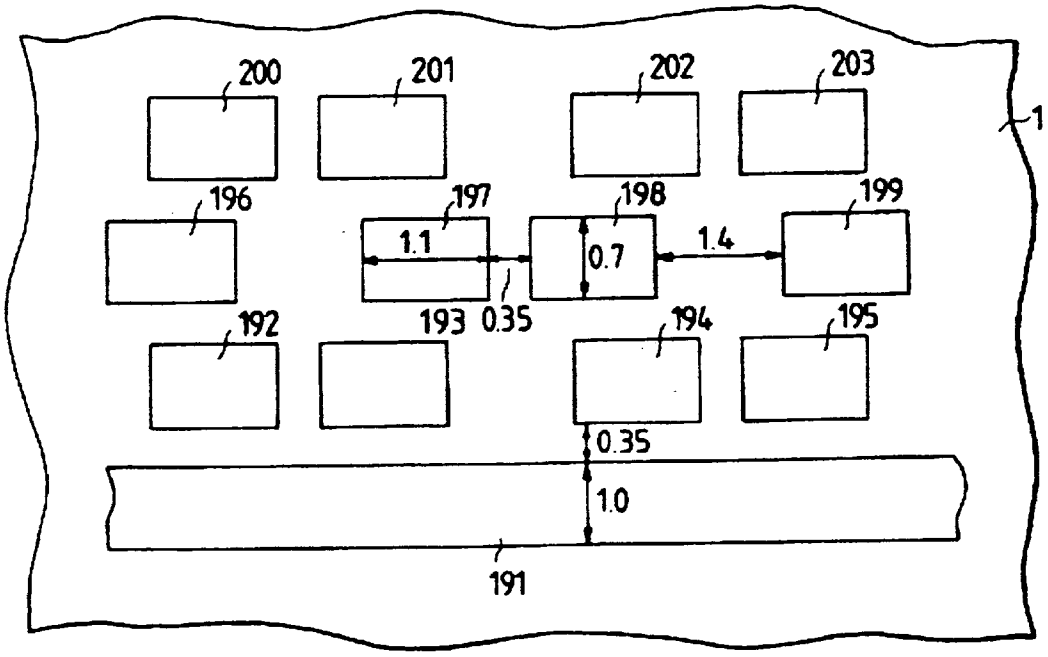

200
201
202
203
1
196
197
198
199
1.1
0.7
1.4
192
193
0.35
194
195
0.35
1.0
191

FIG. 76

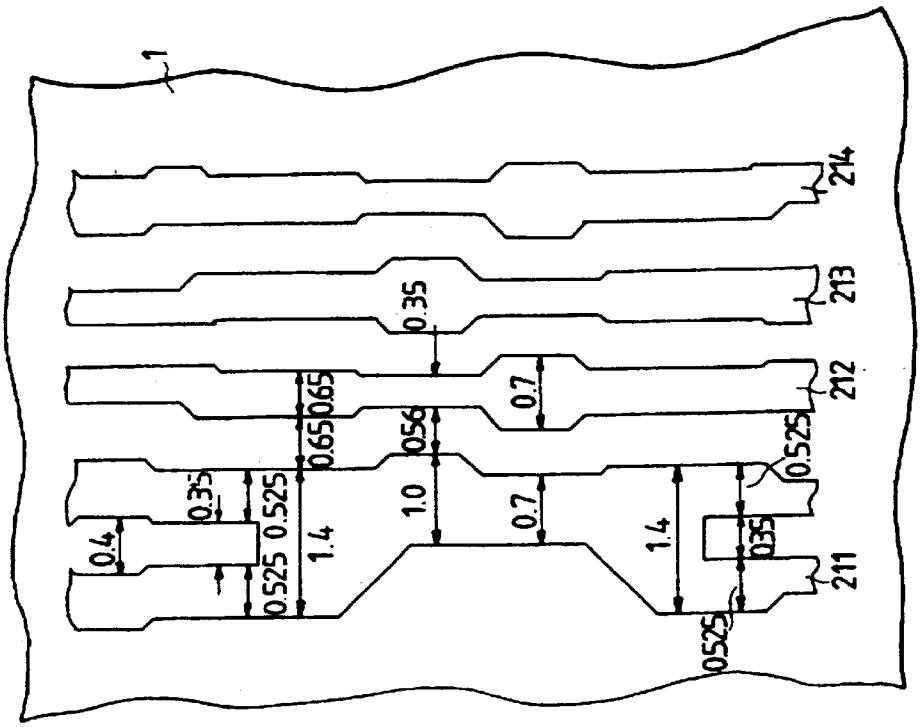

1
214
213
212
211
0.4
0.35
0.525
0.525
1.4
0.65
0.65
0.35
1.0
0.56
0.7
0.7
1.4
0.525
0.35
0.525

FIG. 75

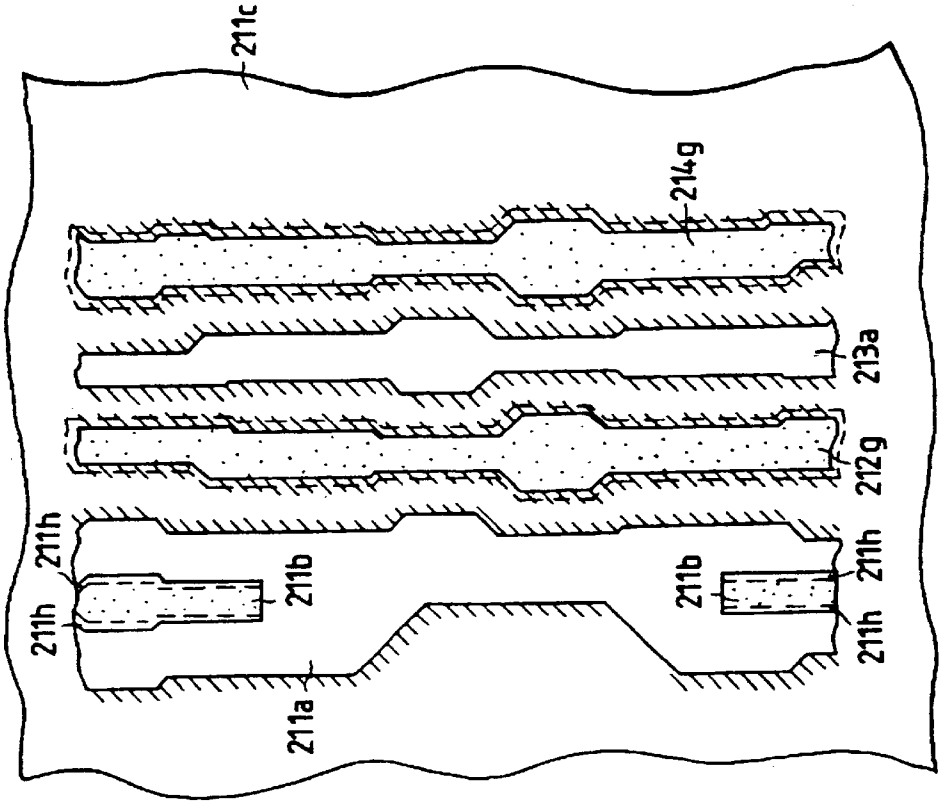

211c
214g
213a
212g
211h
211h
211b
211b
211h
211h
211a

FIG. 77

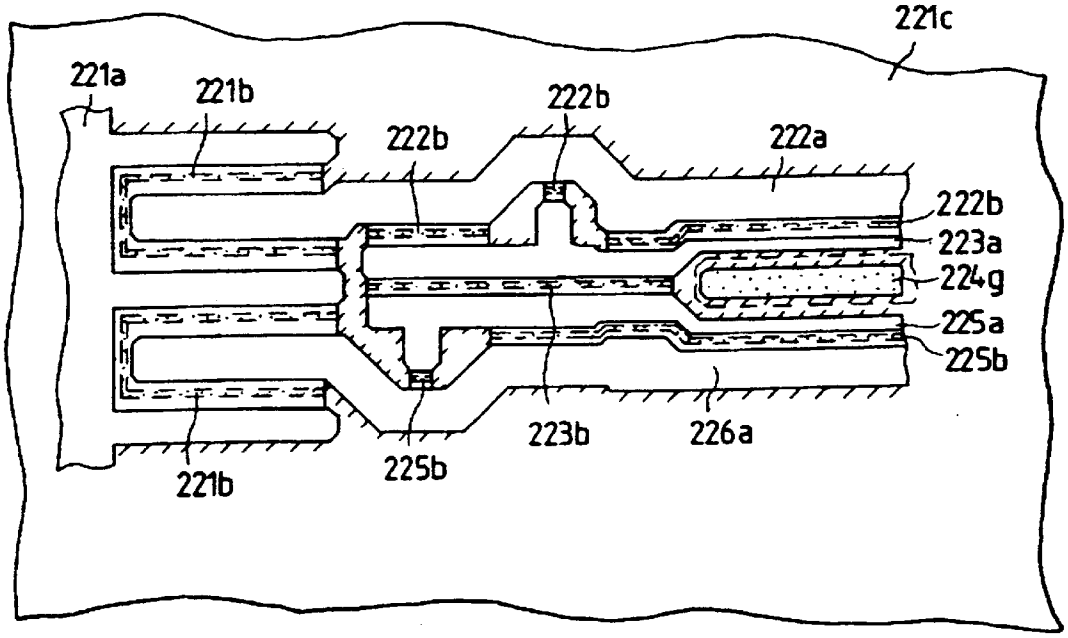

221c
221a
221b
222b
222b
222a
222b
223a
224g
225a
225b
223b
226a
221b
225b

FIG. 78

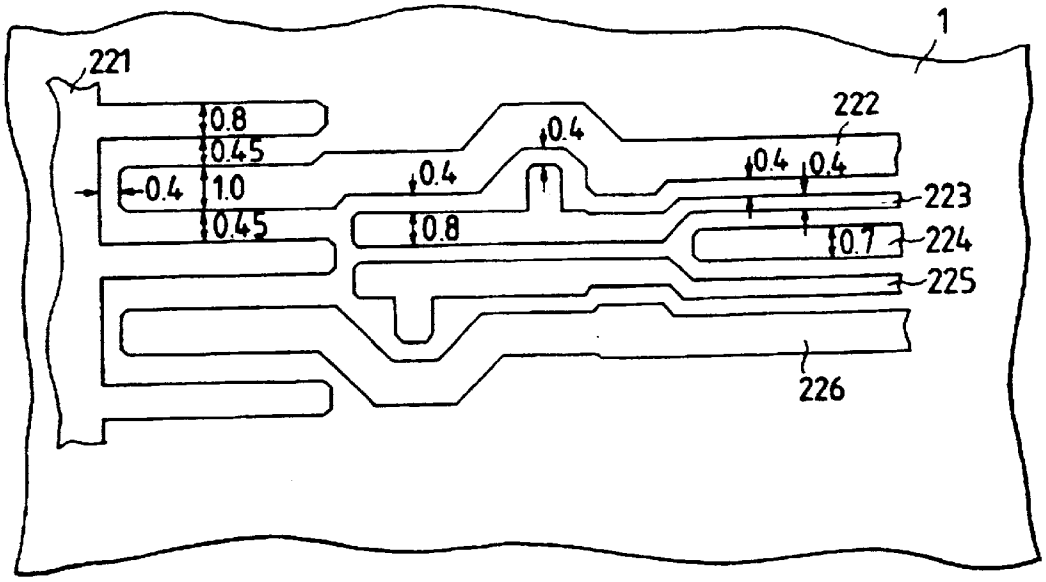

1
221
0.8
0.45
0.4
1.0
0.45
0.4
0.4
0.8
222
0.4
0.4
223
0.7
224
225
226

FIG. 80

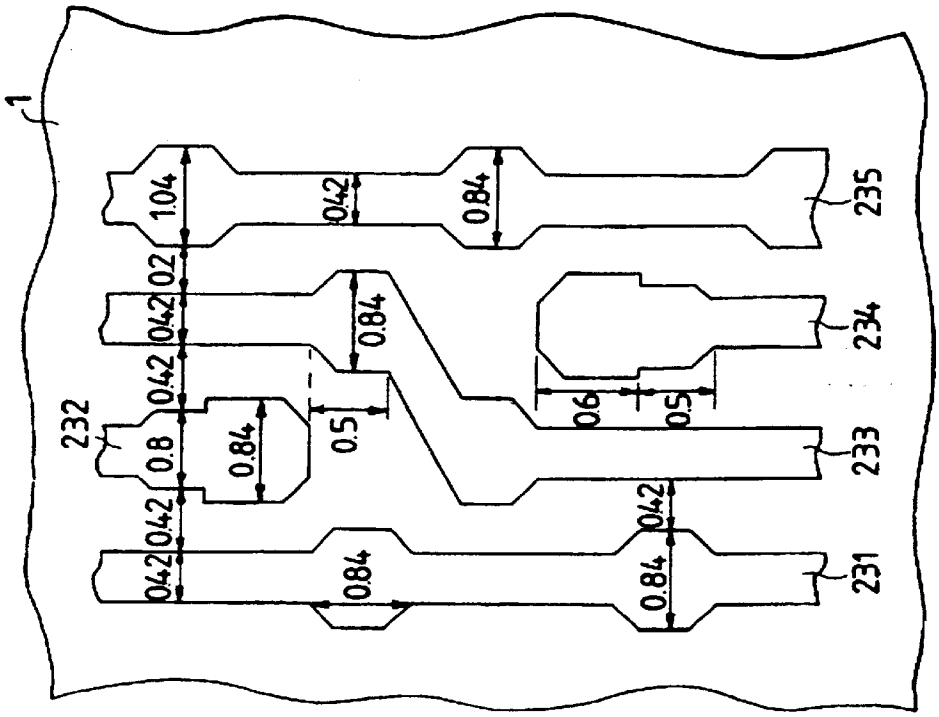

1
232
1.04
0.42
0.84
0.2
0.8
0.5
0.6
231
233
234
235

FIG. 79

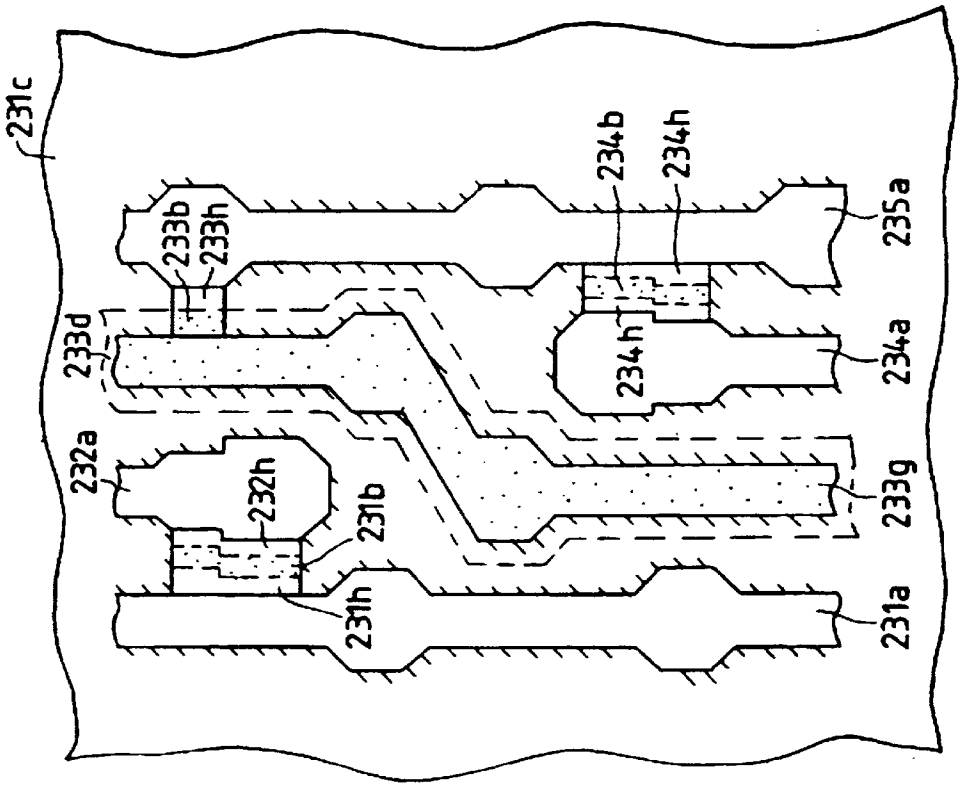

231c
232a
232h
231b
231h
233d
233b
233h
234b
234h
234a
233g
235a
231a

FIG. 81

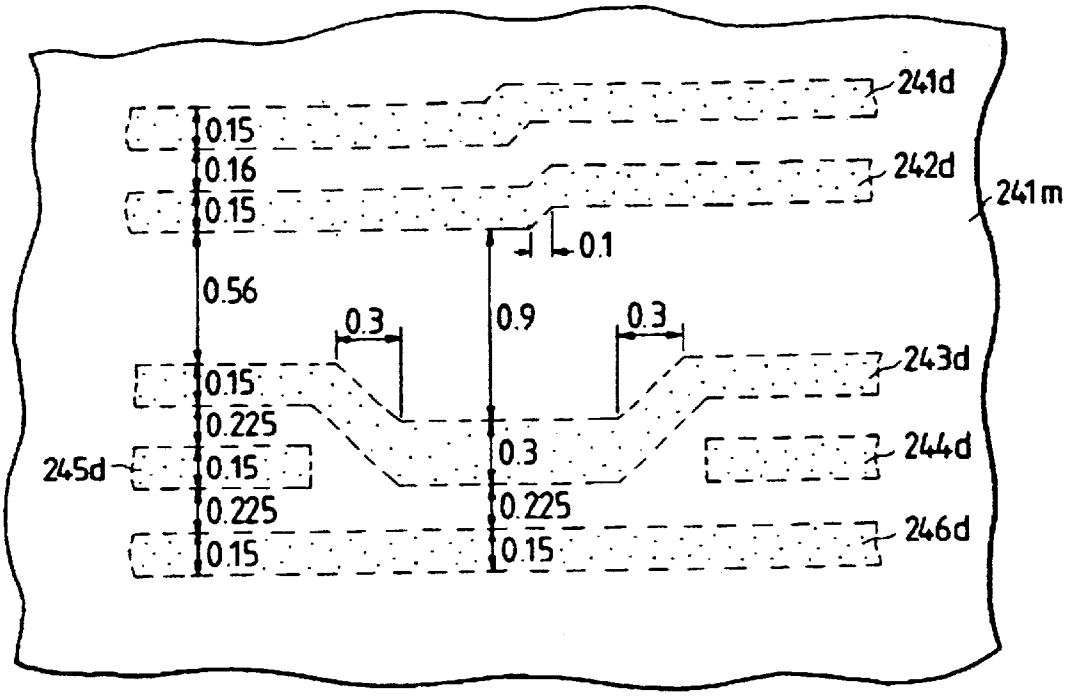

241d
242d
241m
0.15
0.16
0.15
0.1
0.56
0.3
0.9
0.3
243d
0.15
0.225
244d
245d
0.15
0.3
0.225
0.225
246d
0.15
0.15

FIG. 82

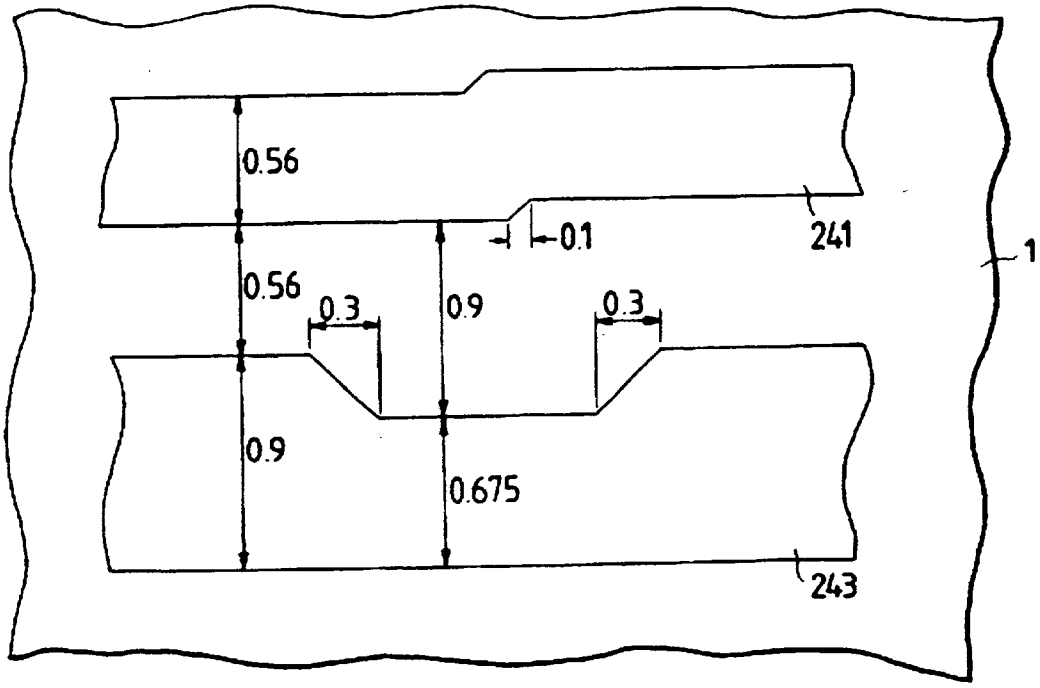

0.56
0.1
241
1
0.56
0.3
0.9
0.3
0.9
0.675
243

FIG. 83

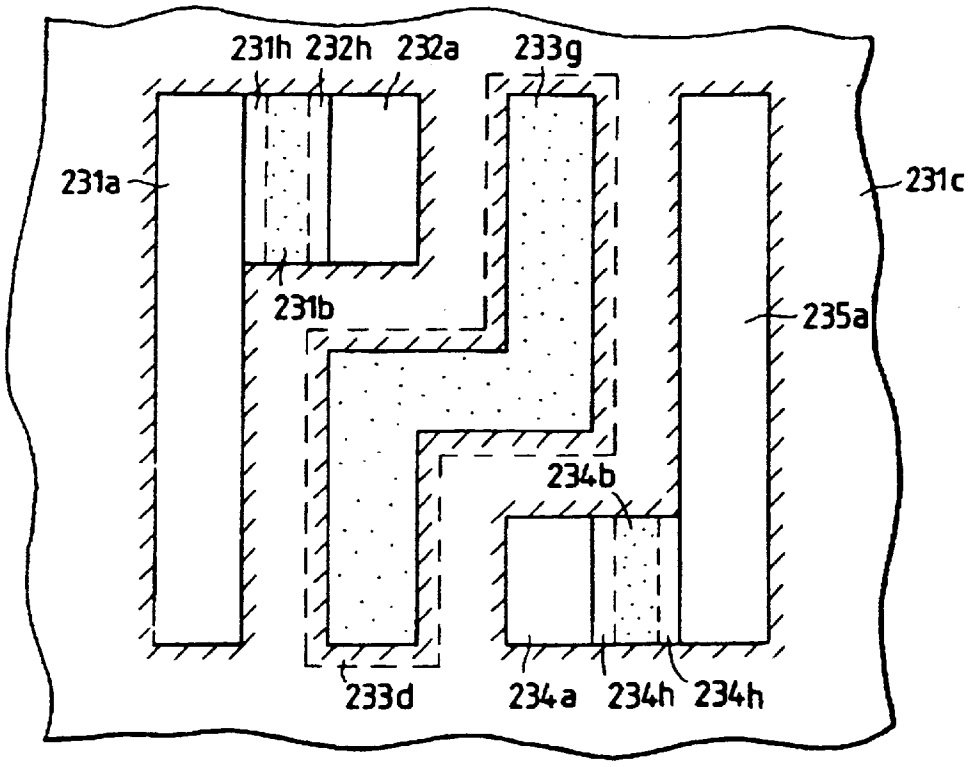
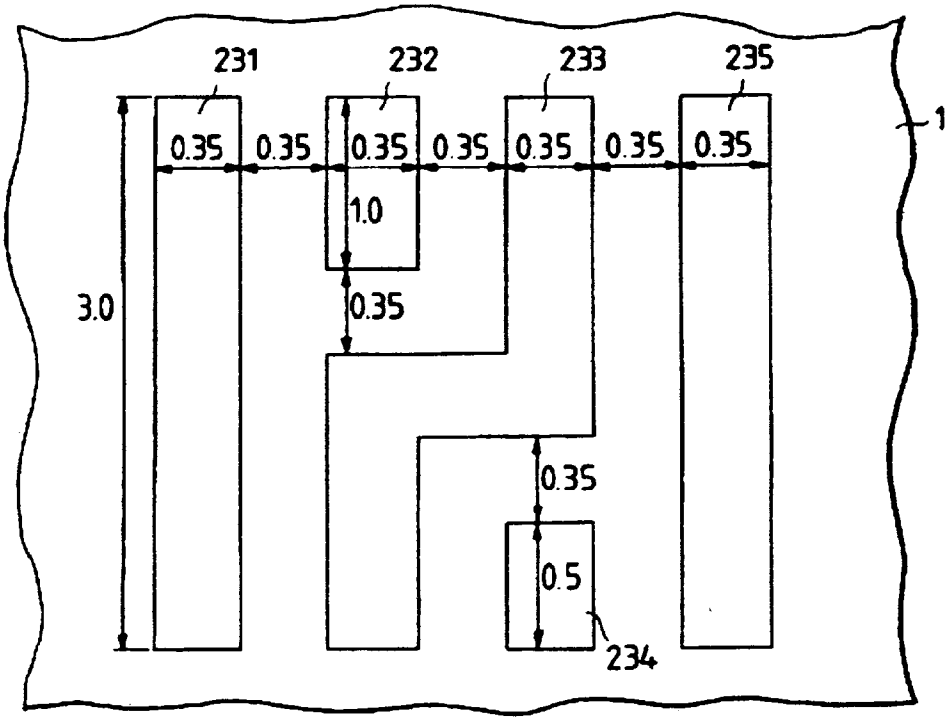

231h
232h
232a
233g
231a
231c
231b
235a
234b
233d
234a
234h
234h

FIG. 84


231
232
233
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0.35
0.35
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0.35
0.35
0.35
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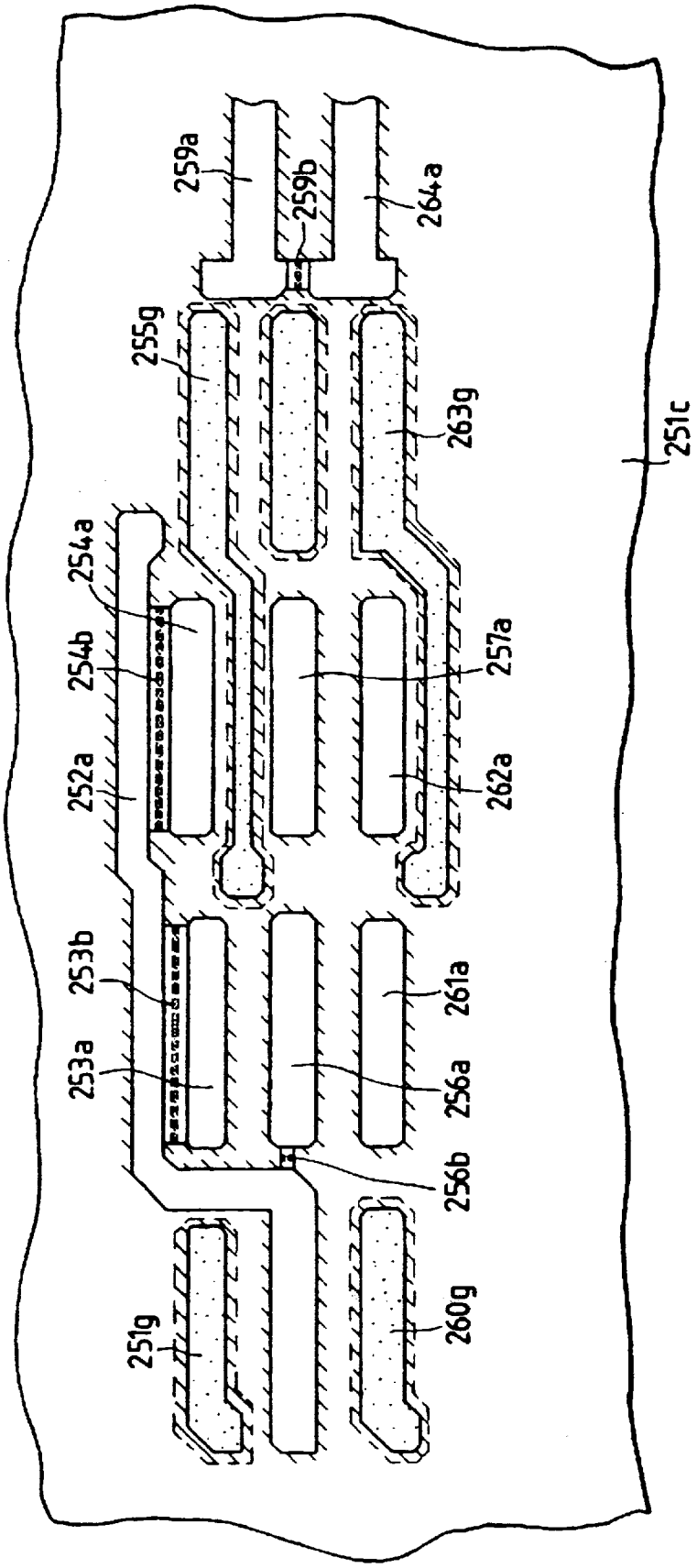
3.0
0.35
0.35
0.5
234

FIG. 85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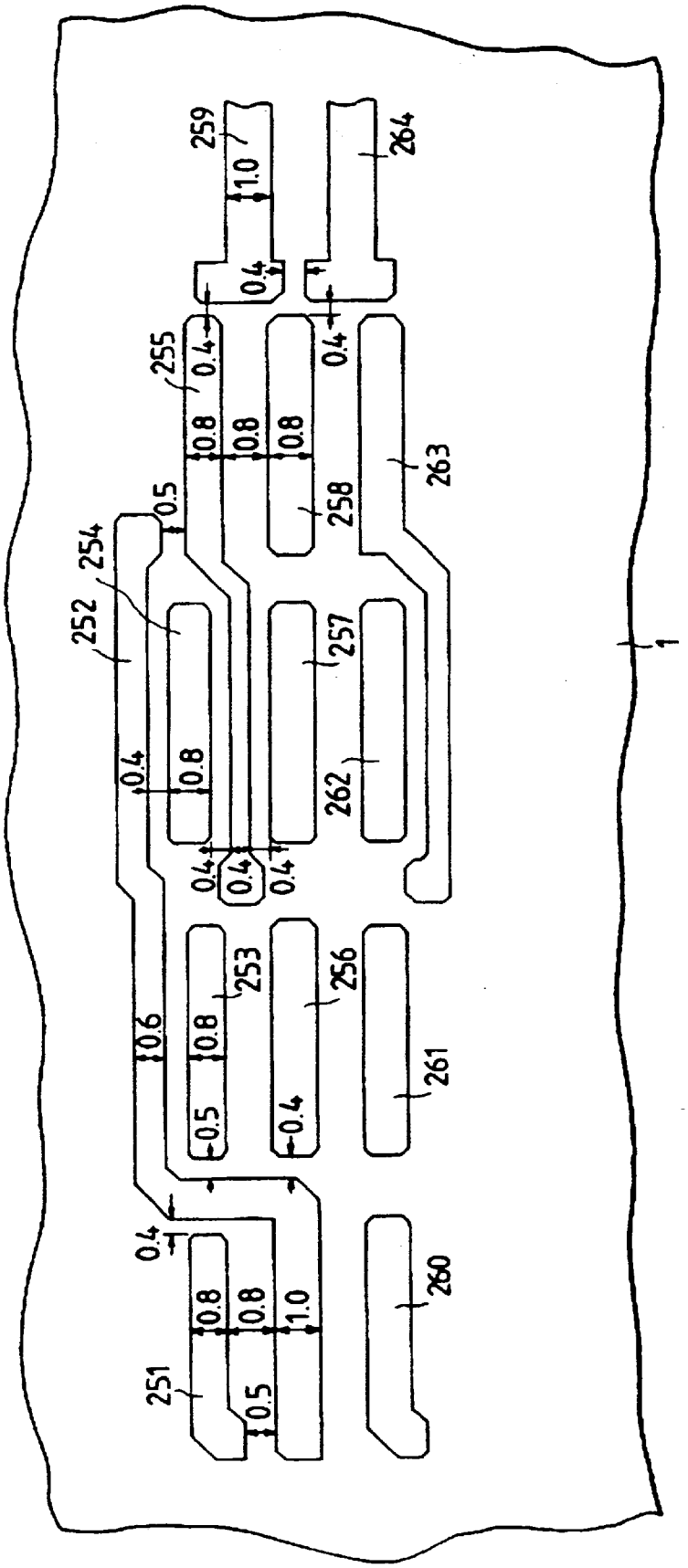
251g
260g


259
1.0
0.4
264
255
0.4
0.4
0.8
0.8
0.8
263
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258
254
252
257
1
0.4
0.8
262
0.4
0.4
0.4
253
256
0.6
0.8
261
0.5
0.4
0.4
0.8
0.8
1.0
260
251
0.5

FIG. 86

FIG. 87

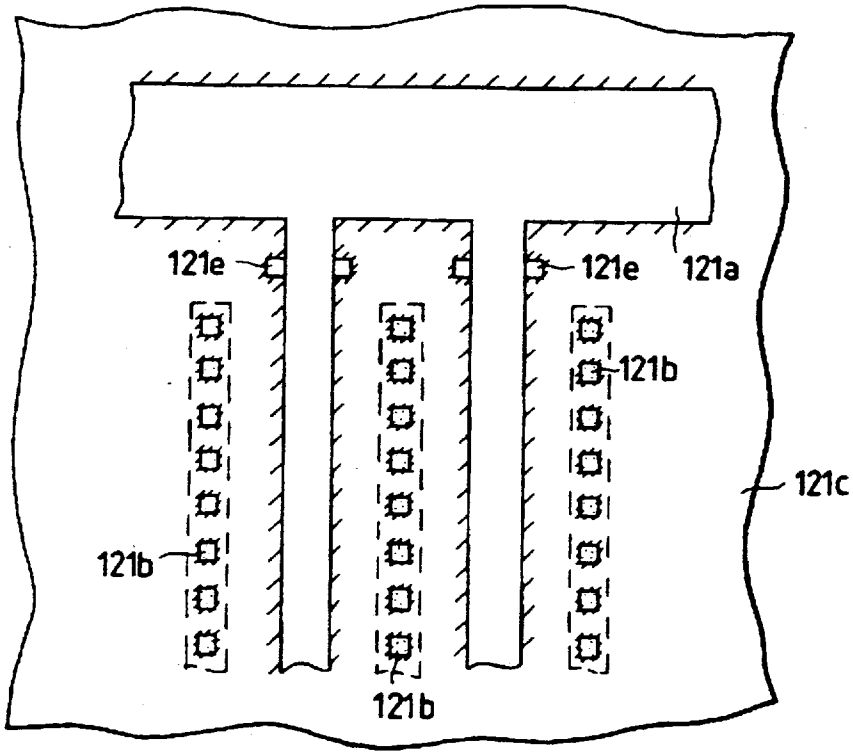


FIG. 88

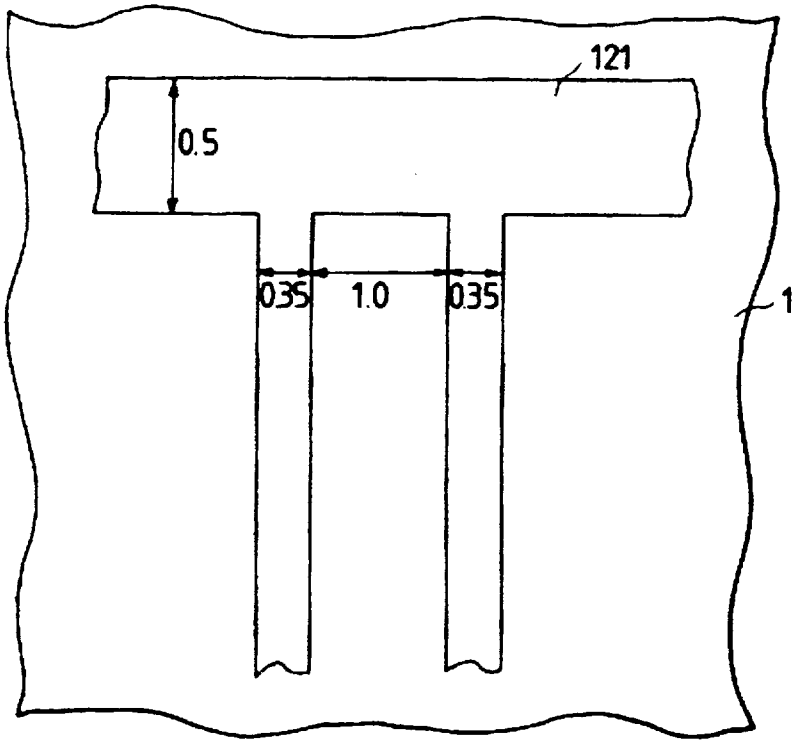


FIG. 89

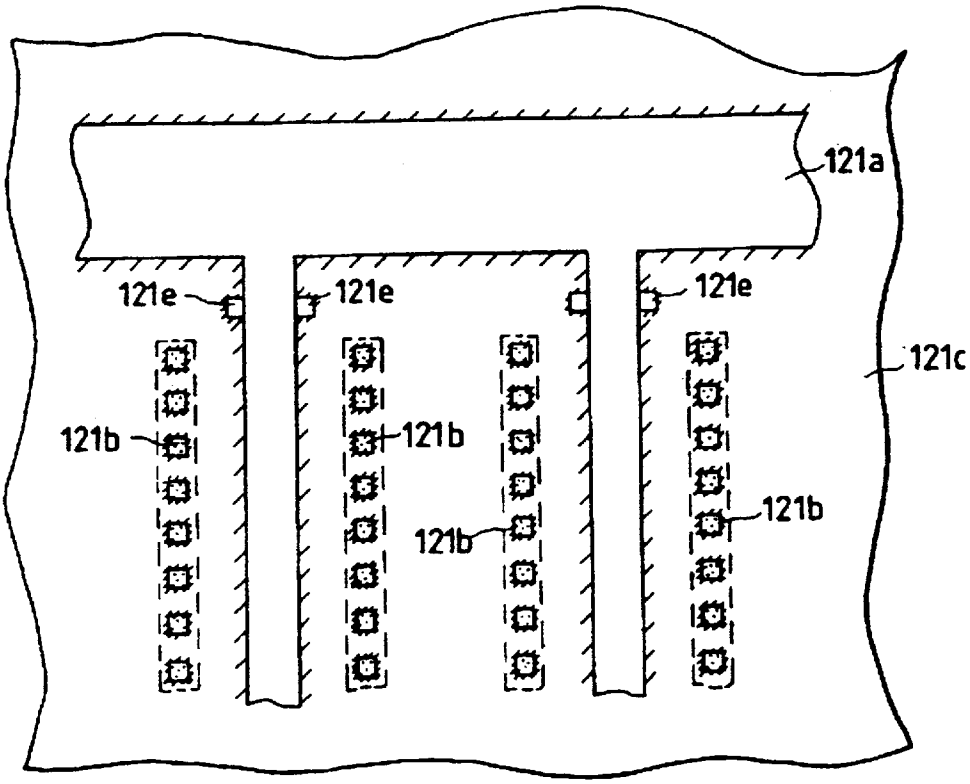
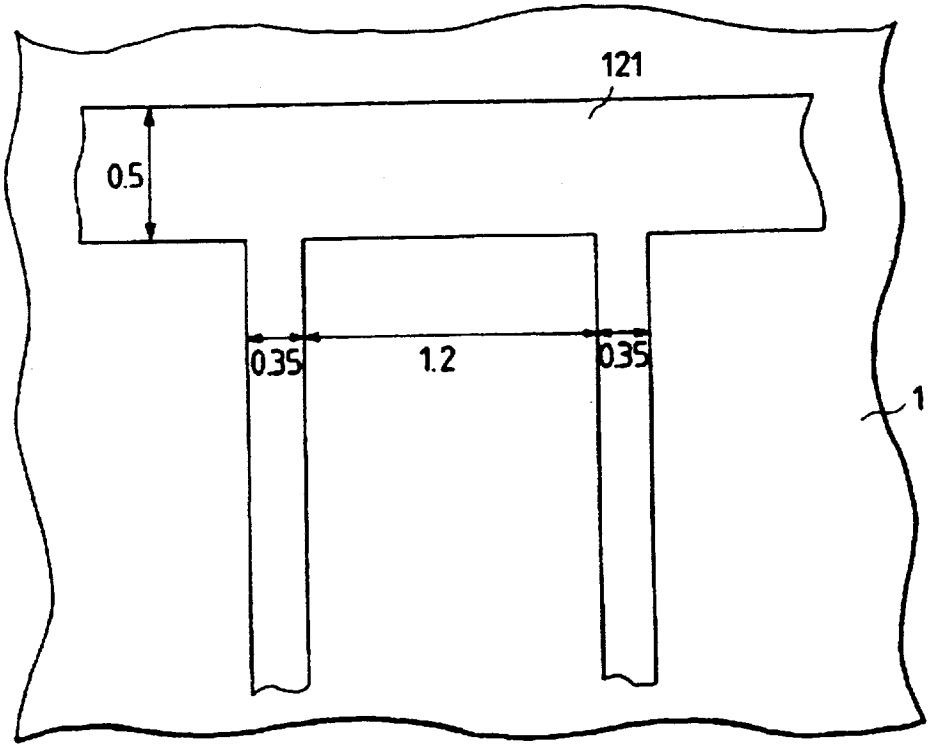

121a
121e
121e
121e
121c
121b
121b
121b
121b

FIG. 90


121
0.5
0.35
1.2
0.35
1

MANUFACTURING METHOD OR AN EXPOSING METHOD FOR A SEMICONDUCTOR DEVICE OR A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND A MASK USED THEREFOR

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

This application is a Continuation application of prior application Ser. No. [08/433,431,] *08/443,431,* filed May 18, 1995 now U.S. Pat. No. 5,578,422, which is a Continuation application of application Ser. No. 07/912,511, filed Jul. 13, 1992 now U.S. Pat. No. 5,436,095.

BACKGROUND OF THE INVENTION

The present invention relates to an exposure technique, for example, relates to technology useful for a transfer technique etc. of circuit patterns in manufacturing processes of semiconductor integrated circuits etc.

When design rules for circuit elements and wirings become on the order of submicrons as high integration of semiconductor integrated circuits advances, in a photolithography process where circuit patterns on masks are transferred onto semiconductor wafers by using lights of g-line and i-line etc., the reduction of accuracy of circuit patterns transferred onto wafers becomes a serious problem. As a measure for improving such a problem, a phase shift technique preventing reduction of contrast of the projected image by varying phases of light transmitted through the mask is proposed. For example, Japanese patent application laid-open No. 173744/1983 discloses a phase shift where a transparent film is provided on one side of a pair of transmission domains between which a shielding domain is inserted, and a phase difference is produced between lights transmitted through the two transparent domains in the exposure, whereby the interference lights weaker each other at the point on the wafer which would become a shielding domain originally (hereinafter referred to as "Levenson type" or "complementary type phase shift method").

Also, Japanese patent application laid-open No. 67514/1987 discloses a phase shift technique where after a part of the shielding domain of a mask is removed and a fine open pattern is formed, a transparent film is provided on either of the open pattern or the transmission domain existing in the vicinity thereof, and a phase difference is produced between the light transmitted through the transmission domain and the light transmitted through the open pattern, whereby the amplitude distribution of lights transmitted through the transmission domain is prevented from spreading laterally (hereinafter referred to as "subshift type phase shift method").

Japanese patent application laid-open No. 140743/1990 discloses a phase shift technique where a phase shifter is provided on a part of the transmission domain of the mask and a phase difference is produced in the transmission lights, thereby the phase shifter boundary is emphasized (hereinafter referred to as "edge emphasized type phase shift method").

BRIEF SUMMARY OF THE INVENTION

However, any of these relates to the improvement of phase shift techniques on the experimental level, and does not fully consider the problems in the case of application to actual devices on the mass production level in which complicated patterns are mixed.

Accordingly, an object of the present invention is to provide a phase shift exposure technique where mask production is easy.

Another object of the present invention is to provide a phase shift exposure technique suitable for exposure of fine patterns in submicron units.

Another object of the present invention is to provide a reduced projection exposure method to enable exposure of various and fine patterns in the manufacturing process of semiconductor devices or semiconductor integrated circuit devices.

Another object of the present invention is to provide a phase shift exposure technique which does not produce unnecessary patterns.

Another object of the present invention is to provide a phase shift exposure technique which produces accurate patterns even at the ends of periodic patterns.

Another object of the present invention is to provide a phase shift exposure technique having a high integration density.

Another object of the present invention is to provide a phase shift exposure technique to enable the production of complicated patterns.

Another object of the present invention is to provide a phase shift exposure technique suitable for the manufacture of a DRAM.

The foregoing and other objects and novel features of the present invention will become apparent from the description of the present specification and the attached drawings.

A brief explanation of one of the summaries of the present invention, to attain such objects, is as follows.

That is, the constitution of the present invention is for carrying out the reducing projection exposure on the end of the mask pattern domain having a definite mode or the boundary of the mask pattern domain having plural modes using a phase shift mask where a prescribed correction pattern is provided.

According to the above constitution, as the end effects etc. cancel each other by the above-mentioned correction pattern, the various and fine patterns can be exposed.

The foregoing and other summaries of the invention included in the present application are itemized as follows.

1. In the manufacturing method or the exposure method for semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in ultraviolet or deep ultraviolet domain (If it has coherence, it need not be monochromatic light, and this applies also in the following items.) is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture (it may be an equi multiplication system. Also, it may be the combination reduced optical system being composed of a lens system and mirrors, and the same applies also in the following items.) so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer, wherein the mask comprises:

(a) a main opening region like a band having a constant width and corresponding to a line pattern isolated at least on one side; and

(b) a plurality of supplementary opening regions like dots or broken lines not forming their own patterns and having phases opposite to the main opening region and provided along one side of the main opening region and close to it spaced by regular intervals.

2. In the manufacturing method or the exposure method for semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in ultraviolet or deep ultraviolet domain (not limited to ultraviolet ray, and the same applies in the above and successive items) is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer,

wherein the mask comprises:

(a) a main opening region corresponding to a pattern whose featuring conversion length is comparable with or not more than the wavelength of the exposure light; and

(b) at least one supplementary opening region not forming its own pattern and corresponding to parts where the patterns for the bright parts focusing on the wafer are liable to become thin by the interference effect of light when the main opening region is exposed as it is, the supplementary opening region having the same phase as that of the main opening region and continuing to the vicinity of the main opening region or to that parts.

3. In the manufacturing method or the exposure method for semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer, wherein the mask comprises:

(a) one corner region of a shifter domain which is a light transmission region where the shifter domain and a mask substrate exposure domain are directly adjacent to each other so that the shifter domain may become convex globally; and

(b) at least one local shifter loss part having the same phase as that of the mask substrate exposure region and not forming its own pattern and installed on the corner region of the shifter domain corresponding to parts where a dark pattern corresponding to the shifter domain focusing onto the wafer is liable to project or thicken undesirably by the interference effect of light when it is exposed intact.

4. In the manufacturing method or the exposure method for semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer, wherein the mask comprises:

(a) a plurality of band-shaped main opening regions with phases reversed alternately, corresponding to a plurality of linear patterns arranged with a constant width and interval; and

(b) a band-shaped dummy opening region being installed along a main opening region of one end of the plurality of main opening regions, with approximately equal intervals and forming its own patterns and having the reversed phases to that of the main opening region of one end with approximately equal width.

5. In the manufacturing method or the exposure method for semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer, wherein the mask comprises:

(a) a plurality of band-shaped main opening regions with phases reversed alternately, corresponding to a plurality of linear patterns arranged at a constant width and interval; and

(b) a band-shaped wide main opening region being installed along a main opening region of one end of the plurality of main opening regions with approximately the same interval as that of the main opening regions and having a larger width than the main opening regions so that it has the same width as that of the main opening regions at the exposure state and forming its own pattern having a reversed phase to that of the main opening region of one end.

6. In the manufacturing method or the exposure method for semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transformed onto the wafer,

wherein the mask comprises:

(a) the first phase shift mask pattern group according to the first mode; and

(b) the second phase shift mask pattern group according to the second mode.

7. In the manufacturing method or the exposure method for semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer, wherein the mask comprises:

(a) first and second main opening regions having approximately equal complicated configurations and arranged closely and having phases reversed to each other.

8. In the manufacturing method or the exposure method for semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer,
wherein the mask comprises:

(a) an approximately square phase shift mask pattern group forming a plurality of approximately square patterns being arranged closely in the oblique direction.

9. In the manufacturing method or the exposure method for semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and wherein the luminous flux passing through mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer,
wherein the mask comprises:

(a) the first and second main opening regions arranged closely and having the same phase;

(b) a supplementary opening region provided to couple the first and second main opening regions and having the same phase as those of the first and second main opening regions over their full ranges; and

(c) a phase shift region having a phase reversed to that of the first and second main opening regions and provided at the center of the supplementary opening region so that the focused patterns on the wafers corresponding to the first and second main opening regions may be separated at the exposure.

10. In a mask for manufacturing or exposing semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer, wherein the mask comprises:

(a) a band-shaped main opening region having a constant width and corresponding to a linear pattern isolated at least on one side; and

(b) a plurality of supplementary opening regions of dot shape or broken line shape being installed along one side of the main opening region closely with a constant spacing therefrom and having reversed phases to the main opening region and not forming their own pattern.

11. In a mask for manufacturing or exposing semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer, wherein the mask comprises:

(a) a main opening region corresponding to a pattern whose featuring conversion length on the wafer is comparable with or not more than the wavelength of the exposure light; and

(b) at least one supplementary opening region not forming its own pattern and corresponding to parts where the patterns for the bright parts focusing on the wafer are liable to become thin by the interference effect of light when the main opening region is exposed as it is, the supplementary opening region having the same phase as that of the main opening region and continuing to the vicinity of the main opening region or to the parts.

12. In a mask for manufacturing or exposing semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer, wherein the mask comprises:

(a) one corner region of a shifter domain which is a light transmission region where the shifter domain and a

mask substrate exposure domain are directly adjacent to each other so that the shifter domain may become convex globally; and

(b) at least one local shifter loss part having the same phase as that of the mask substrate exposure region and not forming its own pattern and installed on the corner region of the shifter domain corresponding to parts where a dark pattern corresponding to the shifter domain focusing onto the wafer is liable to project or thicken undesirably by the interference effect of light when it is exposed intact.

13. In a mask for manufacturing or exposing semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer, wherein the mask comprises:

(a) a plurality of band-shaped main opening regions with phases reversed alternately, corresponding to a plurality of linear patterns arranged with a constant width and interval; and

(b) a band-shaped dummy opening region being installed along a main opening region of one end of the plurality of main opening regions, with approximately equal intervals and forming its own patterns and having reversed phases to that of the main opening region of one end with approximately equal width.

14. In a mask for manufacturing or exposing semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer, wherein the mask comprises:

(a) a plurality of band-shaped main opening regions with phases reversed alternately, corresponding to a plurality of linear patterns arranged with a constant width and interval; and

(b) a band-shaped wide main opening region being installed along a main opening region of one end of the plurality of main opening regions, with approximately the same interval as that of the main opening regions and having a larger width than the main opening regions so that it has the same width as that of the main opening regions at the exposure state and forming its own pattern having a reversed phase to that of the main opening region of one end.

15. In a mask for manufacturing or exposing semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer, wherein the mask comprises:

(a) a first phase shift mask pattern group according to a first model and

(b) the second phase shift mask pattern group according to a second mode.

16. In a mask for manufacturing or exposing semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer, wherein the mask comprises:

(a) an approximately square phase shift mask pattern group forming a plurality of approximately square patterns being arranged closely in the oblique direction.

17. In a mask for manufacturing or exposing semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer, wherein the mask comprises:

(a) first and second main opening regions arranged closely and having the same phase;

(b) a supplementary opening region provided to couple the first and second main opening regions and having the same phase as those of the first and second main opening regions over their full ranges; and

(c) a phase shift region having a phase reversed to that of the first and second main opening regions and provided at the center of the supplementary opening regions so that the focused patterns on the wafers corresponding to the first and second main opening regions may be separated at the exposure.

18. Method of transferring patterns of a photo-mask onto a substrate using light rays and forming patterns onto the substrate, wherein the patterns are formed by combining a system of forming different patterns with lights of the same

phase and a system of forming different patterns with lights of the reverse phase.

19. A mask for exposing patterns in a method of transferring patterns of a photo-mask onto a substrate using light rays and forming patterns onto the substrate, wherein the patterns are formed by combining a system of forming different patterns with lights of the same phase and a system of forming different patterns with lights of the reverse phase.

20. In the manufacturing method or the exposure method for semiconductor devices or semiconductor integrated circuit devices where monochromatic exposure luminous flux having a constant wavelength and being coherent or partially coherent in the ultraviolet or deep ultraviolet domain is irradiated on one mask on which prescribed enlarged patterns are formed, and the luminous flux passing through the mask is reduced and projected by the reducing lens system having a constant numerical aperture so that the desired reduced patterns corresponding to the enlarged patterns on the mask may focus onto the resist film of a treated wafer on one of whose main surfaces is formed the photo-sensitive resist film, thereby the reduced patterns corresponding to the enlarged patterns on the mask are transferred onto the wafer, wherein the mask comprises:

(a) first and second main opening regions arranged closely and having phases reversed to each other;

(b) a first supplementary opening region provided to couple the first main opening region and having the same phase as that of the first main opening region over its full ranges; and

(c) a second supplementary opening region having the same phase as that of the second main opening region and coupled with the first supplementary opening region nearly at the center between the first and second main opening regions so that the focused patterns on the wafers corresponding to the first and second main opening regions may be separated at the exposure.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a front sectional view of a stepper to be used for exposure in the invention;

FIG. **2** is a front sectional view of a reticle or a mask in the invention;

FIG. **3** is a manufacturing process flow chart for masks to be used in the invention;

FIG. **4** is a plan view of a mask for exposure of a DRAM in the invention;

FIG. **5** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **6** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **7** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **8** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **9** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **10** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **11** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **12** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **13** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **14** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **15** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **16** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **17** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **18** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **19** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **20** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **21** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **22** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **23** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **24** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **25** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **26** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **27** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **28** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **29** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **30** is a plan view of a finished pattern corresponding to the mask;

FIG. **31** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **32** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **33** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **34** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **35** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **36** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **37** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **38** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **39** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **40** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **41** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **42** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **43** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **44** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **45** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **46** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **47** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **48** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **49** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **50** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **51** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **52** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **53** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **54** is a plan view of a finished pattern on a treated wafer corresponding to the mask; FIG. **55** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **56** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **57** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **58** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **59** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **60** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **61** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **62** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **63** is a graph showing a relation of width of a shifter and dimension of a finished pattern using Shifter-On-Quartz method;

FIG. **64** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **65** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **66** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **67** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **68** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **69** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **70** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **71** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **72** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **73** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **74** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **75** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **76** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **77** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **78** is a plan view of a finished pattern on a wafer corresponding to the mask;

FIG. **79** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **80** is a plan view of a finished pattern on a wafer corresponding to the mask;

FIG. **81** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **82** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **83** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **84** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **85** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **86** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

FIG. **87** is a plan pattern view of a mask in an embodiment of the invention;

FIG. **88** is a plan view of a finished pattern on a wafer corresponding to the mask;

FIG. **89** is a plan pattern view of a mask in an embodiment of the invention; and

FIG. **90** is a plan view of a finished pattern on a treated wafer corresponding to the mask;

DETAILED DESCRIPTION OF THE INVENTION

Explanation of the present invention will be carried out in embodiments as follows. Although each of the divided embodiments is explained for convenience of explanation, the embodiments are not separated but modifications having relations to each other or constitute a part of another embodiment. Also, the same or similar parts are attached with the same reference numerals in each figure.

(i) Explanation of manufacturing process of a stepper, a mask or the like

FIG. **1** is an explanation diagram indicating the representative constitution of an exposure device to be used for an exposure system of mask patterns of each embodiment of the present invention. As a lens step-and-repeat type i-line 5:1 reduction projection device applicable to this exposure, there is, for example, i-line stepper NRS-175i7A (NA=0.5, exposure area=17.5 mm square) made by the Nihonkogaku (Nikon). In FIG. **1**, numeral **1** designates a treated semiconductor wafer, such as Si single crystal wafer of 5–8 inches, numeral **2** designates a high pressure mercury lamp being a light source for exposure, numeral **3** designates a light collecting mirror, numeral **4** designates a first plane reflecting mirror, numeral **5** designates a shutter, numeral **6** designates a fly eye lens, numeral **7** designates an aperture to adjust the coherence factor σ (used as σ=0.5 in the embodiment), numeral **8** designates a short cut filter to cut light at the deep ultraviolet side having a wavelength shorter than that of the i-line in the case of i-line (365 nm) exposure, numeral **9** designates a second plane reflecting mirror, numeral **10** designates a mask blind determining the range of a transfer domain, numeral **11** designates a condenser lens for forming a Koehler illumination, numeral **12** designates a

phase shift mask being an important part of the present invention, numeral **13** designates a mask holder which holds the mask and can be moved finely at least in the Z-axis direction, and numeral **14** designates a reduction projecting lens generally comprising a group of many lenses. In the stepper as above exemplified, the wafer side is constituted in a telecentric way. Also, the mask side may be constituted in a telecentric way. Numeral **15** designates a wafer adsorption block, numeral **16** designates a Z-axis moving block (in the height direction), numeral **17** designates an X-axis moving block (horizontal lateral direction), and numeral **18** designates a Y-axis moving block (horizontal longitudinal direction). The X-axis moving block **17** together with the Y-axis moving block **18** constitute the XY stage.

FIG. **2** is a sectional view of a phase shift mask of the present invention. In FIG. **2**, numerals **21** to **24** designate chromium shield films, numerals **25** and **26** designate phase shift films or shifters, and numeral **27** designates a mask substrate exposure region or non-shift light transmission region. The substrate exposing region does not always mean that a quartz glass substrate itself be exposed, but the substrate itself may be constituted by a quartz glass substrate as a substrate body and a thin transparent film formed on its surface.

Next, a method of forming the mask will be explained briefly.

The mask is formed in such a way that after a surface of a synthetic quartz glass plate is ground and washed, for example, a chromium film having thickness of about 0.05–0.3 μm is piled throughout its main surface by sputtering method, and subsequently a sensitive resist to an electron beam having film thickness of 0.1–0.8 μm is applied throughout the surface of the chromium film. Next, a desired pattern of the integrated circuit is processed using electron beam exposure technique. The electron beam exposure technique is that a fine resist pattern is formed on a sample using electron beam exposure, and the explanation will be added as follows.

Electron beams are irradiated using an electron beam plotting device onto a sample to which the electron beam sensitive resist is applied. The electron beam plotting device irradiates electron beams to designated positions and designated forms on the mask substrate being the sample, according to pattern data in which position coordinates and shape etc. of integrated circuit patterns are registered. Afterwards, when the resist is positive type, light exposed parts are removed by a prescribed developer, and the exposed metal film is etched by wet etching method or the like and a pattern is formed to a prescribed shape. When the resist is negative type, parts not yet exposed to light are removed by a prescribed developer, and a pattern is formed to a prescribed shape by etching. The resist is removed by a resist stripping liquid, and patterns are washed. Thereby the shielding domain and the transmission domain in prescribed shape are formed.

Subsequently, a pattern comprising a phase shifter for shifting phases of a transmission beam of light is formed onto a synthetic quartz glass substrate on which the chromium pattern is formed. The phase shifter designates the thickness of the transparent substance (thickness at the center of the shifter opening) determined according to the refractive index of the transparent substance and wavelength of the transmission light, and is a thin film of SOG (Spin On Glass), indium oxide (InOx) or the like. SOG is applied to the glass substrate with revolution, and afterwards, the transparent film is piled with hot baking. In this case, in order to invert the phase, the thickness d of the transparent film satisfies the following relation

$$d=\lambda/2(n-1)$$

where the wavelength of the transmission light is made λ, and the refractive index of the transparent film is made n. For example, when the wavelength λ of the light used for the exposure is made 0.365 μm (i-line) and the refractive index n of the transparent film is made 1.5, the thickness of the transparent film may be made about 0.37 μm. However, under the consideration of variation caused by shifter formation (the film thickness of the shifter even at the best condition disperses about 80 angstrom, that is, about 2%), the phase error of about $\lambda/20$–$\lambda/10$ radian should be allowed in the phase inversion or the same phase. Accordingly, the expressions "phase inversion", "π or equivalent thereto", "180° or equivalent thereto", "the same phase" etc. in the present application include these errors and the phase differences equivalent thereto, unless clearly specified.

The processings of necessary parts of the transparent film are carried out on the transparent substrate to which the transparent thin film having the designated thickness is piled, using the electron beam exposure technique as described above. In order to invert the phase, the mask is subjected to hot baking after applying the SOG etc. onto the shading film of the glass substrate. In this case, the transparent film having the above film thickness can be obtained by controlling the viscosity of SOG and the rotating speed of the mask substrate at the SOG application.

When the electron beam exposure technique is used, for example, a charging prevention layer being made of aluminium with thickness 0.05 μm has been formed by the sputtering method of the like on the upper surface over a resist applied surface (lower surface in FIG. **2**). Next, electron beam drawing is carried out, according to the pattern data or phase shifter processing corresponding to the pattern of the above-mentioned integrated circuit.

FIG. **3** indicates flow of the mask formation. In FIG. **3**, numeral **31** designates a formation process of a synthetic quartz substrate for a mask, numeral **32** designates a piling process of a metal shielding film where a chromium film is deposited throughout almost the full surface of one main surface of the substrate, numeral **33** designates a resist application process where a photoresist is spin-applied on the chromium film, numeral **34** designates an electron beam exposure process where the applied resist film is exposed by direct picture drawing with an electron beam exposure apparatus, numeral **35** designates a resist development process where unnecessary parts of the resist are removed and desired resist patterns are formed, numeral **36** designates an etching process of a metal shielding film where the chromium film is etched using the resist as a mask, numeral **37** designates a resist removing process where the resist is fully removed afterwards, numeral **38** designates a correction process of loss or broken parts of the shielding film where loss parts among the shielding film are corrected, numeral **39** designates a correction process of shielding film remainder where the remainder part of unnecessary shielding film on the substrate is removed, and numeral **40** designates a mask washing process where the mask with the chromium pattern being completed is washed. Also in FIG. **3**, numeral **42** designates a piling process of a phase shift film where a phase shift film is applied throughout almost the full surface of the exposure domain with the chromium pattern being completed, numeral **43** designates a piling process of a charging prohibition film where a thin conductive film is

piled on the phase shift film, numeral **44** designates a resist application process where a resist film for patterning the phase shift film is spin-applied, numeral **45** designates an electron beam exposure process where the resist film is exposed by direct picture drawing with electron beams similarly to the above, numeral **46** designates a resist development process where unnecessary parts of the resist film are removed and resist patterns are formed, numeral **47** designates an etching process of a phase shifter film where the phase shifter film is formed to a desired pattern using the resist film as a mask, numeral **48** designates a resist removing process where the resist film is removed afterwards, numeral **49** designates a correction process of loss or broken parts of the shifter where loss parts of the shifter are corrected on the substrate subjected to patterning, numeral **50** designates a correction process of shifter remainder where the remainder part of unnecessary shifter film is removed on the mask substrate similarly, and numeral **51** designates a mask washing process where the mask being completed for the present is washed.

Pattern defects produced in the mask manufacturing process of chromium patterns on the mask forming patterns comprising the shielding domain and the transmission domain can be corrected by using laser light, bundled ion beam etc. That is, when the shielding film remainder occurs in the transmission domain of the mask, it can be corrected by irradiating the laser light spot onto appropriate parts. Also, when any breakage in part of the shielding domain occurs, it can be corrected by piling up carbon films on broken parts by irradiating bundled ion beams while adding organic gases such as the pyrene gas ($C_{16}H_{10}$).

Shifter patterns on the mask similar to the carbon pattern can be corrected by sputtering cutting using irradiation of the bundled ion beams. Then, the depth d of a groove obtained by scraping the transparent substrate becomes

$$d=\lambda/2(n-1)$$

where the wavelength of transmission light is λ, and the refractive index of material forming the groove is n.

In the sputtering process using the ion beams, plasma ashing processing of CF_4 or the like is necessary to be applied after the processing in order to smooth the processed surface and to prevent the reduction of transmittance. The light transmittance having been reduced to about 90% can be improved to about 97% due to the above processing.

FIG. **4** is a plan layout of the mask of the present invention. In FIG. **4**, numerals **61** and **62** designate wafer positioning marks with the wafer (FIG. **1**), numeral **63** designates a chromium shielding band for a mask band, numeral **64** designates a part corresponding to scribe line on the wafer **1**, numerals **71** and **81** designate parts corresponding to unit chip domains (for example, DRAM of 64 kbits) on wafers respectively, numerals **72** and **82** designate parts corresponding to the peripheral circuit domains of memory ICs respectively, and numerals **73–76** and **83–86** designate parts corresponding to memory mats of the ICs respectively.

Furthermore, in the embodiment, the explanation has been carried out in the type where the shifter films are placed on the chromium shielding films, but the invention is not limited to this, and it is needless to say that the invention can be applied to plan patterns in general for the type in which shifters are placed under chromium films and other phase shift masks.

Various kinds of mask patterns corresponding to the embodiments of the present invention will be explained as follows, but the following rules are set about reference symbols of the drawings to avoid repetition. That is, alphabets of small letters attached next to each reference numeral indicate the following things. "a" indicates; a non-shift real opening region (or main opening region) corresponding to the pattern on the wafer of the reference numeral, that is, a chromium opening region without shifter film or a mask surface exposed region (hereinafter referred to "chromium opening region etc."), "b" indicates a shift supplementary opening for supplementing the pattern exposure on the wafer of the reference numeral, that is, a supplementary pattern having a shifter film and not forming the real image of itself (hereinafter, phase shift amount is 180 degrees, unless indicated specifically), "c" indicates a chromium shielding region (indicated by partial hatching along the boundary, to distinguish the part and the boundary from others), "d" indicates a shifter film attached domain (indicated by broken lines, to distinguish the boundary from other line), "e" indicates a non-shift reinforcement opening for reinforcing the pattern exposure intensity on the wafer of the reference numeral, that is, a supplementary pattern having no shifter film and not forming the real image of itself, "f" indicates a shift reinforcement opening for reinforcing the pattern exposure intensity on the wafer of the reference numeral, that is, a supplementary pattern having a shifter film and not forming the real image of itself, "g" indicates a shift real opening region (or main opening region) corresponding to a pattern on the wafer of the reference numeral, that is, a chromium opening region having a shift film or a mask surface having no chromium shielding film, "h" is a non-shift supplementary opening for supplementing the pattern exposure on the wafer of the reference numeral, that is, a supplementary pattern having no shifter film and not forming the real image of itself, "k" indicates a local shifter loss part to shape patterns being formed by shifter-on-quartz method, "m" is a surface where a mask surface is exposed, that is, a part where the phase shift amount is zero degree, "q" indicates an intermediate phase shift region (a buffer zone) having intermediate phase shift amount of 60 degrees, "r" indicates an intermediate phase shift region (a buffer zone) having intermediate phase shift amount of 120 degrees, and the second alphabet "y" indicates that it is associated with the second mask in the process of exposing one pattern using two masks.

Further, the devices, materials and various conditions being used for the exposure and patterning will be summarized as follows. As a stepper, the NSR1755I8A (reduction ratio =5:1, exposure wavelength i-line =365 nm monochromatic light) Nikon Inc. was used under the condition that NA =0.5, partial coherence factor σ=0.5. As a positive resist, the high resolution resist for i-line NPR-A185SH2 of the NAGASE SANGYO corporation was used, and as a negative resist, the high resolution chemical amplification system resist for i-line Ri-1300N of the Hitachi Chemicals Inc. was used.

Then, the following mask pattern will be explained in a DRAM having a line pattern minimum dimension of 0.35 μm and a hole pattern minimum dimension of 0.4 μm taken as an example.

(1) Isolated linear pattern

FIG. **5** shows a pattern where real patterns are not close to each other on the same mask among linear patterns such as aluminium wirings, that is, a phase shift mask pattern for exposing isolated linear patterns on a wafer as shown in FIG. **6**, using negative resist. Dimensions described in FIG. **5** are those in conversion on the wafer in unit of μm unless clearly specified. Accordingly, the shown value may be multiplied by **5** to know a dimension on the actual mask. Also, all these

drawings are those of a wafer or a mask set to the exposure device seen from the upper side. In these drawings, numeral **101**a designates a non-shift real opening region corresponding to a linear pattern **101** on a wafer, many numerals **10**lb designate dot-shaped shift supplementary opening regions having the same shape and arranged at regular intervals respectively, numeral **101**c designates a chromium shielding region, and numeral **101**d designates a shifter film attaching domain. A partial hatching is applied to distinguish the chromium shielding region from the non-shift opening region in FIG. **5**. Also, to indicate opening regions with shifter films, indications by scattered dots are applied to the parts.

The reason why the supplementary opening regions are divided in this way is as follows. Connection with the present width results in the production of undesired patterns in relation to NA, because of partial or overall dissolution. On the other hand, if the width of the band-shaped supplementary opening region is thinned so as not to resolve it at all, patterning of the mask itself by EB becomes difficult. If supplementary opening regions are divided in the above way, both space period of supplementary opening regions as a whole and respective Fourier components in X, Y directions for individual supplementary opening regions fall out of projecting lens, and undesired patterns are not produced.

(2) Projected linear pattern

FIG. **7** is one of the applications of the technique in FIG. **5** and indicates phase shift mask patterns where the linear pattern group with linear patterns projecting every several lines or one line as shown in FIG. **8** is exposed using negative resists as described above. In these drawings, numeral **102** designates a long linear pattern on the wafer **1**, numerals **103** to **105** designate short linear patterns spaced with regular intervals from the long linear pattern, numeral **102**g designates a shift real opening region on the mask corresponding to the long linear pattern **102**, numeral **102**h designates many dot-shaped non-shift supplementary opening regions for preventing the projecting part of the long linear pattern **102** from being thinned, numerals **103**a and **104**a designate non-shift real opening regions corresponding to the short linear patterns **103** and **104** respectively, numeral **105**g designates a shift real opening region corresponding to the short linear pattern **105**, numeral **102**d designates a shifter film attaching domain corresponding to the long linear pattern **102**, numeral **105**d designates a shifter film attaching domain corresponding to the short linear pattern **105**, and numeral **102**c designates a chromium shielding region. Unless treated in this way, as the projection part of the pattern **102** has no positive contribution from both openings **103** and **104**, the pattern becomes thinner.

(3) Supplementary opening on the periodic structure end

FIG. **9** is one of the applications of the technique in FIG. **5** and indicates phase shift mask patterns for preventing the phenomena in which the end pattern becomes thinner at the exposure of many periodic linear patterns by negative resists as shown in FIG. **10**. Further, dimensions on the mask are not repeated, as they are approximately equal to those of the preceding embodiments. In these drawings, numerals **107** to **109** designate many linear patterns with equal width arranged at the same period, and among them, the linear pattern **107** forms the left end. Numeral **107**h designates a supplementary pattern for preventing the end pattern **107** from being thinned. Unless treated in this way, as the pattern **107** has no positive contribution from the left side, the pattern becomes thinner.

(4) Dummy pattern of the periodic structure end

FIG. **11** is a modification of FIG. **9**, and indicates mask patterns where in place of the supplementary pattern disposed at the end, a wide dummy non-shift opening **110**a focusing a real pattern **110** (FIG. **12**) is arranged. In this case, the pattern **110** corresponding to this dummy pattern remains as shown in FIG. **12**.

(5) Widening of pattern width of the periodic structure end

FIG. **13** is a modification of FIG. **9**, and indicates mask patterns where in place of the supplementary pattern disposed at the end, a wide shift real opening **107**g focusing the real pattern **107** (FIG. **10**) with its desired width is arranged under consideration of the effect of thinning due to the end. FIG. **14** is an enlarged plan view of the mask pattern in FIG. **13**, indicating the manner that the wide opening pattern **107**g at the end becomes the pattern **107** on the wafer having the desired width due to the thinning caused by the exposure.

(6) Normal arrangement and alternate phase inversion close hole pattern

FIG. **15** indicates phase shift mask patterns where square hole patterns **111** to **113** arranged in line with regular intervals and having the same shape (the dimension is equal) as shown in FIG. **16** are patterned by positive resists. In this example, one of the supplementary patterns **111**b, **112**h, **113**b having the same shape and arranged on four corners of neighboring real patterns is omitted, and instead, neighboring real openings **111**a, **112**g, **113**a are subjected to phase inversion alternately. The mask pattern in this mode is especially effective when an interval between hole patterns is not more than 0.6 μm.

(7) Normal arrangement supplementary pattern common close hole pattern

FIG. **17** is nearly the same as the case in FIG. **15**, but indicates phase shift mask patterns where hole intervals are slightly larger as shown in FIG. **18**. In the following example, mask dimensions being not clearly specified are the same as those in FIG. **15**. In this case, the real openings have the same phase, and instead, supplementary openings of four corners of each real opening are shared one by one. The mask pattern in this mode is especially effective when interval between hole patterns is not less than 0.6 μm and not more than 1.1 μm.

(8) Shifter film sharing close hole pattern for a normal arrangement supplementary pattern

FIG. **19** is nearly the same as the case in FIG. **17**, but indicates phase shift mask patterns where hole intervals are further made larger and the pattern is similar to a complete isolated pattern as shown in FIG. **20**. In this case, as a shifter film **111**d for supplementary openings **111**b and **112**b to which real openings **111**a and **112**a come close respectively is constituted by a common island, a margin for the pattern formation is large. The mask pattern in this mode is especially effective when an interval between hole patterns is not less than 1.1 μm.

(9) Shifter film sharing close hole pattern for an oblique arranged supplementary pattern

FIG. **21** is nearly the same as the case in FIG. **19**, but indicates phase shift mask patterns where holes are arranged with regular intervals nearly in the diagonal direction. In this case, as a shifter film **111**d (**112**d) for supplementary openings **111**b and **112**b (**112**b and **113**b) to which real openings **111**a and **112**a (**112**a and **113**a) come close respectively is constituted by a common island, margin for the pattern formation is large.

(10) Zigzag configuration alternate phase inversion close hole pattern

FIG. **23** indicates phase shift mask patterns when hole lines **115** to **118** in FIG. **15** are arranged with half a period shifted in zigzag form as shown in FIG. **24**. In this case,

phases of real opening regions **115**a and **117**a in the lateral direction are inverted alternately. Also, a shifter film for a shift real opening region **117**g and a shifter film **115**d of shift supplementary opening regions **115**b and **116**b for non-shift opening regions **115**a and **116**a form a common island. Therefore, a margin for the pattern formation is large. The mask pattern in this mode is especially effective when the lateral interval between hole patterns is not more than 0.6 μm.

(11) Zigzag configuration supplementary opening and shifter film sharing close hole pattern

FIG. **25** is nearly the same as the case in FIG. **23**, but indicates phase shift mask patterns where lateral pitches can be taken a little larger as shown in FIG. **26**. In this case, a part of the supplementary opening regions **115**b and **118**b is intended to be common to real opening regions **115**a and **117**a as well as **116**a and **118**a which are neighboring laterally. In such a configuration, the longitudinal pitches can be compressed, comparing with FIG. **23**. The mask pattern in this mode is especially effective when the lateral interval between hole patterns is not less than 0.6 μm and not more than 1.1 μm.

(12) Hole pattern mixture configuration

FIG. **27** indicates phase shift mask patterns where mask pattern modes in three kinds A, B, C are used together, and many contact holes having the same size as shown in FIG. **28** are formed by positive resists. In this case, mode A is responsive to a completely isolated hole, mode B is responsive to FIG. **17**, and mode C is responsive to FIG. **15**. In the mode C, however, a supplementary opening is not used, but phases of corresponding real openings in neighboring lines are inverted.

(13) T type branch reinforcement opening

FIG. **29** indicates phase shift mask patterns where a T type linear pattern **121** of Al wiring etc. as shown in FIG. **30** is exposed by negative resists shown in FIG. **5** and phase shift supplementary openings **12**lb. In this case, as the thinning of the pattern due to interference is generated at the joint part of the hammer handle of the pattern **121**, a pair of non-shift reinforcement openings **121**e are provided continuous to or very close with the non-shift real opening **121**a, that is, a fine supplementary opening which does not resolve and has the same phase as the real opening corresponding thereto is provided. By carrying out the above, as an apparent quantity of light on the real opening close to a pair of non-shift reinforcement openings **121**e is increased, occurrence of the thinning of pattern due to interference can be prevented at the joint of the hammer handle of the pattern **121**.

FIG. **87** indicates a modification where a plurality of the hammer handles or landing piers are projected, and these are relatively close (interval from 0.8 μm to 1.2 μm).

Moreover, FIG. **89** indicates a modification where the interval is equal to 1.2 μm or more.

(14) Opposite comb teeth branch reinforced opening

FIG. **31** indicates phase shift mask patterns where combs by arranging many hammer handles of T type as shown in FIG. **30** with regular intervals are opposed with half a cycle shifted thereby linear patterns **121** and **122** as shown in FIG. **32** are exposed by negative resists in similar manner to the above. In this case, the phase of the real opening **122**g closely confronted is inverted instead of using supplementary openings. The opening regarding the pattern **122** and that regarding the pattern **121** are in relation of the complete phase reverse state. Accordingly, **122**f is a shift reinforcing opening having the same shape as the non-shift reinforcing opening.

(15) Ladder bar reinforcing opening

FIG. **33** indicates phase shift mask patterns where a ladder-shaped linear wiring **121** as show; in FIG. **34** is exposed by a negative resist in similar manner to the above. Unless performing this processing, parts having nearly the same length as the wavelength of the exposing light from the end of the leg of the ladder is thinned due to the interference effect of the exposing light wave.

(16) Opposite double comb teeth alternate phase compensation

FIG. **35** indicates phase shift mask patterns where patterns each having two comb teeth as shown in FIG. **36** being arranged alternately in the linear wiring similar to FIG. **32** are exposed by a negative resist in similar manner to the above.

(17) Repeated quasi linear pattern alternate phase compensation

FIG. **37** indicates phase shift mask patterns where repeated quasi linear patterns using a pair of linear patterns **125** and **126** having local expansions as shown in FIG. **38** as a repetition unit are exposed by a negative resist in similar manner to the above. In this case, dimensions of opening patterns **125**a and **125**g are the same as those of finished patterns **125** and **126**. Further, the shifter film **126**d is broadened or widened by 0.1 μm than the corresponding pattern in similar manner to other examples.

(18) Repeated U pattern alternate phase compensation

FIG. **39** indicates phase shift mask patterns where U-like patterns **127–129** and **137–139** repeatedly arranged closely as shown in FIG. **40** are exposed by negative resists in similar manner to the above. In this case, close openings are phase reversed to each other. Further, the sizes of the mask real openings are the same as those of the finished ones in similar manner to the above example.

(19) Repeated linear pattern midway cutting

FIG. **41** indicates phase shift mask patterns where specific patterns **142** and **143** among linear repeated patterns **141** to **144** having the same width and the same interval of Al wiring etc. are cut at an intermediate position by the so-called Shifter-On-Quartz method, and patterns by the cutting as shown in FIG. **42** are exposed by negative resists and a so-called Levenson type phase shift mask. In FIG. **41**, **142**h, **143**h and **142**b are supplementary openings in a wide sense, and are patterns on the mask corresponding to cut parts between the linear patterns **142** and **143**. **142**b is a shifter-on-quartz section being a phase inverting shifter layer formed directly on the mask substrate or a shift supplementary opening, and **142**h and **143**h are shifter-on-quartz supplementary openings or non-shift supplementary openings having the same phase as those of **142**a and **143**a. There is no special boundary between the shifter-on-quartz supplementary opening and the real opening neighboring therewith, but it is indicated by solid line for the convenience of illustration in this application. Also, the relation between width of a dark part on the wafer formed by a fine shifter-on-quartz section and width of a shifter-on-quartz section (conversion on the wafer) is shown in FIG. **63**.

(20) Close parallel line shifter-on-quartz separation

FIG. **43** indicates phase shift mask patterns where close parallel patterns **145** and **146** as shown in FIG. **44** are exposed by negative resists. In FIG. **43**, **145**b is a shift supplementary opening similar to the prior example, **145**h and **146**h are non-shift supplementary openings installed with equal width on both sides of the shift supplementary opening respectively, and **145**a and **146**a are non-shift real openings having equal dimensions to those of the finished patterns **145** and **146**.

(21) Close parallel line shifter & chromium separation

FIG. **45** indicates phase shift mask patterns where close parallel patterns **147** and **148** as shown in FIG. **46** are exposed by negative resists. In FIG. **45**, **147**b is a shift supplementary opening similar to the prior example, **147**h and **148**h are non-shift supplementary openings installed with equal width on both sides of the shift supplementary opening respectively, and **147**a and **148**a are non-shift real openings having equal dimensions to those of the finished patterns **147** and **128**. This method is especially effective when pattern interval for the portion having wide pattern interval is further wider in comparison with the portion having narrow interval.

(22) Close parallel L pattern shifter-on-quartz separation

FIG. **47** indicates phase shift mask patterns where close parallel L-like patterns **149** and **150** as shown in FIG. **48** are exposed by negative resists. In FIG. **47**, **149**b is a shift supplementary opening similar to the prior example, **149**h and **150**h are non-shift supplementary openings installed with equal width on both sides of the shift supplementary opening respectively, and **149**a and **150**a are non-shift real openings having equal dimensions to those of the finished patterns **149** and **150**.

(23) Close parallel S pattern shifter-on-quartz separation

FIG. **49** indicates phase shift mask patterns where close parallel S-like patterns **151** and **152** as shown in FIG. **50** are exposed by negative resists. In FIG. **49**, **151**b is a shift supplementary opening similar to the prior example, **151**b and **152**h are non-shift supplementary openings installed with equal width on both sides of the shift supplementary opening respectively, and **151**a and **152**a are non-shift real openings having equal dimensions to those of the finished patterns **151** and **152**.

(24) Partial close pattern shifter-on-quartz separation

FIG. **51** indicates phase shift mask patterns where partially close parallel repeated patterns **154** and **155** as shown in FIG. **52** (In the drawing, the repetition in the lateral direction is indicated by its unit part only. The same applies to following examples.) are exposed by negative resists. In FIG. **51**, **154**b is a shift supplementary opening similar to the prior example, **154**h and **155**h are non-shift supplementary openings installed with equal width on both sides of the shift supplementary opening respectively, and **154**a and **155**a are non-shift real openings having equal dimensions to those of the finished patterns **154** and **155**.

(25) Partial close pattern alternate phase inversion separation

FIG. **53** indicates phase shift mask patterns where partially close parallel repeated patterns **156** and **157** as shown in FIG. **54** are exposed by negative resists. In FIG. **53**, **157**b is a shift supplementary opening, **156**h is a non-shift supplementary opening forming a dark part together with the shift supplementary opening **157**b, and **156**a and **157**g are non-shift real openings having equal dimensions to those of the finished patterns **156** and **157**.

(26) Close parallel L pattern shifter-on-quartz separation corner correction

FIG. **55** indicates phase shift mask patterns where closely parallel L-like patterns **158** and **159** as shown in FIG. **56**, capable of preventing excessive expansion of a dark part at the corner during the exposure by the mask in FIG. **47**, are exposed by negative resists. In FIG. **55**, **158**k is a correcting shifter loss part being a non-shift opening of 0.06 μm square for preventing expansion of the dark part at the corner, **158**b is a shift supplementary opening similar to the prior example, **158**h and **159**h are non-shift supplementary openings installed with equal width on both sides of the shift supplementary opening respectively, and **158**a and **159**a are non-shift real openings having equal dimensions to those of the finished patterns **158** and **159**.

(27) Close parallel S pattern shifter-on-quartz separation corner correction

FIG. **57** indicates phase shift mask patterns where closely parallel S-like patterns **161** and **162** as shown in FIG. **58**, capable of preventing excessive expansion of a dark part at the corner region during the exposure by the mask in FIG. **49**, are exposed by negative resists. In FIG. **57**, **161**k and **162**k are correcting shifter loss parts being non-shift opening regions for preventing expansion of the dark part at the corner, **161**b is a shift supplementary opening similar to the prior example, **161**h and **162**h are non-shift supplementary openings installed with equal width on both sides of the shift supplementary opening respectively, and **161**a and **162**a are non-shift real openings having equal dimensions to hose of the finished patterns **161** and **162**.

(28) Shifter-on-quartz fine hole pattern corner correction

FIG. **59** indicates improved mask patterns to solve a problem that hole patterns **164**–**168** shown in FIG. **60** are excessively expanded in the diagonal direction during the exposure by shifter-on-quartz method using negative resists. In FIG. **59**, **164**m is a quartz glass surface of the mask, **164**g–**168**g are shift patterns or shift real opening regions comprising phase inverting shifter films being formed directly on the mask substrate corresponding to the hole patterns **164**–**168**, and **165**g is a shifter loss part of 0.06 μm square provided on each apex of the shifter patterns **164**g–**168**g.

(29) Close parallel lines shifter-on-quartz separation pattern thinning prevention

FIG. **61** indicates improved mask patterns to solve a problem that when concave parts exists on a part of the closely parallel linear patterns as shown in FIG. **62**, the patterns are excessively thinned at the concave parts during the exposure, by the Shifter-On-Quartz method using negative resists. In FIG. **61**, **169**e and **170**e are non-shift reinforcement openings of 0.15 μm square to reinforce the concave parts.

(30) Shifter screening dog bone patterning

FIG. **64** indicates phase shift mask patterns where dog bone patterns as shown in FIG. **65** are exposed by a shifter screen method combining a Shifter-On-Quartz method and screening by chromium patterns, using positive type resists.

(31) Double exposure shifter screen patterning

FIG. **66** and FIG. **67** indicate phase shift masks where line patterns (when positive resists are used) or space patterns (when negative resists are used) as shown in FIG. **68** are exposed two times using two masks, thereby the resists can be prevented from remaining undesirably (when positive resists are used) or from being removed undesirably (when negative resists are used), when only masks in FIG. **66** are used. Here, FIG. **66** indicates the first mask and FIG. **67** indicates the second mask. As processes, after the first exposure is carried out using the first mask, the second exposure is carried out using the second mask so that the boundary of the shifter **174**d between the chromium screen parts **174**c **17**c is exposed fully. After these processes, the development is carried out thereby patterns as shown in FIG. **68** can be obtained.

(32) Intermediate phase shifter screen dog bone patterning

In FIG. **69**, the problem in the mask of FIG. **66** can be executed using one mask, patterns as shown in FIG. **70** can be exposed by the exposure of one time. In FIG. **69**, **176**q and **176**r are intermediate phase shifters forming buffer zones having width of 0.15 μm, and when the phase of the

mask substrate surface **176**m is made zero degree, **176**q is 60 degrees and **176**r is 120 degrees.

FIG. **71** is an example of applications where the above-mentioned various phase shift mask techniques are applied to the exposure for patterns as indicated in FIG. **72** of an Si gate of a DRAM using negative resists. The principal techniques used here are the close pattern alternate phase inversion, close pattern shift-on-quartz on-quartz separation etc. In this case, the central section of periodic patterns in a unit of two closely arranged rectangular patterns **184** and **185** etc. is processed by an alternate phase shift method (Levenson system), and the end is processed by the Shifter-On-Quartz method as the alternate phase shift method cannot be applied.

FIG. **73** is an application where the above-mentioned various phase shift mask techniques are applied to the exposure for patterns as indicated in FIG. **74** of an Si gate of a DRAM using negative resists. The principal techniques used here are the close pattern alternate phase inversion, the close pattern shift-on-quartz separation etc. In this case similar to FIG. **71**, repeated patterns of matrix form in a unit of the rectangular patterns **192** and **193** are basically processed by simple alternate phase inversion, and at the end of the matrix, the end processing is applied using the technique of the close pattern shift-on-quartz separation.

FIG. **75** is an application of the above-mentioned various phase shift mask techniques to the exposure of patterns as indicated in FIG. **76** of layers a of WL (word line) of a DRAM using negative resists. The principal techniques used here are the close pattern alternate phase inversion, the close pattern shift-on-quartz separation etc. In this case, quasi repeated patterns in a unit of quasi linear patterns of **212** etc. are basically processed with simple alternate phase inversion, and the end processing is carried out using the technique of close pattern shift-on-quartz separation at the part having a branch of the end of the matrix.

FIG. **77** is an application of the above-mentioned various phase shift matrix techniques to the exposure of the complicated patterns of the first layer Al of a DRAM as indicated in FIG. **78**, using negative resists. The principal techniques used here are the close pattern alternate phase inversion, the close pattern shift-on-quartz separation, the chromium & shifter separation etc. In this case, where the alternate phase shift method is possible, the alternate phase method is applied, and at the part where phase inversion is impossible and patterns are close to each other, the Shifter-On-Quartz method is applied, and further at the part where the phase inversion is impossible and the patterns are not close to each other, the separation of neighboring patterns is carried out by the chromium screen film.

FIG. **79** is an application of the above-mentioned various phase shift mask techniques to the exposure of patterns having complicated crossings of layers of bit lines of a DRAM as indicated in FIG. **80**, using negative resists. The principal techniques used here are the close pattern phase inversion as shown in FIG. **53**, the close pattern shift-on-quartz separation, the chromium & shifter separation etc. In this case, at the part such as patterns of both ends **231** and **232** or **234** and **235** where the alternate phase shift method can not be applied, the separation of patterns is carried out by the Shifter-On-Quartz method, and the interference of the boundary of the shifter film **233**d like the part extending longitudinally in FIG. **69** is used at the part being specially close between patterns **233** and **235** (for example, the interval =0.2 μm).

FIG. **81** is an application of the Shifter-On-Quartz painting method in which a plurality of fine shifters are made close and comparatively thick patterns **241** and **242** are formed, to the exposure for the second layer Al wiring of a DRAM as indicated in FIG. **82** by negative resists.

FIG. **83** indicates the simplified extraction of main techniques of the mask pattern of FIG. **79** as shown in FIG. **84**.

FIG. **85** is an application of the above-mentioned various phase shift mask techniques to the exposure of patterns having complicated crossings of the first layer of the Al wiring layer of a DRAM as indicated in FIG. **86**, using negative resists. The principal techniques used here are the close pattern alternate phase inversion, the close pattern shift-on-quartz separation, the chromium & shifter separation etc. In this case, as the free phase inversion can not be carried out because of complicated patterns, the phase shift is not applied to relatively distant parts thereby the degree of freedom is secured. At other close parts, the alternate inversion method is applied if possible, and at other parts where the phase inversion can not be carried out, the Shifter-On-Quartz method is applied.

(34) Citation of references to supplement embodiments

Details of the edge emphasizing type phase shift method and the mask design technique thereof are described in Japanese patent application laid-open No. 140743/1990 (patent application No. 29350/1988, filed on Nov. 22, 1988) by Okamoto laid-open on May 30, 1990, which shall be made a part of the description of the present application.

Further, the pattern layout of masks in the edge emphasizing type phase shift method, Levenson type phase shift method and the supplementary shift type phase shift method, negative or positive resist substances and resist process thereof, light sources for exposure, and the application thereof to semiconductor integrated circuit devices such as DRAM or SRAM are described in Japanese patent application No. 247100/1990 (filed on Sep. 19, 1990) by Okamoto, which shall be made a part of the present application.

Also, details of the negative resist substances for i-line stepper are explained in detail in Japanese patent application No. 290917/1990 (filed on Oct. 30, 1990) by Uchino et al., which shall be made a part of the present application.

Further, the design automation techniques regarding phase shift masks are indicated in Japanese patent application No. 11735/1991 (filed on May 22, 1991) by Takekuma et al., which shall be made a part of the present application.

Although the invention made by the present inventor has been described concretely based on embodiments, the present invention is not limited to the embodiments but various modifications may be done without departing from the scope and spirit of the invention. That is, the present embodiment has been described in an example of exposure by i-line, but it is needless to say that the present invention is not limited to the above example, and can be applied also to exposure using an excimer laser light source.

Additionally, regarding the phases of the mask patterns, only either of a positive phase pattern or a phase reversal pattern with the phase thereof reversed is indicated, but it is needless to say that the reversed pattern thereof may be entirely used.

The effects obtained by the representative invention disclosed in the present application are described as follows.

Reduced projection exposure is carried out on the end of the mask pattern domain of a definite mode or on the boundary of the mask pattern domain of a plurality of modes using phase shift masks provided with prescribed correction patterns, thereby various and fine patterns can be exposed as the end effect can be canceled by the correction patterns.

The technical field forming the background of the present invention, that is, memory ICs has been explained, but the

present invention is not limited to the above and various modifications may be done without departing from the scope and spirit of the invention. For example, it can be applied to logic IC, IC for microcomputers and IC for communications.

What is claimed is:

1. An integrated circuit device fabrication method, comprising the steps of:

(i) irradiating a coherent or partially coherent ultraviolet or deep ultraviolet exposure light beam to a first major surface of a phase shift mask having an enlarged mask pattern;

(ii) projecting light transmitted through the mask and forming a reduced pattern image corresponding to the enlarged mask pattern onto a photoresist film overlying a first major surface of an integrated circuit wafer by an optical reduction projection exposure apparatus; and

(iii) transferring a reduced pattern corresponding to the enlarged mask pattern onto the first major surface of the integrated circuit wafer, said phase shift mask comprising:

(a) a light shielding region;

(b) a plurality of first hole mask opening groups corresponding to first hole patterns disposed at substantially regular intervals and adjacent to each other on the wafer, each of said first hole mask opening groups having a first real opening and a first auxiliary opening group having a plurality of first auxiliary openings in the light shielding region, said first auxiliary openings respectively being disposed and oriented along four sides of their adjacent first real opening and isolated therefrom with the light shielding region, the first auxiliary openings extending in lengthwise directions along the four sides of their adjacent first real opening, the first auxiliary openings being inverted in phase with respect to their adjacent first real opening;

(c) a second hole mask opening group corresponding to second hole patterns disposed at substantially regular intervals and adjacent to each other on the wafer, said second hole mask opening group having a plurality of second hole real openings in the light shielding region, said second hole real openings being of substantially a same shape, same dimensions, and same phase;

(d) a common auxiliary opening group having a plurality of common auxiliary openings in the light shielding region, said common auxiliary openings being disposed one by one between adjacent pairs of second hole real openings, each of said common auxiliary openings being isolated by the light shielding region from its adjacent second hole real opening and substantially inverted in phase with respect thereto; and

(e) a second peripheral auxiliary opening group having a plurality of second peripheral auxiliary openings in the light shielding region, said second peripheral auxiliary openings being disposed and oriented one by one along a periphery of the second hole real openings so that a respective second peripheral auxiliary opening directly faces its adjacent second hole real opening, each of said second peripheral auxiliary openings being isolated by the light shielding region from its adjacent second hole real opening and substantially inverted in phase with respect thereto.

2. An integrated circuit device fabrication method according to claim **1**, wherein any most adjacent pair of the first hole mask opening groups are disposed and oriented so that sides extending in the lengthwise directions, of a most adjacent pair of the auxiliary openings between any most adjacent pair of the first hole mask opening groups, face each other.

3. An integrated circuit device fabrication method according to claim **1**, wherein the second peripheral auxiliary openings, constituting the second peripheral auxiliary opening group, are disposed along an entirety of the periphery of the second hole mask opening group.

4. An integrated circuit device fabrication method according to claim **3**, wherein any most adjacent pair of the first hole mask opening groups are disposed and oriented so that sides extending in the lengthwise directions, of a most adjacent pair of the auxiliary openings between any most adjacent pair of the first hole mask opening groups, face each other.

5. An integrated circuit device fabrication method according to claim **1**, said mask further comprising:

(e) a third hole mask opening group corresponding to third hole patterns disposed at substantially regular intervals and adjacent to each other on the wafer, said third hole mask opening group having a plurality of third hole real openings in the light shielding region, said third hole real openings being alternately inverted in phase and of substantially a same shape and same dimensions; and

(f) a third peripheral auxiliary opening group having a plurality of third auxiliary openings in the light shielding region, said third auxiliary openings being disposed and oriented one by one along a periphery of the third hole mask opening group so that each third auxiliary opening directly faces its adjacent third hole real opening, each third auxiliary opening being isolated by the light shielding region from its adjacent third hole real opening and substantially inverted in phase with respect thereto.

6. An integrated circuit device fabrication method according to claim **5**, wherein the third auxiliary openings constituting the third peripheral auxiliary opening group are disposed along an entirety of the periphery of the third hole mask opening group.

7. An integrated circuit device fabrication method according to claim **5**, wherein any most adjacent pair of the first hole mask opening groups are disposed and oriented so that sides extending in the lengthwise directions, of a most adjacent pair of the first auxiliary openings between any most adjacent pair of the first hole mask opening groups, face each other.

8. An integrated circuit device fabrication method according to claim **5**, wherein the second peripheral auxiliary openings, constituting the second peripheral auxiliary opening group, are disposed along an entirety of the periphery of the second hole mask opening group.

9. An integrated circuit device fabrication method according to claim **8**, wherein any most adjacent pair of the first hole mask opening groups are disposed and oriented so that sides extending in the lengthwise directions, of a most adjacent pair of the first auxiliary openings between any most adjacent pair of the first hole mask opening groups, face each other.

10. An integrated circuit device fabrication method according to claim **8**, wherein the third auxiliary openings constituting the third peripheral auxiliary opening group are disposed along an entirety of the periphery of the third hole mask opening group.

11. An integrated circuit device fabrication method according to claim **10**, wherein any most adjacent pair of the

first hole mask opening groups are disposed and oriented so that sides extending in the lengthwise directions, of a most adjacent pair of the first auxiliary openings between any most adjacent pair of the first hole mask opening groups, face each other.

12. An integrated circuit device fabrication method according to claim **1**, wherein a pattern of said plurality of first hole mask opening groups differs from a pattern of said second hole mask opening group.

13. An integrated circuit device fabrication method according to claim **1**, wherein the substantially regular intervals between first hole patterns to which the plurality of the first hole mask opening groups correspond are different from the substantially regular intervals between the second hole patterns to which the second hole mask opening group corresponds.

14. An integrated circuit device fabrication method, comprising the steps of:

(i) irradiating a coherent or partially coherent ultraviolet or deep ultraviolet exposure light beam to a first major surface of a phase shift mask having an enlarged mask pattern;

(ii) projecting light transmitted through the mask and forming a reduced pattern image corresponding to the enlarged mask pattern onto a photoresist film overlying a first major surface of an integrated circuit wafer by an optical reduction projection exposure apparatus; and

(iii) transferring a reduced pattern corresponding to the enlarged mask pattern onto the first major surface of the integrated circuit wafer, said phase shift mask comprising:

(a) a light shielding region;

(b) a plurality of first hole mask opening groups corresponding to first hole patterns disposed at substantially regular intervals and adjacent to each other on the wafer, each of said first hole mask openings groups having a first real opening and a first auxiliary opening group having a plurality of first auxiliary openings in the light shielding region, said first auxiliary openings respectively being disposed and oriented along four sides of their adjacent first real opening and isolated therefrom with the light shielding region, the first auxiliary openings extending in lengthwise directions along the four sides of their adjacent first real opening, the first auxiliary openings being inverted in phase with respect to their adjacent first real opening;

(c) a second hole mask opening group corresponding to second hole patterns disposed at substantially regular intervals and adjacent to each other on the wafer, said second hole mask opening group having a plurality of second hole real openings in the light shielding region, said second hole real openings being alternately inverted in phase and of substantially a same shape and same dimensions; and

(d) a second peripheral auxiliary opening group having a plurality of second auxiliary openings in the light shielding region, said second auxiliary openings being disposed and oriented one by one along a periphery of the second hole mask opening group so that each second auxiliary opening directly faces its adjacent second hole real opening, each second auxiliary opening being isolated by the light shielding region from its adjacent second hole real opening and substantially inverted in phase with respect thereto.

15. An integrated circuit device fabrication method according to claim **14**, wherein any most adjacent pair of the first hole mask opening groups are disposed and oriented so that sides extending in the lengthwise directions, of a most adjacent pair of the first auxiliary openings between any most adjacent pair of the first hole mask opening groups, face each other.

16. An integrated circuit device fabrication method according to claim **14**, wherein the second auxiliary openings constituting the second peripheral auxiliary opening group are disposed along an entirety of the periphery of the second hole mask opening group.

17. An integrated circuit device fabrication method according to claim **16**, wherein any most adjacent pair of the first hole mask opening groups are disposed and oriented so that sides extending in the lengthwise directions, of a most adjacent pair of the first auxiliary openings between any most adjacent pair of the first hole mask opening groups, face each other.

18. An integrated circuit device fabrication method according to claim **14**, wherein a pattern of said plurality of first hole mask opening groups differs from a pattern of said second hole mask opening group.

19. An integrated circuit device fabrication method according to claim **14**, wherein the substantially regular intervals between first hole patterns to which the plurality of the first hole mask opening groups correspond are different from the substantially regular intervals between the second hole patterns to which the second hole mask opening group corresponds.

20. An integrated circuit device fabrication method, comprising the steps of:

(i) irradiating a coherent or partially coherent ultraviolet or deep ultraviolet exposure light beam to a first major surface of a phase shift mask having an enlarged mask pattern;

(ii) projecting light transmitted through the mask and forming a reduced pattern image corresponding to the enlarged mask pattern onto a photoresist film overlying a first major surface of an integrated circuit wafer by an optical reduction projection exposure apparatus; and

(iii) transferring a reduced pattern corresponding to the enlarged mask pattern onto the first major surface of the integrated circuit wafer, said phase shift mask comprising:

(a) a light shielding region;

(b) a first hole mask opening groups corresponding to first hole patterns disposed at substantially regular intervals and adjacent to each other on the wafer, said first hole mask opening group having a plurality of first hole real openings in the light shielding region, said first hole real openings being of substantially a same shape, same dimensions, and same phase;

(c) a common auxiliary opening group having a plurality of common auxiliary openings in the light shielding region, said common auxiliary openings being disposed one by one between adjacent pairs of first hole real openings, each of said common auxiliary openings being isolated by the light shielding region from its adjacent first hole real opening and substantially inverted in phase with respect thereto;

(d) a first peripheral auxiliary opening group having a plurality of first peripheral auxiliary openings in the light shielding region, said first peripheral auxiliary openings being disposed and oriented one by one along a periphery of the first hole real openings so that a respective first peripheral auxiliary opening directly faces its adjacent first hole real opening, each second first peripheral auxiliary openings being

isolated by the light shielding region from its adjacent first hole real opening and substantially inverted in phase with respect thereto;

(e) a second hole mask opening group corresponding to second hole patterns disposed at substantially regular intervals and adjacent to each other on the wafer, said second hole mask opening group having a plurality of second hole real openings in the light shielding region, said second hole real openings being alternately inverted in phase and of substantially a same shape and same dimensions; and

(f) a second peripheral auxiliary opening group having a plurality of second auxiliary openings in the light shielding region, said second auxiliary openings being disposed and oriented one by one along a periphery of the second hole mask opening group so that each second auxiliary opening directly faces its adjacent second hole real opening, each second auxiliary opening being isolated by the light shielding region from its adjacent second hole real opening and substantially inverted in phase with respect thereto.

21. An integrated circuit device fabrication method according to claim **20**, wherein the second auxiliary openings constituting the second peripheral auxiliary opening group are disposed along an entirety of the periphery of the second hole mask opening group.

22. An integrated circuit device fabrication method according to claim **20**, wherein the first peripheral auxiliary openings constituting the first peripheral auxiliary opening group are disposed along an entirety of the periphery of the first hole mask opening group.

23. An integrated circuit device fabrication method according to claim **22**, wherein the second auxiliary openings constituting the second peripheral auxiliary opening group are disposed along an entirety of the periphery of the second hole mask opening group.

24. An integrated circuit device fabrication method according to claim **20**, wherein a pattern of said first hole mask opening group differs from a pattern of said second hole mask opening group.

25. An integrated circuit device fabrication method according to claim **20**, wherein the substantially regular intervals between first hole patterns to which the first hole mask opening group corresponds are different from the substantially regular intervals between second hole patterns to which the second hole mask opening group corresponds.

26. A method of manufacturing a semiconductor device, comprising the steps of:

(1) irradiating a mask, having enlarged patterns, with a monochromatic exposure light flux having a substantially constant wavelength and being coherent or partially coherent in ultraviolet or deep ultraviolet domain, and

(2) reducing and projecting the exposure light flux passing through the mask, by an optical reducing projection system, so that reduced patterns corresponding to the enlarged patterns of the mask can be focused onto a photosensitive resist film over a major surface of a wafer, said mask comprising:

(a) a first main opening region, in a shape of a pier, protruding substantially at right angles from one side of a second main opening region, corresponding to a protruding pattern over the wafer, the first and second main opening regions being connected by a connecting portion;

(b) a third opening region with an opposite phase to that of the first main opening region, adjacent to one side of the first main opening region, to form a clear image of the first main opening region over the wafer; and

(c) at least one supplementary opening region, not to form its own independent image over the wafer, disposed along the one side of the first main opening region and adjacent to the connecting portion of the first main opening region to the second main opening region where the image of the first main opening region over the wafer is liable to become thin by interference effects of the exposure light flux when said first main opening region is exposed without the at least one supplementary opening region, said at least one supplementary opening region having substantially a same phase as that of the first main opening region and continuing thereto or in the vicinity of a side portion of the first main opening region.

27. A method of manufacturing a semiconductor device, comprising the steps of:

(1) irradiating a phase shift mask, having enlarged patterns, with an exposure light flux having substantially constant wavelength and being coherent or partially coherent in ultraviolet or deep ultraviolet domain, and

(2) reducing and projecting the exposure light flux passing through the mask, by a reducing optical projection system, so that reduced patterns corresponding to the enlarged patterns of the mask can be focused onto a photosensitive resist film over a major surface of a wafer, said mask comprising:

(a) a plurality of principal opening region, having a same phase to each other, constituting a rhombic two-dimensional lattice having a rhombus as a unit cell of the lattice; and

(b) auxiliary opening regions, having an inverted phase with respect to that of the principal opening regions, disposed at about the center of each sub-unit cell divided by a minor diagonal of the unit cell.

28. A method of manufacturing a semiconductor device according to claim 27, wherein the auxiliary opening regions are rectangular in shape.

29. A method of manufacturing a semiconductor device according to claim 28, wherein the principal opening regions are rectangular in shape.

30. A method of manufacturing a semiconductor device, comprising the steps of:

(1) irradiating a phase shift mask, having enlarged patterns, with an exposure light flux having a substantially constant wavelength and being coherent or partially coherent in ultraviolet or deep ultraviolet domain, and

(2) reducing and projecting the exposure light flux passing through the mask, by a reducing optical projection system, so that reduced patterns corresponding to the enlarged patterns of the mask can be focused onto a photosensitive resist film over a major surface of a wafer, said mask comprising:

(a) a plurality of first principal opening regions, having a same phase to each other, constituting a first rhombic two-dimensional lattice having a rhombus as a unit cell of the lattice; and

(b) a plurality of second principal opening regions, having an inverted phase with respect to that of the first principal opening regions, constituting a second rhombic two-dimensional lattice having the rhombus as a unit cell of the lattice, the second rhombic

two-dimensional lattice being superposed upon the first rhombic two-dimensional lattice by displacing the second rhombic two-dimensional lattice along a major diagonal of the rhombus so that the first principal opening regions do not overlap with the second principal opening regions.

31. A method of manufacturing a semiconductor device according to claim 30, wherein the first principal opening regions are rectangular in shape and have same sizes.

32. A method of manufacturing a semiconductor device according to claim 31, wherein the second principal opening regions are rectangular in shape, and have the same shape and sizes as those of the first principal opening regions.

33. A method of manufacturing a semiconductor device, comprising the steps of:

(1) irradiating a mask, having enlarged patterns, with a monochromatic exposure light flux having a substantially constant wavelength and being coherent or partially coherent in ultraviolet or deep ultraviolet domain, and

(2) reducing and projecting the exposure light flux passing through the mask, by an optical reducing projection system, so that reduced patterns corresponding to the enlarged patterns of the mask can be focused onto a photosensitive resist film over a major surface of a wafer, said mask comprising:

(a) a long main opening region having a shape of a continuous band, having a substantially constant width and corresponding to a line pattern isolated at least on one side; and

(b) supplementary opening regions, in the shape of dots or broken lines, having dimensions so as not to form their own images over the wafer, and having phases opposite to that of said long main opening region and disposed along said one side of the long main opening region and adjacent to it spaced by regular intervals so as to form a clear image of the long main opening region onto the photosensitive resist film over the major surface of the wafer, a plurality of the supplementary opening regions being distributed along said one side of the long main opening region.

34. A method of manufacturing a semiconductor device, comprising the steps of:

(1) irradiating a mask, having enlarged patterns, with a monochromatic exposure light flux having a substantially constant wavelength and being coherent or partially coherent in ultraviolet or deep ultraviolet domain, and

(2) reducing and projecting the exposure light flux passing through the mask, by an optical reducing projection system, so that reduced patterns corresponding to the enlarged patterns of the mask can be focused onto a photosensitive resist film over a major surface of a wafer, said mask comprising:

(a) a long main opening region having a shape of a continuous band isolated at least on one side; and

(b) supplementary opening regions, in the shape of dots or broken lines, having dimensions so as not to form their own images over the wafer, and having phases opposite to that of said long main opening region and disposed along said one side of the long main opening region and adjacent to it spaced by regular intervals so as to form a clear image of the long main opening region onto the photosensitive resist film over the major surface of the wafer.

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