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(54) Title: THERMAL METHODS FOR CLEANING POST-CMP WAFERS

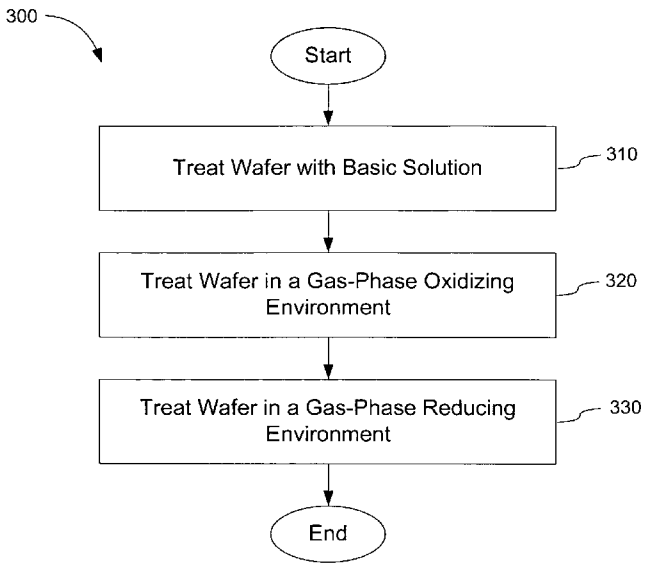

FIG. 3

(57) Abstract: Methods for cleaning semiconductor wafers following chemical mechanical polishing are provided. An exemplary method exposes a wafer to a thermal treatment in an oxidizing environment followed by a thermal treatment in a reducing environment. The thermal treatment in the oxidizing environment both removes residues and oxidizes exposed copper surfaces to form a cupric oxide layer. The thermal treatment in the reducing environment then reduces the cupric oxide to elemental copper. This leaves the exposed copper clean and in condition for further processing, such as electroless plating.

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Thermal Methods for Cleaning Post-CMP Wafers

BACKGROUND OF THE INVENTION

Field of the Invention

[01] The present invention relates generally to the field of semiconductor device fabrication and more particularly to wafer cleaning.

Description of the Prior Art

[02] Semiconductor devices, including the Back-End of Line (BEoL) interconnect structures thereof, include conductive lines and other features that are formed from copper. During semiconductor device fabrication on a wafer, the copper is typically deposited within trenches or vias defined in a dielectric layer. The copper and dielectric layers are then planarized to provide a smooth and planar surface on which to deposit additional layers. A common method for planarizing is chemical mechanical planarization (CMP). CMP processes typically leave a residue on the exposed surface of the wafer that must be removed prior to the formation of subsequent layers.

[03] Typical approaches to removing the CMP residue involve washing the wafer. For example, the wafer can be washed first in an acidic solution and then in a basic solution, or first in a basic solution followed by an acidic solution. However, these methods are disadvantageous as they tend to remove copper, leaving the copper features recessed with respect to the surrounding dielectric layer. Other methods for removing the CMP residue expose the wafer to an energetic plasma to etch away the residue.

[04] What is provided by the present invention are novel methods for removing CMP residue that do not harm either the exposed copper or the dielectric layer.

SUMMARY

[05] An exemplary post-CMP cleaning method comprises treating a wafer in a gas-phase oxidizing environment at a temperature above about 100°C, then treating the wafer in a gas-phase reducing environment at a temperature above about 100°C. Treating the wafer in the oxidizing environment can include treating the wafer in an atmosphere comprising O_2 or O_3 while treating the wafer in the reducing environment can include treating the wafer in an atmosphere comprising H_2. The method can further comprise treating the wafer with a basic solution prior to treating the wafer in the oxidizing environment. The basic solution can have a pH in the range of about 8 to about 11, for example, and in some embodiments comprises tetramethyl ammonium hydroxide.

[06] The present invention also provides a method for cleaning a post-CMP wafer that includes a conductive feature having a Cu_2O surface layer. This exemplary method comprises oxidizing the Cu_2O surface layer in a first gas-phase environment to form a CuO surface layer, then reducing the CuO surface layer in a second gas-phase environment to elemental Cu. Oxidizing the Cu_2O surface layer can comprise treating the wafer in an atmosphere including O_2 or O_3 at a temperature above about 100°C, while reducing the CuO surface layer can comprise treating the wafer in an atmosphere including H_2 at a temperature above about 100°C. The method can further comprise substantially removing a residue layer with a basic solution prior to oxidizing the Cu_2O surface layer.

[07] Another method of the invention is directed to selectively forming a capping layer over a conductive feature of a wafer. This exemplary method comprises cleaning the wafer and forming the capping layer selectively over the conductive feature by electroless deposition. In this method, cleaning the wafer can include oxidizing a Cu_2O surface layer of the conductive

feature in a first gas-phase environment to form a CuO surface layer, then reducing the CuO surface layer in a second gas-phase environment to elemental Cu. In some embodiments, the capping layer comprises cobalt or a cobalt alloy.

BRIEF DESCRIPTION OF DRAWINGS

[08] FIG. 1 is a cross-section view of a post-CMP wafer including a conductive feature disposed within a dielectric layer.

[09] FIG. 2 is a cross-section view of the top portion of the conductive feature of FIG. 1.

[010] FIG. 3 is a flow-chart representation of a method for cleaning the post-CMP wafer of FIG. 1 according to an embodiment of the present invention.

[011] FIG. 4 is a cross-section view of the top portion of the conductive feature shown in FIG. 2 following treatment in an oxidizing environment according to an embodiment of the present invention.

[012] FIG. 5 is a cross-section view of the top portion of the conductive feature shown in FIG. 3 following treatment in a reducing environment according to an embodiment of the present invention.

[013] FIG. 6 is a cross-section view of a wafer including a capping layer selectively disposed on a conductive feature according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[014] The present invention provides methods for cleaning semiconductor wafers following chemical mechanical polishing. An exemplary method exposes a wafer to a thermal treatment in an oxidizing environment followed by a thermal treatment in a reducing environment. The thermal treatment in the oxidizing environment both removes residues and oxidizes exposed copper surfaces to form a cupric oxide layer. The thermal treatment in the reducing environment then reduces the cupric oxide to elemental copper. This leaves the exposed copper clean and in condition for further processing, such as electroless plating.

[015] FIG. 1 is a cross-sectional view of a wafer 100 following a chemical mechanical polishing (CMP) process. The wafer 100 comprises a dielectric layer 110 and an exposed conductive feature 120 disposed within the dielectric layer 110. FIG. 1 also shows a residue layer 130 left by the CMP process on the surfaces of the dielectric layer 110 and the conductive feature 120. The residue layer 130 can include, for example, cleaning residues and corrosion inhibitors, which are typically copper-organic complexes. The residue layer 130 should be removed as completely as possible prior to further processing, such as electroless deposition on the conductive feature 120.

[016] The dielectric layer 110 can comprise SiO_2 or a low dielectric constant ("low-k") material that has a dielectric constant less than that of SiO_2. Such low-k materials, especially those with dielectric constants lower than 3, are increasingly favored in semiconductor device fabrication as they impart superior electrical properties to the finished devices. Examples of suitable low-k materials include fluorosilicate glass (FSG), organosilicate glass (OSG), and highly porous SiO_2.

[017] The conductive feature 120 can be a conductive line or via made of copper, for example. Although only one conductive feature 120 is shown in FIG. 1, the conductive feature 120 is used to represent the large number of conductive features that are typically present on a wafer 100.

[018] FIG. 2 shows an enlarged view of a top portion of the conductive feature 120 in FIG. 1. The residue layer 130 has been omitted from FIG. 2 for clarity. As shown in FIG. 2, when the conductive feature 120 comprises copper, the CMP process leaves the conductive feature 120 with a thin surface layer 200 of cuprous oxide (Cu_2O).

[019] FIG. 3 is a flow-chart representation of an exemplary method 300 for cleaning the wafer 100 to remove the residue layer 130. The method comprises optionally treating 310 the wafer 100 with a basic solution, treating 320 the wafer in a gas-phase oxidizing environment, and treating 330 the wafer in a gas-phase reducing environment. Here, "gas-phase" indicates that the phase of matter within the environment is a gas, as opposed to a plasma.

[020] The method 300 optionally begins by treating 310 the wafer 100 with a basic solution. In some embodiments, the basic solution has a pH of 10; a suitable pH range for the basic solution is about 8 to about 11. An exemplary basic solution comprises tetramethyl ammonium hydroxide. A suitable dwell time in the basic solution under these conditions is about 30 seconds to about 2 minutes. Treating 310 the wafer 100 with the basic solution serves to remove a substantial portion of the residue layer 130 from the surface of the dielectric layer 110 and the surface of the conductive feature 120. In some embodiments, the treatment 310 leaves approximately a monolayer of the residue layer 130 on both the surface of the dielectric layer 110 and the surface of the conductive feature 120. Treating 310 with the basic solution does not meaningfully alter the Cu_2O surface layer 200 (FIG. 2).

[021] Next, the wafer 100 is treated 320 in an oxidizing environment. As treating 310 the wafer 100 with the basic solution is optional, in some embodiments the method 300 begins with treating 320 in the oxidizing environment. An exemplary oxidizing environment comprises an atmosphere including about 1% to about 10% molecular oxygen (O_2), or about 1% to about 2%

ozone (O_3), with the balance of the atmosphere being an inert gas such as nitrogen, helium, or argon. All percentages used herein are volume percents unless noted otherwise.

[022] A suitable temperature range for the oxidizing environment is about 100°C to about 400°C. A more preferable temperature is in the range of about 150°C to about 250°C. The pressure within the oxidizing environment can be at or below normal atmospheric pressure. An exemplary pressure is about 1 Torr. A suitable dwell time in the oxidizing environment under these conditions is about 2 minutes, but can be in the range of about 1 minute to about 5 minutes. Omitting the optional treating 310 the wafer 100 with the basic solution generally results in longer dwell times.

[023] Treating 320 in the oxidizing environment serves to decompose and volatilize the organic materials in the residue layer 130. The elevated temperature of the oxidizing environment also serves to desorb water in the residue layer 130. Additionally, the oxidizing environment serves to oxidize the Cu_2O surface layer 200 of the conductive feature 120. As shown in FIG. 4, the Cu_2O surface layer 200 (FIG. 2) is oxidized to form a cupric oxide (CuO) surface layer 400.

[024] Next, the wafer 100 is treated 330 in a reducing environment. An exemplary reducing environment comprises an atmosphere including molecular hydrogen (H_2). The atmosphere can be essentially entirely hydrogen, or can comprise a mixture of hydrogen with an inert gas such as nitrogen, helium, or argon. The pressure within the reducing environment can be at or below normal atmospheric pressure. At normal atmospheric pressure, a suitable concentration of hydrogen is about 4%. At lower pressures, such as in the range of about 1 Torr to about 10 Torr, the atmosphere can be entirely hydrogen. A suitable temperature range for the reducing environment is about 100°C to about 400°C. A more preferable temperature is in the range of about 150°C to about 250°C. In some embodiments, the same temperature is maintained through

both treatments 320 and 330. A suitable dwell time in the reducing environment under these conditions is about 1 minute to about 2 minutes.

[025] As shown in FIG. 5, treating 330 in the reducing environment serves to reduce the CuO surface layer 400 (FIG. 4) to a surface layer 500 of elemental copper (Cu). Following treating 330 in the reducing environment, the wafer 100 can be further processed, for example, by selective electroless plating of a capping layer on the conductive feature 120. Methods for electroless plating of cobalt and cobalt alloys are taught, for example in US patent application 11/644,697 filed on December 22, 2006 and entitled "Electroless Deposition of Cobalt Alloys," and US patent application 11/513,634 filed on August 30, 2006 and entitled "Processes and Systems for Engineering a Copper Surface for Selective Metal Deposition" each of which is incorporated herein by reference. FIG. 6 shows the wafer 100 after a capping layer 600 has been selectively formed on the conductive feature 120 by electroless plating. Advantageously, the elemental copper surface layer 500 provides a superior surface for the nucleation and growth of cobalt and cobalt alloy capping layers than the Cu_2O surface layer 200.

[026] In the foregoing specification, the invention is described with reference to specific embodiments thereof, but those skilled in the art will recognize that the invention is not limited thereto. Various features and aspects of the above-described invention may be used individually or jointly. Further, the invention can be utilized in any number of environments and applications beyond those described herein without departing from the broader spirit and scope of the specification. The specification and drawings are, accordingly, to be regarded as illustrative rather than restrictive.

CLAIMS

What is claimed is:

1. A post-CMP cleaning method comprising:

   treating a wafer in a gas-phase oxidizing environment at a temperature above about 100°C; then

   treating the wafer in a gas-phase reducing environment at a temperature above about 100°C.

2. The method of claim 1 wherein treating the wafer in the oxidizing environment includes treating the wafer in an atmosphere comprising O_2.

3. The method of claim 2 wherein the atmosphere comprises between about 1% to about 10% O_2.

4. The method of claim 1 wherein treating the wafer in the oxidizing environment includes treating the wafer in an atmosphere comprising O_3.

5. The method of claim 4 wherein the atmosphere comprises between about 1% to about 2% O_3.

6. The method of claim 1 wherein the temperature of the oxidizing environment is between about 150°C to about 250°C.

7. The method of claim 1 wherein a pressure within the oxidizing environment is about 1 Torr.

8. The method of claim 1 wherein treating the wafer in the oxidizing environment includes holding the wafer in the oxidizing environment for a dwell time of between about 1 minute to about 5 minutes.

9. The method of claim 1 wherein treating the wafer in the reducing environment includes treating the wafer in an atmosphere comprising H_2.

10. The method of claim 9 wherein the atmosphere comprises a mixture of H_2 and an inert gas.

11. The method of claim 1 wherein a pressure within the reducing environment is between about 1 Torr to about 10 Torr.

12. The method of claim 1 wherein the temperature of the reducing environment is between about 150°C to about 250°C.

13. The method of claim 1 wherein a temperature of the oxidizing environment and a temperature reducing environment are the same.

14. The method of claim 1 wherein treating the wafer in the reducing environment includes holding the wafer in the reducing environment for a dwell time of between about 1 minute to about 2 minutes.

15. The method of claim 1 further comprising treating the wafer with a basic solution prior to treating the wafer in the oxidizing environment.

16. The method of claim 15 wherein the basic solution has a pH in the range of about 8 to about 11.

17. The method of claim 15 wherein the basic solution comprises tetramethyl ammonium hydroxide.

18. The method of claim 15 wherein treating the wafer in the basic solution includes holding the wafer in the basic solution for a dwell time of between about 30 seconds to about 2 minutes.

19. A method for cleaning a post-CMP wafer including a conductive feature having a Cu_2O surface layer, the method comprising:

oxidizing the Cu_2O surface layer in a first gas-phase environment to form a CuO surface layer; then

reducing the CuO surface layer in a second gas-phase environment to elemental Cu.

20. The method of claim 19 wherein the first gas-phase environment comprises an atmosphere including O_2 at a temperature above about 100°C.

21. The method of claim 19 wherein the first gas-phase environment comprises an atmosphere including O_3 at a temperature above about 100°C.

22. The method of claim 19 wherein the second gas-phase environment comprises an atmosphere including H_2 at a temperature above about 100°C.

23. The method of claim 19 further comprising substantially removing a residue layer with a basic solution prior to oxidizing the Cu_2O surface layer.

24. The method of claim 23 wherein the basic solution has a pH in the range of about 8 to about 11.

25. The method of claim 23 wherein the basic solution comprises tetramethyl ammonium hydroxide.

26. A method for selectively forming a capping layer over a conductive feature of a wafer, the method comprising:

cleaning the wafer, including

oxidizing a Cu_2O surface layer of the conductive feature in a first gas-phase environment to form a CuO surface layer; then

reducing the CuO surface layer in a second gas-phase environment to Cu; and

forming the capping layer selectively over the conductive feature by electroless deposition.

27. The method of claim 26 wherein cleaning the wafer further includes, before oxidizing the Cu_2O surface layer, treating the wafer with a basic solution.

28. The method of claim 26 wherein the capping layer comprises cobalt or a cobalt alloy.

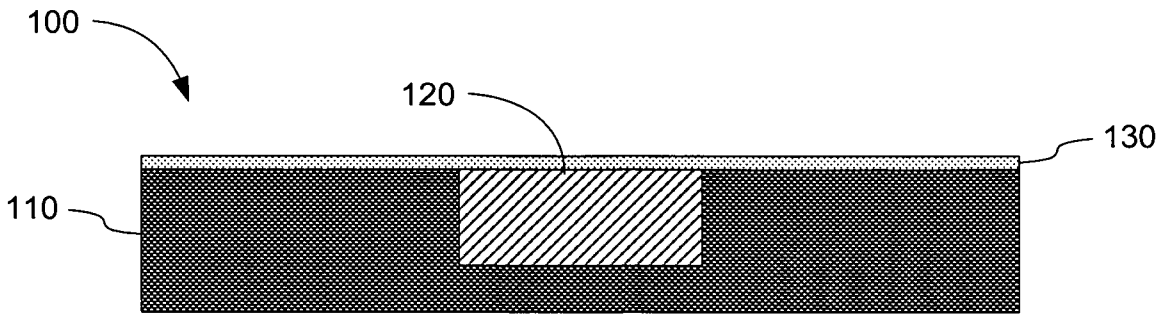

FIG. 1

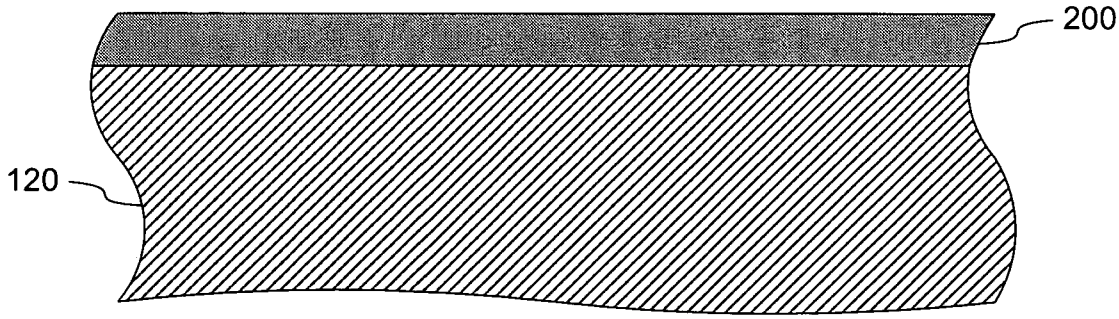

FIG. 2

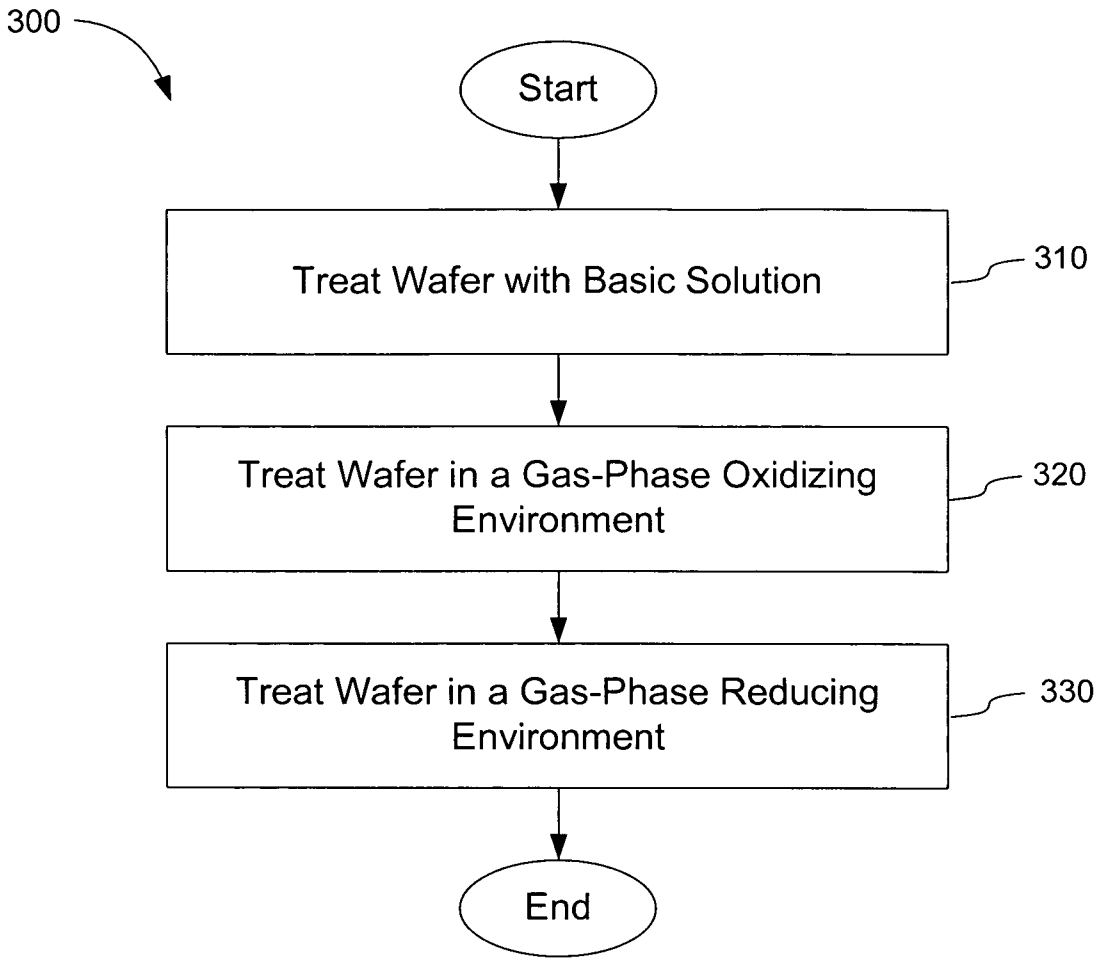
300
Start
Treat Wafer with Basic Solution
310
Treat Wafer in a Gas-Phase Oxidizing Environment
320
Treat Wafer in a Gas-Phase Reducing Environment
330
End

FIG. 3

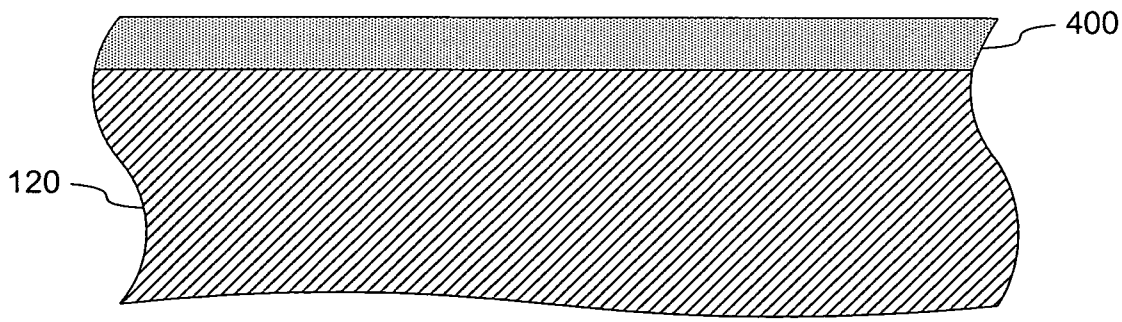
400
120

FIG. 4

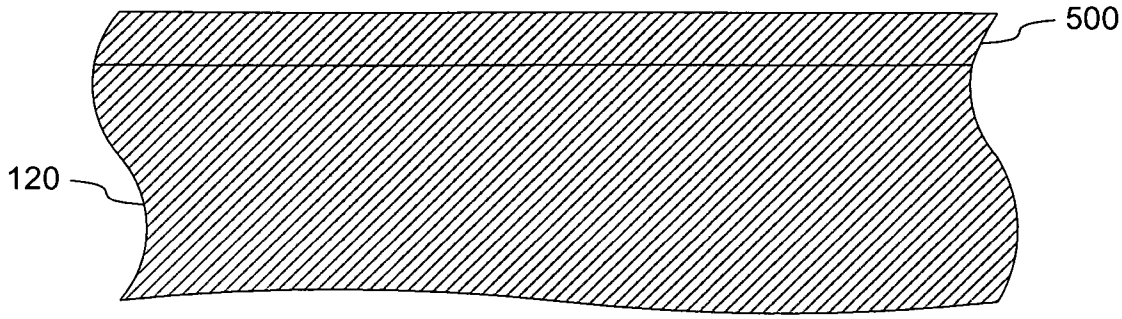

FIG. 5

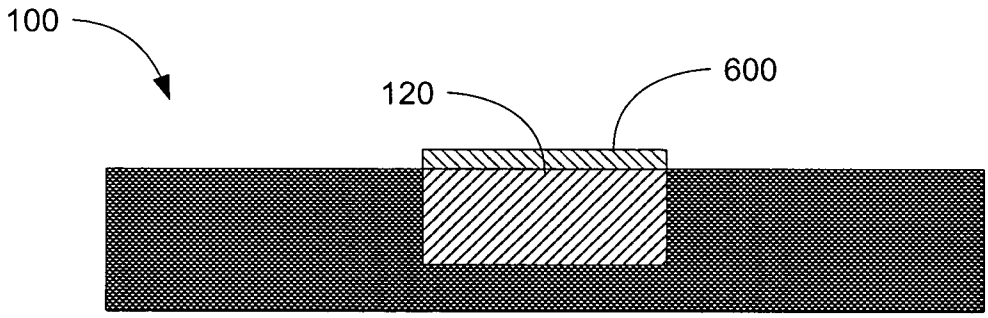

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/005744

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/304(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 B08B 3/00, H01L 21/28, 21/302, 21/304

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

KOREAN UTILITY MODELS AND APPLICATIONS FOR UTILITY MODELS SINCE 1975
JAPANESE UTILITY MODELS AND APPLICATIONS FOR UTILITY MODELS SINCE 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS(KIPO internal) & keyword : post-CMP, clean, oxidizing, and reducing

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2002-0025806 A (HITACHI.LTD.) 04 April 2002 See the abstract; claim 1; and Fig. 22	1-28
A	US 6,127,282 A (SERGEY LOPATIN et al.) 03 October 2000 See the abstract; Column 3, line 32 - Column 5, line 5; claim 1; and Figs. 2-5	1-28
A	KR 10-2001-0089722 A (KONINKLIJKE PHILIPS ELECTRONICS N.V.) 08 October 2001 See the abstract; page 6, line 33 - page 7, line 14; claim 1; and Fig. 5	1-28
A	US 6,878,628 A (AUGUSTE J. L. SOPHIE et al.) 12 April 2005 See the abstract; Column 5, line 64 - Column 6, line 48; claim 1; and Fig. 10	1-28

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 OCTOBER 2008 (24.10.2008)	**24 OCTOBER 2008 (24.10.2008)**

Name and mailing address of the ISA/KR

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Facsimile No. 82-42-472-7140

Authorized officer

KIM, Kap Byung

Telephone No. 82-42-481-8498

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2008/005744

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