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(54) Title: CIRCUITS FOR PROVIDING CLASS-E POWER AMPLIFIERS

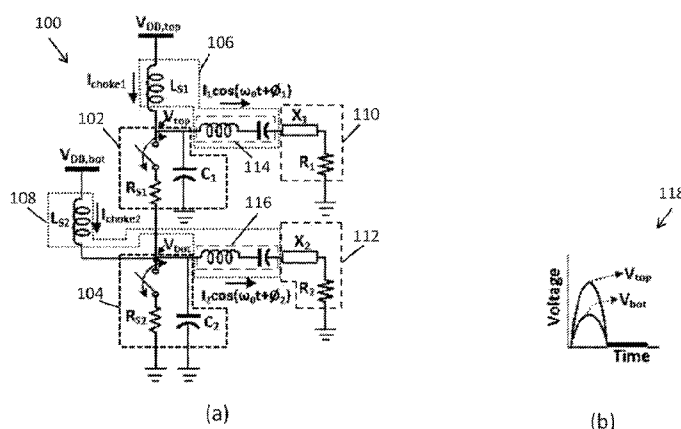


FIG. 1

(57) Abstract: In some embodiments, circuits for providing Class-E power amplifiers are provided, the circuits comprising: a first switch having a first side and a second side; a first Class-E load network coupled to the first side of the first switch; a second Class-E load network; and a second switch having a first side and a second side, the first side of the second switch being coupled the second side of the first switch and the second Class-E load network. In some embodiments, the circuits further comprise: a third switch having a first side and a second side; a third Class-E load network coupled to the first side of the third switch; a fourth Class-E load network; and a fourth switch having a first side and a second side, the first side of the fourth switch being coupled the second side of the third switch and the fourth Class-E load network.

CIRCUITS FOR PROVIDING CLASS-E POWER AMPLIFIERS

Cross Reference To Related Applications

[0001] The application claims the benefit of United States Provisional Patent Applications Nos. 61/471,645, filed April 4, 2011, and 61/620,361, filed April 4, 2012, each of which is hereby incorporated by reference herein in its entirety.

Statement Regarding Federally Funded Research

[0002] This invention was made with government support under Grant No. FA8650-10-1-7042 awarded by DARPA MTO. The government has certain rights in the invention.

Technical Field

[0003] The disclosed subject matter relates to circuits for providing Class-E power amplifiers.

Background

[0004] The Class-E family of switching Power Amplifiers (PAs) finds favor in applications requiring efficiency. In a conventional, single-transistor, Class-E PA, ideally 100% efficiency is achieved (in the absence of device and passive component losses) through the achievement of "Class-E switching conditions." "Class-E switching conditions" refers to the phenomena of Zero Voltage at Switching (ZVS) and Zero Derivative of Voltage at Switching (ZDVS) of the output node voltage. For conventional, single-transistor Class-E PAs, these

conditions can be achieved by placing a “Class-E output network” (which can include a parallel combination of an inductor to a supply voltage and a tuned load network) at the output node.

[0005] In a particular technology (e.g., CMOS, SiGe, etc.), the output power that can be obtained from a Class-E PA employing a single transistor can be limited by the breakdown voltage of that technology. Thus, a common practice to boost the output power is to stack two or more transistors, thus doubling the breakdown voltage at the final output node. In a stacked configuration, while all stacked devices may be explicitly driven, it is also possible to drive only the bottom-most device and allow the output swing of each device to turn on/off the device above it, thus reducing input power and enhancing efficiency. The main challenge in stacking multiple devices is to retain the Class-E-like behavior for all the stacked devices. Deviation from Class-E behavior leads to degradation in performance in terms of output power and efficiency. Typically, to mitigate this issue (with two stacked devices), an inductor is connected from the intermediate terminal of the stacked devices through a DC-blocking capacitor to ground, or a feed-forward capacitor is connected from the output node of the top device to the intermediate terminal of the stacked devices. However, these techniques are only partially successful in achieving Class-E behavior of both/all devices, even in an ideal situation when there are no losses in the circuit.

[0006] Accordingly, new circuits for providing Class-E power amplifiers are desired.

Summary

[0007] Circuits for providing Class-E power amplifiers are provided. In some embodiments, circuits for providing Class-E power amplifiers are provided, the circuits comprising: a first switch having a first side and a second side; a first Class-E load network

coupled to the first side of the first switch; a second Class-E load network; and a second switch having a first side and a second side, the first side of the second switch being coupled the second side of the first switch and the second Class-E load network.

Brief Description of the Drawings

[0008] FIG. 1 is a drawing of a topology for a circuit for a Class-E power amplifier in accordance with some embodiments.

[0009] FIG. 2 is a drawing of a circuit for a Class-E power amplifier in accordance with some embodiments.

[0010] FIG. 3 is a graph of switching device drain voltages in a circuit for a Class-E power amplifier in accordance with some embodiments.

[0011] FIG. 4 is a drawing of another circuit for a Class-E power amplifier in accordance with some embodiments.

[0012] FIG. 5 shows chip microphotographs of two Class-E power amplifiers like those shown in FIGS. 2 and 4 in accordance with some embodiments.

Detailed Description

[0013] Circuits for providing Class-E power amplifiers are provided.

[0014] In accordance with some embodiments, circuits for providing Class-E power amplifiers that employ stacked switching devices, each having a Class-E load network, are provided. In some embodiments, a “Class-E load network” (which can include a DC-feed inductor to a power supply in parallel with a series resonant filter connected to a Class-E load impedance) is connected at the drain node of each stacked device. The resulting topology can

result in a stacking of two (or more) single-device Class-E PAs that each retain individual Class-E characteristics. In some embodiments, output power can be derived from the intermediary node(s) in addition to the drain of the top stacked device.

[0015] FIG. 1a illustrates an example of a topology 100 for a Class-E amplifier that can be used in accordance with some embodiments.

[0016] As shown, topology 100 can include two stacked switching devices 102 and 104, two Class-E load networks 106 and 108, and two Class-E load impedances 110 and 112.

[0017] Devices 102 and 104 can be any suitable switching devices. For example, in some embodiments, switching devices 102 and 104 can be MOSFETs, BJTs, and/or any other suitable switching devices in some embodiments.

[0018] Switching devices 102 and 104 can be represented by switches S_1 and S_2 with output capacitances C_1 and C_2 and “ON” resistances R_{s1} and R_{s2} , respectively. Each of switches 102 and 104 can be driven by a square wave input with 50% duty-cycle (not shown), sine wave, and/or any other suitable input signal. In this representation, the output capacitance C_1 consists of the C_{gd} (gate to drain capacitance) and C_{db} (drain to bulk capacitance) of the top device, and the output capacitance C_2 consists of the C_{gs} (gate to source capacitance) and C_{sb} (source to bulk capacitance) of the top device, and C_{gd} and C_{db} of the bottom device.

[0019] Because each switch has a “Class-E load network” of its own and because each switch has an equal duty cycle, each switch can exhibit independent Class-E-like behavior and Class-E design equations can apply directly to each switch 102 and 104 and its load network 106 and 108, respectively. Thus, the switches can be sized to drive independent load impedances 110 and 112.

[0020] As described above and as shown in FIG. 1a, load network 106 can include a DC-feed inductor L_{S1} connected between a power supply $V_{DD,top}$ and the drain node of switch device 102 and a series resonant filter 114 connected between Class-E load impedance 110 and the drain node of switch device 102. Load network 108 can include a DC-feed inductor L_{S2} connected between a power supply $V_{DD,bot}$ and the drain node of switch device 104 and a series resonant filter 116 connected between Class-E load impedance 112 and the drain node of switch device 104.

[0021] Class-E load impedances 110 and 112 can be any suitable Class-E load impedances. As shown in FIG. 1a, these impedances can be represented by a transmission line X_1 and X_2 and a resistance R_1 and R_2 , respectively.

[0022] In some embodiments, $V_{DD,bot}$ can be chosen so that the maximum instantaneous drain-source voltage swing for the bottom device is twice the nominal supply voltage. $V_{DD,top}$ can be adjusted so that drain-source voltage swings for top and bottom devices are similar in some embodiments.

[0023] An example of a circuit 200 consistent with topology 100 in accordance with some embodiments is shown in FIG. 2. As illustrated, circuit 200 includes MOSFET switches 202 and 204 in place of switching devices 102 and 104, respectively, of FIG. 1a. Circuit 200 also includes transmission lines 220 and 226 in place of DC-feed inductors L_{S1} and L_{S2} , respectively, of FIG. 1a, and impedance transformation network 236 in place of series resonant filters 114 and 116, respectively, of FIG. 1a. Finally, circuit 200 includes switch gate bias resistors 222 and 232, a bypass capacitor 224, and input impedance transformation network 228 (which includes a transmission line and a capacitor as shown).

[0024] As shown, circuit 200 can receive an input signal at input pad 218. Any suitable input signal can be used to drive circuit 200 in some embodiments. For example, in some embodiments, circuit 200 can be driven by a sinusoidal source at input 218. Input impedance transformation network 228 can provide impedance matching so that input 218 matches the impedance of the input signal source. The resulting signal from network 228 can then be biased by resistor 232 and provided to the gate of switch 204.

[0025] Similarly, the gate of switch 202 can be DC biased by resistor 222 and AC coupled to ground by bypass capacitor 224.

[0026] In some embodiments, in order to utilize the power available from intermediary node 206 as well as the power from the drain of switch 202, the load currents of switches 202 and 204 can be power combined. Power combining can be performed in any suitable manner. For example, as shown in FIG. 2, power combining can be performed by combining the outputs from switches 202 and 204 using impedance transformation network 236.

[0027] In some embodiments, to design an impedance transformation network 236 as shown in FIG. 2, load impedances for each switching device 202 and 204 can first be determined, and then a suitable impedance transformation network to convert the load impedances to the desired power amplifier output impedance can be calculated. For example, as shown, the load impedance for device 202 can be determined to be 76 ohms and the load impedance for device 204 can be determined to be 27 ohms. This determination can be made in any suitable manner. For example, in some embodiments, for each switching device, the following equations can be solved by sweeping the output currents and phases for specified operating conditions using any suitable mechanism, such as MATLAB:

$$\frac{dV_{S,ON}}{dt} + \left(\frac{R_{on}}{L} \right) V_{S,ON} - i_0 \omega_0 R_{on} \sin(\omega_0 t + \phi) - \left(\frac{V_{DD} R_{on}}{L} \right) = 0$$

$$\frac{d^2 V_{S,OFF}}{dt^2} + \frac{V_{S,OFF}}{LC_{out}} - \frac{i_0 \omega_0}{C_{out}} \sin(\omega_0 t + \phi) - \frac{V_{DD}}{LC_{out}} = 0$$

$$P_{loss,cap} = 0.5 f_0 C_{out} \left[V_{S,OFF}^2 \left(\frac{T}{2}^- \right) - V_{S,ON}^2 \left(\frac{T}{2}^+ \right) \right]$$

$$P_{loss,switch} = R_{on} * \frac{1}{T} \int_{\frac{T}{2}}^T \left(\frac{V_{S,ON}}{R_{on}} \right)^2 dt$$

$$P_{in} = k f_0 C_{in} V_{on}^2$$

$$P_{loss,choke} = R_{choke} * \frac{1}{T} \left(\int_0^{\frac{T}{2}} i_{L,OFF}^2 dt + \int_{\frac{T}{2}}^T i_{L,ON}^2 dt \right)$$

wherein:

C_{in} is the input capacitance the switch;

C_{out} is the output capacitance of the switch;

f_0 is the operating frequency;

$i_{L,OFF}$ is the current through the choke (here, transmission line 220 or 226) when the switch is not conducting;

$i_{L,ON}$ is the current through the choke when the switch is conducting;

k is a constant of proportionality;

L is the inductance of the choke;

P_{in} is the input power expended for switching;

$P_{loss,cap}$ is the power loss in the output capacitance of the switch;

$P_{loss,choke}$ is the power loss in the choke;

$P_{loss,switch}$ is the switch power loss in the switch when it is conducting;

R_{choke} is the resistance of the choke;

R_{on} is the on resistance of switch when conducting;

T is the period of operation;

V_{on} is the amplitude of the input signal;

$V_{S,ON}$ is the voltage across switch when conducting;

$V_{S,OFF}$ is the voltage across switch when not conducting; and

ω_0 is the operating frequency in radians.

[0028] In some embodiments, because the power combined output at output pad 208 may be required to drive a 50 ohm load (not shown) (e.g., when driving a 50 ohm impedance antenna, test equipment, etc.), the load resistances for each of switches 202 and 204 can be selected so that their parallel combination is 50 ohms. For example, as illustrated in FIG. 2, load resistances 210 and 212 can each be 100 ohms, making the parallel combination 50 ohms.

[0029] In some embodiments, the load resistances seen at output pad 208 for the top and the bottom switches 202 and 204 can additionally or alternatively be chosen to be equal (e.g., each 100 ohms) so that the top and bottom switches 202 and 204 deliver equal output power.

[0030] In some embodiments, the load voltages for the top and bottom switches 202 and 204 can be selected to be identical or similar in swing and phase as shown in FIG. 1b to minimize cancellation during current-combining. As also shown in FIG. 1b, the drain voltage swing of the top device can be twice that of the bottom device in some embodiments.

[0031] Another example of waveforms V_{top} and V_{bot} that can be produced at the drains of switches 202 and 204, respectively, in response to a sinusoidal input signal in accordance with some embodiments is shown in FIG. 3.

[0032] In some embodiments, two such Class-E power amplifier unit cells, as shown in FIG. 2, can be current-combined, as shown in FIG. 4.

[0033] As illustrated in FIG. 4, two quarter-wave transmission lines 402 and 404 can be used to equally split the input power from an input pad 406 to two Class-E amplifiers 408 and 410 in some embodiments. Each of amplifiers 408 and 410 can be implemented in any suitable manner, such as shown by circuit 412 in area 414. As shown, circuit 412 is similar to circuit 200 except that impedance transformation network 416 is implemented differently than impedance transformation network 236.

[0034] As described above in connection with FIG. 2, the output impedance at output pad 418 can be configured to match the impedance (e.g., 50 ohm) of any suitable load (e.g., an antenna, test equipment, etc.) connected thereto. Because there are four transistors driving output pad 418, the output impedance of each can be transformed to be 200 ohms so that the parallel combination of these impedances is 50 ohms in some embodiments.

[0035] In some embodiments, the DC-feed inductances and the transmission lines in the impedance matching networks can be implemented using Coplanar Waveguides (CPWs) with continuous ground plane. As shown in FIGS. 2 and 4, the transmission lines can have the lengths specified (e.g., 350 μm for transmission line 220 of FIG. 2) and the impedances specified (e.g., 66 ohms for transmission line 220 of FIG. 2), or any other suitable values. Vertical Natural Capacitors (VNCAPs) can be utilized for the capacitors in the circuits in some embodiments.

[0036] In some embodiments, such CPWs can have a measured quality factor of ≈ 15 -18 in the Q-band, and the measured quality factor of a $W=7.3\ \mu\text{m} \times L=8\ \mu\text{m}$ 70fF VNCAP and a $W=19\ \mu\text{m} \times L=9\ \mu\text{m}$ 214fF VNCAP can be 13 and 7, respectively, at 45GHz.

[0037] In some embodiments, Class-E power amplifiers as described herein can be fabricated in IBM's 45nm SOI CMOS technology using 56-nm body-contacted N-type Metal-Oxide-Semiconductor (NMOS) devices stacked as described above. Chip microphotographs of two such Class-E power amplifiers like those shown in FIGS. 2 and 4, respectively, are shown in FIGS. 5(a) and 5(b). These Class-E power amplifiers can occupy $0.8\text{mm} \times 0.6\text{mm}$ and $1.06\text{mm} \times 0.6\text{mm}$ of die area, respectively, in some embodiments. The operating frequency of these amplifiers can be 45 GHz or any other suitable frequency in some embodiments.

[0038] More particularly, for example, in some embodiments, the top switch 202 in FIG. 2 can have a channel length of 56 nm and 60 fingers (each with a width of 1.5 μm), while the

bottom switch 204 in FIG. 2 can have a channel length of 56 nm and 60 fingers (each of width 3 μm).

[0039] As another more particular example, the top switch in FIG. 4 can have a channel length of 56 nm and 100 fingers (each with a width of 1.5 μm), while the bottom switch in FIG. 4 can have a channel length of 56 nm and 100 fingers (each of width 3 μm).

[0040] In some embodiments, with IBM's 45 nm SOI CMOS technology, the 2.225 μm thick topmost metal layer (LB) can constitute a signal conductor while the three lowermost metal layers (M1-M3) can be used for a ground plane.

[0041] In some embodiments, usage of 40 nm floating-body devices and splitting the overall device into several smaller devices wired appropriately in parallel can be used to improve the f_{max} , and hence the gain available from the device.

[0042] In some embodiments, power amplifiers as described herein can be used in any suitable application. For example, in some embodiments, these power amplifiers can be used in applications that involve the use of efficient, high-power wireless transmitters. More particularly, for example, potential applications can include handset and base-station power amplifiers for cellular telephony, transmitters for wireless LAN, Bluetooth and other radio-frequency wireless applications, millimeter-wave vehicular radar currently being explored and deployed in the 22-29 GHz and 77 GHz frequency ranges, and transmitters for 60 GHz wireless personal area networks (WPANs).

[0043] Although the invention has been described and illustrated in the foregoing illustrative embodiments, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the details of implementation of the invention can be made without departing from the spirit and scope of the invention, which is limited only by the

claims that follow. Features of the disclosed embodiments can be combined and rearranged in various ways.

What is claimed is:

1. A circuit for forming a Class-E power amplifier comprising:
 - a first switch having a first side and a second side;
 - a first Class-E load network coupled to the first side of the first switch;
 - a second Class-E load network; and
 - a second switch having a first side and a second side, the first side of the second switch being coupled the second side of the first switch and the second Class-E load network.
2. The circuit of claim 1, wherein the first Class-E load network includes a first choke having a first side and a second side, the first side of the first choke being coupled to a first power supply voltage and the second side of the first choke being coupled to the first side of the first switch.
3. The circuit of claim 1, wherein the first Class-E load network includes a first resonant filter having a first side and a second side, the first side of the resonant filter being coupled to a load and the second side of the resonant filter being coupled to the first side of the first switch.
4. The circuit of claim 1, wherein the second Class-E load network includes a second choke having a first side and a second side, the first side of the second choke being coupled to a second power supply voltage and the second side of the second choke being coupled to the first side of the second switch.

5. The circuit of claim 1, wherein the second Class-E load network includes a second resonant filter having a first side and a second side, the first side of the second resonant filter being coupled to a load and the second side of the second resonant filter being coupled to the first side of the second switch.
6. The circuit of claim 1, wherein each of the first switch and the second switch include a field effect transistor, and wherein the first side and the second side of each of the first switch and the second switch correspond to a source and a drain of the field effect transistor.
7. The circuit of claim 1, wherein the first choke and the second choke include an inductor.
8. The circuit of claim 1, wherein the first resonant filter includes an inductor and a capacitor.
9. The circuit of claim 1, wherein the first Class-E load network includes a transmission line coupled to the first side of the first switch and to a first power supply voltage.
10. The circuit of claim 1, wherein the second Class-E load network includes a transmission line coupled to the first side of the second switch and to a second power supply voltage.
11. The circuit of claim 1, wherein the first Class-E load network includes at least a portion of an impedance transformation network.

12. The circuit of claim 11, wherein the second Class-E load network includes at least a portion of the impedance transformation network.
13. The circuit of claim 11, wherein the impedance transformation network includes a first capacitor, a second capacitor, and a transmission line.
14. The circuit of claim 1, wherein the second switch includes a control input coupled to an input signal.
15. The circuit of claim 14, wherein the control input of the second switch is a gate of a field effect transistor.
16. The circuit of claim 14, wherein the control input is coupled to the input signal by an impedance transformation network.
17. The circuit of claim 16, wherein the impedance transformation network includes a transmission line and a capacitor.
18. The circuit of claim 1, further comprising:
 - a third switch having a first side and a second side;
 - a third Class-E load network coupled to the first side of the third switch;
 - a fourth Class-E load network; and

a fourth switch having a first side and a second side, the first side of the fourth switch being coupled the second side of the third switch and the fourth Class-E load network.

19. The circuit of claim 18, further comprising:

a first transmission line having a first side and a second side, wherein the first side is coupled to an input signal and the second side is coupled to a control input of at least one of the first switch and the second switch; and

a second transmission line having a first side and a second side, wherein the first side is coupled to the input signal and the second side is coupled to a control input of at least one of the third switch and the fourth switch.

20. The circuit of claim 18, further comprising an output coupled to at least one of the first Class-E load network and the second Class-E load network and to at least one of the third Class-E load network and the fourth Class-E load network.

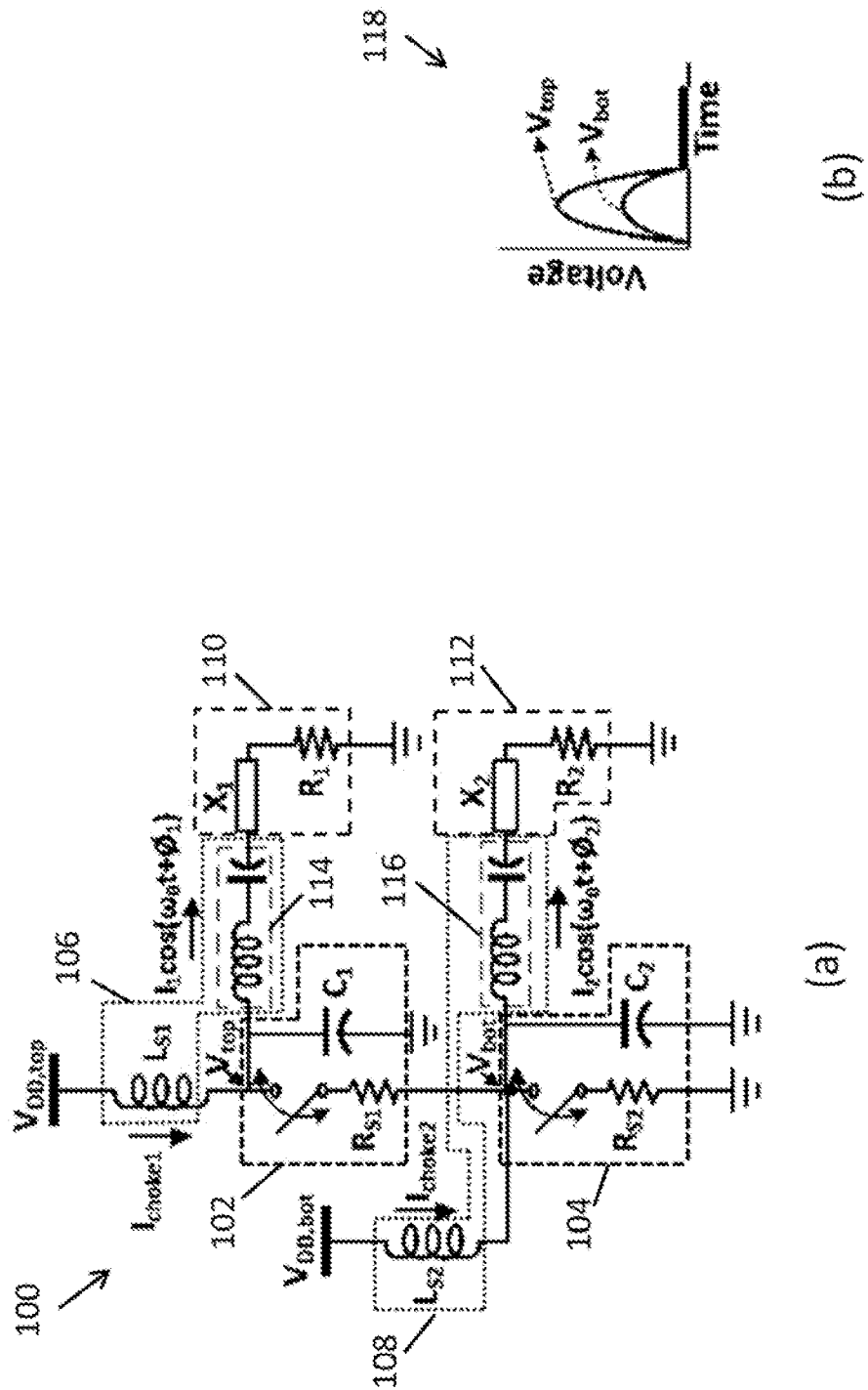


FIG. 1

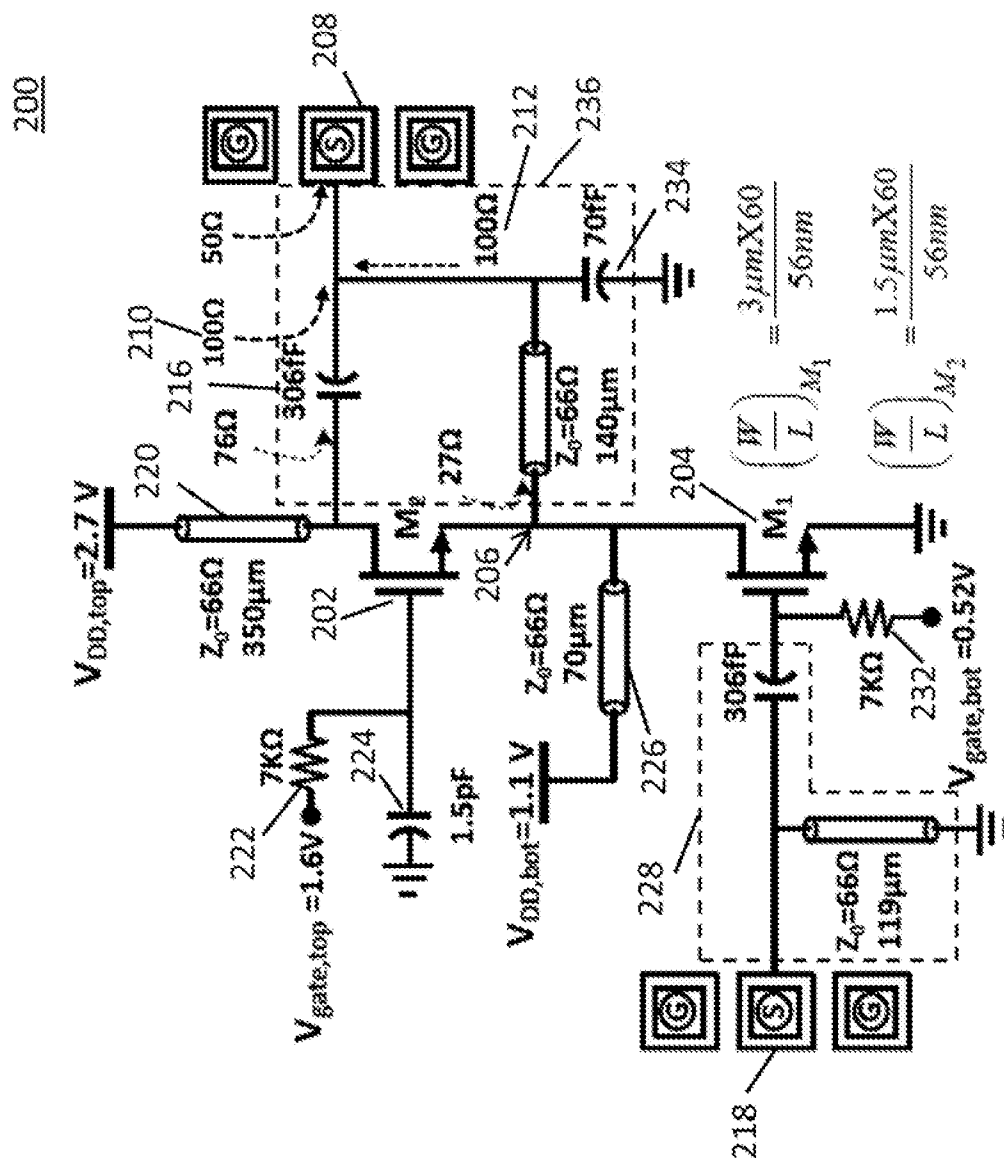


FIG. 2

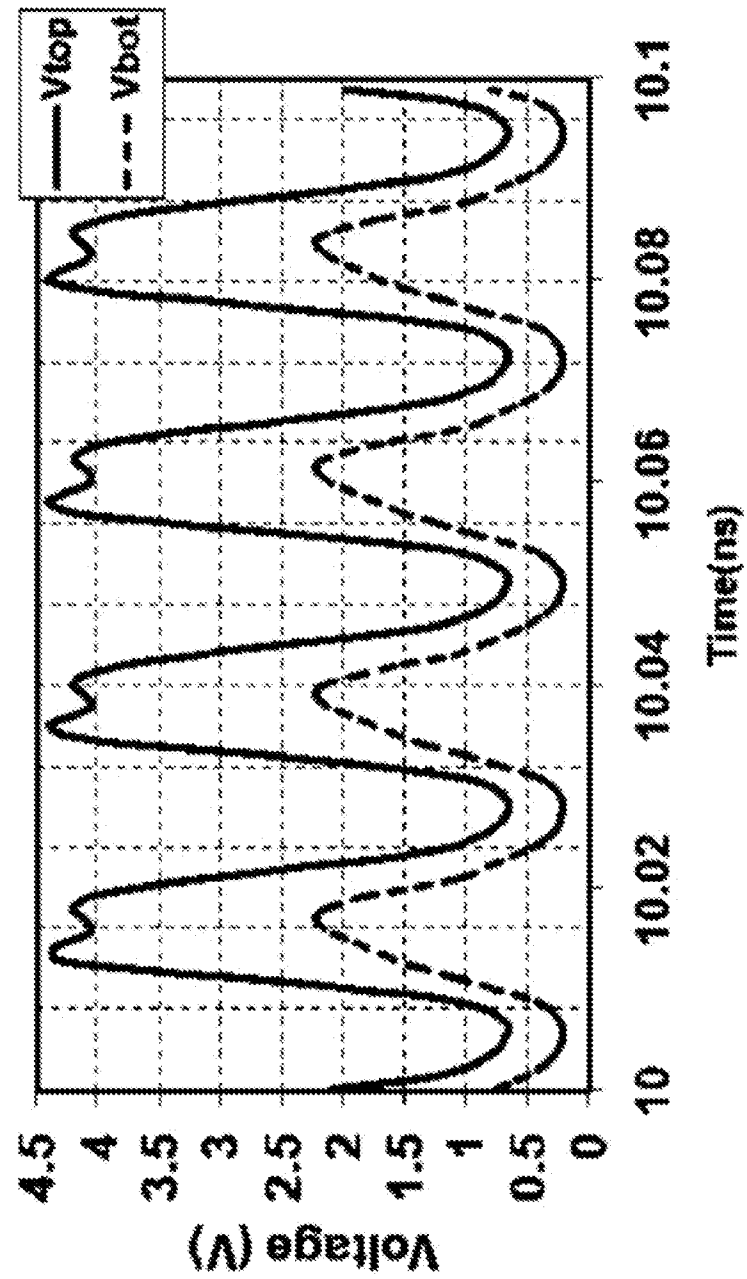
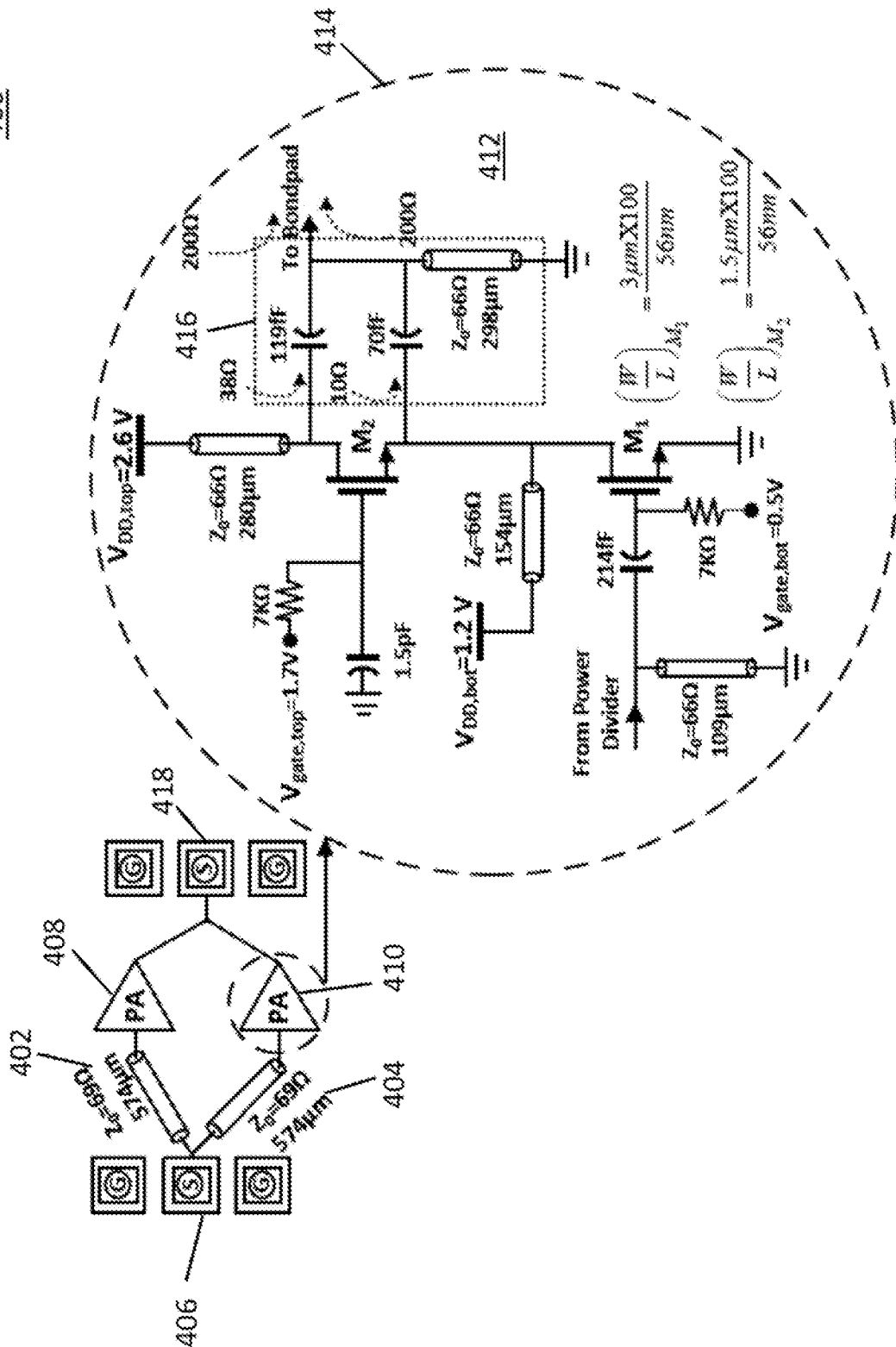


FIG. 3

400



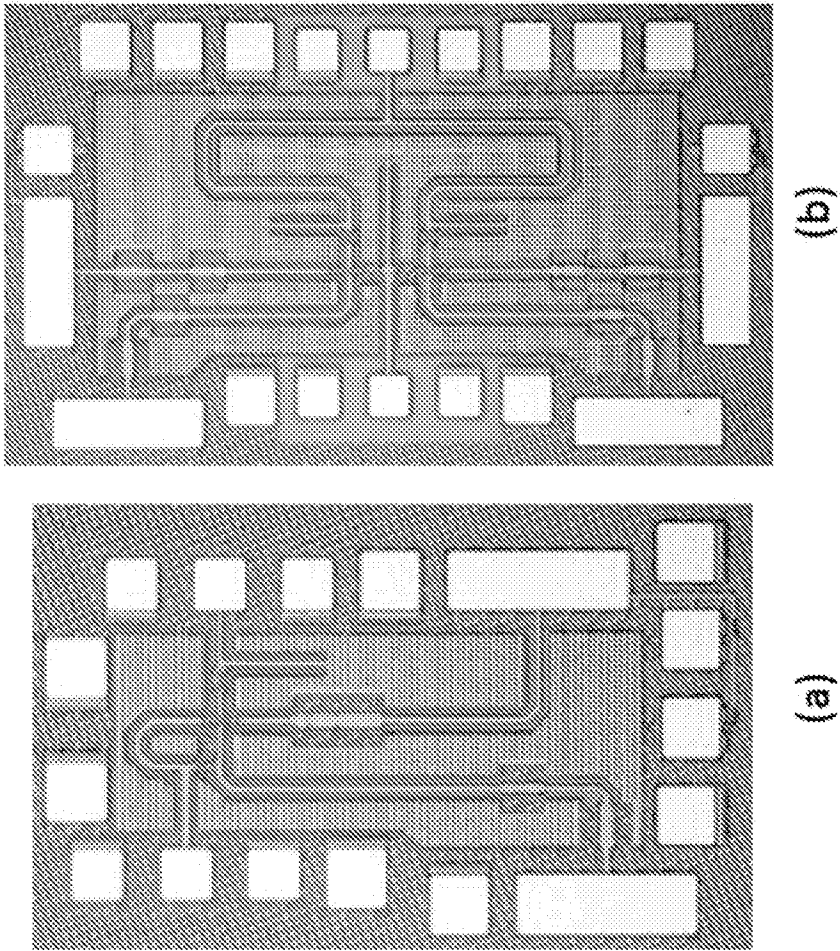


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 12/32218

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H03F 3/16 (2012.01)

USPC - 330/300

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 330/300

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 330/51, 105, 299, 300 (keyword limited - see search terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PubWEST (PGPB, USPT, USOC, EPAB, JPAB); GOOGLE; Google Scholar

Terms: amplifier, power, class, e, filter, choke, voltage, transistor, switch, stack, resonant, impedance, load, field, effect, transmission, line.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2006/0270367 A1 (Burgener et al.) 30 November 2006 (30.11.2006), entire document, especially abstract, Fig. 2, para [0009], [0011], [0013], [0041], [0054], [0061], [0067], [0090].	1-20
Y	US 2004/0113689 A1 (Hajimiri et al.) 17 June 2004 (17.06.2004), entire document, especially abstract, Fig. 1, para [0008], [0012], [0014], [0020], [0076].	1-20
A	US 2006/0261890 A1 (Floyd et al.) 23 November 2006 (23.11.2006), entire document, especially abstract, para [0002], [0003], [0027], [0030], [0039], [0046].	1-20

☐ Further documents are listed in the continuation of Box C.

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Date of the actual completion of the international search

12 July 2012 (12.07.2012)

Date of mailing of the international search report

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