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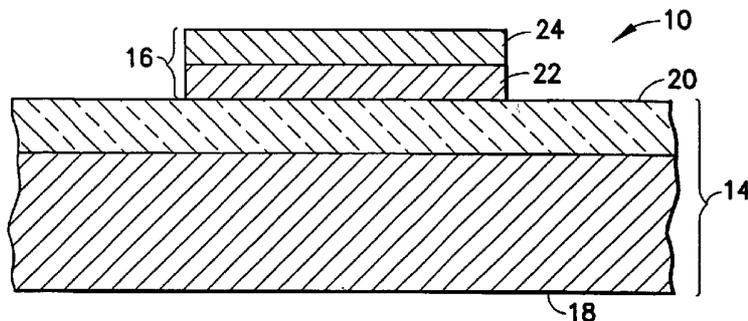
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(54) Title: IMPROVED ELECTRODE FOR THIN FILM CAPACITOR DEVICES



(57) Abstract: A method of forming a conductor (16) on a substrate (14) including steps of depositing tantalum (22) on a glass layer (20) of the substrate; oxidizing the tantalum; and depositing a noble metal (24) on the oxidized tantalum to form the conductor. The method can be used to form a ferroelectric capacitor (12) or other thin film ferroelectric device. The device can include a substrate comprising a glass layer (20); and an electrode (16) connected to the glass layer. The electrode comprising can include a noble metal (24) connected to the glass layer (20) by an adhesion layer (22) comprising Ta<sub>2</sub>O<sub>5</sub>.



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**IMPROVED ELECTRODE FOR THIN FILM CAPACITOR DEVICES**

## GOVERNMENT RIGHTS

This invention was made with U.S. Government support under contract No. F33615-98-2-1357 awarded by the Department of the Air Force. The U.S. Government has certain rights in this invention.

## BACKGROUND OF THE INVENTION

## 1. Field of the Invention

The present invention relates to thin film capacitor devices or ferroelectric devices and, more particularly, to a method of forming an electrode on a glass layer of a substrate.

## 2. Brief Description of Prior Developments

Platinum (Pt) is commonly used as an electrode material for thin-film ferroelectric devices. This is due to its resistance to oxidation at temperatures above 600° C in oxygen (O<sub>2</sub>); an environment which is required to obtain good electrical characteristics from materials such as (BaSr)TiO<sub>3</sub> (BST), (PbZr)TiO<sub>3</sub> (PZT), SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub> (SBT), SrBi<sub>2</sub>Nb<sub>2</sub>O<sub>9</sub> (SBN), SrBi<sub>2</sub>(TaNb)<sub>2</sub>O<sub>9</sub> (SBTN) and others. Devices using these materials are frequently made using oxidized silicon wafers as a substrate.

Adhesion of a platinum electrode to the oxide of the silicon wafer has always been a problem. The problem has been exacerbated due to the unique properties of platinum and challenges of thin film ferroelectric processing. Platinum has a tendency to plastic flow in response to stress at temperatures above 600° C. Ferroelectric thin

film deposition is frequently performed using spin-on methods which result in a very high tensile stress due to film shrinkage as it is sintered. The ferroelectric material can contain metals such as Bi. These metals can alloy with the platinum.

The ferroelectric processes often incorporate long anneals in O<sub>2</sub> at elevated temperature to improve performance. Even if the platinum adheres to the substrate, these processes frequently cause the formation of hillocks or bumps on the surface of the platinum electrode. These hillocks can cause localized high electric fields, high leakage, and early breakdown. In more severe cases, hillocks can be large enough to directly short out the ferroelectric device or combine with other defects in the film to short out the devices resulting in reduced yield or unusable devices.

Historically a thin film of titanium (Ti) has been added between the platinum and the oxide of the silicon wafer. This titanium layer is about 10% of the thickness of the platinum electrode and greatly improves adhesion of the platinum to the oxide. An example of this electrode is given in U.S. Patent No. 5,723,171. The use of a titanium adhesion layer has two major problems. First, the process windows are very narrow. Changes in anneal times or temperatures or changes in the thickness of the ferroelectric often require a re-optimization of the titanium and platinum layer thicknesses. Second, titanium is very mobile and can migrate through the platinum electrode causing degraded performance of the ferroelectric layer. This is a known problem with BST, SBT, SBTN and others where variations in film

composition, due to titanium incorporation degrade film performance.

Other methods to improve adhesion have been employed with a wide variety of metallic layers such as Cr, Ta, Vd, Nb, 5 Sr, Ru, Os, Pd (see U.S. Patent Nos. 6,103,400 and 6,054,311). While these other metals may work over some range of conditions, these processes all suffer from either poor adhesion or from volume expansion of the adhesion layer due to oxidation during high temperature 10 oxygen anneals which results in an unstable foundation for the platinum and limits their utility.

#### SUMMARY OF THE INVENTION

In accordance with one method of the present invention, a method of forming a conductor on a substrate is provided 15 comprising steps of depositing tantalum on a glass layer of the substrate; oxidizing the tantalum; and depositing a noble metal on the oxidized tantalum to form the conductor.

In accordance with another method of the present 20 invention, a thin film ferroelectric device is provided comprising a substrate comprising a glass layer; and an electrode connected to the glass layer. The electrode comprises a noble metal connected to the glass layer by an adhesion layer comprising Ta<sub>2</sub>O<sub>5</sub>.

25 In accordance with one aspect of the present invention, a thin film ferroelectric device is provided comprising a substrate comprising a glass layer; and an electrode connected to the glass layer. The electrode comprises a

noble metal connected to the glass layer by an adhesion layer comprising Ta<sub>2</sub>O<sub>5</sub>.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and other features of the present invention are explained in the following description, taken in connection with the accompanying drawings, wherein:

Fig. 1 is a schematic cross sectional diagram of a component incorporating features of the present invention;

Fig. 2 is a schematic cross sectional diagram of the component shown in Fig. 1 before the electrode is formed;

Fig. 3 is a process flow chart of steps used to form the component shown in Fig. 1;

Fig. 4 is a diagram of some of the devices used to form the component shown in Fig. 1; and

Fig. 5 is a schematic cross sectional diagram of a ferroelectric capacitor incorporating features of the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Fig. 1, there is shown a diagram of a cross section of a subcomponent 10 incorporating features of the present invention. Although the present invention will be described with reference to the exemplary embodiment shown in the drawings, it should be understood

that the present invention can be embodied in many alternate forms of embodiments. In addition, any suitable size, shape or type of elements or materials could be used.

5 The subcomponent 10 is generally intended to be used in fabricating a larger electrical component, such as a thin film ferroelectric device. For example, the component 10 could be used to fabricate a ferroelectric device, such as a ferroelectric capacitor 12 (see Fig. 5). The  
10 subcomponent 10 generally comprises a substrate 14 and an electrode 16.

The substrate 14, in the embodiment shown, is preferably a semiconductor wafer. However, in alternate  
15 embodiments, any suitable type of substrate could be provided. The substrate 14 generally comprises a base 18 and a top layer 20. The base 18 preferably comprises a 3-15 ohm-cm Phosphorous doped silicon substrate. However, any suitable type of base could be provided. In  
20 the embodiment shown, the top layer 20 is comprised of glass. In a preferred embodiment, the glass layer 20 comprises silicon dioxide ( $\text{SiO}_2$ ). For example, the glass layer 20 could comprise 5000 Å thick wet silicon oxide. However, in alternate embodiments, the substrate 14 could be comprised of any suitable type of a top layer.

25 The electrode 16, in the embodiment shown, generally comprises an adhesion layer 22 and a electrical conductor layer 24. The adhesion layer 22 is preferably comprised of tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ). The adhesion layer could be selected from a group consisting of tantalum oxide,  
30 titanium oxide, zirconium oxide, hafnium oxide and vanadium oxide. The electrical conductor layer 24 is

comprised of a noble metal, preferably platinum. The noble metal conductor could be selected from a group consisting of platinum, palladium, gold and rhodium. The electrical conductor layer 24 is attached to the top player 20 of the substrate 14 by the adhesion layer 22.

Adhesion of platinum (Pt) to glasses, such as silicon oxide ( $\text{SiO}_2$ ), has been a longstanding problem. Traditionally, the adhesion issue has been dealt with by including a thin metallic adhesion layer between the platinum and the glass. This layer is typically composed of Ti, Cr, Ta, Va, Nb, Pd, Ir, Ru and is typically about 10% of the thickness of the platinum layer. Use of such adhesion layers results in very narrow process windows if the platinum electrode is to survive in oxidizing environments at temperatures above about  $600^\circ\text{C}$ . This is due to a combination of the tendency of platinum to plastic flow at these temperatures in response to stress and the poor performance of the platinum as a barrier to oxygen, which allows oxidation of the adhesion layer causing a volume expansion. This means that the typical metallic adhesion layer is an unstable surface for the platinum in this environment.

The most commonly used adhesion layer, titanium (Ti), has the further problem of migrating through the platinum electrodes. When used in an electrode for thin ceramic films, this causes stoichiometry changes and/or contamination issues which can result in degraded performance. Examples of this degradation include a reduction in relative permittivity for BST and reduced remnant polarization in SBTN or PZT.

The new electrode system of the present invention combines heated deposition, to control stresses in the metal layers, and oxidation of the adhesion layer before depositing the conductive layer. Oxidation of the adhesion layer before depositing the conductive layer prevents volume expansion from occurring during subsequent thermal processing. This results in a smooth, highly adherent surface which remains smooth during subsequent processing. Further, these electrodes show little sensitivity to variations in thickness of either the platinum or the adhesion layer, little sensitivity to the purity of the deposited materials, and little sensitivity to anneal processes. This allows use of thicker electrodes which, for many applications, are required for increased power/current handling or reduced resistive loss. These electrodes of the present invention remain smooth and planar even when exposed to very high compressive stresses and through anneals as long as 10 hours at 725° C in oxygen. These electrodes also show higher remnant polarization (2Pr) in SBTN and lower leakage and higher breakdown fields in BST.

Referring also to Figs. 2 and 3, Fig. 2 shows the subcomponent 10 of Fig. 1 before the electrical conductor layer 24 is formed thereon. Fig. 3 illustrates some of the method steps used to form the subcomponent 10. As shown by block 26, tantalum is deposited on the top glass layer 20. After the tantalum is deposited on the top glass layer 20, the tantalum is then oxidized as illustrated by block 28. This forms the assembly as shown in Fig. 2. With the tantalum oxide 22 attached to the top glass layer 20, a noble metal (in this embodiment

Pt) is deposited on the tantalum oxide as illustrated by block 30.

Referring also to Fig. 4, in a preferred method, an evaporator 32 is used for heated deposition of the tantalum and the platinum on the wafer which eventually forms the subcomponent 10. However, in alternate embodiments, the tantalum and the platinum could be deposited on the wafer by any suitable method, and perhaps by different methods. The evaporator 32 is preferably an e-beam evaporator which can heat the wafer 15 in a vacuum. However, in alternate embodiments, any suitable evaporator or metal deposition method could be used. In order to oxidize the tantalum, the system comprises a rapid thermal processor (RTP) 34. However, in alternate embodiments, any suitable device for oxidizing the tantalum could be used, including in-situ oxidations within the metal deposition system by the introduction of oxygen, direct evaporation of  $TA_2O_5$  or reactive sputter of  $TA_2O_5$  in an  $O_2$  environment. The metal oxide adhesion layer may be deposited by direct sputtering of a metal oxide target; by vacuum deposition using MOCVD of an appropriate precursor; by spin-on deposition and firing of a MOD or sol-gel precursor; or by any method suitable for depositing metal oxide films. The rapid thermal processor can expose the wafer 15 to an elevated temperature for a predetermined time in an oxygen ambient atmosphere. This process completely oxidizes the metallic tantalum layer.

After the tantalum layer has been oxidized to form the tantalum oxide layer 22, the wafers 15 are then placed back into the evaporator 32 and heated to a predetermined temperature in a vacuum where the noble metal (Pt in the

embodiment shown) layer can be deposited. In a preferred embodiment, the predetermined temperature is about 310 degrees Celsius. However, in alternate embodiments, any suitable temperature could be used. In a preferred  
5 embodiment, the platinum layer 24 has a thickness of about 2500 angstroms. However, in alternate embodiments, the platinum layer could have any suitable thickness. For example, the electrical conductor layer 24 could be from about 1600 angstroms to about 3500 angstroms.

10 Referring now also to Fig. 5, the subcomponent 10 is shown as part of a ferroelectric capacitor 12. The capacitor 12 generally comprises the subcomponent 10, a ferroelectric layer (FE) 42, a top electrode (TE) 44, an interlayer dielectric (ILD) 46, and an interconnect metal  
15 (M3) 48. In the embodiment shown, the electrode 16 forms the bottom electrode for the capacitor 12. In a preferred embodiment, the electrode 16 is about 2500 Å. However, in alternate embodiments, the electrode could have any suitable thickness.

20 In the preferred embodiment shown, the ferroelectric layer 42 is about 2000 Å, the top electrode 44 is about 1100 Å, the inter layer dielectric 46 is about 3000 Å, and the interconnect metal 48 is about 1850 Å. However, in alternate embodiments, these components could have any  
25 suitable thickness. The ferroelectric thin film layer 42 could comprise barium titanate, strontium titanate, barium strontium titanate, lead zirconate titanate, strontium bismuth tantalate or strontium bismuth tantalate niobate. In the preferred embodiment shown,  
30 the top electrode 44 is comprised of platinum. However, in alternate embodiments, the top electrode 44 could comprise any suitable type of electrical conductor

material. In the embodiment shown, the interlayer dielectric 46 is comprised of low pressure chemical vapor deposition (LPCVD)  $\text{SiO}_2$ . However, an alternate embodiments, the interlayer dielectric could be comprised of any suitable type of material and formed by any suitable method. In the embodiment shown, the interconnect metal 48 is comprised of platinum. However, in alternate embodiment, the interconnect metal 48 could be comprised of any suitable type of electrical conductor material.

The present invention can provide improved performance of thin-film dielectric and ferroelectric devices. Both leakage current and breakdown voltage of thin insulating films are dependant on the morphology of the underlying electrode. This invention allows the formation of a stable, smooth, and highly adherent electrode even with the relatively large thermal budgets required to produce high-quality ceramic thin films. Traditional films are marginal in adhesion and have a tendency to form a rough hillocked surface when exposed to high temperature oxidizing environments and high stresses.

This new adhesive layer comprises a metal oxide, for example  $\text{Ta}_2\text{O}_5$ , such as formed by evaporating tantalum metal and oxidizing it in a rapid thermal processor, as a stable adhesion layer before deposition of the platinum (or other noble metal) electrode. When this is combined with heated deposition of the platinum to control stresses, the electrode remains planar and very smooth over a wide range of anneal and process conditions. This electrode also appears to be quite insensitive to process variations such as thickness of the tantalum layer,

tantalum anneal conditions, thickness of the platinum layer, and age of the platinum melt.

5 Ferroelectric devices fabricated on this new electrode show improved yield, higher breakdown resistance, and improved electrical properties when compared to previous conventional electrode structures. Use of this electrode structure has proven important to work on a BST varactor (such as described in U.S. Patent No. 6,101,102) which requires very thick electrode layers to minimize  
10 resistive losses and high breakdown fields to achieve a wide tuning range and high current density.

In a preferred embodiment the substrate is a silicon wafer which has been wet oxidized to produce a 5000A thick SiO<sub>2</sub> film. The wafer is then placed in an e-beam  
15 evaporator and heated to a temperature of 250° C in a vacuum. A tantalum layer, approximately 200A thick, is then evaporated onto the heated substrate. The system is vented and the wafer is allowed to cool. Neither the wafer temperature during evaporation nor the thickness of  
20 the tantalum layer are critical. The wafer is then removed from the system and the tantalum metal is oxidized by using a rapid thermal processor (RTP) to expose the wafer to a temperature of 725° C for two minutes in an oxygen ambient atmosphere. Again, neither  
25 the time nor the temperature of this process is critical as long as the tantalum layer is fully oxidized.

Good results were achieved for anneal times from 1 to 7 minutes. The anneal temperature of 725° C was chosen for convenience since 725° C is the normal anneal temperature  
30 used for ferroelectric films. Other temperatures were not explored, but certainly could be possible. While use

of an RTP to perform this oxidation was initially chosen for convenience, it is likely that the use of a RTP to perform this anneal might be preferred. Long furnace tube anneals may result in a smoother Ta<sub>2</sub>O<sub>5</sub> surface with a large grain size which platinum may not adhere to very well.

After the tantalum layer has been oxidized, the wafer is then placed back into the evaporator and heated to a temperature of 310° C in a vacuum where a platinum layer about 2500A thick is deposited. The thickness of the platinum layer is not critical. In tests, there has been success with platinum layer ranging from 1600A to 3500A and greater with this process. The temperature of the wafer during this deposition might be important due to its effect on the tensile stress of the wafers after cooling. Depositions at temperatures at or above 300° C show an improvement in surface smoothness and adhesion compared to lower temperature depositions. This result in essentially featureless surfaces at magnifications up to 1000X. In a test of the process, maximum deposition temperature was limited by VITON™ seals in the vacuum system, so significantly higher temperature depositions have not been explored, but may be possible.

After venting and cooling, the wafer is removed from the vacuum system. At this stage the wafer is reasonably adherent and smooth. If necessary, improved adhesion can be obtained by a brief exposure to a higher temperature such as 30 seconds at 725° C in an RTP, either as a separate anneal on the electrode only, or combined with the crystallization anneal on a subsequently deposited ferroelectric layer. The electrode surface will remain

very smooth through the remainder of the ferroelectric processing including anneals totaling 10 hours at 725° C.

These improved electrodes have been tested with several ferroelectric materials including Bi containing  
5 ferroelectric films (SBT(N)) and BST films having very high tensile stress. The devices made with the improved electrodes have improved ferroelectric performance, leakage currents, and greater current handling ability. The use of metal oxides such as Ta<sub>2</sub>O<sub>5</sub> as an adhesion layer  
10 for platinum electrodes used with ceramic thin films is not known to exist in the prior art.

As an overview of a capacitor array process, the process can comprises the following steps:

- Prepared starting wafer with 5000 Å wet oxidation
- 15 • Deposit Bottom Electrode (BE)
- Spin On Ferroelectric Precursor And Fire (FE)
- Deposit Top Electrode (TE)
- Etch Capacitor Stack
- Test Point 1 To Verify Good Ferroelectric Properties
- 20 • Deposit Interlayer Dielectric (ILD)
- Open Contacts (CT)
- Deposit Interconnect Metal (M3)
- Etch Interconnect Metal
- Test Point 2 To Screen For Yield

- Deposit Overglass
- Open Pads (GL)
- Final Parametric Test

As an overview of the improved bottom electrode process  
5 of the present invention, the process can comprise the following steps:

- deposit Ta adhesion layer
  - o for example, 200A evaporated into wafer at 250°  
C
- 10 • oxidize adhesion layer
  - o for example, RTA 2 minutes at 725° C in O<sub>2</sub>
- deposit Pt electrode
  - o for example, 2500A evaporated onto wafers at  
310° C
- 15 • if used in process without an RTP FE crystallization step, then an adhesion anneal may be desirable
  - o for example, RTA 30 seconds at 725° in O<sub>2</sub>.

The improved electrodes of the present invention can  
provide many benefits. The electrodes can provide an  
20 improved performance, such as improved switching characteristics for ferroelectrics (2Pr, 2Ec), and larger NDRO signal for ferroelectrics. The electrodes can comprise smoother electrode surfaces both before and after FE firing. This can provide significantly improved  
25 yield, lower leakage current, and increased breakdown.

The improved electrode forming process can also allow thicker electrodes to be used. This can reduce conductive loss in electrodes which can dominate device performance at higher frequencies. The improved  
5 electrode forming process can provide larger process windows which are relatively insensitive to RTP oxidation time, Ta thickness, Pt thickness, and Pt purity. The present invention can provide benefits for a variety of materials such as SBTN, SBT and BST.

10 It should be understood that the foregoing description is only illustrative of the invention. Various alternatives and modifications can be devised by those skilled in the art without departing from the invention. Accordingly,  
15 the present invention is intended to embrace all such alternatives, modifications and variances which fall within the scope of the claims.

**Claims**

What is claimed is:

1. An electrode (16) for a thin film capacitor device (12) comprising:

a metal oxide adhesion layer (22); and

a noble metal conductor (24) connected on the metal oxide adhesion layer.

2. An electrode as in claim 1 wherein the adhesion layer (22) is selected from a group consisting of tantalum oxide, titanium oxide, zirconium oxide, hafnium oxide and vanadium oxide.

3. An electrode as in claim 1 wherein the noble metal conductor (24) is selected from a group consisting of platinum, palladium, gold and rhodium.

4. An electrode as in claim 1 wherein the adhesion layer (22) comprises tantalum pentoxide.

5. An electrode as in claim 1 wherein the noble metal conductor (24) comprises platinum.

6. A method of forming an electrode (16) for a thin film capacitive device (12) comprising steps of:

deposition of a metal oxide adhesion layer (22) on a top layer (20) of a glass substrate (14); and

deposition of a noble metal conductor (24) on the metal oxide adhesion layer (22).

7. A method as in claim 6 wherein the metal oxide adhesion layer (22) is formed by deposition of a metal followed by oxidation.

8. A method as in claim 7 wherein the step of oxidation comprises heat treatment in an oxygen containing environment.

9. A method as in claim 7 wherein the step of oxidation comprises heat treatment in a rapid thermal processor in an oxygen containing environment.

10. A method as in claim 6 wherein the metal oxide adhesion layer (24) comprises tantalum oxide.

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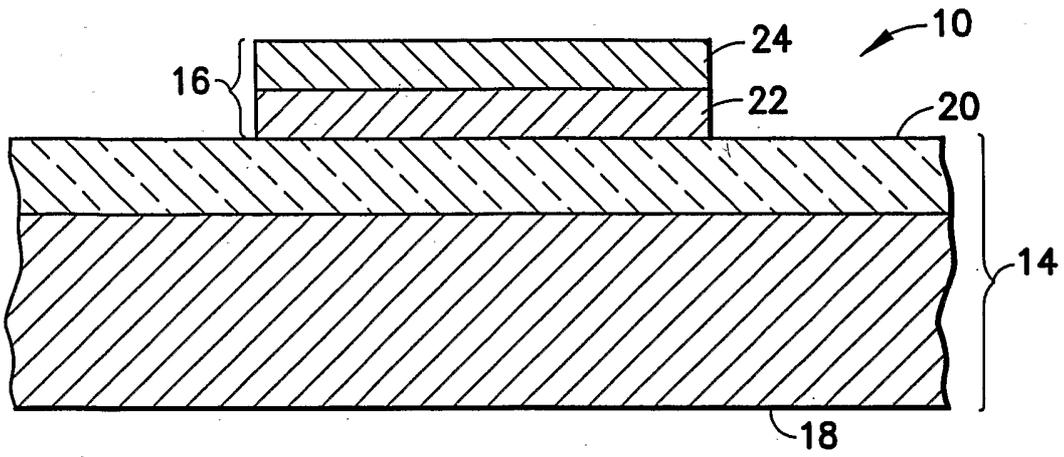


FIG. 1

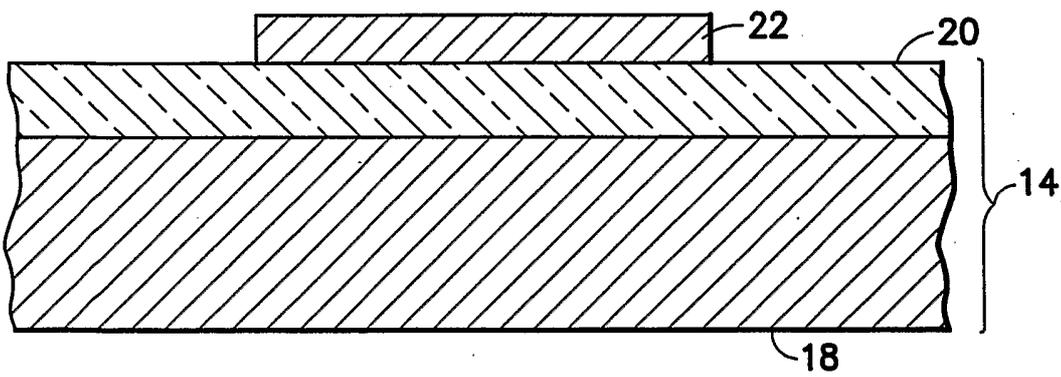


FIG. 2

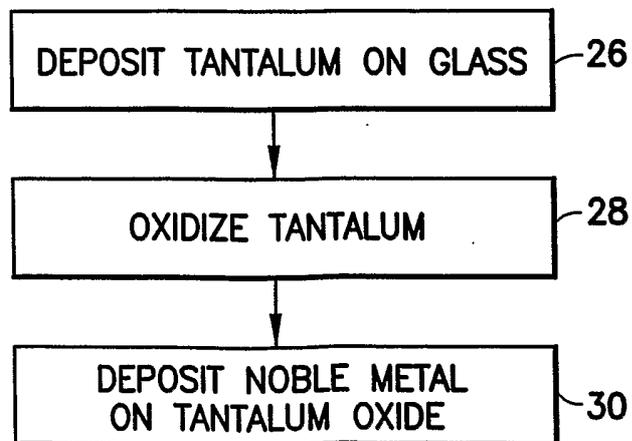


FIG. 3

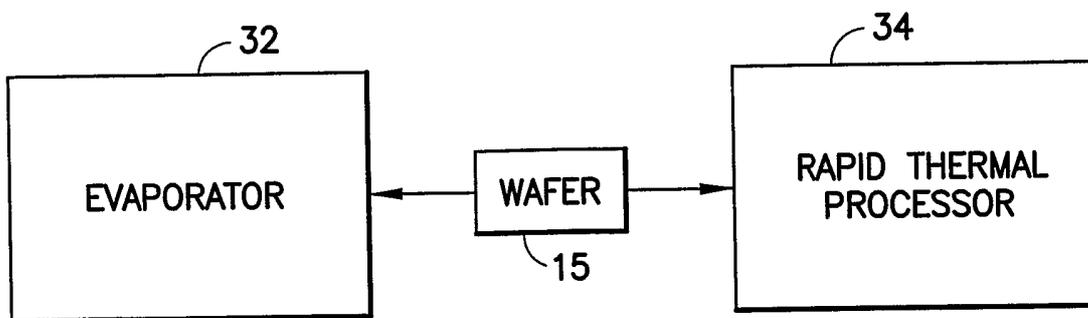


FIG.4

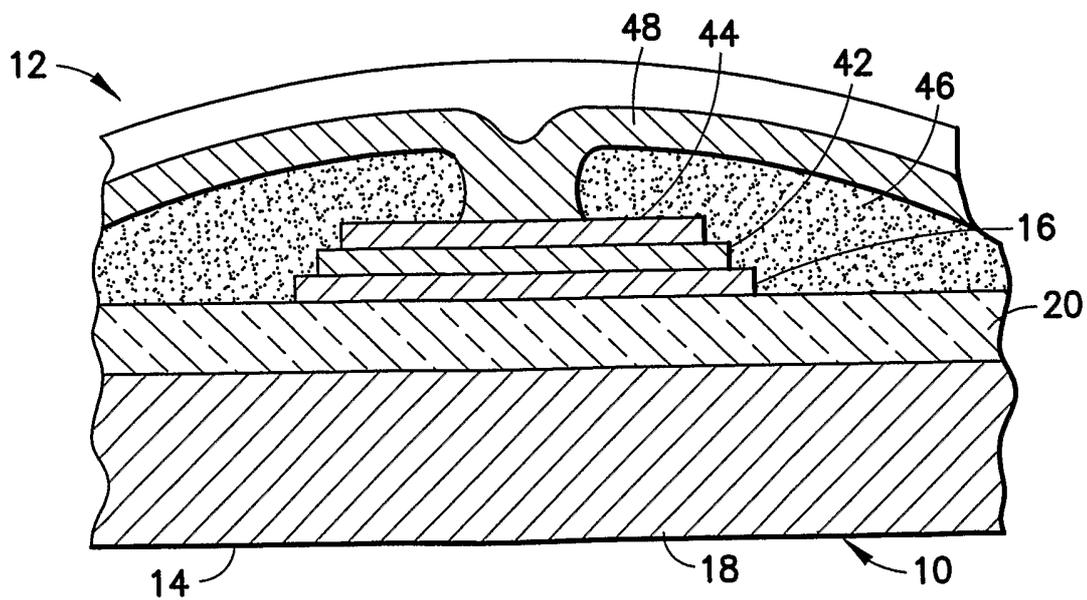


FIG.5

## INTERNATIONAL SEARCH REPORT

Internal Application No  
PCT/JP 03/14934A. CLASSIFICATION OF SUBJECT MATTER  
IPC 7 H01G1/005 H01G4/008 H01G4/10 H01L21/283

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01G H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 785 579 A (ROHM CO LTD) 23 July 1997 (1997-07-23)	1-3,5-10
Y	column 3, line 11 - column 4, line 9 column 5, line 18 - line 42 column 7, line 5 - line 47; claims 6-8,13	4
X	US 2001/019874 A1 (INOUE ATSUO ET AL) 6 September 2001 (2001-09-06)	1-3,5-10
Y	paragraph '0008! - paragraph '0009! paragraph '0015! - paragraph '0020!; claims 1-13; figures 1-10	4
Y	GB 1 544 506 A (SIEMENS AG) 19 April 1979 (1979-04-19)	4
A	page 2, line 75 - line 97; figure 1	1-3,5-10

 Further documents are listed in the continuation of box C. Patent family members are listed in annex.

° Special categories of cited documents:

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Date of the actual completion of the international search

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## INTERNATIONAL SEARCH REPORT

Internationa	Application No
PCT, JP	03/14934

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 0785579	A	23-07-1997	JP 9022829 A	21-01-1997
			CA 2197491 A1	30-01-1997
			EP 0785579 A1	23-07-1997
			US 6454914 B1	24-09-2002
			CN 1155943 A ,B	30-07-1997
			WO 9703468 A1	30-01-1997
			US 2002189933 A1	19-12-2002
			US 2001019874	A1
			JP 8186236 A	16-07-1996
			JP 9045877 A	14-02-1997
			US 6204111 B1	20-03-2001
			CN 1345088 A	17-04-2002
			CN 1129354 A ,B	21-08-1996
			DE 69525827 D1	18-04-2002
			DE 69525827 T2	14-11-2002
			DE 69527160 D1	25-07-2002
			DE 69527160 T2	28-11-2002
			DE 69531070 D1	17-07-2003
			EP 0720213 A2	03-07-1996
			EP 0971392 A1	12-01-2000
			EP 0971393 A1	12-01-2000
			US 6214660 B1	10-04-2001
			US 5929475 A	27-07-1999
GB 1544506	A	19-04-1979	DE 2513858 A1	30-09-1976
			AT 363569 B	10-08-1981
			AT 59676 A	15-01-1981
			BE 840072 A1	27-09-1976
			CH 604353 A5	15-09-1978
			DK 132676 A	28-09-1976
			FR 2305839 A1	22-10-1976
			IT 1058510 B	10-05-1982
			JP 51121172 A	22-10-1976
			NL 7603137 A	29-09-1976
			SE 412662 B	10-03-1980
			SE 7602900 A	28-09-1976
			US 4058445 A	15-11-1977