United States Patent [19]

Mauro, Jr.

[11] **3,903,516**

[45] **Sept. 2, 1975**

[54] **CONTROL LOGIC FOR GAS DISCHARGE DISPLAY PANEL**

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[73] Assignee: **International Business Machines Corporation,** Armonk, N.Y.

[22] Filed: **June 26, 1973**

[21] Appl. No.: **373,700**

[52] **U.S. Cl.** ..... **340/324 M;** 315/169 R

[51] **Int. Cl.** **G08b 5/36**

[58] **Field of Search** ..... 340/324 M, 173 PL; 315/169 R, 169 TV; 178/7.3 D

[56] **References Cited**

UNITED STATES PATENTS

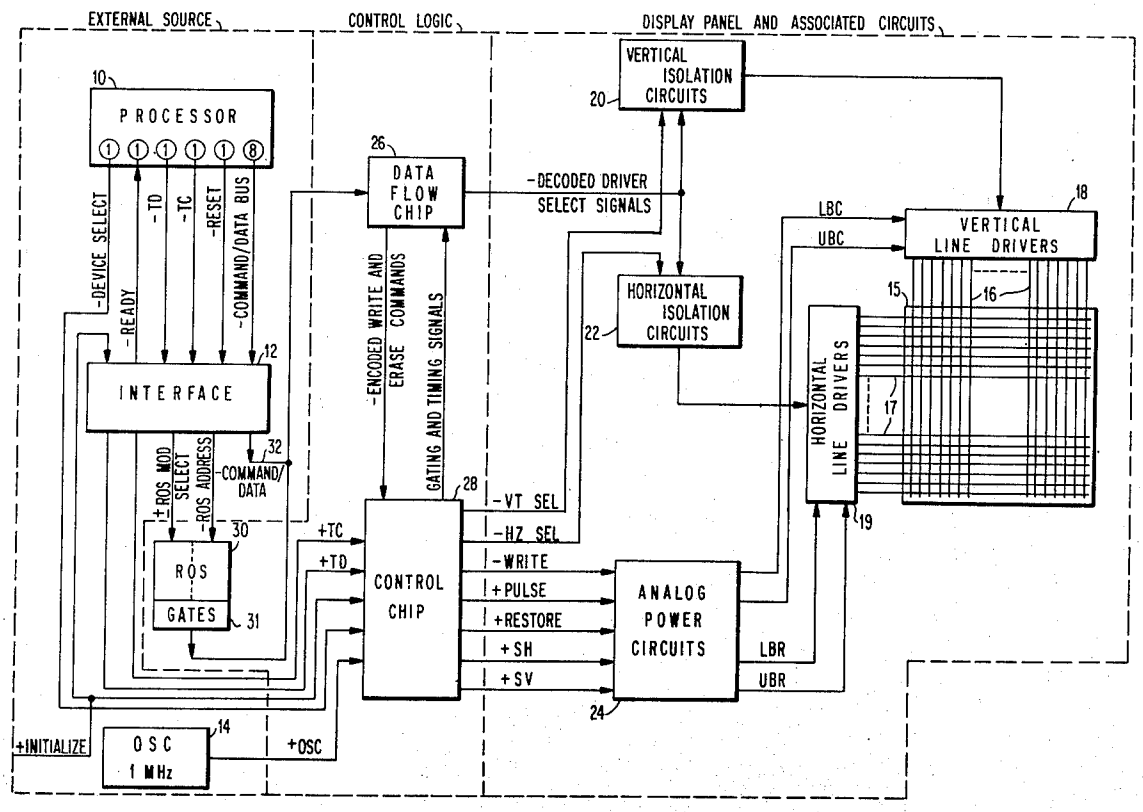
3,090,041	5/1963	Dell	340/324 AD
3,747,073	7/1973	Sharpless	340/324 M
3,753,038	8/1973	Liddle	340/324 M
3,754,230	8/1973	Auger	340/324 M

Primary Examiner—David L. Trafton
Attorney, Agent, or Firm—Sughrue, Rothwell, Mion, Zinn and Macpeak

[57] **ABSTRACT**

An external source supplies command and data bytes which are decoded to control the energization of a gas discharge display panel in order to display thereon alpha-numeric characters and other symbols. Each command is decoded to determine whether it is a POSITION command or one of the following commands: WRITE CHARACTER, WRITE SLICE, ERASE DATA and ERASE PANEL. If a POSITION command is decoded, following data bytes are decoded and stored as the starting cell address of the gas panel. If the next command is a WRITE CHARACTER or WRITE SLICE command, the following data byte specifies the code of a character or the horizontal data slice, respectively, to be written or displayed in the panel beginning at the starting cell address. Corresponding individual row and column latchable drivers or bistable switching circuits are then set to select the panel drive lines which are to be energized to illuminate the gas cells designated by the character or slice data byte. If the next command had been an ERASE DATA command, the following data byte would have specified the width and height of a block of cells to be erased, and the corresponding panel line drivers would have been set to permit extinguishment or erasure of the cells in the specified block. An ERASE PANEL command causes all the cells of the panel to be simultaneously erased. At an appropriate time after the selected drivers are latched, an analog power circuit causes the set drivers to apply appropriate sustain, write or erase voltages to the selected panel lines.

10 Claims, 25 Drawing Figures



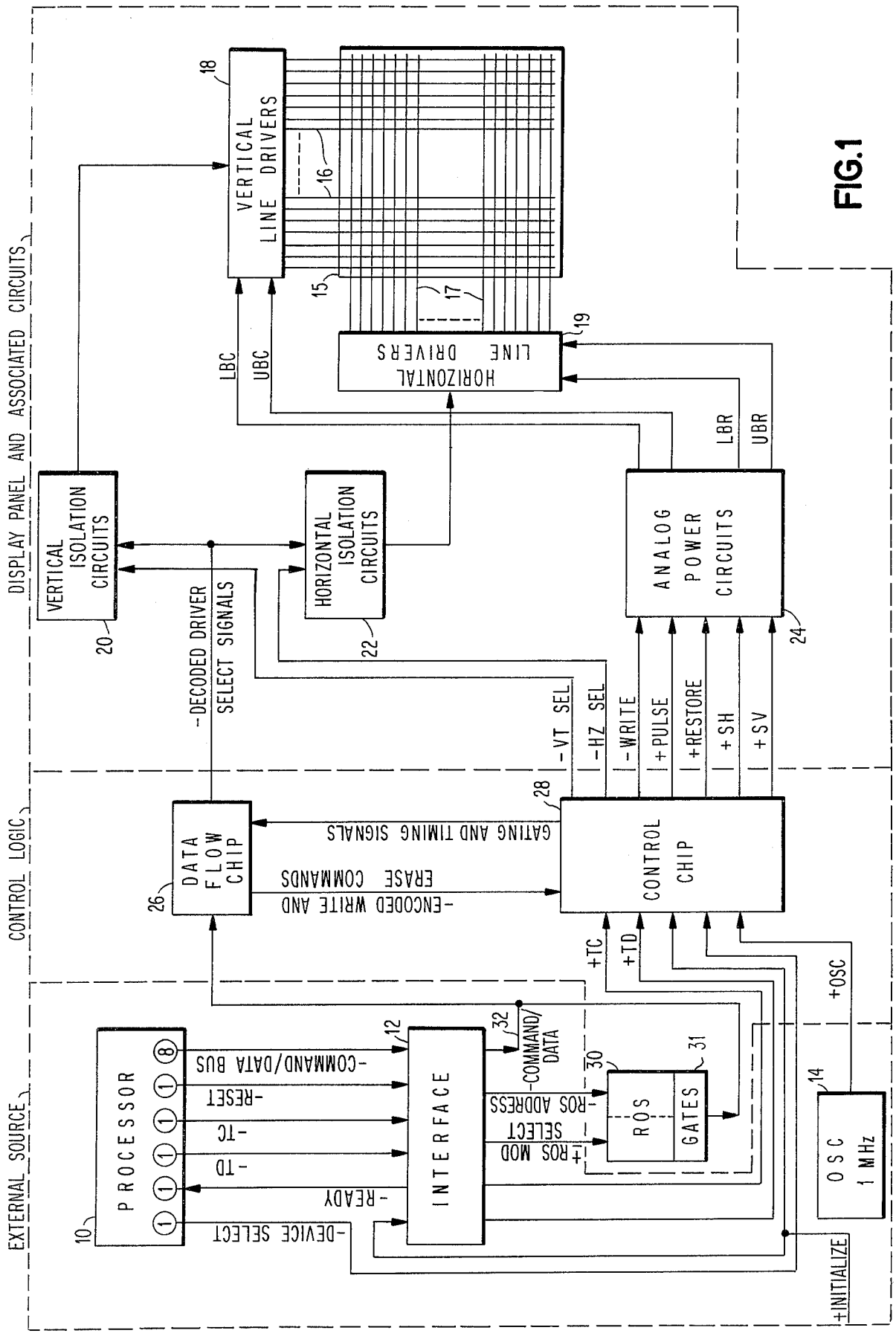

DISPLAY PANEL AND ASSOCIATED CIRCUITS
CONTROL LOGIC
EXTERNAL SOURCE
VERTICAL LINE DRIVERS
HORIZONTAL LINE DRIVERS
VERTICAL ISOLATION CIRCUITS
HORIZONTAL ISOLATION CIRCUITS
ANALOG POWER CIRCUITS
DATA FLOW CHIP
CONTROL CHIP
PROCESSOR
INTERFACE
ROS
GATES
OSC 1 MHz
LBC
UBC
LBR
UBR
-DECODED DRIVER SELECT SIGNALS
-VT SEL
-HZ SEL
-WRITE
+PULSE
+RESTORE
+SH
+SV
GATING AND TIMING SIGNALS
-ENCODED WRITE AND ERASE COMMANDS
+TC
+TD
+OSC
-COMMAND/DATA BUS
-RESET
-TC
-TD
-READY
-DEVICE SELECT
-COMMAND/DATA
ROS ADDRESS SELECT
+ROS MOD
+INITIALIZE
10
12
14
15
16
17
18
19
20
22
24
26
28
30
31
32

FIG.1

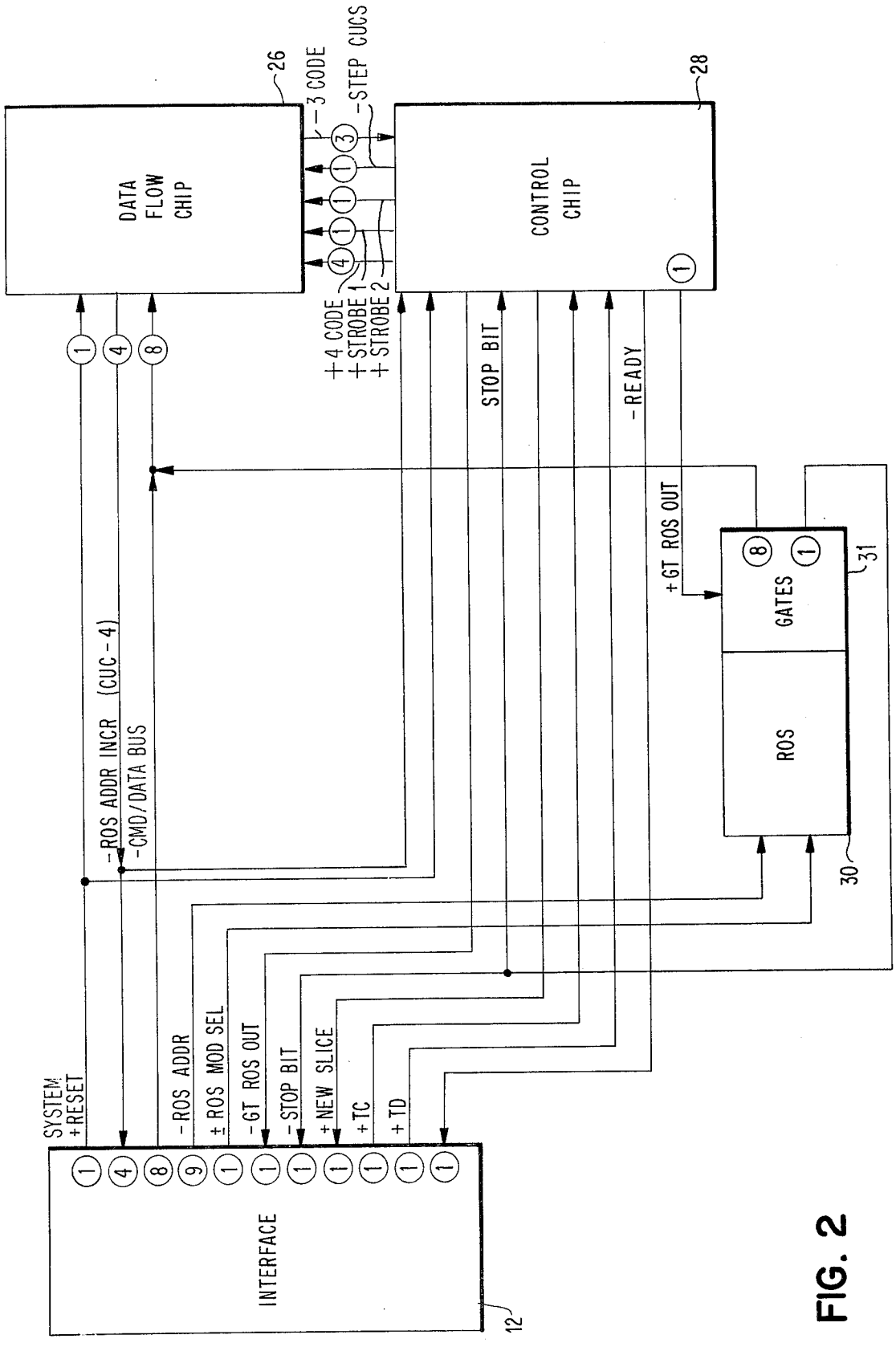

DATA FLOW CHIP
26
CONTROL CHIP
28
INTERFACE
12
GATES
31
ROS
30
-3 CODE
-STEP CUCS
+4 CODE
+STROBE 1
+STROBE 2
STOP BIT
-READY
+GT ROS OUT
-ROS ADDR INCR (CUC-4)
-CMD/DATA BUS
SYSTEM +RESET
-ROS ADDR
± ROS MOD SEL
-GT ROS OUT
-STOP BIT
+NEW SLICE
+TC
+TD

FIG. 2

FIG. 3A

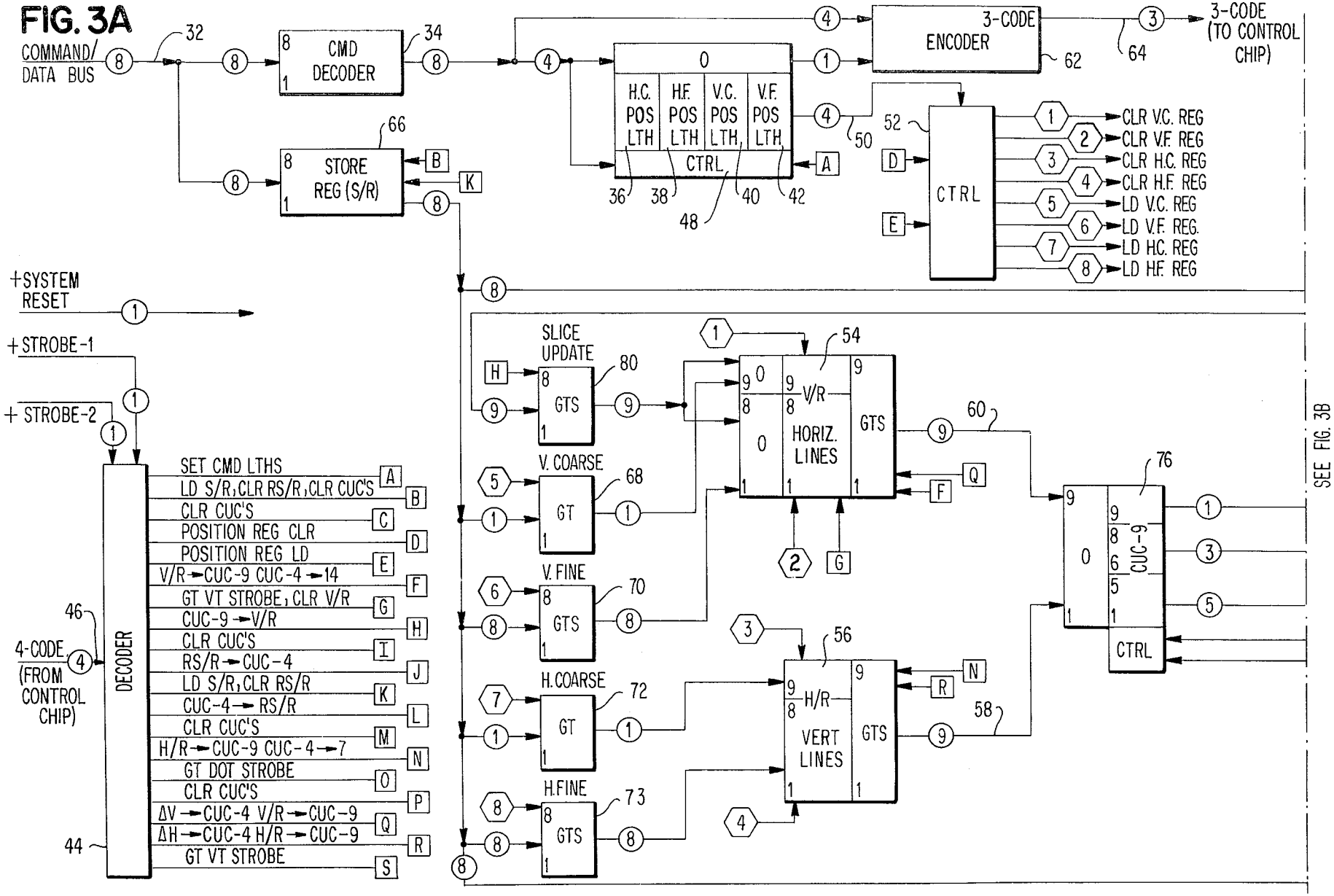

COMMAND/ DATA BUS
32
CMD DECODER
34
STORE REG (S/R)
66
3-CODE ENCODER
62
64
3-CODE (TO CONTROL CHIP)
H.C. POS LTH
H.F. POS LTH
V.C. POS LTH
V.F. POS LTH
CTRL
36
38
48
40
42
50
52
CTRL
CLR V.C. REG
CLR V.F. REG
CLR H.C. REG
CLR H.F. REG
LD V.C. REG
LD V.F. REG.
LD H.C. REG
LD H.F. REG
+SYSTEM RESET
+STROBE-1
+STROBE-2
SET CMD LTHS
LD S/R, CLR RS/R, CLR CUC'S
CLR CUC'S
POSITION REG CLR
POSITION REG LD
V/R → CUC-9 CUC-4 → 14
GT VT STROBE, CLR V/R
CUC-9 → V/R
CLR CUC'S
RS/R → CUC-4
LD S/R, CLR RS/R
CUC-4 → RS/R
CLR CUC'S
H/R → CUC-9 CUC-4 → 7
GT DOT STROBE
CLR CUC'S
ΔV → CUC-4 V/R → CUC-9
ΔH → CUC-4 H/R → CUC-9
GT VT STROBE
46
4-CODE (FROM CONTROL CHIP)
DECODER
44
SLICE UPDATE
80
GTS
V. COARSE
68
GT
V. FINE
70
GTS
H. COARSE
72
GT
H. FINE
73
GTS
54
V/R
HORIZ. LINES
GTS
60
56
H/R
VERT LINES
GTS
58
76
CUC-9
CTRL
SEE FIG. 3B

FIG. 3B

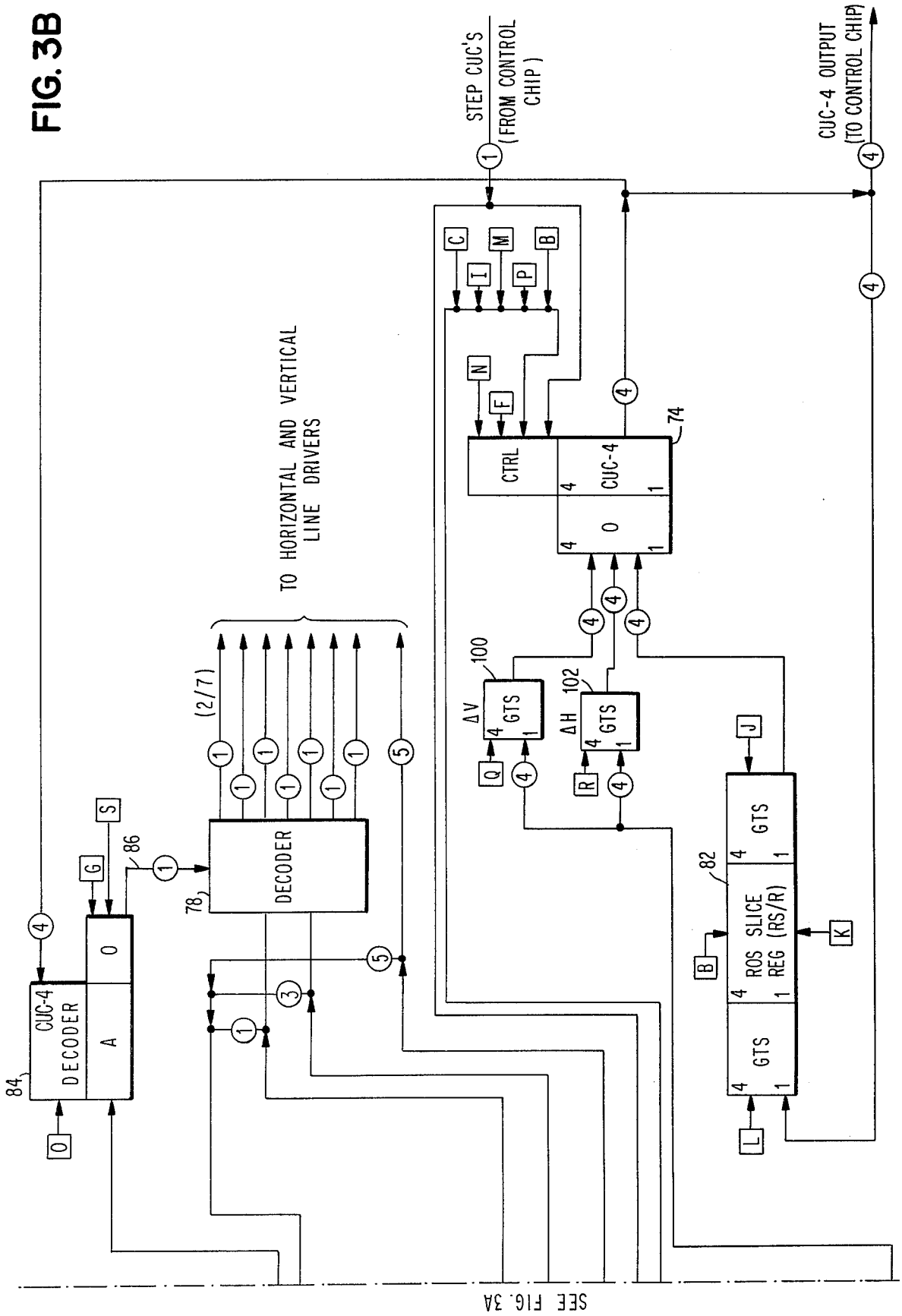

STEP CUC'S (FROM CONTROL CHIP)
CUC-4 OUTPUT (TO CONTROL CHIP)
TO HORIZONTAL AND VERTICAL LINE DRIVERS
CUC-4 DECODER
DECODER
CTRL
CUC-4
ROS SLICE REG (RS/R)
GTS
ΔV
ΔH
(2/7)
SEE FIG. 3A

FIG. 4

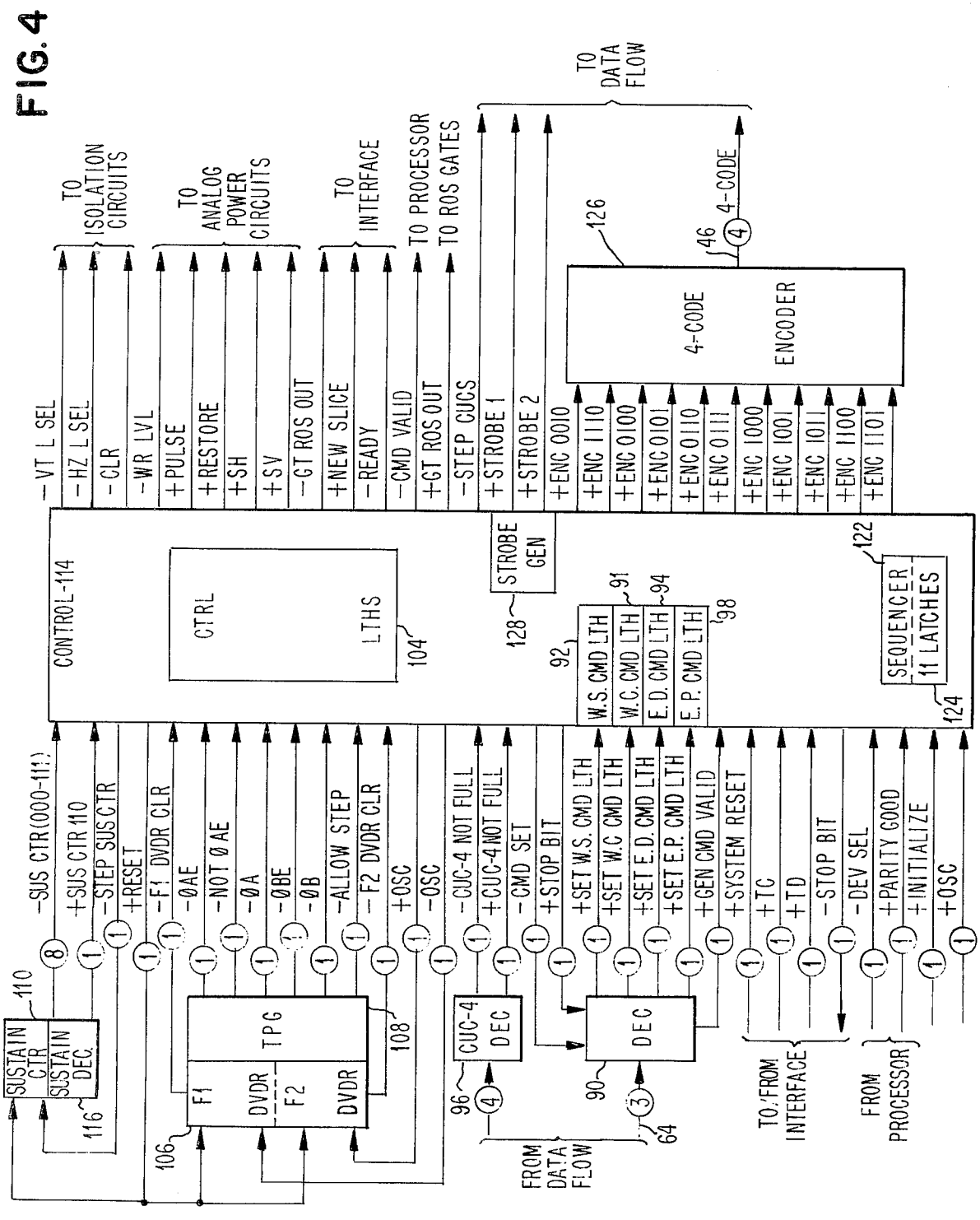

TO ISOLATION CIRCUITS
TO ANALOG POWER CIRCUITS
TO INTERFACE
TO PROCESSOR
TO ROS GATES
TO DATA FLOW
-VT L SEL
-HZ L SEL
-CLR
-WR LVL
+PULSE
+RESTORE
+SH
+SV
-GT ROS OUT
+NEW SLICE
-READY
-CMD VALID
+GT ROS OUT
-STEP CUCS
+STROBE 1
+STROBE 2
+ENC 0010
+ENC 1110
+ENC 0100
+ENC 0101
+ENC 0110
+ENC 0111
+ENC 1000
+ENC 1001
+ENC 1011
+ENC 1100
+ENC 1101
4-CODE
ENCODER
126
46
4-CODE
CONTROL-114
CTRL
LTHS
104
STROBE GEN
128
W.S. CMD LTH
W.C. CMD LTH
E.D. CMD LTH
E.P. CMD LTH
92
91
94
98
SEQUENCER
11 LATCHES
122
124
-SUS CTR (000-111)
+SUS CTR 110
-STEP SUS CTR
+RESET
-F1 DVDR CLR
-ØAE
-NOT Ø AE
-ØA
-ØBE
-ØB
-ALLOW STEP
-F2 DVDR CLR
+OSC
-OSC
-CUC-4 NOT FULL
+CUC-4 NOT FULL
-CMD SET
+STOP BIT
+SET W.S. CMD LTH
+SET W.C CMD LTH
+SET E.D. CMD LTH
+SET E.P. CMD LTH
+GEN CMD VALID
+SYSTEM RESET
+TC
+TD
-STOP BIT
-DEV SEL
+PARITY GOOD
+INITIALIZE
+OSC
SUSTAIN CTR
SUSTAIN DEC.
110
116
TPG
F1
DVDR
F2
DVDR
106
108
CUC-4 DEC
96
DEC
90
64
FROM DATA FLOW
TO/FROM INTERFACE
FROM PROCESSOR

FIG. 5A RESET, TPG & COMMAND DECODE

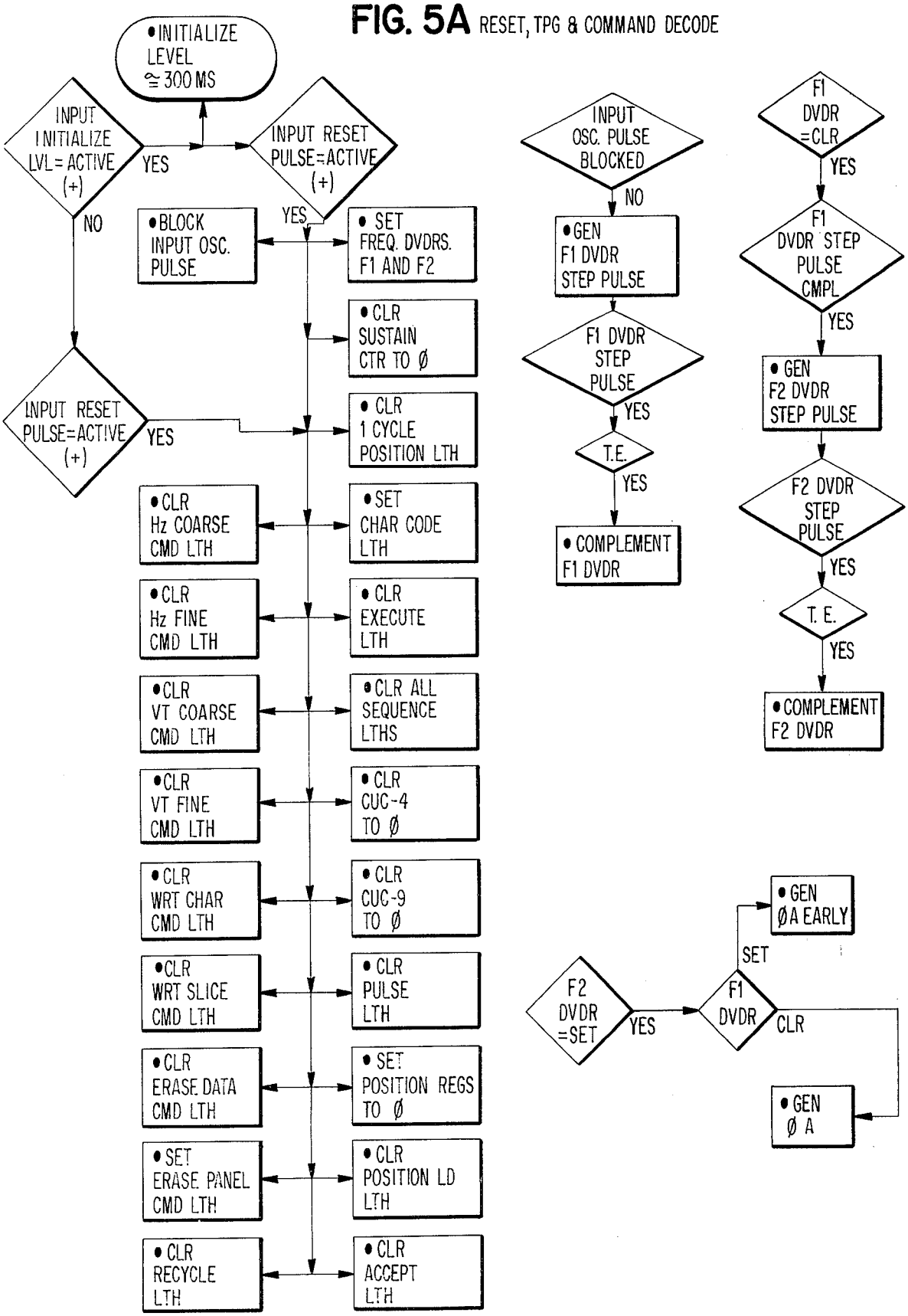
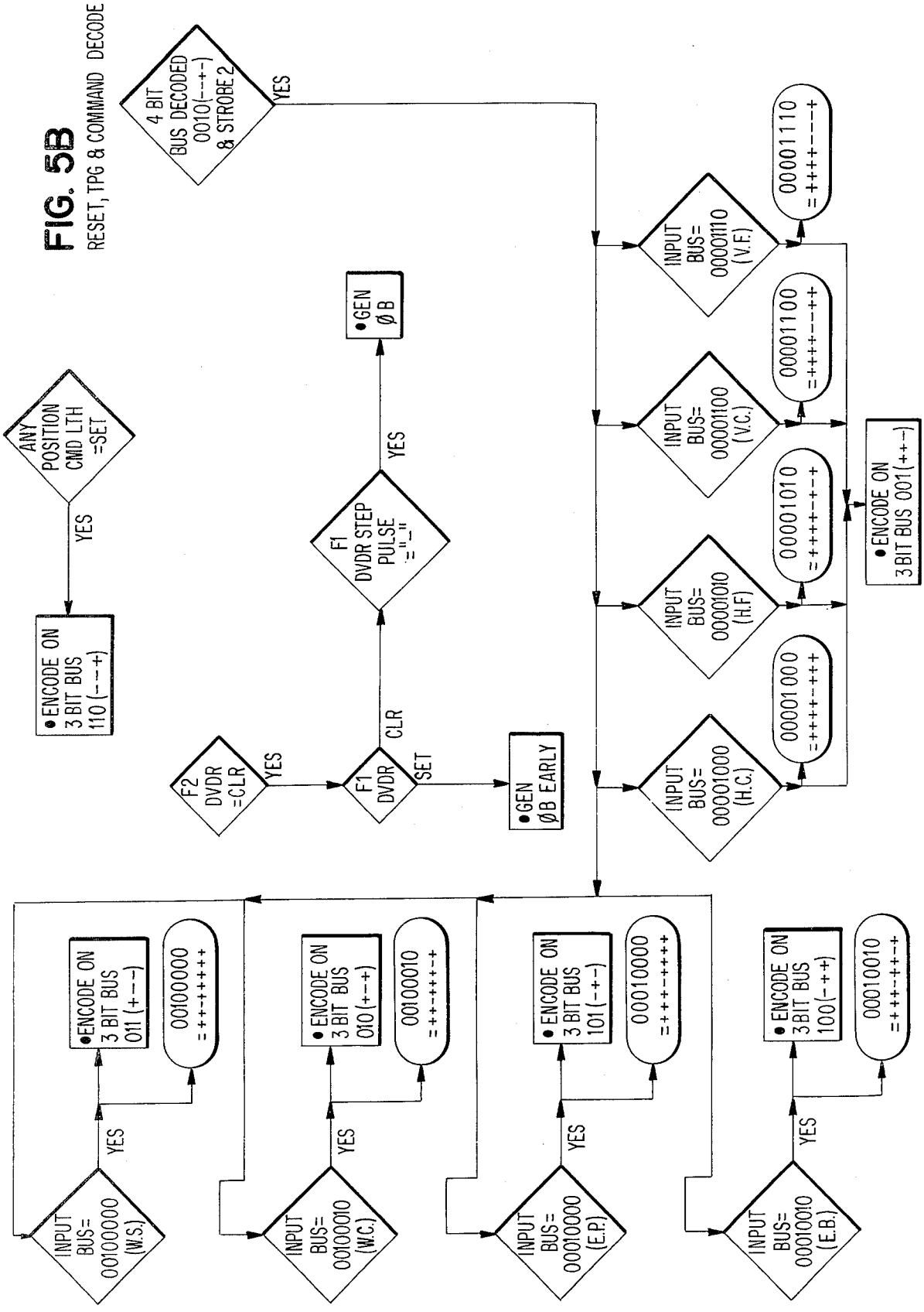


FIG. 5B

RESET, TPG & COMMAND DECODE



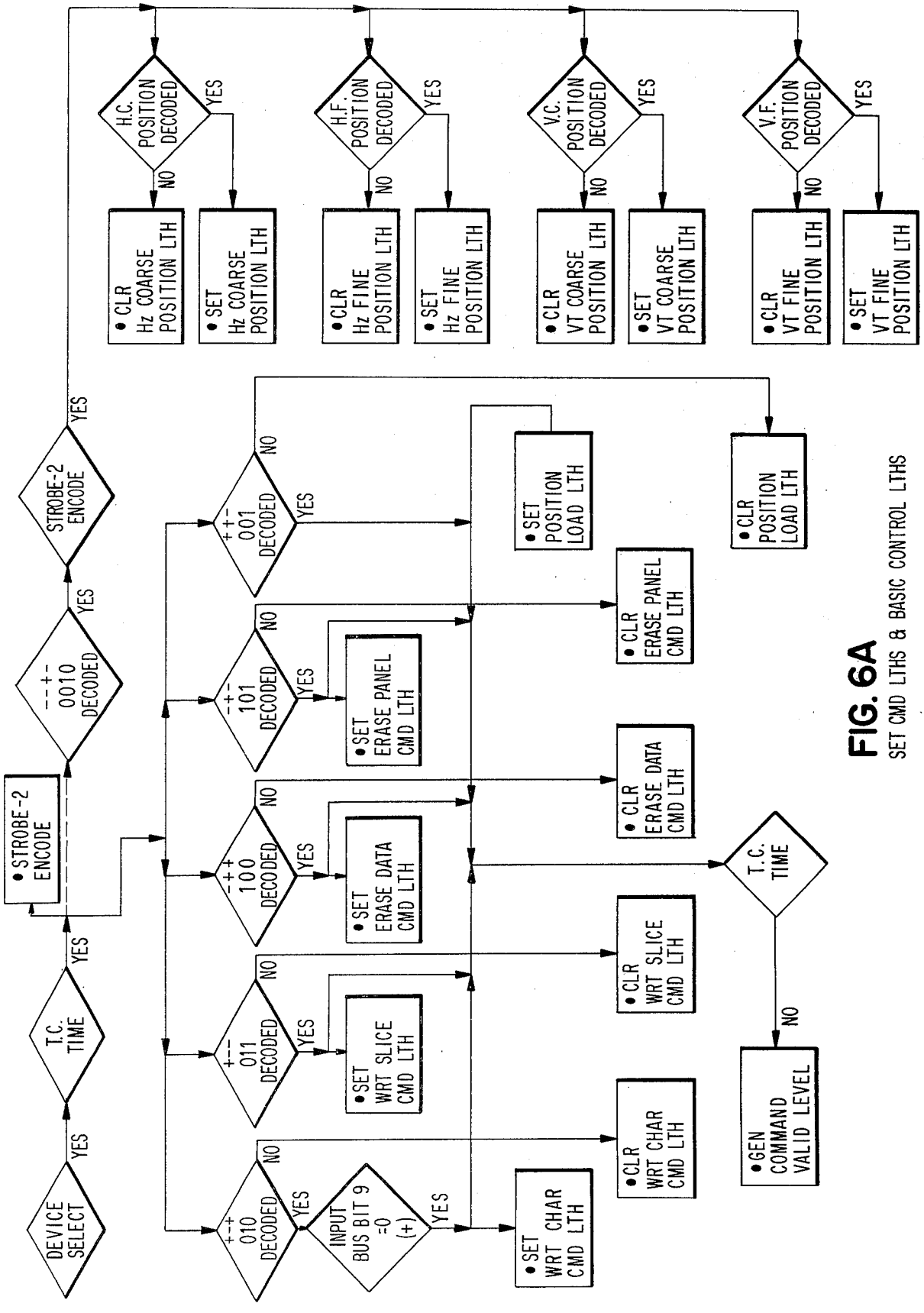


FIG. 6A

SET CMD LTHS & BASIC CONTROL LTHS

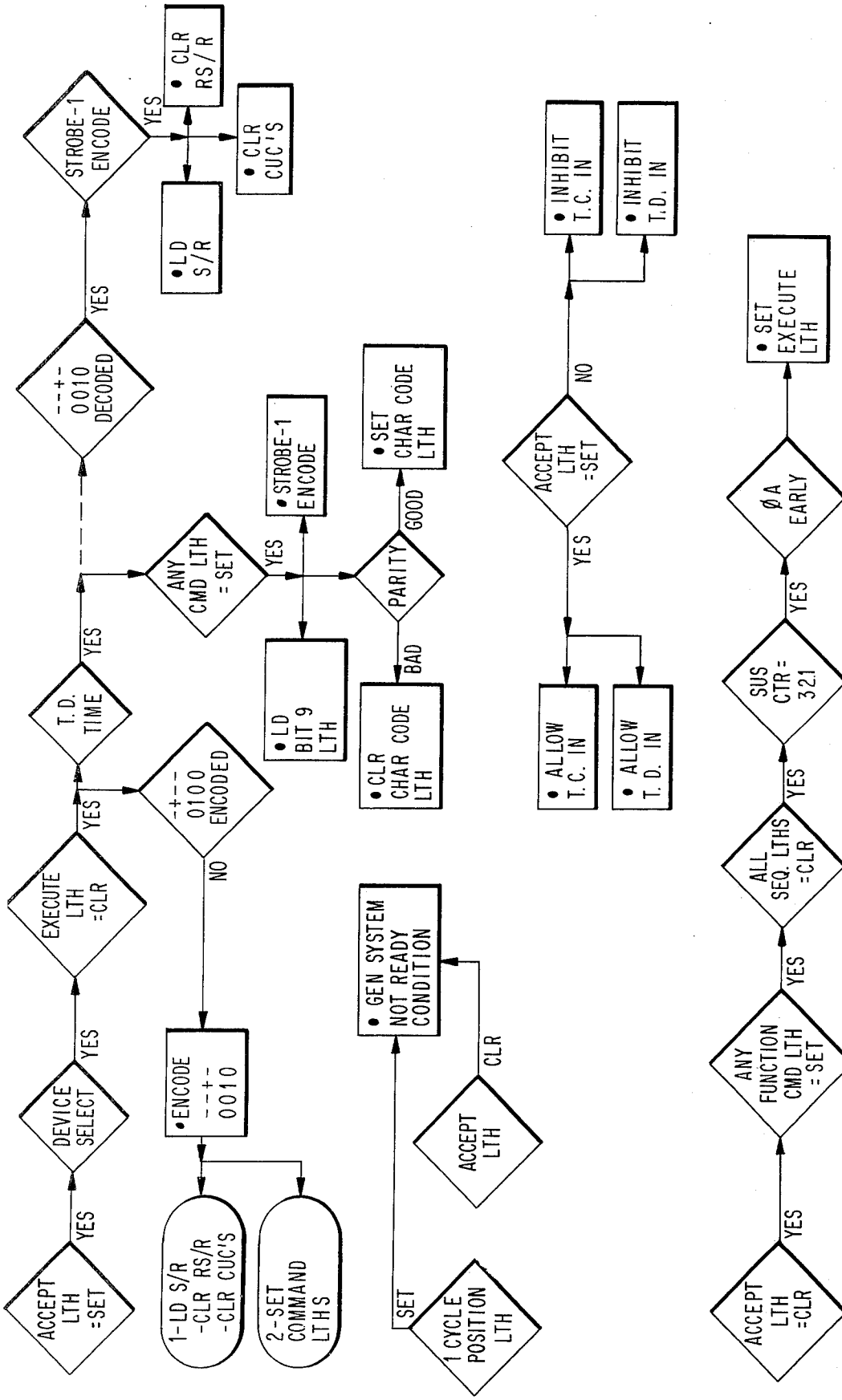


FIG. 6B

SET CMD LTHS & BASIC CONTROL LTHS

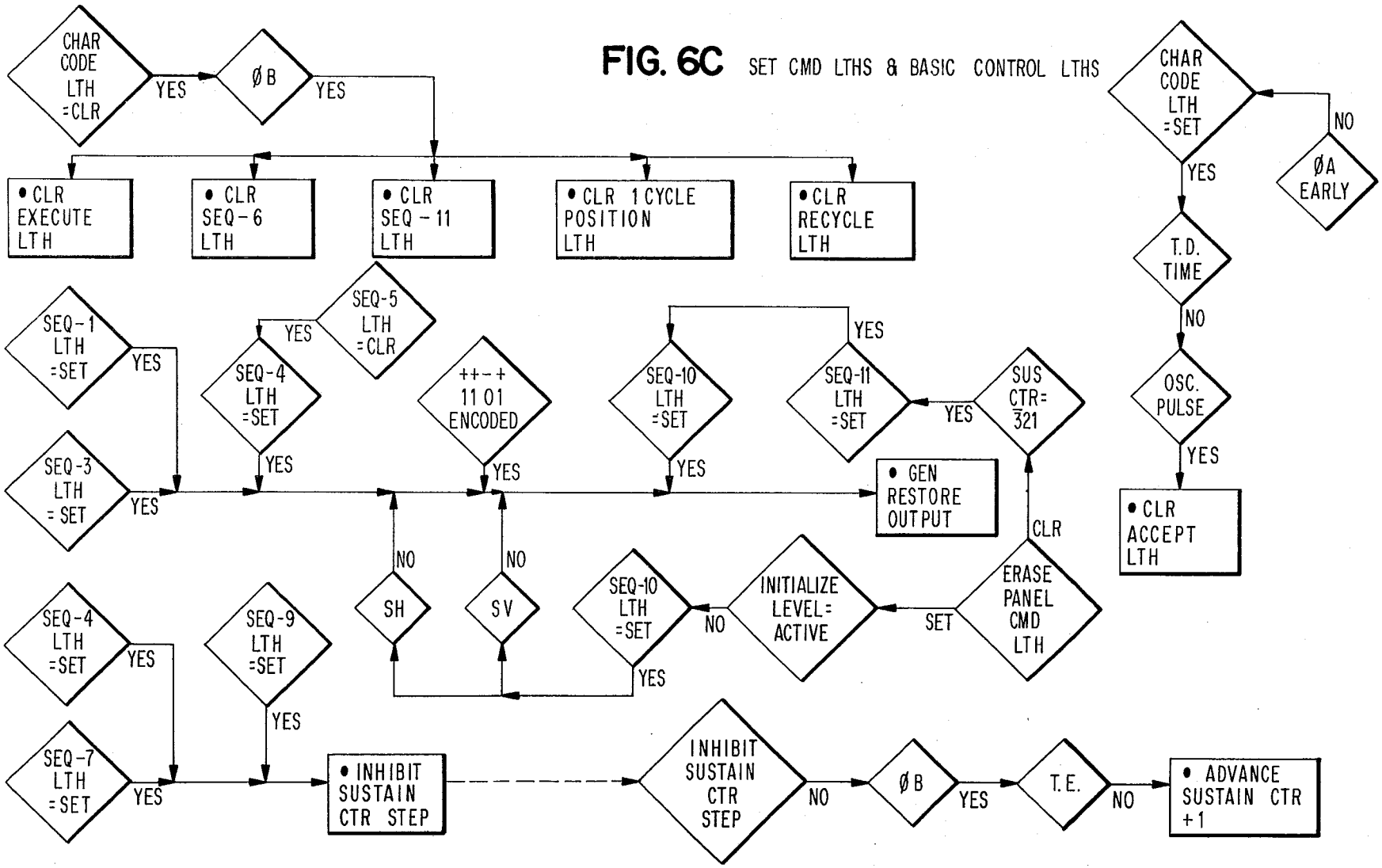


FIG. 6C SET CMD LTHS & BASIC CONTROL LTHS

FIG. 7A FUNCTION CONTROLS

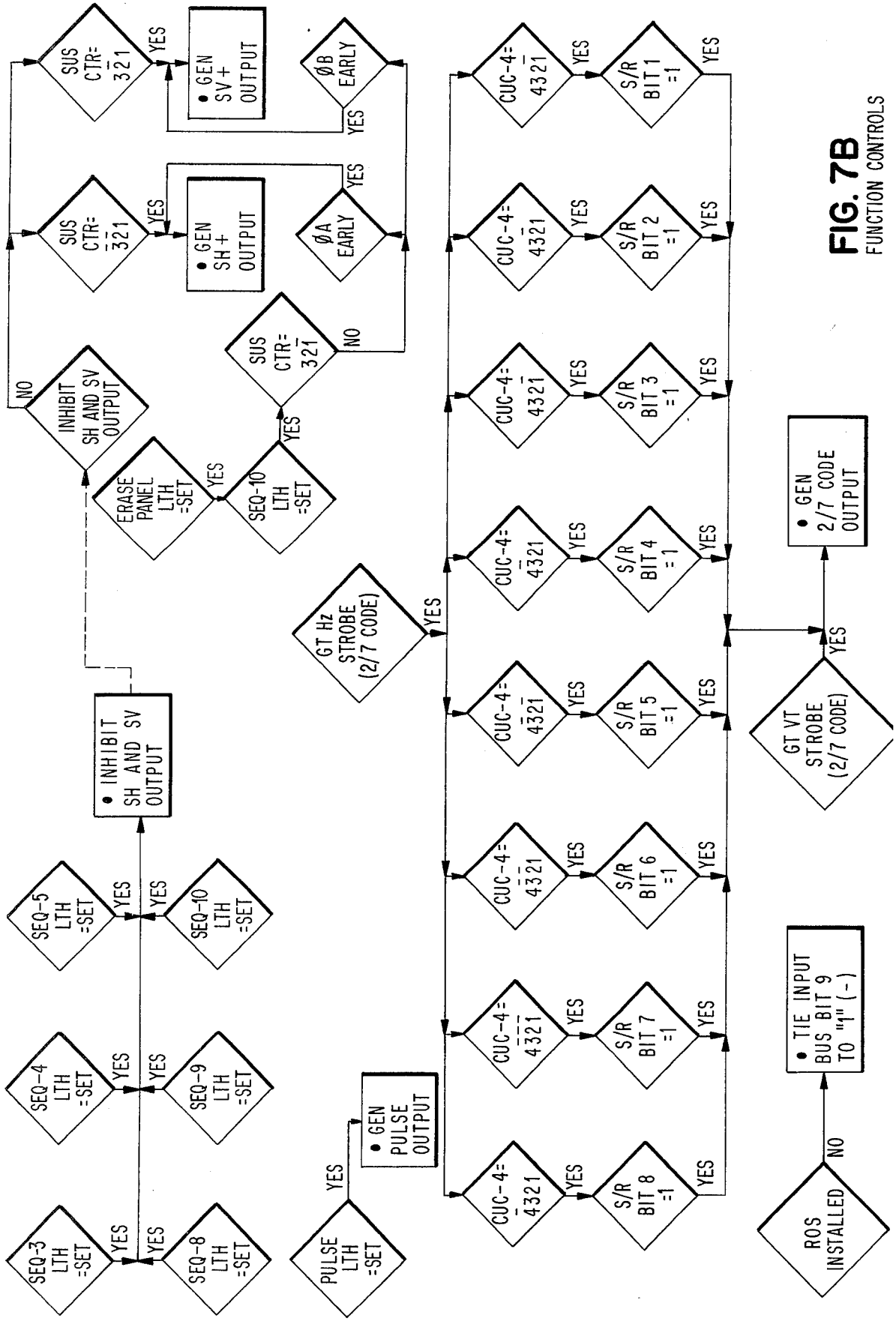


FIG. 7B
FUNCTION CONTROLS

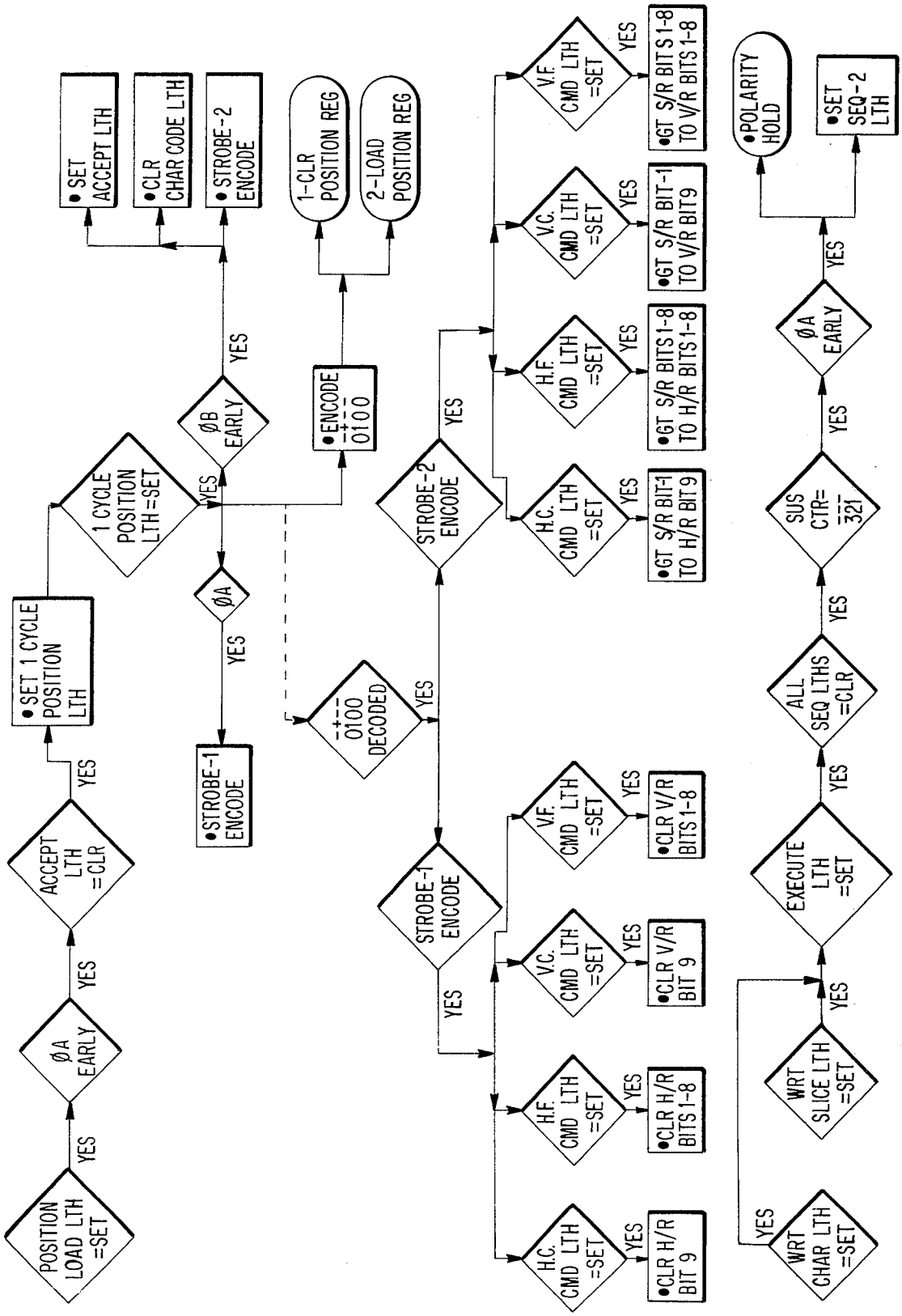


FIG. 8A POSITION LOAD & START WRITE

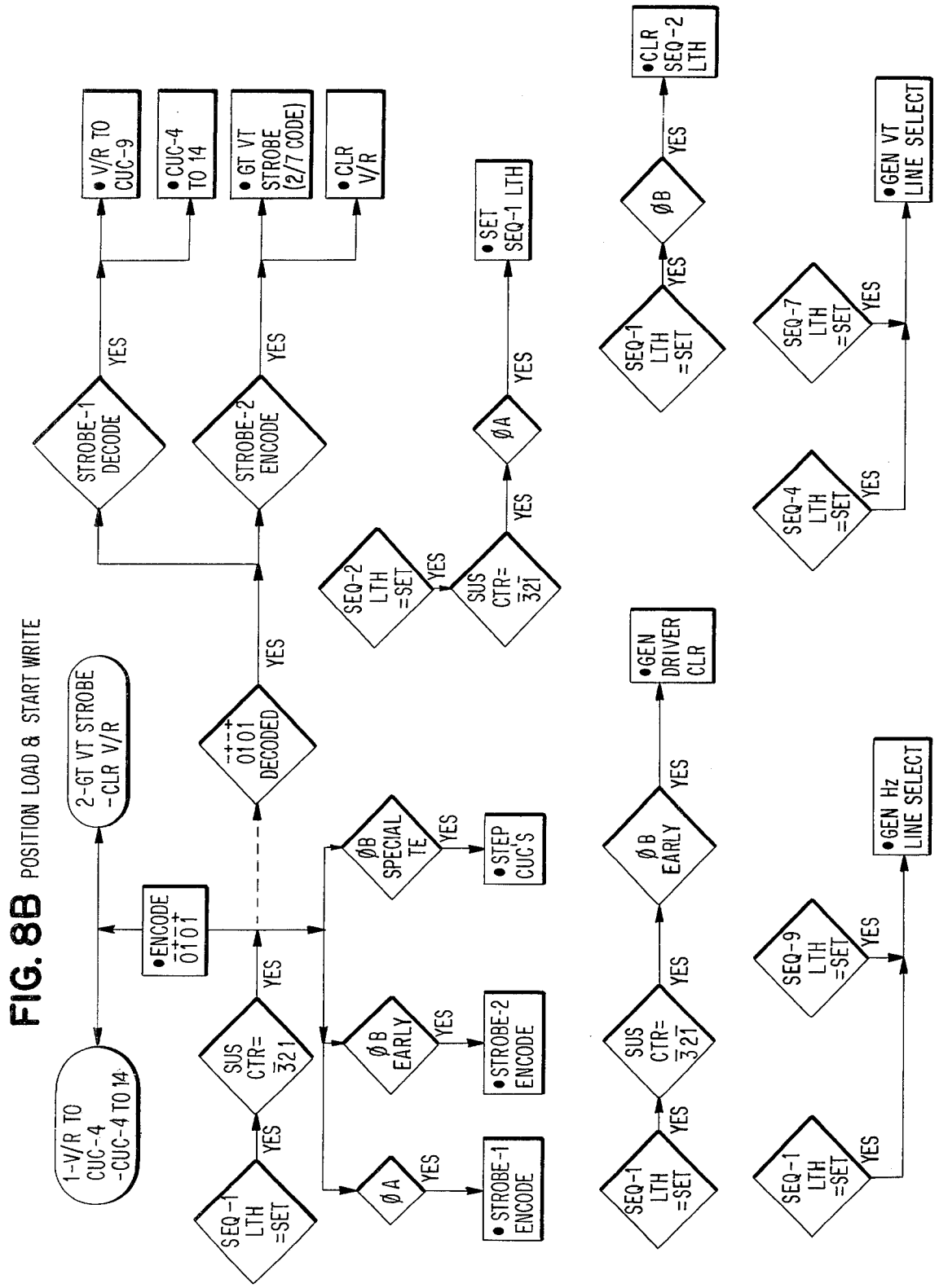


FIG. 8B POSITION LOAD & START WRITE

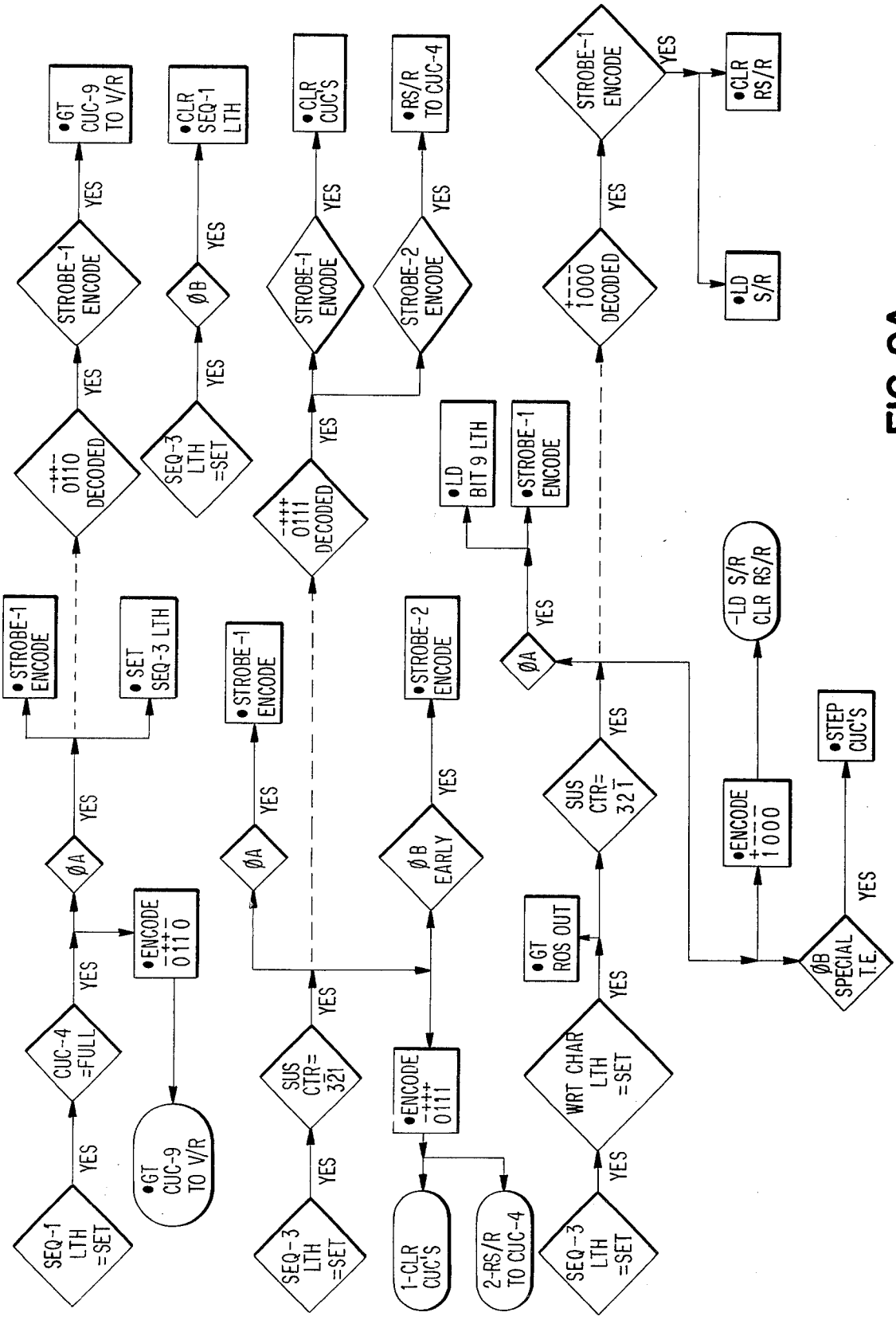


FIG. 9A WRITE SEQUENCE

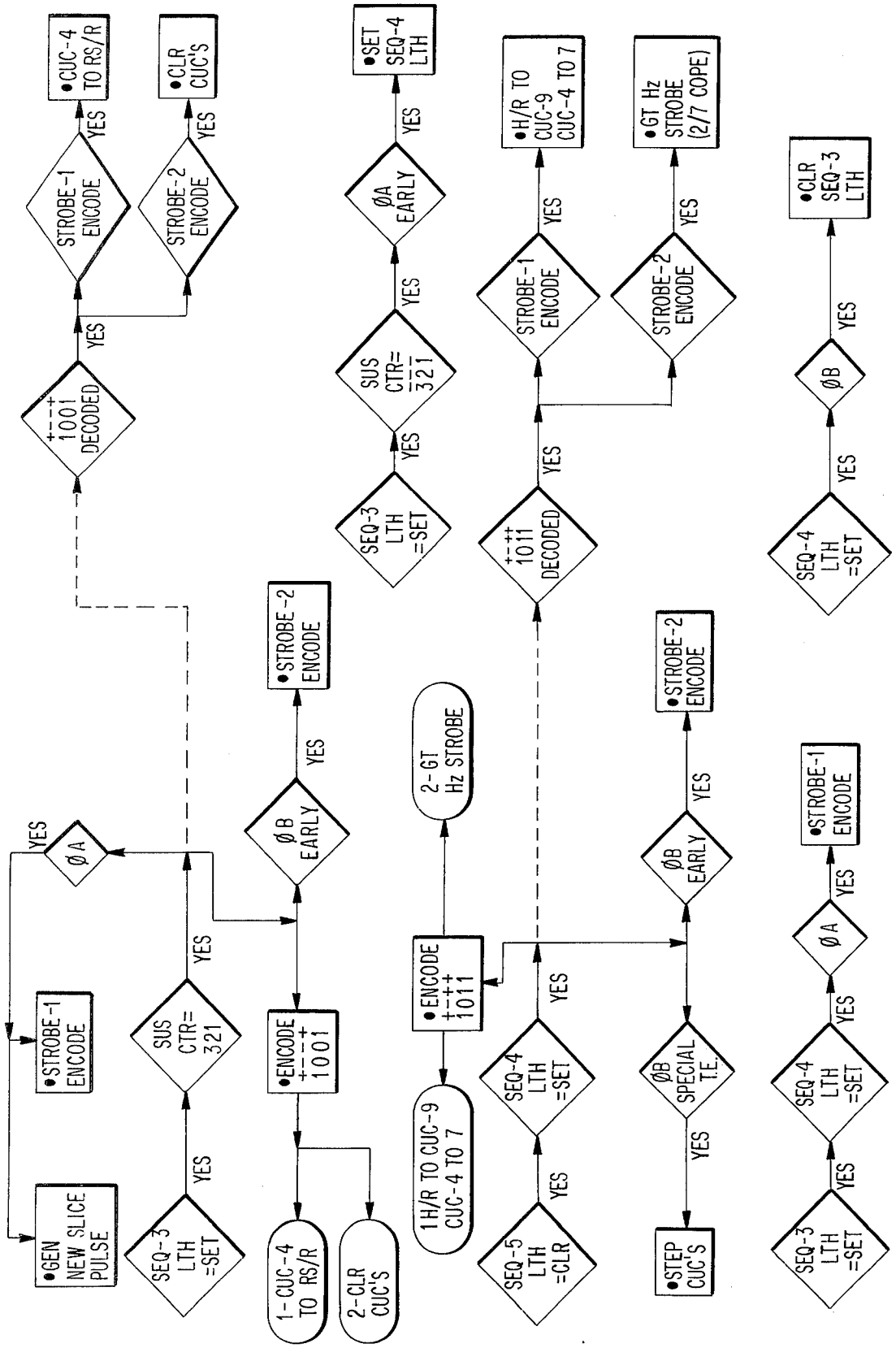


FIG. 9B WRITE SEQUENCE

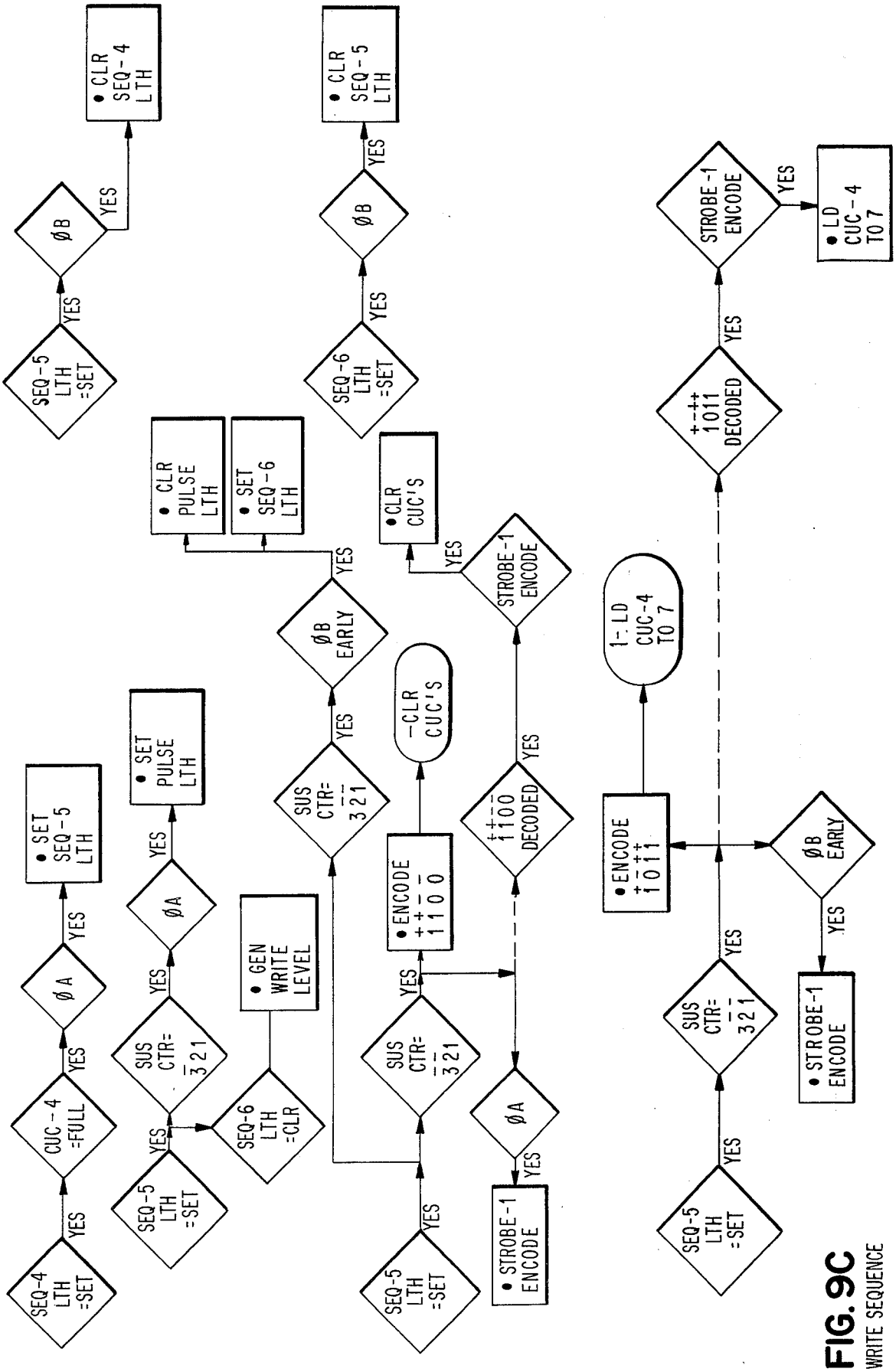


FIG. 9C
WRITE SEQUENCE

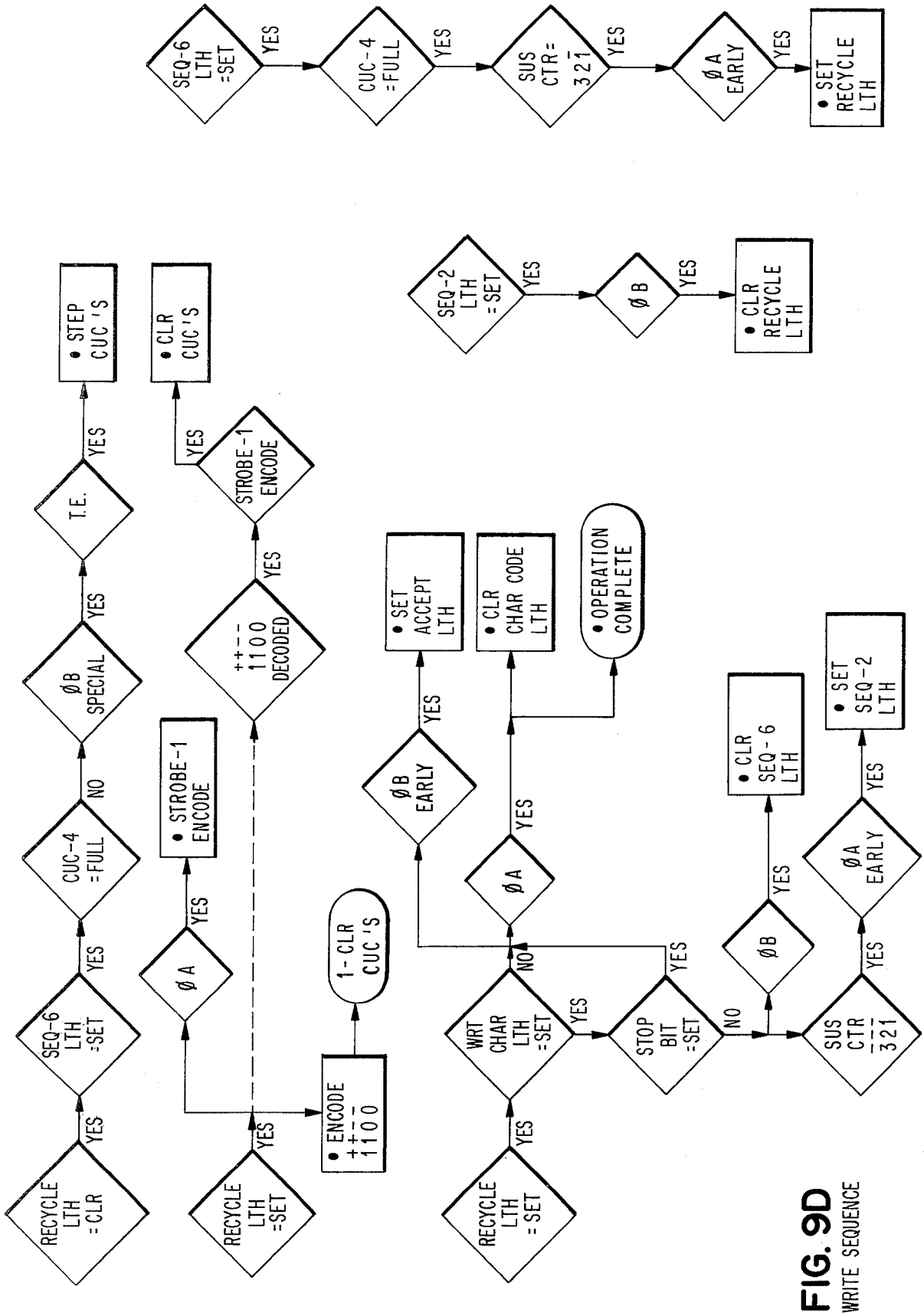


FIG. 9D
WRITE SEQUENCE

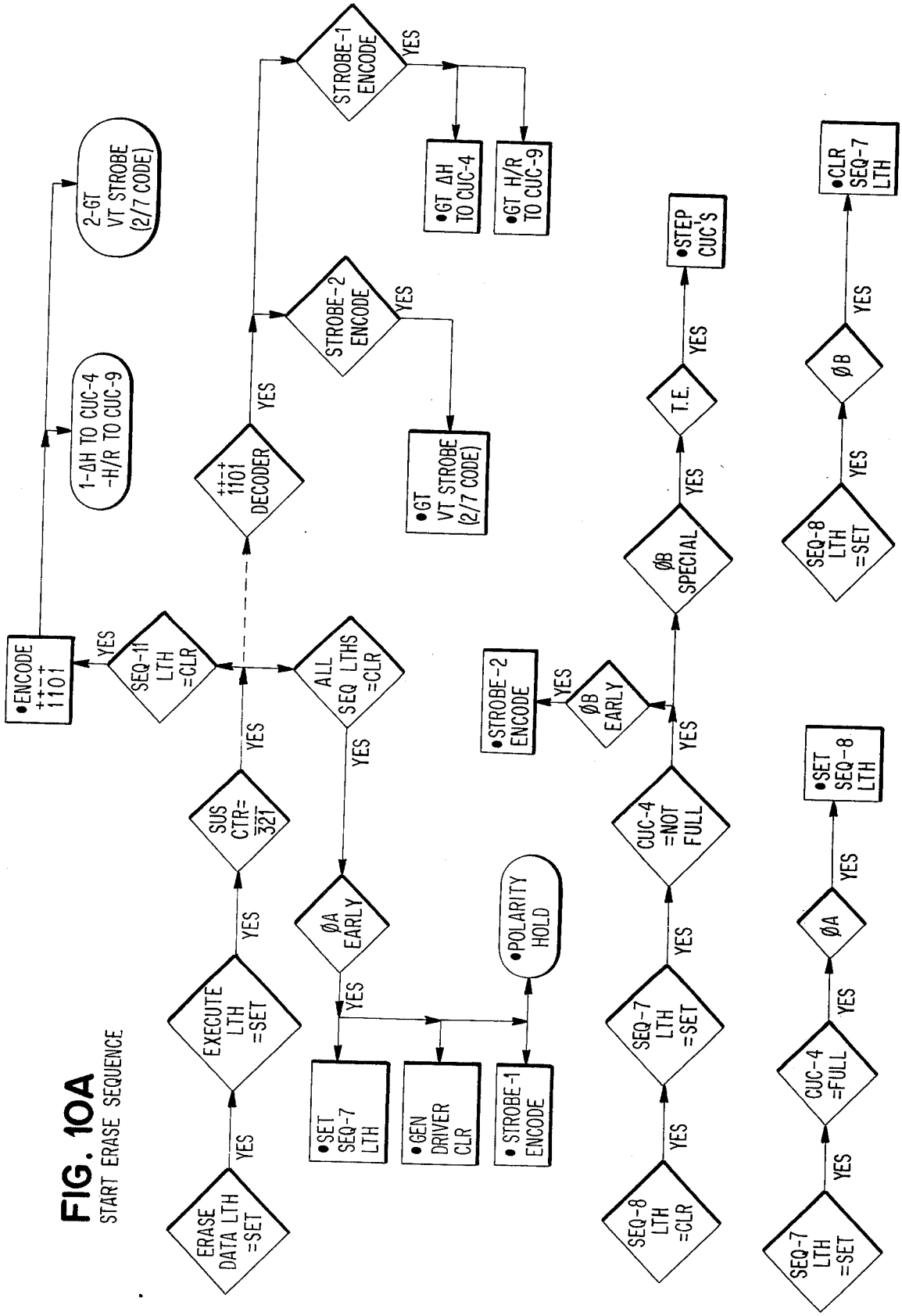


FIG. 10A
START ERASE SEQUENCE

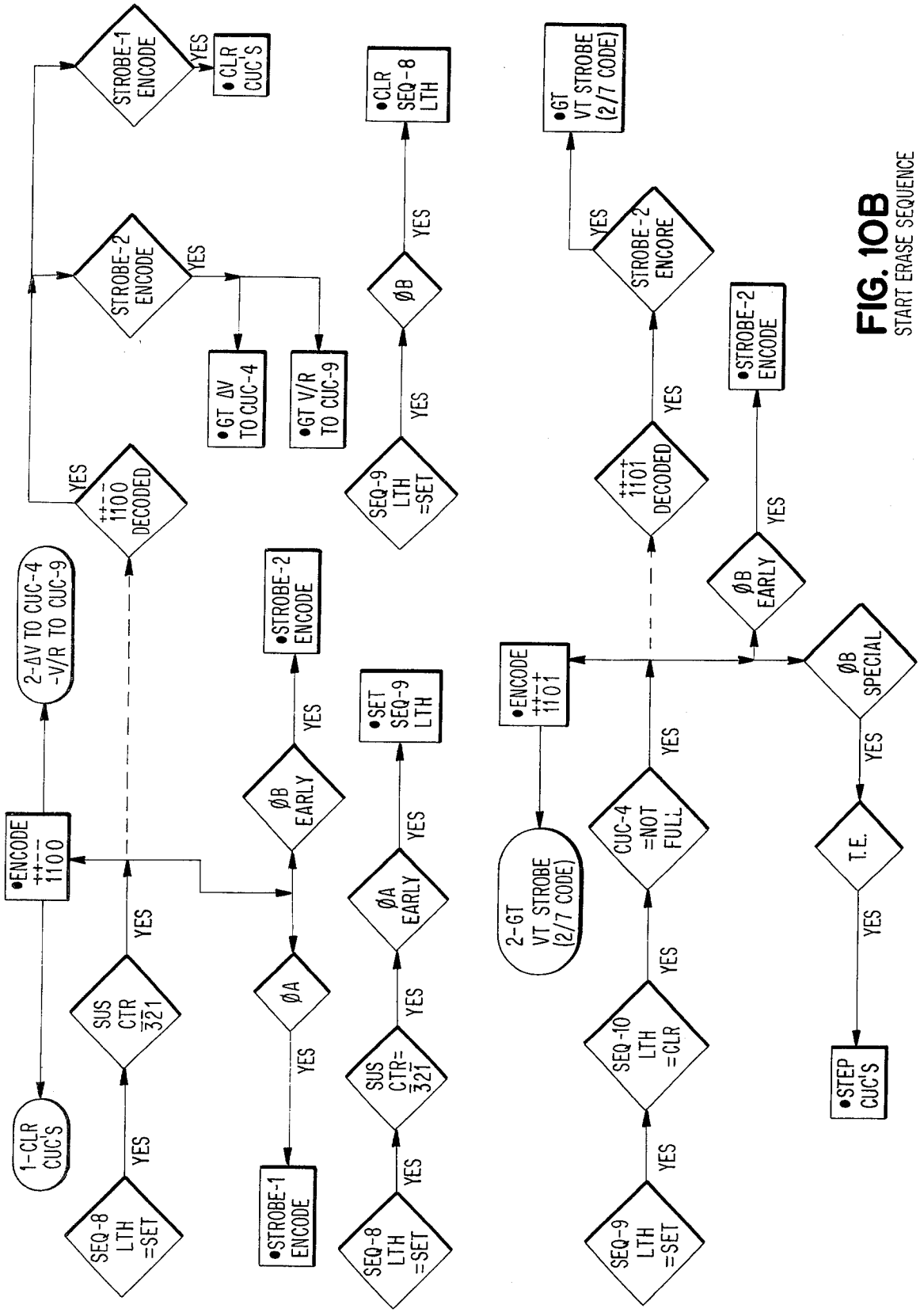


FIG. 10B
START ERASE SEQUENCE

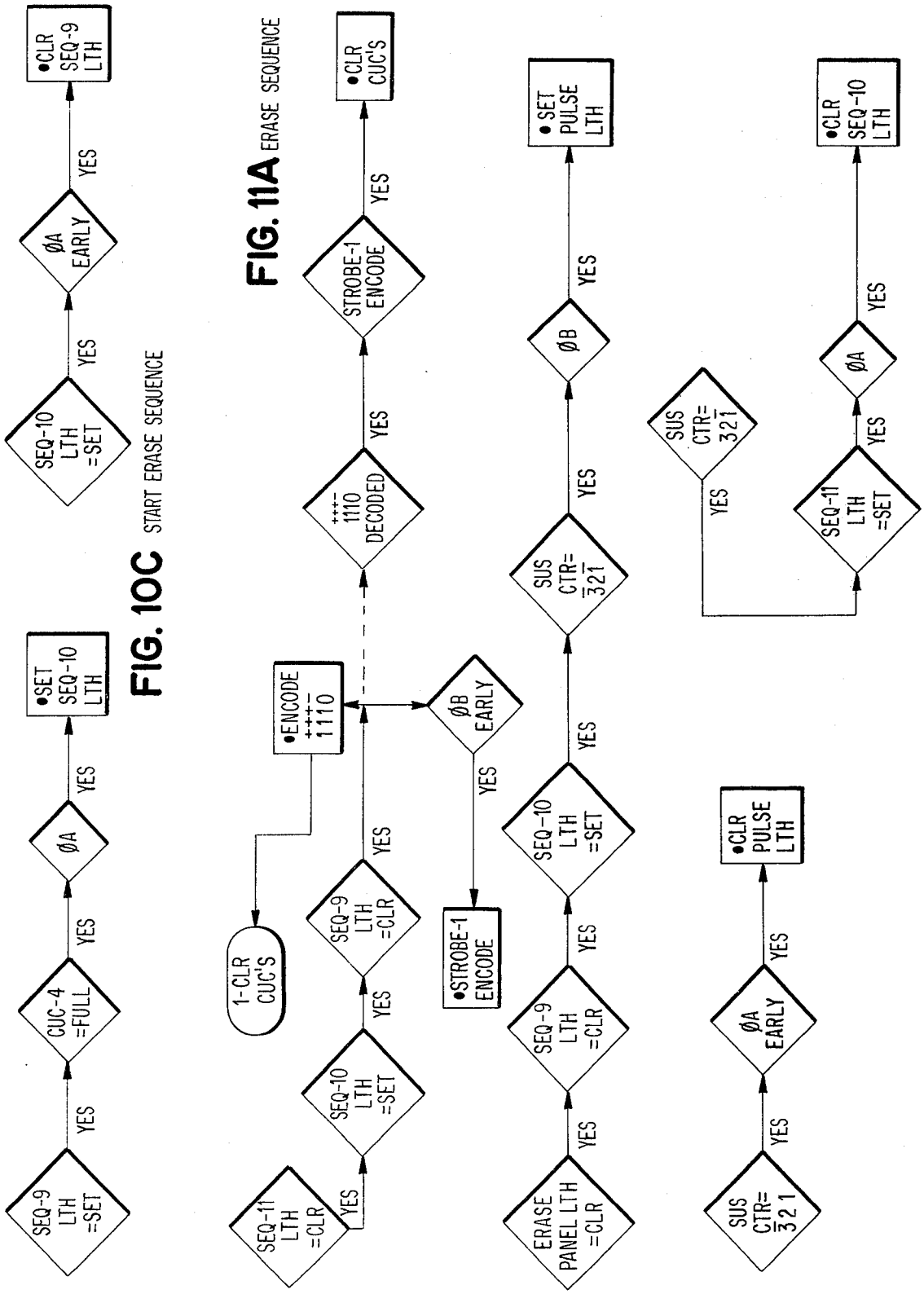


FIG. 10C START ERASE SEQUENCE

FIG. 11A ERASE SEQUENCE

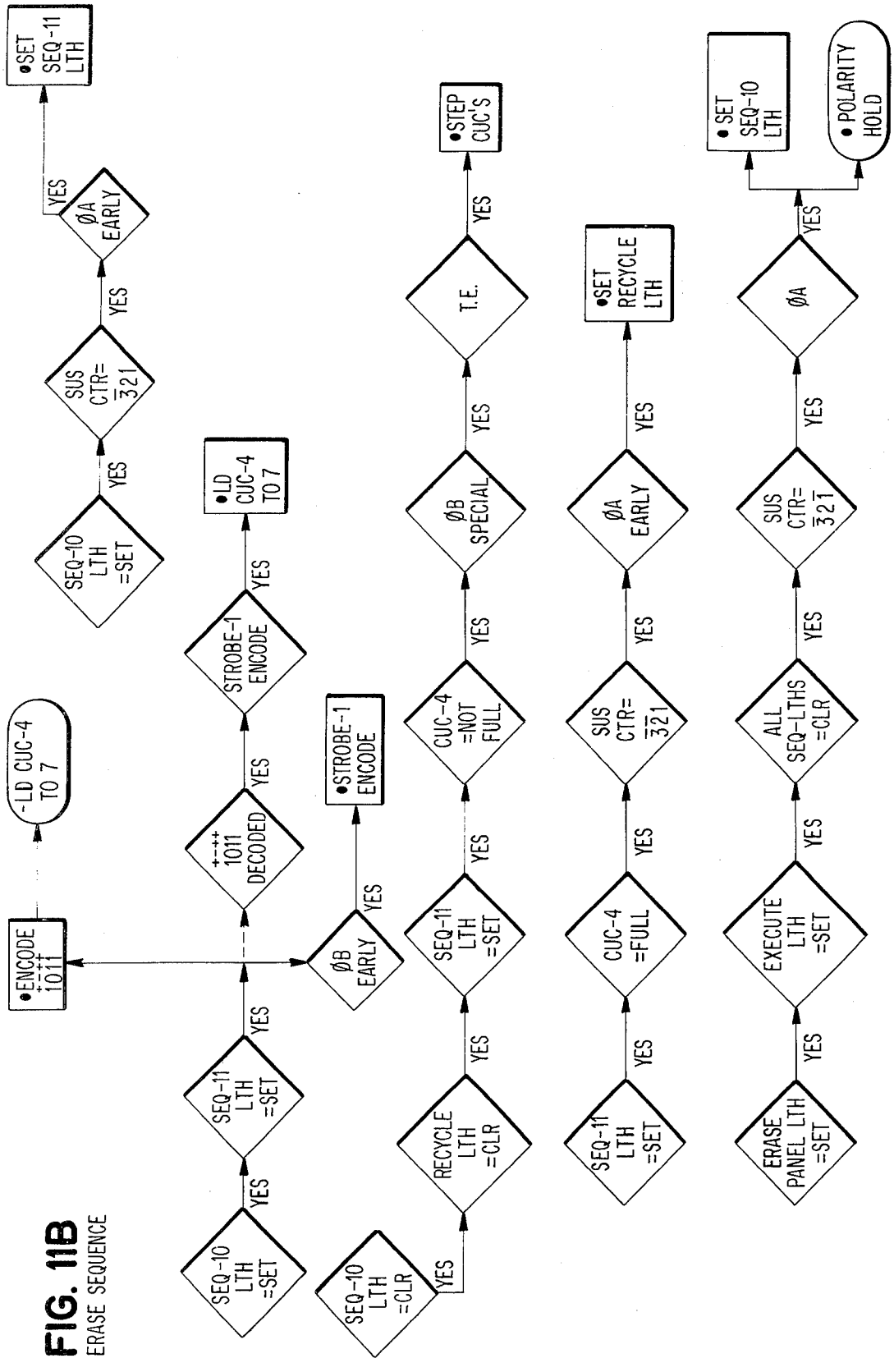
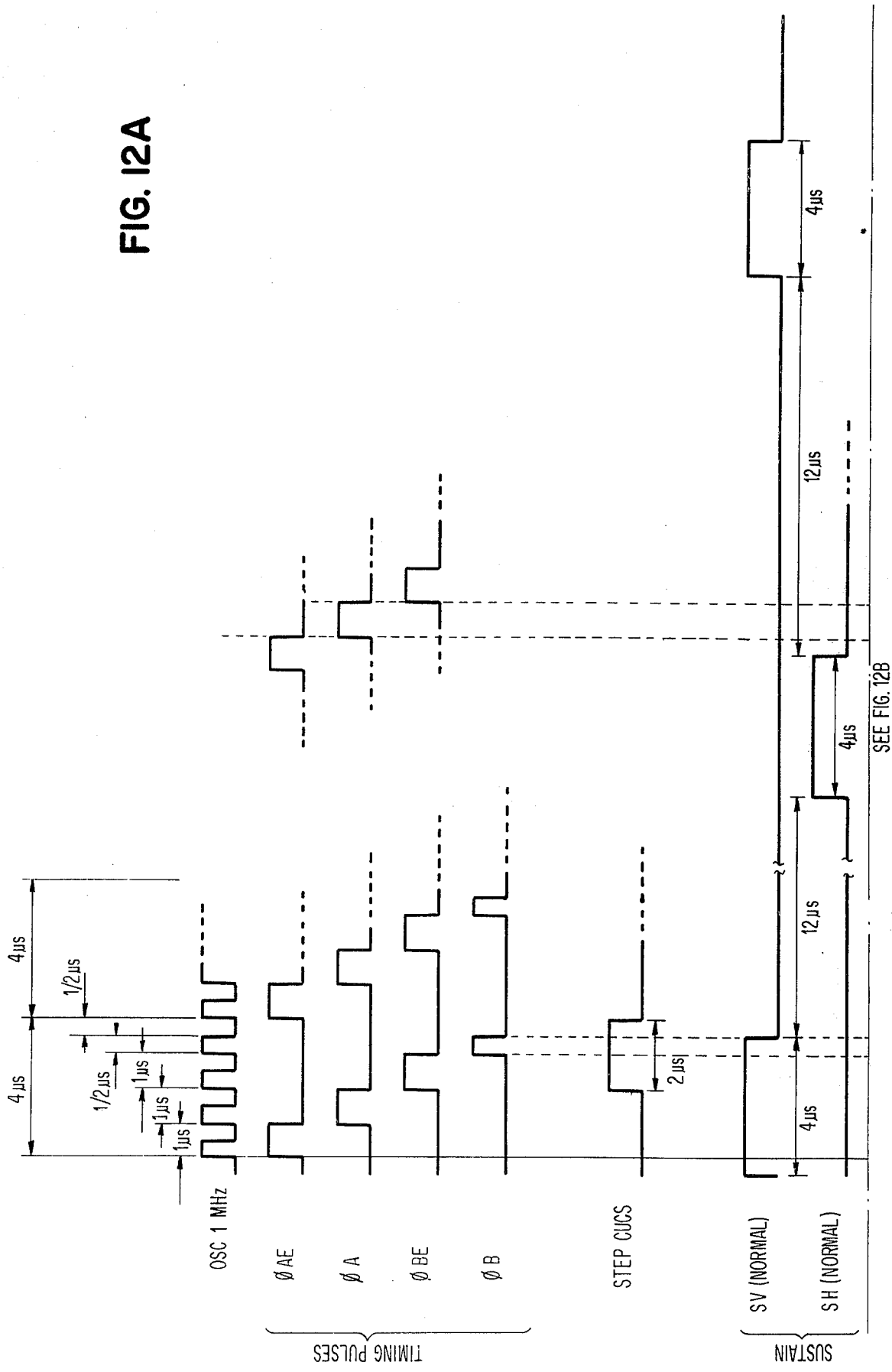


FIG. 11B
ERASE SEQUENCE

FIG. 12A


4µs
1/2µs
4 µs
1/2µs
1µs
1µs
1µs
OSC 1 MHz
ØAE
Ø A
Ø BE
Ø B
TIMING PULSES
STEP CUCS
2µs
SV (NORMAL)
SH (NORMAL)
SUSTAIN
4µs
12µs
12µs
4µs
SEE FIG. 12B

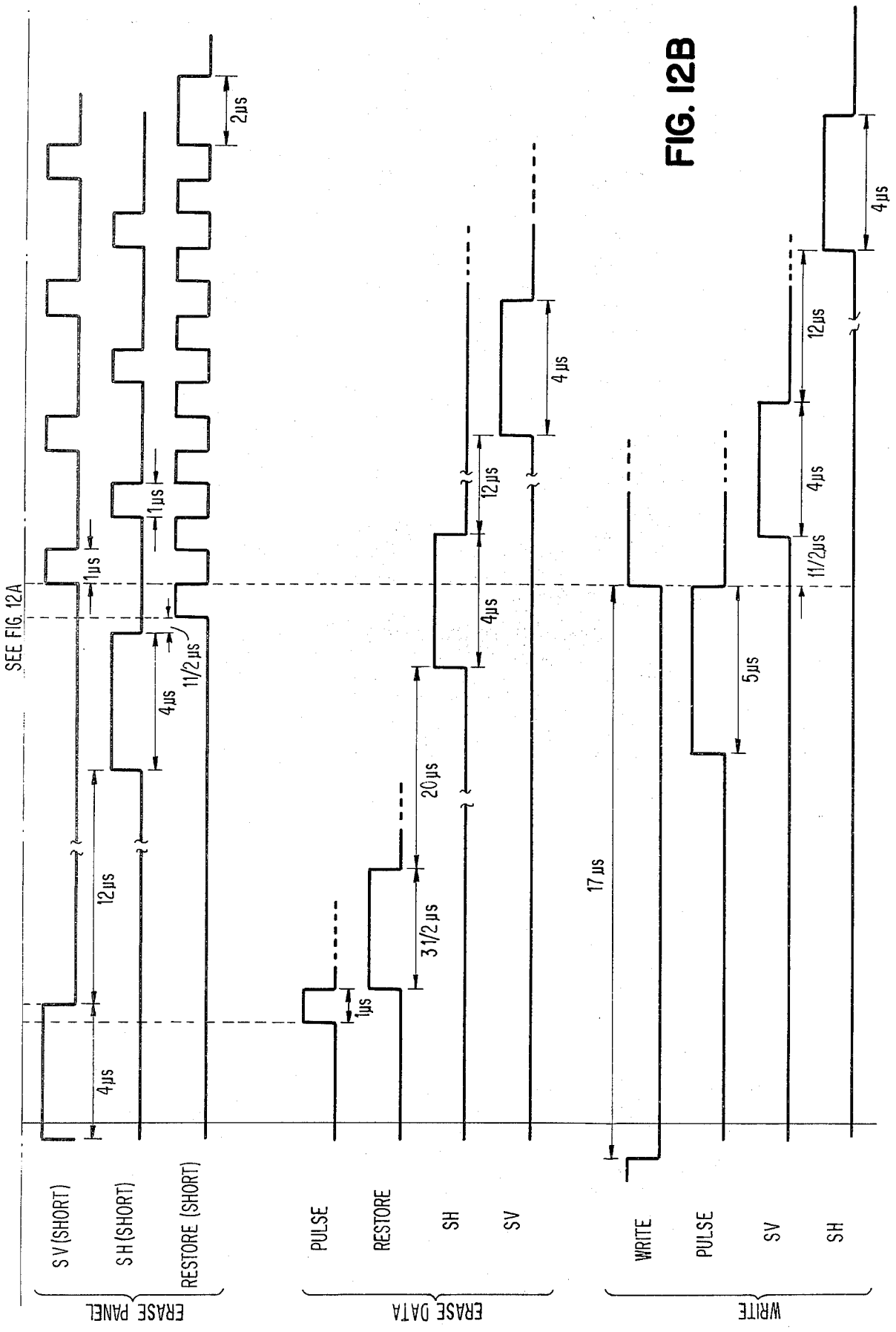

SEE FIG. 12A
SV (SHORT)
SH (SHORT)
RESTORE (SHORT)
ERASE PANEL
PULSE
RESTORE
SH
SV
ERASE DATA
WRITE
PULSE
SV
SH
WRITE
1µs
4µs
12µs
1µs
4µs
11/2µs
2µs
1µs
3 1/2 µs
20µs
4µs
12µs
4 µs
17 µs
5µs
11/2µs
4µs
12µs
4µs

FIG. 12B

CONTROL LOGIC FOR GAS DISCHARGE DISPLAY PANEL

CROSS-REFERENCES TO RELATED APPLICATIONS

This application concerns control logic for generating digital control signals for selecting the coordinate line drivers of a gas discharge display panel such as described in copending patent application Ser. No. 261,773, filed June 12, 1972, by Kleen et al. for "Co-Packaged All-Solid-State Low Level Coupling and Drive Control Circuits for Gas Discharge Display Panel" and now U.S. Pat. No. 3,811,124.

This application also incorporates a data storage addressing circuit as described in copending patent application Ser. No. 309,387, filed Nov. 24, 1972, by Pearson et al. for "Storage Access Apparatus" and now U.S. Pat. No. 3,794,970.

Both of these copending applications are assigned to the assignee of the present application, and disclosures of both of these applications are hereby expressly incorporated by reference into the present application.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to the field of gas discharge display panels and, more particularly, to control logic for generating control signals to select desired discharge cells or sites in such a display panel.

2. Description of the Prior Art

Gas discharge panels per se are well known as evidenced by U.S. Pat. Nos. 3,559,190 and 3,573,542. These patents describe the physics and operation of such panels, and the copending patent application, Ser. No. 261,773 also describes isolation and switched or latched panel line driver circuits which may be selected for determining the display panel lines which are to be energized by sustaining, write or erase operating voltages necessary to determine the condition of a particular cell or site in the display panel.

However, gas discharge display panels are a relatively new technology, and the prior art has been concerned with the physics, structure and energization of the panel. That is, the prior art has not concerned itself with control logic necessary to control the energization of a panel in order to obtain the display of particular configurations on the panel in the form of illuminated panel cells corresponding to a desired configuration, e.g., alpha-numeric characters and other symbols. Therefore, there is a need in this technology to provide control logic responsive to computer or processor signals for selecting or setting latchable gas panel line driver circuits which are associated with individual panel drive lines in order to display desired configurations on the panel.

SUMMARY OF THE INVENTION

The object of the invention is to provide control logic for generating digital control signals for selecting driver circuits associated with the individual coordinate panel drive lines of a gas panel in accordance with a desired configuration to be displayed on the panel.

This object is accomplished in general by providing control logic circuits responsive to appropriate command and data signals for producing low voltage digital control signals for selecting the starting cell or site in the panel for a character to be displayed on the panel, and for then selected on a line-by-line, i.e., horizontal-by-horizontal slice, basis the line drivers corresponding to the panel cells which are to be illuminated in order to display a desired character or horizontal data slice. Provisions are also made for producing digital control signals for controlling the erasing of a portion of the panel or the simultaneous erasing of the entire panel.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a complete gas discharge display panel including the control logic of this invention.

FIG. 2 is a block diagram showing the signals which are transmitted between the interface and the control logic of this invention.

FIGS. 3A and 3B are block diagrams illustrating the components of, and the signals associated with, the data flow chip of the logic control of this invention.

FIG. 4 is a block diagram illustrating the components of, and the signals associated with, the control chip of the logic control of this invention.

FIGS. 5A and 5B are flow charts illustrating the control functions for the reset, timing pulse generator and command decode functions of the control logic of this invention.

FIGS. 6A, 6B, and 6C are flow charts illustrating the setting of the command latches and the operation of the basic control latches of the logic control of this invention.

FIGS. 7A and 7B are flow charts illustrating the generation of some logic control functions.

FIGS. 8A and 8B are flow charts illustrating the position load and start WRITE operations of the control logic of this invention.

FIGS. 9A, 9B, 9C and 9D are flow charts illustrating the WRITE sequence of the control logic of this invention.

FIGS. 10A, 10B and 10C are flow charts illustrating the start ERASE sequence of the control logic of this invention.

FIGS. 11A and 11B are flow charts illustrating the ERASE sequence of the control logic of this invention.

FIGS. 12A and 12B are a timing diagram showing the control logic timing signals and other control signals.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 is a block diagram of a complete gas discharge display panel system including three main sections: (1) an External Source of command data and housekeeping signals; (2) Control Logic for generating digital control signals in response to the signals received from the external source; and (3) a gas discharge Display Panel with associated high voltage analog power circuits, high voltage isolation circuits, and panel line driver circuits.

This invention is concerned with the Control Logic section of the overall system illustrated in FIG. 1. The External Source may be considered the "outside world" with respect to this invention and includes a computer or processor 10, an interface 12 and a 1 MHz oscillator 14. All of these elements are conventional and per se form no part of the invention. Similarly, the Display Panel and Associated Circuits per se form no part of the present invention as all the elements in this section are fully described in the copending application

Ser. No. 261,773. More specifically, the display panel **15** is a gas discharge panel having a plurality of gas discharge cells or sites defined by the intersection of vertical (column) panel lines **16** and horizontal (row) panel lines **17.** As described in the aforesaid copending application Ser. No. 261,773, all the horizontal or row line drivers are connected to a high voltage drive control circuit (analog power circuits **24**) by means of two buses or conductors which are designated LBR (LOWER BUS ROW) and UBR (UPPER BUS ROW). Similarly, the vertical or column drivers are connected to the high voltage circuit by means of two buses designated LBC (LOWER BUS COLUMN) and UBC (UPPER BUS COLUMN).

The vertical line drivers **18** and the horizontal line drivers **19** are individual latchable or bistable panel line driver circuits which may be selectively set, latched, selected or pre-conditioned in accordance with low voltage control signals (Decoded Driver Select Signals) passing through the vertical and horizontal high voltage isolation circuits **20** and **22.** Selected individual vertical and horizontal line drivers are then energized by appropriate high voltage pulses produced by the analog power circuits **24.** These voltage pulses have an amplitude, polarity and duration determined by whether they are sustain, write or erase pulses for respectively sustaining, writing or erasing a cell or site defined by the intersection of a selected pair of vertical and horizontal panel lines. Detailed operation of the gas panel and the detailed structure of the line drivers, isolation circuits and analog power circuits are described in detail in the copending application Ser. No. 261,773 and also in U.S. Pat. Nos. 3,559,190 and 3,573,542.

FIG. **2** shows in more detail the signals transmitted between interface **12** and data flow chip **26,** control chip **28** and ROS **30.** These signals are used in the flow charts shown in the drawing. ROS **30** in practice actually comprises two ROS Modules which are selected by the ±ROS MOD SEL signal. The interface contains a nine bit ROS address register and a four bit slice address register to permit sequential addressing of nine slices of a ROS character generated as described in copending application Ser. No. 309,387. In FIG. **2** and other Figures, the encircled numbers specify the number of conductors represented by a line.

As stated previously, this invention concerns the Control Logic section shown in FIG. **1** and which consists of three basic elements: a data flow chip **26,** a control chip **28** and an optional ROS (READ ONLY STORAGE) **30.**

The logical circuit elements comprising the data flow and control chips **26** and **28** are illustrated in other figures of the drawing and will be described in more detail below. The operation of these chips in responding to various control signals and in generating other control signals is shown in the flow charts in still other figures of the drawing.

The preferred embodiment of the invention is designed to respond to eight 8-bit commands from the External Source. Four of these commands are POSITION commands and the others are WRITE CHARACTER, WRITE SLICE, ERASE DATA and ,ERASE PANEL.

As will be described in more detail below, the POSITION commands and associated data bytes determine the coordinates of a starting discharge cell or site in the gas panel. The WRITE CHARACTER command is optional and calls for the display on the panel of a complete character stored in ROS **30** and defined by a character code contained in a data byte following such a command. An ERASE DATA command calls for the erasure or extinguishment of a block of data displayed on the panel, which block is defined by height and width in a following data byte. An ERASE PANEL command calls for the simultaneous erasure of all the cells in the gas discharge display panel.

A first set of key digital control signals produced by the Control Logic as shown in FIG. **1** are the data chip outputs DECODED DRIVER SELECT SIGNALS and control chip outputs VT SEL and HZ SEL which together set, select or pre-condition the individual vertical and horizontal gas panel line drivers in accordance with the command and data signals received from the external source. A second set of key digital control signals are the control chip outputs labeled WRITE (or WRITE LEVEL), PULSE, RESTORE S_H (Horizontal Sustain) and S_V (Vertical Sustain). The control chip also provides VT SEL (Vertical Select) and HZ SEL (Horizontal Select) signals and other gating and timing signals. The digital control signals produced by the Control Logic of this invention correspond to the low voltage digital select and control signals alluded to in copending application Ser. No. 261,773. In fact, with the exception of the optional ROS signals, the Control Logic of this invention can be considered to provide the function of block **17** labeled LV DIGITAL SELECT CONTROL SOURCE in said copending application. In the copending application, the WRITE GATE signal corresponds to the WRITE signal of this application, and the WRITE/ERASE signal corresponds to the PULSE signal.

FIG. **3** is a block diagram of the data flow chip illustrated in FIG. **1.** As mentioned previously, there are eight possible commands; four POSITION commands plus WRITE CHARACTER, WRITE SLICE, ERASE DATA and ERASE PANEL. If a tag TC (time of command) signal is present, an incoming 8-bit byte command is decoded in a command decoder **34.** The data chip contains four position latches **36, 38, 40** and **42** corresponding respectively to the four possible POSITION commands: HORIZONTAL COARSE (H.C.), HORIZONTAL FINE (H.F.), VERTICAL COARSE (V.C.) and VERTICAL FINE (V.F.).

Also located on the data chip is a decoder **44** which responds to a 4-bit code appearing on line **46** and which is generated by the control chip. The names of the decoded control signals from decoder **44** are located on the output lines of the decoder and for convenience are assigned alphabetical letters enclosed in a box. These control signals from decoder **44** will be used to describe the operation of the data control chip.

For example, when command decoder **34** decodes one of the POSITION commands and the SET COMMAND LATCHES signal A is up, the latch control circuit **48** causes the corresponding one of the position latches **36, 38, 40** and **42** to be set. A 4-bit code corresponding to the set latch then appears on line **50** and is applied to a position register control circuit **52** which generates, in response to the appropriate decoder **44** signals D and E, one of eight signals for clearing or loading the vertical position (horizontal lines) data register (V/R) **54** and the horizontal position (vertical lines) data register (H/R) **56.** Each of these registers is divided into a 1-bit coarse register and a 8-bit fine register. Use of two registers in both the vertical and hori-

zontal position to define the horizontal and vertical coordinates of a cell in the gas panel is imposed by hardware restraints. That is, for the preferred embodiment described, the command/data bus **32** is limited to 8-bits, but it is desired to address a gas panel having a matrix of 512 × 512 lines, i.e., 512 horizontal panel lines and 512 vertical lines, with each of the lines having an individual line driver which may be selectively set or preconditioned by the decoded driver select signals produced by the data chip. Consequently, to select a horizontal position (driver) of the gas display panel, a horizontal coarse command is first received on the command data bus, and then is followed by a horizontal coarse data byte, the least significant position of which is stored in the horizontal coarse register. Then a horizontal fine command is received and followed by an 8-bit horizontal fine data byte which is stored in the horizontal fine register to produce on the horizontal register output line **58** a 9-bit code or address uniquely identifying one of the vertical drivers of the gas panel. The same procedure is followed for selecting a horizontal driver and a 9-bit address or code appears on the output line **60** of the vertical position register **54.** If the command is not one of the POSITION commands, then it is encoded by an encoder **62** into a 3-bit code which appears on line **64** which is connected to the control chip.

After one of the position latches **36, 38, 40, 42** is set, a following data byte specifying the appropriate position appears on the command/data bus **32** and is stored in the storage register (S/R) **66.** The corresponding data bytes following each of the POSITION commands are gated through corresponding position gate circuits **68, 70, 72** and **73** under the control of the register load signals **5, 6, 7** and **8** from the control **52** into the 9-bit vertical and horizontal position registers **54** and **56** with the ninth bit of each register corresponding to the least significant bit of the coarse position data byte and the other eight bits corresponding to the fine position data byte. The 9-bit bytes stored in the position registers **54** and **56** define the coordinates of a panel cell (two line drivers) and, in particular, the starting cell of a horizontal line or slice to be displayed on the gas panel or of a data block to be erased. More specifically, when a character is to be displayed, the defined cell is in the upper left corner of the 7 × 9 matrix of cells within which the character will be displayed slice-by-slice from top to bottom.

Let us assume that a WRITE CHARACTER command and its associated TD (time of data) signal are now received on the control/data bus **32.** As previously explained, this command is encoded by encoder **62** and sent as a 3-bit code to the control chip **28** via line **64.** As shown in FIG. **4,** a decoder **90** decodes this code to set the WRITE CHARACTER command latch **91.** As will be explained below, the control chip contains a sequencer comprising **11** SEQUENCE LATCHES, the first six of which are used to implement the WRITE CHARACTER command. The WRITE CHARACTER command initiates operation of the sequencer to cause a character specified by a following character code data byte to be displayed as a pattern of illuminated gas cells within a 7 × 9 matrix of cells in the gas panel, the position of this matrix having already been stored in the position registers **54** and **56.**

The ROS **30** stores various characters, and the character code data byte is the ROS address of the first horizontal slice of one of those stored characters. When the character code byte is received with the associated TD signal on the input bus, it is converted to a bit address and stored in the ROS address register in interface **12.** The conversion of the 8-bit byte to a 9-bit address is described in copending application Ser. No. 309,387. This address identifies the first horizontal slice of the 7 × 9 character block stored in ROs **30** and gated out through the ROS gates **31** to the data flow chip **26** under the control of a GT ROS OUT signal from the control chip.

During the first two sequences of the sequencer in the control chip, i.e., during the period in which SEQUENCE LATCHES **1** or **2** are set, the horizontal line address stored in the register V/R [54] is transferred to 9-bit binary count up (CUC **9**) counter **76.** Bits **6-9** of the counter **76** are then decoded by a decoder **78** into a 2/7 code which together with the counter bits 1–5 forms the horizontal driver select signal which is applied through the horizontal isolation circuits **22** of the gas panel to set or precondition the corresponding horizontal or row line driver. This driver then identifies the horizontal line or row of panel cells which will display the first horizontal slice of the character stored in ROS. The contents of counter **76** are then incremented by one by a STEP CUC's signal from the control chip, and the incremented count is stored back in register **54** via the slice update gates **80.** Consequently, register **54** now stores the address of the next lower horizontal line driver of the gas panel, and counter **76** is free to use for another purpose.

The third sequence begins by transferring the contents of a ROS slice register (RS/R) **82** (which had been reset to 0 when the WRITE CHARACTER command was received) to a 4-bit binary count-up counter (CUC **4**) **74.** The count stored in the CUC **4** counter **74** is returned to the interface **12** and used to increment the ROS address of the horizontal slices of the character stored in ROS **30.** The initial CUC4 count of 0 defines the ROS address of the first slice within the character block selected by the character code data byte following the WRITE CHARACTER command. An 8-bit horizontal slice (the 9th bit in ROS is a stop bit for indicating whether a slice is the last slice of a character) is then gated through ROS output gates into the storage register **66,** and the contents of the CUC **4** counter **74** are incremented by one and gated back into the ROS slice register **82** in order to free the counter **74** for another purpose.

The fourth sequence begins when the vertical lines register **56** is loaded into the CUC9 counter **76** to select the first vertical line driver of the gas panel. While counter **76** is being loaded, the CUC4 counter **74** is also being loaded with a count of seven. The outputs of the CUC9 counter **76** are again decoded by the decoder **78,** but the vertical panel line driver identified by the count stored in counter **76** is set or preconditioned only if an output is also received from the CUC4 decoder **84** on the decoder output line **86.** The CUC4 decoder **84** generates an output when the first bit of the slice stored in the store register **66** is a one and the count stored in CUC4 counter equals seven, the second bit in the storage register is one and the CUC4 counter equals eight, the third bit in the storage register is one and the CUC4 counter equals nine, etc. Therefore, each of the vertical or column line drivers sequentially selected by CUC4 **74** is either set or not set depending

upon whether the corresponding bit position in the horizontal slice stored in the storage register **66** is a one or a zero.

The CUC4 counter **74** and CUC9 counter **76** are continually stepped until the count of the CUC4 counter equals **15**, thereby indicating that all seven vertical line drivers have been set or not in accordance with the horizontal slice pattern stored in register **66.** In the preferred embodiment, the eighth bit is not used since two vertical lines of the gas panel remain inactive to provide horizontal spacing between adjacent characters displayed on the panel.

During sequences five and six, i.e., when sequence latches **5** or **6** are set, the control chip **28** produces WRITE (or WRITE LEVEL), S_H and S_V digital control pulses which are applied to the analog power circuits **24** which in turn apply the necessary write and sustain operating voltages to the horizontal and vertical panel lines whose drivers have been set or preconditioned. Only the panel cells or sites having these operating voltages applied to both their horizontal and vertical panel lines will be illuminated, as described in detail in copending application Ser. No. 261,773, thereby displaying an illuminated pattern corresponding to the bit pattern stored in storage register **66.**

During sequence **6,** after the proper number of cycles of sustain voltage have been applied to sustain illumination of the selected cells, the stop bit at the end of the ROS slice is examined to determine if the displayed slice is the last one of the character. If not, the address of the next slice is transferred from the ROS slice register **82** to CUC4 counter **74** whose output increments by one the ROS address stored in the ROS address register of interface **12.** The above-described sequence is then repeated until a stop bit is sensed, thereby indicating that the last slice of the character stored in ROS **30** has been addressed.

The WRITE SLICE mode of operation is similar to the WRITE CHARACTER operation. In this case, the WRITE SLICE command is decoded in command decoder **34,** encoded into a 3-bit code by the encoder **62,** and then sent to the control chip **28** where it is decoded by the decoder **90** to set the WRITE SLICE COMMAND LATCH (W.S. CMD. LTH.) **92.** The following data byte, rather than specifying a character stored in ROS, is the actual bit pattern of a horizontal slice to be written or displayed in the gas panel. The four POSITION commands may or may not be needed in order to write a slice. For example, if the immediately preceding command was also a WRITE SLICE command, then the horizontal lines register (V/R) **54** would have been incremented to the next horizontal slice via the slice update gates **80** and thus will contain the next lower horizontal slice location. After the WRITE SLICE COMMAND LATCH **92** is set, the following data byte specifying the bit pattern of the horizontal slice is loaded into the storage register **66.** The described six sequences involving the setting of sequence latches one through six in the control chip **28** are then performed with the function of sequence three being inhibited so that the ROS is not addressed.

Thus, during the first two sequences the contents of the register **54** are transferred to CUC9 counter **76** and decoded by the decoder **78** to select or precondition the corresponding horizontal panel line driver. The contents of CUC9 **76** are then incremented and stored back into the register **54** through the slice update gates **80.** The function of sequence three, as previously described with respect to the WRITE CHARACTER command, is inhibited. Sequence four proceeds as previously described to cause the eight vertical or column line drivers to be set or preconditioned in accordance with the slice bit pattern stored in the storage register **66.**

In Sequences five and six, the digital control signals WRITE and S_H and S_V are then generated by the control chip and applied to the analog power circuits **24** to cause the appropriate write and sustain operating voltages to be applied to the row and column conductors of the gas panel, thereby illuminating the gas panel cells corresponding to the bit pattern stored in the storage register **66.**

By virtue of the fact that position command latches **36, 38, 40, 42** and function command latches **91, 92,** 94 and **98** are not reset until a new command is received, a single write slice command can be followed by a plurality of sequential data bytes. The sequential data bytes will be displayed as sequential horizontal slices because the WRITE SLICE COMMAND LATCH **92** will remain set and horizontal lines register **54** will be incremented via slice update gates **80** as each sequential data byte is displayed. This function permits processor generated alphanumeric characters, special characters or symbols and graphics to be displayed without the need for additional WRITE SLICE commands to precede each data byte.

The operations for ERASE DATA and ERASE PANEL commands are substantially different from that for the WRITE CHARACTER and WRITE SLICE commands. An ERASE DATA command will usually follow a sequence of the four POSITION commands and position data bytes as described above to identify the upper left hand panel cell of the data block to be erased from the gas display panel. Therefore, the position registers **54** and **56** store the horizontal and vertical line addresses, respectively, of the line driver associated with the starting cell.

When the ERASE DATA command is received with its TC tag signal, it is decoded by decoder **34,** encoded into a 3-bit code by encoder **62,** and then sent to the control chip where it is decoded by decoder **90** to set the ERASE DATA COMMAND LATCH (E.D. CMD. LTH.) **94.** A following data byte (with a TD tag) defining the size of the data block to be erased is then received on the command/data input bus **32** and is stored in the store register **66.** The first four bits of the data define the width of the data block by specifying the number Δ H of vertical lines in the block to be erased. The last 4 bits define the height of the block by specifying the number Δ V of horizontal lines in the block. Each 4-bit dimension is actually in a 16 complement form. For example, if the width Δ H of the data block is three vertical lines, then the corresponding 4 bits in the data byte represent a count of 12.

The decoded ERASE DATA command is then executed in sequences seven through eleven by sequence latches **7–11** in the control chip and as described in the flow charts illustrated in the drawings.

During sequence seven, when decoder **44** produces the appropriate control signal in response to the **4**-code and STROBE **1** and STROBE **2** signals, the leftmost vertical line address of the starting cell is transferred from vertical lines register **56** to CUC9 counter **76** and the Δ H block width is transferred through gates **102** to

CUC4 counter **74.** Typically, when the data to be erased is a 7 × 9 character matrix, Δ H = 8 lines, and therefore, the complement count of 7 is stored in CUC4. The CUC4 count is decoded by CUC4 decoder **84,** and decoder **78** in response to the outputs of both the CUC9 counter **76** and the CUC4 decoder together with the 5-bit output of CUC9 counter **76** causes the leftmost vertical line driver in the data block to be set or preconditioned. Both the CUC4 and the CUC9 are then simultaneously incremented by one by the STEP CUC's signal to cause the next vertical line driver to be preconditioned. When the CUC4 is full, that is, reaches a count of **15,** all the vertical line drivers within the width Δ H have been set.

Next, during sequence eight, the CUC9 counter **76** and the CUC4 counter **74** are first cleared. Then, the contents of the horizontal line register **54** are transferred to CUC9 counter **76** to identify the first horizontal row of drivers connected to the panel lines in the data block to be erased. The complement of Δ V, the height of the data block to be erased, is transferred through gates **100** to CUC4 counter **74.**

During Sequence nine, the horizontal drivers connected to panel row lines in the data block to be erased are then set or preconditioned by the outputs of decoder **78** together with the 5-bit output of the CUC9 counter **76,** as described above for the vertical lines. Again, the CUC9 counter and the CUC4 counter are simultaneously stepped by the STEP CUC's signal in order sequentially to set all the horizontal drivers within the height Δ V. When the CUC4 counter reaches a count of 15, all the specified horizontal drivers have been set, and thus the data block to be erased is defined by a grid of panel lines whose drivers have been set or preconditioned.

During sequence **10,** a pulse latch in the control chip is set and a 1-microsecond wide PULSE signal is applied to the analog power circuits (there is no WRITE signal at this time) which then apply the necessary erase operating voltages through the preconditioned drivers to the panel lines so that all the cells defined by the data block grid of preconditioned horizontal and vertical drivers are extinguished or erased.

Sequence **11** is a synchronizing wait sequence during which normal sustain voltages are applied to the panel to refresh the remainder of the panel which has not been erased. When an ERASE PANEL command is received, the erase panel latch (E.P. CMD. LTH.) **98** on the control chip **28** is set. In this case, sequences 7, 8 and 9 are not required since all the cells of the panel are to be extinguished. Consequently, a modified sequence 10 is entered to produce a series of shortened (one microsecond) S_H and S_L SUSTAIN control signals interleaved with appropriate one microsecond RESTORE control signals. These control signals are applied to the analog power circuits **24** which generate the panel operating voltages necessary to extinguish the entire panel, all as described in detail in copending application Ser. No. 261,773. Sequence 11 is next performed in an identical manner to that described above for the ERASE DATA operation.

FIG. **4** is a block diagram of control chip **28** and includes prime or external signals necessary to carry out the commands described above. All of the actual hardware or logic circuitry for producing these prime signals and other internal signals of the control chip is not shown. However, the flow charts illustrated in FIGS. **5** through **11** show all the logical functions necessary to implement these commands in addition to some housekeeping functions. The various control latches such as EXECUTE, ACCEPT, etc., referred to in the flow charts are conventional and are included within the block **104** labeled "CTRL LTHS" in FIG. **4.** The term T.E. means trailing edge. The flow charts plus the other drawing figures would enable one skilled in the art to which this invention pertains to design logic circuits for implementing the functions specified in the flow charts.

Dashed flow lines in the flow charts indicate a connection external to the control chip **28,** such as a connection to the data flow chip **26.** Interrupted lines in FIGS. **3A, 3B** and **4** also indicate an external connection.

As shown in FIG. **4,** a 1MHz square wave signal from oscillator **14** is applied to a conventional frequency divider **106** and timing pulse generator (TPG) **108** combination which produces the basic timing signals for the control logic of the invention. The basic timing signals are identified as ϕAE, ϕA, ϕBE and ϕB. The oscillator signal and the timing signals are shown in the first five lines of the timing diagram shown in FIG. **12.** The basic timing cycle is 4 microseconds long and includes ϕAE, ϕA, ϕBE and ϕB in succession with the first three signals being of 1-microsecond duration and ϕB of one-half microsecond duration. The STEP CUC's pulse when it is produced rises at the leading of ϕBE and falls at the leading edge of the ϕAE thereby providing a signal having a 2-microsecond duration.

The frequency divider **106** effectively divides the oscillator signal by four and actually includes two frequency dividers which are referred to as F_1 DVDR and F_2 DVDR in the flow charts.

Sustain counter **110** is a three stage binary counter with full look ahead feature and is driven by appropriately gated signals on the -STEP SUS CTR line. Its count is decoded by a sustain decoder **116** having nine output lines which are connected to the control logic block **114** to cause appropriate S_H and S_L sustain control signals to be applied to the analog power circuits **24** as previously described.

The functions of the CUC4 decoder **96,** the three-code decoder **90,** and the four command latches **91,** 92, 94 and **98** have already been described. The operation of the sequencer **122** comprising 11 sequence latches **124** has already been described and is shown in detail in the flow charts.

Control signals from control block are encoded into a 4-bit code by a four-code encoder **126** and sent to decoder **44** in the data flow chip **26.** STROBE **1** and STROBE **2** signals produced at the appropriate times by the strobe generator **128** are combined with the 4-bit code signals in decoder **44** to produce the flow control signals A through S. The control block **114** also produces other Function Control Signals which are sent to other portions of the system illustrated in FIG. **1.**

The timing diagram of FIG. **12** has already been alluded to and shows the oscillator **14** signal waveform and the four basic timing pulses ϕAE, ϕA, ϕBE and ϕB. Additional key signals relating to the WRITE and ERASE commands described above are also shown on the diagram. These signals are shown individually or in groups properly referenced in phase relative to the oscillator signal and the basic timing pulses, but since these signals are actually spaced over relatively long

periods of time, their actual position in time with respect to each other is not indicated on the diagram.

The S_V (normal) and S_H (normal) are the normal sustain pulses which are applied to the analog power circuits which supply corresponding high voltages to sustain the illumination of gas panel cells which have already been ignited, by a WRITE operation for example. The normal sustain cycle is 32 microseconds long and consists of alternate S_V and S_H pulses each 4 microseconds long and spaced apart by 12 microseconds.

The ERASE PANEL operation is shown as being performed by a series of short (seven 1-microsecond and one 2-microsecond) RESTORE pulses starting 1½ microseconds after an S_H (normal) sustain pulse interleaved with four short (1 microsecond) S_V (short) and three short S_H (short) SUSTAIN pulses spaced 4 microseconds apart.

The ERASE DATA operation is shown as being performed by a 1-microsecond PULSE signal, followed by a 3½ microsecond RESTORE signal, followed 22 microseconds later by a series of normal horizontal and vertical sustain pulses S_H (normal) and S_V (normal).

The WRITE operation for the WRITE SLICE and WRITE CHARACTER commands is shown as being performed by a 17 microsecond WRITE level coincident over its last 5 microseconds with a 5-microsecond PULSE signal and then followed in 1½ microseconds by a series of normal sustain pulses S_V and S_H.

The control logic of this invention is universal in the sense that it provides low voltage digital control signals for controlling the operation of any gas discharge display panel.

However, as previously mentioned, the control logic and signal terminology of this invention are also particularly keyed to the gas discharge panel and associated circuits disclosed in copending application Ser. No. 261,773. More specifically, the control logic of this invention corresponds to the block labeled "L.V. Digital Select Control Source" in the copending application. The "row and column digital inputs 17*a*, 17*b*" of the copending application correspond, respectively, to the horizontal and vertical line "Decoded Driver Select Signals" of this invention and which appear at the outputs of CUC9 counter **76** and decoder **78** in the data flow chip **26** as illustrated in FIGS. **1** and **3B**.

The "WRITE GATE" signal of the copending application corresponds to the WRITE (or WRITE LEVEL) control signal of this invention.

The "WRITE/ERASE CONTROL" signal of the copending application corresponds to the PULSE control signal of this invention wherein the combination of a 5-microsecond PULSE signal with a WRITE level designates a WRITE operation, and a 1-microsecond PULSE in the absence of a WRITE level but in conjunction with a RESTORE level designate an ERASE DATA operation.

FIG. **3** of the copending application illustrates one of the latchable line drivers which are represented by blocks **18** and **19** in FIG. **1** of this invention.

FIGS. 4 and 5 of the copending application illustrate the analog power or high voltage circuits **24** shown in FIG. **1** of this invention. The horizontal SUSTAIN control signals would be transformer-coupled to the windings "T_1" shown in the copending application, and the vertical SUSTAIN control signals would be transformer-coupled to the windings "T_2".

The "ROW/COLUMN SEL. STROBES" of the copending application correspond, respectively, to the "HZ.L.SEL." and "VT.L.SEL." signals of this invention.

While the invention has been particularly shown and described with reference to the preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. Control logic for controlling the display of a pattern in a gas discharge display panel including: a matrix of mxn gas discharge cells defined by the intersections of *m* row panel conductors and *n* column panel conductors; a selectable driver circuit connected to each panel conductor and selectable in response to low voltage control signals; and high voltage circuit means for applying, in response to low voltage control signals, high voltage sustain, write or erase operating signals through selected drivers to their connected panel conductors to affect the condition of each gas cell whose associated row and column driver is selected, whereby one or more illuminated gas cells forming a displayed pattern may be sustained in a state of illumination or extinguished or whereby one or more gas cells may be illuminated to form a display pattern; said control logic comprising:

a. command decoder means for decoding digital command signals specifying a command to be executed;

b. position data storage means for storing data associated with a decoded position command signal and identifying a pair of row and column driver circuits connected to a corresponding pair of row and column panel conductors whose intersection defines the address of a starting gas cell;

c. pattern data storage means for storing pattern data associated with a decoded panel operation command signal and identifying a pattern of cells whose conditions are to be affected in accordance with the stored data pattern;

d. counter means responsive to the stored position data, to the stored pattern data and to the decoded panel operation command signal for producing first low voltage control signals for sequentially selecting a plurality of pairs of row and column driver circuits, beginning with said pair of driver circuits associated with said starting cell; and

e. logic control means responsive to the decoded panel operation command signal for producing second low voltage control signals and applying them to the high voltage circuit means, so that appropriate high voltage operating signals are applied through said selected pair of driver circuits to affect the condition of the gas cells identified by the pairs of row and vertical panel conductors connected to said selected pairs of driver circuits.

2. Control logic as defined in claim **1** wherein said panel operation command is a write-pattern command, and wherein said logic control means comprises means responsive to the decoder write-pattern command for producing a low voltage write control signal in response to which the high voltage circuit means applies write operating voltages to said pairs of row and column panel conductors connected to said selected pairs of

driver circuits, whereby the identified gas cells are illuminated in accordance with the stored pattern data.

3. Control logic as defined in claim 1 wherein said panel operation command is a write-pattern command, and wherein said logic control means comprises means responsive to a decoded write-pattern command and to a series of row pattern data for sequentially transferring the series of row pattern data to said pattern data storage means; said counter means being responsive to the sequentially stored rows of pattern data for sequentially selecting corresponding row driver circuits and corresponding column driver circuits within each selected row of driver circuits, whereby the identified gas cells are illuminated in accordance with the sequentially stored series of row pattern data.

4. Control logic as defined in claim 1 wherein said panel operation command is a write-character command, and further comprising read-only storage means for storing a plurality of unique characters each consisting of rows of pattern data; said logic control means comprising means responsive to a decoded write-character command and to a unique character data for sequentially transferring the rows of pattern data corresponding to said unique character data to said pattern data storage means; said counter means being responsive to the sequentially stored rows of pattern data for sequentially selecting corresponding row driver circuits and corresponding column driver circuits within each selected row of driver circuits, whereby the gas cells identified by the sequentially stored rows of pattern data are illuminated to display the unique character.

5. Control logic as defined in claim 1 wherein said panel operation command is an erase-data block command, and wherein the stored pattern data identifies the number of row panel conductors and the number of column panel conductors whose intersections identify a block of gas cells to be extinguished, beginning with said starting gas cell; said counter means being responsive to the decoded erase-data block command for sequentially selecting row and column driver circuits identified by the stored data pattern and said starting gas cell; said logic control means comprising means responsive to the decoded erase-data block signal for producing a second low voltage erase-data block signal in response to which the high voltage circuit means applies high voltage operating signals to all selected drive circuits so that said block of cells is extinguished.

6. Control logic for controlling the display of a pattern in a gas discharge display panel including: a matrix of $m \times n$ gass discharge cells defined by the intersections of m row panel conductors and n column panel conductors; a selectable driver circuit connected to each panel conductor and selectable in response to low voltage control signals; and high voltage circuit means for applying, in response to low voltage control signals, high voltage sustain, write or erase operating signals through selected drivers to their connected panel conductors to affect the condition of each gas cell whose associated row and column driver is selected, whereby one or more illuminated gas cells forming a displayed pattern may be sustained in a state of illumination or extinguished or whereby one or more gas cells may be illuminated to form a displayed pattern; said control logic comprising:

a. command decoder means for decoding an erase panel command; and

b. logic control means responsive to the decoded erase panel command for producing a plurality of alternate shortened, low voltage vertical and horizontal sustain control signals interleaved between shortened low voltage restore control signals, said shortened sustain and restore control signals controlling said high voltage circuit means to provide to said panel conductors erase operating signals in the form of a plurality of shortened high voltage sustain operating signals to cause all illuminated panel gas cells to be extinguished.

7. Control logic as defined in claim 2 wherein said counter means comprises:

position counter means responsive to the contents of said position data storage means defining the address of a starting gas cell, said position counter means incrementing said contents of said position data storage means for sequentially selecting a row driver circuit and a plurality of column driver circuits in response to said stored pattern data beginning with the driver circuits associated with said starting cell.

8. Control logic as defined in claim 7 wherein said counter means further comprises multipurpose counter means responsive to said command decoder means for controlling the number of increments taken by said position counter means.

9. Control logic as defined in claim 4 wherein said counter means comprises:

position counter means responsive to the row position contents of said position data storage means for selecting a row driver circuit, said position counter means incrementing said row position contents of said position data storage means to allow the sequential selection of said corresponding row driver circuits; and

multipurpose counter means for controlling said read only storage means for transferring a row of pattern data corresponding to said unique character data for each selected row driver to said pattern data storage means, said position counter means being responsive to said stored row of pattern data and controlled by said multipurpose counter means for sequentially selecting said corresponding column driver circuits.

10. Control logic as defined in claim 5 wherein said counter means comprises:

position counter means responsive to the contents of said position data storage means defining the address of a starting gas cell; and

multipurpose counter means responsive to said number of column panel conductors of said stored pattern data for controlling said position counter means to sequentially select said column driver circuits identified by said stored pattern data and responsive to said number of row panel conductors of said stored pattern data for controlling said position counter means to sequentially select said row driver circuits identified by said stored pattern data, thereby identifying said block of gas cells to be extinguished.

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