#### (12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization

International Bureau





(10) International Publication Number WO 2016/076562 A1

(43) International Publication Date 19 May 2016 (19.05.2016)

(51) International Patent Classification: H03K 17/955 (2006.01) G06K 9/00 (2006.01)

(21) International Application Number:

PCT/KR2015/011623

(22) International Filing Date:

2 November 2015 (02.11.2015)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data: 10-2014-0155400

10 November 2014 (10.11.2014)

KR

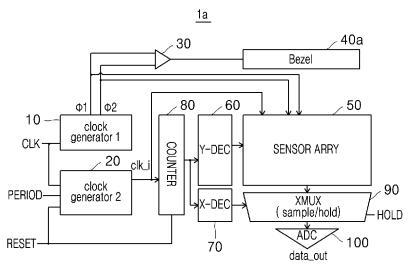
- (71) Applicant: HANSHIN UNIVERSITY IN-DUSTRY-ACADEMIC COOPERATION FOUNDA-TION [KR/KR]; 137, Hanshindae-gil, Osan-si, Gyeonggido 18101 (KR).
- (72) Inventors: YEO, Hyeop Goo; 330, 45, Geumban 1-gil, Hwaseong-si, Gyeonggi-do 18440 (KR). JUNG, Seung Min; 135-404, 152, Naejeong-ro, Bundang-gu, Seongnamsi, Gyeonggi-do 13599 (KR).
- (74) Agents: NAM, Seung-Hee et al.; (Dongchan Bldg., Yeoksam-dong), 4F, 125, Teheran-ro, Gangnam-gu, Seoul 06133 (KR).

- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

#### Published:

with international search report (Art. 21(3))

(54) Title: CHARGE TRANSFER CIRCUIT FOR CAPACITIVE SENSING AND APPARATUS FOR DETECTING FINGER-PRINT HAVING THEREOF



(57) Abstract: A charge transfer circuit for capacitive sensing according to an embodiment of the present disclosure includes a variable capacitor defined through a sensor plate connected to one end of a drive line and one end of an X-drive line, an X-drive part disposed between a voltage input terminal and another end of the X-drive line opposing the variable capacitor, a switched capacitor integrator disposed between a voltage output terminal and another end of the drive line of which the one end is connected to the variable capacitor, and a shielding plate connected to a first input terminal of the switched capacitor integrator, wherein the first input terminal is connected to the other end of the drive line.





# **Description**

# Title of Invention: CHARGE TRANSFER CIRCUIT FOR CA-PACITIVE SENSING AND APPARATUS FOR DETECTING FIN-GERPRINT HAVING THEREOF

### **Technical Field**

[1] The present disclosure relates to a charge transfer technology for capacitive sensing, and more particularly, to a charge transfer circuit for capacitive sensing which is insensitive to parasitic capacitance and in which a switched capacitor integrator or an active output voltage feedback technique is used, and a fingerprint recognition device including the same.

### **Background Art**

- [2] A fingerprint has been most frequently used among various fields of biometrics due to a high identification rate and security, and a substantially enough amount of personal data is currently retained. Recently, with the development of an automatic fingerprint recognition technology, a fingerprint recognition system for acquiring a fingerprint in real time has been required.
- [3] As the prices of fingerprint sensors for use in such a fingerprint recognition system have been recently reduced, the fingerprint sensors are applied to not only a special security device but also peripheral devices of personal computers, such as a keyboard, a mouse, and the like, so as to be used for electronic commerce.
- [4] Therefore, in order to enter such a market, a technology for manufacturing a fingerprint sensor that is easy to use, consumes low power, and has a compact size, a low price and high definition should be secured. Researches have been conducted over the last several decades to develop a technology for electrically sensing a fingerprint. Fingerprint sensing methods proposed up to the present time may be generally classified into an optical type, a thermal type, and a capacitive type.
- According to the capacitive type that is based on the principle in which capacitance varies with a distance between two electrodes, a fingerprint image may be obtained by recognizing a valley and a ridge of a fingerprint on the basis of a difference between capacitance generated between a sensing electrode and the valley of the fingerprint and capacitance generated between the sensing electrode and the ridge of the fingerprint. Since the capacitive type can be implemented using a standard complementary metal oxide semiconductor (CMOS) process technology, the capacitive type enables a simple structure of a sensor and does not require an additional device or a special process, thereby bringing about the advantages of compact size, low power consumption and low cost. However, the sensed capacitance of the ridge or the valley has a very small

value such as several femto farads, and electrodes generally formed of indium tin oxide (ITO) in a touch screen panel have parasitic elements such as capacitance and resistance which may cause serious performance degradation in terms of touch sensitivity and accuracy.

### Disclosure of Invention

#### **Technical Problem**

- [6] The present disclosure provides a fingerprint recognition device having improved touch sensitivity over a wide dynamic range in touch devices including large parasitic elements.
- [7] The present disclosure also provides a charge transfer circuit for capacitive sensing which may be effectively used in a fingerprint recognition device having improved touch sensitivity over a wide dynamic range in touch devices including large parasitic elements.
- [8] The purposes of the present disclosure are not limited to the above-mentioned purposes, and other purposes not mentioned would be clearly understood by those skilled in the art from the disclosure below.

### Solution to Problem

[9]

- In accordance with an exemplary embodiment, a charge transfer circuit for capacitive sensing includes: a variable capacitor defined through a sensor plate connected to one end of a drive line and one end of an X-drive line; an X-drive part disposed between a voltage input terminal and another end of the X-drive line opposing the variable capacitor; a switched capacitor integrator disposed between a voltage output terminal and another end of the drive line of which the one end is connected to the variable capacitor; and a shielding plate connected to a first input terminal of the switched capacitor integrator, wherein the first input terminal of the switched capacitor integrator is connected to the other end of the drive line.
- [11] In an embodiment, the first input terminal of the switched capacitor integrator may receive a reference voltage.
- [12] In an embodiment, the sensor plate and the shielding plate may have a parasitic capacitor therebetween.
- In an embodiment, the switched capacitor integrator may include: an operational amplifier; a third switch of which one terminal is connected to the other end of the drive line and of which another terminal is connected to an inverting input terminal of the operational amplifier; a fourth switch of which one terminal is connected to the other end of the drive line and the one terminal of the third switch and of which another terminal is connected to a non-inverting input terminal of the operational

amplifier and the shielding plate; a storage capacitor of which one terminal is connected to the other terminal of the third switch and the inverting input terminal of the operational amplifier and of which another terminal is connected to an output terminal of the operational amplifier; and a reset switch of which one terminal is connected to the other terminal of the third switch, the inverting input terminal of the operational amplifier, and the one terminal of the storage capacitor and of which another terminal is connected to the output terminal of the operational amplifier and the other terminal of the storage capacitor, wherein the non-inverting input terminal of the operational amplifier is connected to the other end of the drive line and the shielding plate.

- In an embodiment, the X-drive part may include: a first switch configured to be turned on by a first clock signal and turned off by a second clock signal; and a second switch configured to be turned off by the first clock signal and turned on by the second clock signal.
- In an embodiment, the X-drive part may include: a first switch configured to be turned on by a second clock bar signal and turned off by a first clock bar signal; and a second switch configured to be turned off by the second clock bar signal and turned on by the first clock bar signal.
- [16] In an embodiment, the first clock signal and the second clock signal may not overlap with each other.
- [17] In an embodiment, a preset voltage or a reset voltage may be applied to the voltage input terminal.
- In accordance with another exemplary embodiment, a charge transfer circuit for capacitive sensing includes: a variable capacitor defined through a sensor plate connected to one end of a drive line and one end of an X-drive line; an X-drive part disposed between a voltage input terminal and another end of the X-drive line opposing the variable capacitor; an active output voltage feedback unit disposed between a voltage output terminal and another end of the drive line of which the one end is connected to the variable capacitor; and a shielding plate connected to an output terminal of the active output voltage feedback unit, wherein the output terminal of the active output voltage feedback unit opposing the one end of the drive line is connected to the other end of the drive line.
- In an embodiment, the active output voltage feedback unit may include: a third switch and a fourth switch connected in parallel to the other end of the drive line; a buffer circuit unit connected to one terminal of the third switch opposing the drive line; a storage capacitor of which one terminal is connected between the one terminal of the third switch and an input terminal of the buffer circuit unit and of which another terminal is grounded; and a reset switch of which one terminal is connected to the one

terminal of the third switch, the input terminal of the buffer circuit unit, and the storage capacitor and of which another terminal is grounded, wherein an output terminal of the buffer circuit unit opposing the third switch is connected to the other end of the drive line.

- [20] In an embodiment, the third switch may be turned off by a first clock signal and turned on by a second clock signal, and the fourth switch may be turned on by the first clock signal and turned off by the second clock signal.
- [21] In an embodiment, the third switch may be turned off by a second clock bar signal and turned on by a first clock bar signal, and the fourth switch may be turned on by the second clock bar signal and turned off by the first clock bar signal.
- [22] In an embodiment, the first clock signal and the second clock signal may not overlap with each other.
- [23] In an embodiment, the buffer circuit unit may be an operational amplifier.
- [24] In an embodiment, a non-inverting input terminal of the operational amplifier may be connected to the one terminal of the third switch, and an inverting input terminal of the operational amplifier may be connected between an output terminal of the operational amplifier and the fourth switch.
- In accordance with another exemplary embodiment, a fingerprint recognition device includes: a charge transfer circuit for capacitive sensing, the charge transfer circuit including: a variable capacitor defined through a sensor plate connected to one end of a drive line and one end of an X-drive line; an X-drive part disposed between a voltage input terminal and another end of the X-drive line opposing the variable capacitor; a switched capacitor integrator disposed between a voltage output terminal and another end of the drive line of which the one end is connected to the variable capacitor; and a shielding plate connected to a first input terminal of the switched capacitor integrator, wherein the first input terminal of the switched capacitor integrator is connected to the other end of the drive line; and a bezel of which one end is connected to the one end of the X-drive line and of which another end is directly contactable by a finger.
- In accordance with another exemplary embodiment, a fingerprint recognition device includes: a charge transfer circuit for capacitive sensing, the charge transfer circuit including: a variable capacitor defined through a sensor plate connected to one end of a drive line and one end of an X-drive line; an X-drive part disposed between a voltage input terminal and another end of the X-drive line opposing the variable capacitor; an active output voltage feedback unit disposed between a voltage output terminal and another end of the drive line of which the one end is connected to the variable capacitor; and a shielding plate connected to an output terminal of the active output voltage feedback unit, wherein the output terminal of the active output voltage feedback unit opposing the one end of the drive line is connected to the other end of

the drive line; and a bezel of which one end is connected to the one end of the X-drive line and of which another end is directly contactable by a finger.

- [27] In an embodiment, the bezel may be made of metal or conductive polymers.
- In accordance with another exemplary embodiment, a fingerprint recognition device includes: a charge transfer circuit for capacitive sensing, the charge transfer circuit including: a variable capacitor defined through a sensor plate connected to one end of a drive line and one end of an X-drive line; an X-drive part disposed between a voltage input terminal and another end of the X-drive line opposing the variable capacitor; a switched capacitor integrator disposed between a voltage output terminal and another end of the drive line of which the one end is connected to the variable capacitor; and a shielding plate connected to a first input terminal of the switched capacitor integrator, wherein the first input terminal of the switched capacitor integrator is connected to the other end of the drive line; and a top metal of which one end is connected to the one end of the X-drive line and of which another end is contactable by a finger through a passivation layer.
- In accordance with another exemplary embodiment, a fingerprint recognition device includes: a charge transfer circuit for capacitive sensing, the charge transfer circuit including: a variable capacitor defined through a sensor plate connected to one end of a drive line and one end of an X-drive line; an X-drive part disposed between a voltage input terminal and another end of the X-drive line opposing the variable capacitor; an active output voltage feedback unit disposed between a voltage output terminal and another end of the drive line of which the one end is connected to the variable capacitor; and a shielding plate connected to an output terminal of the active output voltage feedback unit, wherein the output terminal of the active output voltage feedback unit opposing the one end of the drive line is connected to the other end of the drive line; and a top metal of which one end is connected to the one end of the X-drive line and of which another end is contactable by a finger through a passivation layer.
- [30] In an embodiment, the top metal may be spaced apart from another top metal so that the one end of the top metal is only connected to the one end of the X-drive line and the other end of the top metal is contactable by the finger through the passivation layer.
- In accordance with another exemplary embodiment, a fingerprint sensing method includes: receiving capacitances of a ridge and a valley of a fingerprint; integrating the received capacitances according to a variable clock; sampling or holding the integrated capacitances; converting the sampled or held capacitances into digital values; and determining whether a fingerprint part is the ridge or the valley on the basis of the digital values converted according to a difference in the capacitances of the ridge and the valley.

[32] In an embodiment, the integrating the received capacitances according to the variable clock may be discrete-time integrating.

[33]

### **Advantageous Effects of Invention**

[34] As described above, according the present disclosure, a charge transfer circuit for capacitive sensing includes a switched capacitor integrator or an active output voltage feedback unit, and thus may minimize the parasitic effects caused by parasitic elements. Accordingly, the present disclosure may provide a charge transfer circuit for capacitive sensing which has improved touch sensitivity over a wide dynamic range and a fingerprint recognition device including the same.

[35]

### **Brief Description of Drawings**

- [36] FIG. 1 is a block diagram illustrating a fingerprint recognition device according to an embodiment of the present disclosure;
- [37] FIG. 2 is a block diagram illustrating a fingerprint recognition device according to another embodiment of the present disclosure;
- [38] FIG. 3 illustrates switch control signals applied to the fingerprint recognition device illustrated in FIG. 1 or 2.
- [39] FIG. 4 is a timing diagram of fingerprint recognition devices according to embodiments of the present disclosure;
- [40] FIG. 5 is a circuit diagram of a charge transfer circuit for capacitive sensing according to an embodiment of the present disclosure included in fingerprint recognition devices according to embodiments of the present disclosure;
- [41] FIG. 6 is a circuit diagram of a charge transfer circuit for capacitive sensing according to another embodiment of the present disclosure included in fingerprint recognition devices according to embodiments of the present disclosure;
- [42] FIG. 7 is a timing diagram illustrating switch control signals applied to charge transfer circuits for capacitive sensing according to embodiments of the present disclosure and an output voltage according to a ridge and a valley of a fingerprint;
- [43] FIG. 8 is a schematic diagram illustrating a situation in which the charge transfer circuit for capacitive sensing of FIG. 5 is used in the fingerprint recognition device based on a direct method of FIG. 1;
- [44] FIG. 9 is a schematic diagram illustrating a situation in which the charge transfer circuit for capacitive sensing of FIG. 6 is used in the fingerprint recognition device based on the direct method of FIG. 1;
- [45] FIG. 10 is a schematic diagram illustrating a situation in which the charge transfer circuit for capacitive sensing of FIG. 5 is used in the fingerprint recognition device

- based on a pseudo-direct method of FIG. 2;
- [46] FIG. 11 is a schematic diagram illustrating a situation in which the charge transfer circuit for capacitive sensing of FIG. 6 is used in the fingerprint recognition device based on the pseudo-direct method of FIG. 2; and
- [47] FIG. 12 is a layout top-view of the fingerprint recognition device based on the pseudo-direct method of FIG. 1.

[48]

### **Best Mode for Carrying out the Invention**

- [49] Specific structures or operations described herein are only intended to describe embodiments of the present disclosure. However, the embodiments of the present disclosure may be implemented in various forms, and should not be construed as being limited to the embodiments described herein.
- [50] The present invention may be variously modified and may have various forms. However, particular embodiments are exemplarily illustrated in the drawings and are described in detail below. However, it should be understood that the present invention is not limited to specific forms, but rather cover all modifications, equivalents or alternatives that fall within the spirit and scope of the present invention.
- [51] The terms "first", "second" and the like may be used for describing various elements, but the elements should not be construed as being limited by the terms. Such terms are only used for distinguishing one element from other elements. For example, without departing the scope of the present invention, a first element may be referred to as a second element, and, likewise, a second element may be referred to as a first element.
- [52] It will be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present. Other terms for describing relationships among elements, such as "between", "directly between", "adjacent to", "directly adjacent to", and the like, should be interpreted in the same manner.
- The terminology used herein is not for delimiting the present invention but for describing specific embodiments. The terms of a singular form may include plural forms unless otherwise specified. It will be further understood that the terms "comprise", "comprising,", "include", "including", "have" or "having", when used herein, specify the presence of stated features, numbers, steps, operations, elements, components or combinations thereof, but do not preclude the presence or addition of one or more other features, numbers, steps, operations, elements, components or combinations thereof.

[54] The terms used herein, including technical or scientific terms, have the same meanings as understood by those skilled in the art. Terms in common usage such as those defined in commonly used dictionaries should be interpreted as is customary in the relevant art, but should not be interpreted in an idealized or overly formal sense unless otherwise defined herein.

- [55] In the case where some embodiments can be differently implemented, functions or operations described with respect to specific blocks may be performed in a different sequence from that described in a flowchart. For example, two successive blocks may be operated substantially at the same time, or may be operated reversely depending on related functions or operations.
- [56] Preferred embodiments of the present disclosure are described below with reference to the accompanying drawings.
- [57] FIG. 1 is a block diagram illustrating a fingerprint recognition device 1a according to an embodiment of the present disclosure. FIG. 2 is a block diagram illustrating a fingerprint recognition device 1b according to another embodiment of the present disclosure. FIG. 3 illustrates switch control signals applied to the fingerprint recognition device 1a or 1b illustrated in FIG. 1 or 2.
- [58] Referring to FIG. 1, the fingerprint recognition device 1a may include a first clock generator 10, a second clock generator 20, a bezel driver 30, a bezel 40a, a sensor cell array 50, a Y-drive part 60, an X-drive part 70, a counter 80, an X-multiplexer (XMUX) 90, and an analog-to-digital converter (ADC) 100.
- The first clock generator 10 may generate a first clock signal  $\phi 1$  and/or a second clock signal  $\phi 2$  in synchronization with a system clock CLK. Furthermore, the first clock generator 10 may generate a first clock bar signal  $\frac{1}{\phi} 1$  and/or a second clock bar signal  $\frac{1}{\phi} 2$ .
- Here, as illustrated in FIG. 3, the first and second clock signals  $\varphi 1$  and  $\varphi 2$  may not overlap with each other. The first clock bar signal  $\frac{1}{\phi 1}$  is an inverted version of the first clock signal  $\varphi 1$ , and the second clock bar signal  $\frac{1}{\phi 2}$  is an inverted version of the second clock signal  $\varphi 2$ .
- The second clock generator 20 may generate, on the basis of the system clock CLK, a signal clk\_i that is a reset/evaluation pulse having a variable period, and may generate various periods according to a signal PERIOD. The second clock generator 20 receives a signal RESET initially to start to operate.
- The bezel driver 30 may receive the first clock signal  $\phi$ 1 and/or the second clock signal  $\phi$ 2 to output a signal for driving the bezel. Furthermore, the bezel driver 30 may

- receive the first clock bar signal  $\frac{1}{\phi 1}$  and/or the second clock bar signal  $\frac{1}{\phi 2}$  to output a signal for driving the bezel.
- [63] The bezel 40a may be used to directly apply a power input signal to a finger. The bezel 40a may be made of metal, conductive polymers, or electrically conductive objects. As described below, a method in which an operation is performed by directly contacting a finger through the bezel 40a is referred to as a direct method.
- The sensor cell array 50 may be a plurality of sensor plates arranged in a matrix with a unit of one pixel, and may detect capacitance generated according to whether a contacted fingerprint part is a ridge or a valley.
- [65] The Y-drive part 60 may sequentially select and drive sensor cells arranged in each row of the sensor cell array 50. The X-drive part 70 may sequentially select and drive sensor cells arranged in each column of the sensor cell array 50.
- [66] The counter 80 may sequentially activate each sensor cell by increasing values of each row and each column of the sensor cell array 50 in order to detect capacitance of each sensor cell generated from a contacted fingerprint.
- [67] The X-multiplexer 90 may sample/hold, according to an input signal HOLD, a capacitance value sensed from a sensor cell of one pixel selected from the sensor cell array 50. The ADC 100 may convert the capacitance value sampled/held by the X-multiplexer 90 into a digital value.
- [68] A microprocessor, a central processing unit (CPU), an application processor (AP), or the like disposed in the inside or the outside may determine whether the fingerprint part is a ridge or a valley according to the capacitance value converted into the digital value.
- [69] FIG. 2 is a block diagram illustrating the fingerprint recognition device 1b according to another embodiment of the present disclosure. The same elements as described above are referred to by the same reference numerals, and detailed descriptions of the same elements are omitted below.
- [70] The fingerprint recognition device 1b illustrated in FIG. 2 is different from the fingerprint recognition device 1a in that an electrode for applying a power input signal is replaced with a Tx plate 40b which is a top metal of a chip, whereas the bezel 40a is used as an electrode in the fingerprint recognition device 1a. As described below, a method in which a finger is allowed to contact a Tx plate through a passivation layer so as to perform an operation is referred to as a pseudo-direct method.
- [71] FIG. 4 is a timing diagram illustrating operations of the fingerprint recognition devices 1a and 1b according to the embodiments of the present disclosure.
- [72] Referring to FIG. 4, when a signal RESET at a low level is applied to the fingerprint recognition device 1a or 1b, the fingerprint recognition device 1a or 1b starts to

- operate. The signal PERIOD is increased by 1 at an interval of one period.
- [73] The signal CLK\_I may be generated so as to have a variable period by the second clock generator 20 in response to the system clock CLK and/or the signal PERIOD, and may be input to each sensor cell of the sensor cell array 50 to generate a reset/ evaluation pulse. Here, a reset signal may be a precharge signal. Furthermore, the signal CLK\_I may be input to the counter 80.
- [74] When the signal CLK\_I is at a high level, a selected sensor cell may be precharged, and, when the signal CLK\_I is at a low level, the capacitance value of the selected sensor cell may be output.
- [75] During one period of the signal CLK\_I, a voltage value according to the capacitance value of each sensor cell may be sampled/held if the signal HOLD is at a low level.
- [76] FIG. 5 is a circuit diagram of a charge transfer circuit 200a for capacitive sensing according to an embodiment included in the fingerprint recognition device 1a or 1b, and FIG. 6 is a circuit diagram of a charge transfer circuit 200b for capacitive sensing according to another embodiment included in the fingerprint recognition device 1a or 1b.
- [77] FIG. 7 is a timing diagram illustrating switch control signals applied to the charge transfer circuit 200a or 200b for capacitive sensing and an output voltage Vout according to a ridge and a valley of a fingerprint.
- [78] Referring to FIG. 5, the charge transfer circuit 200a for capacitive sensing may include an X-drive part 70, an X-drive line 71, a drive line 61, a variable capacitor Cfinger and a parasitic resistor Rfinger defined between the X-drive line 71 and the drive line 61, a parasitic capacitor Cshield generated between a shielding plate (metal shielding) and a sensor plate described below, and a switched capacitor integrator 210a.
- [79] A first switch MP1 and a fourth switch TG2 may be turned on or off by the first clock signal  $\phi 1$  and the first clock bar signal  $-\frac{1}{\phi} 1$ . A second switch MN1 and a third switch TG1 may be turned on or off by the second clock signal  $-\frac{1}{\phi} 2$ .
- [80] The parasitic resistor Rfinger and the variable capacitor Cfinger connected to each other in series may represent simple modeling of a contacted finger.
- [81] The X-drive part 70 may be disposed between one end of the X-drive line 71 which opposes the variable capacitor Cfinger and a voltage input terminal Vin1. The X-drive part 70 may include the first switch MP1 and the second switch MN1.
- [82] The first switch MP1 may be disposed between one end of the X-drive line 71 which opposes the variable capacitor Cfinger and the voltage input terminal Vin1. One

terminal of the second switch MN1 may be connected to the one end of the X-drive line 71 which opposes the variable capacitor Cfinger, and another terminal of the second switch MN1 may be connected to a ground.

- [83] A preset voltage VDD or GND or a reset voltage may be applied to the voltage input terminal Vin1 and/or the ground. Here, the reset voltage may represent that a bias may be differently established to obtain a desired degree of charge transfer. For example, a first power supply voltage Vin1 and/or a second power supply voltage Vin2 may be input to the voltage input terminal Vin1 and/or the ground.
- [84] Referring to FIG. 7, the first clock signal  $\varphi 1$  and the second clock signal  $\varphi 2$  may adjust the output voltage Vout of the switched capacitor integrator 210a and switches together with the first clock bar signal  $\frac{1}{\phi} 1$  and the second clock bar signal  $\frac{1}{\phi} 2$ .
- As illustrated in FIG. 7, the first and second clock signals  $\varphi 1$  and  $\varphi 2$  may not overlap with each other. The first clock bar signal  $\frac{1}{\phi}1$  is an inverted version of the first clock signal  $\varphi 1$ , and the second clock bar signal  $\frac{1}{\phi}2$  is an inverted version of the second clock signal  $\varphi 2$ .
- [86] Referring back to FIG. 5, as described below, the parasitic capacitor Cshield may be generated between the sensor plate connected to the drive ling 61 and the shielding plate (metal shielding) for blocking a noise generated by a circuit under the sensor plate to improve a touch sensitivity. The circuit under the sensor plate may include the switched capacitor integrator 210a, an active output voltage feedback unit 210b, or other circuits. Here, the other circuits may not related to an operation of extracting the variable capacitor Cfinger from a finger.
- [87] The switched capacitor integrator 210a may be disposed between the voltage output terminal Vout and the other end of the drive line 61 connected to one terminal of the variable capacitor Cfinger.
- The switched capacitor integrator 210a may include the third switch TG1 of which one terminal is connected to the fourth switch TG2 and the driving line 61 and of which another terminal is connected to an inverting input terminal of an operational amplifier 211, the fourth switch TG2 of which one terminal is connected to the drive line 61 and of which another terminal is connected to a reference voltage input terminal Vref, and the operational amplifier 211 of which the inverting input terminal is connected to the other terminal of the third switch TG1 and of which a non-inverting input terminal receives a reference voltage Vref.
- [89] Furthermore, the switched capacitor integrator 210a may include a storage capacitor Cs of which one terminal is connected to the other terminal of the third switch TG1

and the inverting terminal of the operational amplifier 211 and of which another terminal is connected to the voltage output terminal Vout, and a reset switch rst of which one terminal is connected to the other terminal of the third switch TG1, the inverting terminal of the operational amplifier 211, and the one terminal of the storage capacitor Cs and of which another terminal is connected to the voltage output terminal Vout and the other terminal of the storage capacitor Cs.

- [90] In general, charges flow from a high-voltage side to a low-voltage side until voltages of both the sides are equalized. Therefore, it may be required to charge the parasitic capacitor Cshield so that a voltage vp of the drive line 61 is equal to a voltage vg of the inverting input terminal of the operational amplifier 211, in order to avoid the parasitic effect of the parasitic capacitor Cshield generated between the shielding plate (metal shielding) and the sensor plate connected to the drive line 61 as described below, when charges are transferred from the variable capacitor Cfinger to the storage capacitor Cs.
- When the first clock signal  $\phi 1$  is turned on, an output node of the parasitic capacitor Cshield is charged with the reference voltage Vref. The inverting input terminal of the operational amplifier 211 is virtually short-circuited with the non-inverting input terminal to which the reference voltage Vref is input.
- [92] Therefore, when charges are transferred from the variable capacitor Cfinger to the storage capacitor Cs, the output node voltage vp of the drive line 61 is equal to the inverting input node voltage vg of the operational amplifier 211, and thus no charges are transferred from the parasitic capacitor Cshield to the storage capacitor Cs. As a result, charges stored in the parasitic capacitor Cshield of the drive line 61 are unable to affect an output voltage, and the parasitic effect of the parasitic capacitor Cshield of the drive line 61 may be avoided.
- [93] A transfer function of the charge transfer circuit 200 for capacitive sensing according to an embodiment of the present disclosure is expressed as Equation 1.

[94] 
$$\mathcal{H}(z) = \frac{C_f}{C_S} \cdot \frac{1}{z - 1}$$
 (Equation 1)

- [95] Where z denotes a parameter of z-transform, Cf denotes a capacitance of the variable capacitor Cfinger, and Cs denotes a capacitance of the storage capacitor Cs.
- The storage capacitor Cs may integrate charges transferred from the variable capacitor Cfinger at a rising time of the second clock signal  $\varphi 2$ . Here, a gradient of an integral value varies with a capacitance value of the variable capacitor Cfinger. The capacitance value of the variable capacitor Cfinger is high at a ridge and is low at a valley.
- [97] Therefore, as illustrated in FIG. 7, the output voltage Vout of the operational amplifier 211 which starts from the reference voltage Vref more increases at a ridge

than at a valley as the number of clocks increases.

- [98] FIG. 6 is a circuit diagram of the charge transfer circuit 200b for capacitive sensing according to another embodiment of the present disclosure included in the fingerprint recognition device 1a or 1b. The same elements as described above are referred to by the same reference numerals, and detailed descriptions of the same elements are omitted below.
- [99] Differences between the charge transfer circuit 200b for capacitive sensing of FIG. 6 and the above-mentioned charge transfer circuit 200a for capacitive sensing are described below.
- [100] The non-inverting input terminal of the operation amplifier 211 included in the active output voltage feedback unit 210b may be connected to each one terminal of the third switch TG1, the storage capacitor Cs, and the reset switch rst, and the other terminals of the storage capacitor Cs and the reset switch rst may be connected to the ground. The other terminal of the third switch TG1 may be connected to one terminal of the fourth switch TG2 and one terminal of the parasitic terminal Cshield.
- [101] A buffer circuit unit 212 may be a voltage follower in which the inverting input terminal of the operational amplifier 211 is connected to the output terminal thereof.
- The inverting input terminal of the operational amplifier 211 may be connected to the output terminal thereof and the other terminals of the parasitic capacitor Cshield and the fourth switch TG2. Accordingly, the output voltage Vout may be supplied to the voltage follower and may be fed back to the fourth switch TG2 and the parasitic capacitor Cshield, thereby preventing charges from being transferred from the parasitic capacitor Cshield. When the first clock signal φ1 is at a high level at which the first switch MP1 and the fourth switch TG2 are turned on, the parasitic capacitor Cshield may be charged such that the voltage vp of the drive line 61 is equalized to the input terminal voltage vg of the buffer circuit by a feedback output voltage generated by the voltage follower of the input terminal of the buffer circuit including the operational amplifier 211. As a result, the charges stored in the parasitic capacitor Cshield are unable to affect the output voltage. A circuit for performing such operations is referred to as the active output voltage feedback unit 210b in the present disclosure.
- [103] FIG. 8 is a schematic diagram illustrating a situation in which the charge transfer circuit 200a for capacitive sensing of FIG. 5 is used in the fingerprint recognition device 1a based on the direct method of FIG. 1.
- [104] Referring to FIG. 8, the first clock bar signal  $\frac{1}{\phi}$  is an inverted version of the first clock signal  $\phi$ 1, and the second clock bar signal  $\frac{1}{\phi}$ 2 is an inverted version of the second clock signal  $\phi$ 2. The first switch MP1 is a P-channel metal-oxide semi-

conductor (PMOS) transistor, and the second switch MN1 is an N-channel MOS (NMOS) transistor. The third switch TG1 and the fourth switch TG2 are transmission gates in which a PMOS transistor and an NMOS transistor are connected to each other in parallel.

- [105] The first switch MP1 and the fourth switch TG2 may be turned on or off by the first clock signal  $\phi$ 1 or the first clock bar signal  $\frac{1}{\phi}$ 1. The second switch MN1 and the
  - third switch TG1 may be turned on or off by the second clock signal  $\varphi$ 2 or the second clock bar signal  $\frac{1}{2}$ .
- [106] A shielding plate (metal shielding) 500 may block a noise generated by a circuit under a sensor plate 400, thereby improving the touch sensitivity. The circuit under the sensor plate may include the switched capacitor integrator 210a or other circuits not related to an operation of extracting the variable capacitor Cfinger from a finger.
- [107] Here, the parasitic capacitor Cshield may be generated between the sensor plate 400 and the shielding plate 500. For example, the parasitic capacitor Cshield may have a value between several tens of fF and several hundreds of fF according to a sensor cell size.
- [108] As described above with reference to FIG. 5, it may be required for the active output voltage feedback unit 210b to charge the parasitic capacitor Cshield so that the voltage vp of the drive line 61 is equal to the voltage vg of the inverting input terminal of the operational amplifier 211, in order to avoid the parasitic effect of the parasitic capacitor Cshield generated between the shielding plate (metal shielding) and the sensor plate connected to the drive line 61.
- When the first clock signal  $\phi 1$  is turned on, the output node of the parasitic capacitor Cshield is charged with the reference voltage Vref. The inverting input terminal of the operational amplifier 211 is virtually short-circuited with the non-inverting input terminal to which the reference voltage Vref is input.
- [110] Therefore, when charges are transferred from the variable capacitor Cfinger to the storage capacitor Cs, the output node voltage vp of the drive line 61 is equal to the inverting input node voltage vg of the operational amplifier 211, and thus the parasitic effect of the parasitic capacitor Cshield may be avoided.
- [111] The bezel 40a may contact a finger to directly apply the power input signal Vin1 or Vin2. As described above, the method in which an operation is performed by directly contacting a finger through the bezel is referred to as the direct method.
- [112] The bezel 40a may be made of metal, conductive polymers, or electrically conductive objects.
- [113] As illustrated in FIG. 8, a finger may be simply modeled as the variable capacitor

Cfinger and the parasitic resistor Rfinger connected to each other in series. Here, the variable capacitor Cfinger may be a ridge capacitor Cridge or a valley capacitor Cvalley.

- [114] The sensor plate 400 may be separated from a finger by a passivation layer. Therefore, the finger capacitor Cfinger may include an air capacitor Cair between a chip surface and a finger skin and a passivation layer capacitor Cpass between the sensor plate and the chip surface, which are connected to each other in series.
- [115] The power input signal Vin1 or Vin2 driven by a driver of the X-drive part 70 is directly introduced to a finger via a bezel contact.
- [116] Charges accumulated in the finger capacitor Cfinger may be transferred to the storage capacitor Cs. The finger capacitor Cfinger may have different values depending on the ridge capacitor Cridge or the valley capacitor Cvalley.
- The valley capacitor Cvalley corresponds to the air capacitor Cair between a chip [117]surface and a finger skin and the passivation layer capacitor Cpass between the sensor plate 400 and the chip surface, which are connected to each other in series, whereas the ridge capacitor Cridge corresponds to the passivation layer capacitor Cpass between the sensor plate 400 and the chip surface. This may be expressed as an equation as below.

[118] 
$$C_{ridge} = C_{pass}^{\text{(Equation 2)}}$$

[118] 
$$C_{\textit{ridge}} = C_{\textit{pass}}^{\text{(Equation 2)}}$$
 
$$C_{\textit{val/ey}} = \frac{C_{\textit{air}} \cdot C_{\textit{pass}}}{C_{\textit{air}} + C_{\textit{pass}}}^{\text{(Equation 3)}}$$

A variation of the finger capacitor Cfinger defined as a difference between the ridge [120] capacitor Cridge and the valley capacitor Cvalley may be expressed as an equation as below.

[121] 
$$\Delta C_{\textit{finger}} = C_{\textit{ridge}} - C_{\textit{valley}} \quad ^{\text{(Equation 4)}}$$

- [122] The parasitic capacitor Cshield generated between the sensor plate 400 and the shielding plate 500 may be electrically connected to one terminal of the fourth switch TG2 and the non-inverting input terminal of the operational amplifier 211. Here, the reference voltage Vref may be input to the non-inverting input terminal.
- Therefore, when the fourth switch TG2 is turned on, a voltage of the senor plate 400 [123] is equalized to a voltage of the shielding plate 500 by the reference voltage Vref input to the non-inverting input terminal of the operational amplifier 211, and thus the parasitic capacitor Cshield may be effectively removed from the drive line 61. Therefore, the output voltage Vout per single charge transfer of the charge transfer

circuit for capacitive sensing of the present disclosure may be expressed as below.

[124] 
$$V_{out}(t) \cong -\frac{C_{finger}}{C_{finger} + C_{S}} V_{dd}$$
 (Equation 5)

[125] Where the capacitor Cfinger is the ridge capacitor Cridge or the valley capacitor Cvalley. A transfer function with a parameter z may be defined as below.

[126] 
$$H(Z) = -\frac{C_{finger}}{C_{finger} + C_S} \frac{1}{Z - 1}$$
 (Equation 6)

[127] Output voltages of the ridge capacitor Cridge and the valley capacitor Cvalley may be obtained from Equation 5, and a difference between the output voltages of the ridge capacitor Cridge and the valley capacitor Cvalley may be defined as below.

[128] 
$$V_{diff} = \left(\frac{C_{ridge}}{C_{ridge} + C_S} - \frac{C_{valley}}{C_{valley} + C_S}\right) V_{dd}$$
 (Equation 7)

[129] As a result, a sense voltage Vsense which is the difference between the output voltages of the ridge capacitor Cridge and the valley capacitor Cvalley is defined as below after nth integration.

[130] 
$$V_{sense} = n \cdot V_{diff}$$
 (Equation 8)

- [131] FIG. 9 is a schematic diagram illustrating a situation in which the charge transfer circuit 200b for capacitive sensing of FIG. 6 is used in the fingerprint recognition device 1a based on the direct method of FIG. 1. The same elements as described above are referred to by the same reference numerals, and detailed descriptions of the same elements are omitted below.
- The active output voltage feedback unit 210b is operated in the same manner as described above with reference to FIG. 6. That is, when the first clock signal  $\phi 1$  is at a high level at which the first switch MP1 and the fourth switch TG2 are turned on, the parasitic capacitor Cshield may be charged such that the voltage vp of the drive line 61 is equalized to the input terminal voltage vg of the buffer circuit by a feedback output voltage generated by the voltage follower of the input terminal of the buffer circuit including the operational amplifier 211. Therefore, the parasitic capacitor Cshield may be removed.
- [133] FIG. 10 is a schematic diagram illustrating a situation in which the charge transfer circuit 200a for capacitive sensing of FIG. 5 is used in the fingerprint recognition

device 1b based on the pseudo-direct method of FIG. 1. The same elements as described above are referred to by the same reference numerals, and detailed descriptions of the same elements are omitted below.

- [134] The fingerprint recognition device 1b illustrated in FIG. 10 is different from the fingerprint recognition device 1a in that an electrode for transferring the power input signal Vin1 or Vin2 is replaced with the Tx plate 40b which is a top metal of a chip, whereas the bezel 40a is used as an electrode in the fingerprint recognition device 1a. As described above, the method in which a finger is allowed to contact a Tx plate through a passivation layer so as to perform an operation is referred to as the pseudo-direct method.
- [135] Here, a passivation layer capacitor Cperi may be generated due to a passivation layer between a Tx plate 300b and a finger. As illustrated in FIG. 10, the passivation layer capacitor Cperi may be connected to the capacitor Cfinger and a ground node through a finger and a resistor.
- [136] Therefore, the passivation layer capacitor Cperi may be connected in series to the finger capacitor Cfinger, and a total capacitance Ctotal may be expressed as an equation as below.

[137] 
$$C_{total} = \frac{C_{peri}C_{finger}}{C_{peri} + C_{finger}}$$
(Equation 9)

- It may be understood that the total capacitance Ctotal generally follows the finger capacitor Cfinger on the assumption that the value of the passivation layer capacitor Cperi is larger than that of the finger capacitor Cfinger. If the size of the Tx plate is sufficiently larger than the sensor cell size, a change of the finger capacitor Cfinger due to the passivation layer capacitor Cperi may be substantially ignored. Furthermore, since the pseudo-direct method of the present disclosure is based on an active output voltage feedback integrator, a voltage output range may be an entire interval of a power supply voltage.
- [139] FIG. 11 is a schematic diagram illustrating a situation in which the charge transfer circuit 200b for capacitive sensing of FIG. 6 is used in the fingerprint recognition device 1b based on the pseudo-direct method of FIG. 1.
- [140] The same elements as described above are referred to by the same reference numerals, and detailed descriptions of the same elements are omitted below.
- [141] Since the pseudo-direct method is used, the Tx plate 40b which is a top metal transfers the power input signal Vin1 or Vin2 to a finger contacted via a passivation layer, unlike the method in which a bezel is used as an electrode. The circuit operation is the same as described above with reference to FIG. 6.

[142] FIG. 12 is a layout top-view of the fingerprint recognition device based on the pseudo-direct method of FIG. 2.

[143] The Tx plate which is a top metal surrounds the exterior of a chip. The Tx plate may be spaced apart from a sensor cell block such that a gap capacitor Cgap is sufficiently small, thereby preventing an input signal applied to a Tx electrode from being directly transferred to a sensor cell array. This gap may be appropriately adjusted according to a thickness of the passivation layer.

### **Claims**

[Claim 1] A charge transfer circuit for capacitive sensing, the charge transfer circuit comprising:

a variable capacitor defined through a sensor plate connected to one end of a drive line and one end of an X-drive line;

an X-drive part disposed between a voltage input terminal and another end of the X-drive line opposing the variable capacitor;

a switched capacitor integrator disposed between a voltage output terminal and another end of the drive line of which the one end is connected to the variable capacitor; and

a shielding plate connected to a first input terminal of the switched capacitor integrator,

wherein the first input terminal of the switched capacitor integrator is connected to the other end of the drive line.

The charge transfer circuit of claim 1, wherein the first input terminal of the switched capacitor integrator receives a reference voltage.

The charge transfer circuit of claim 1, wherein the sensor plate and the shielding plate have a parasitic capacitor therebetween.

The charge transfer circuit of claim 1, wherein the switched capacitor integrator comprises:

an operational amplifier;

a third switch of which one terminal is connected to the other end of the drive line and of which another terminal is connected to an inverting input terminal of the operational amplifier;

a fourth switch of which one terminal is connected to the other end of the drive line and the one terminal of the third switch and of which another terminal is connected to a non-inverting input terminal of the operational amplifier and the shielding plate;

a storage capacitor of which one terminal is connected to the other terminal of the third switch and the inverting input terminal of the operational amplifier and of which another terminal is connected to an output terminal of the operational amplifier; and

a reset switch of which one terminal is connected to the other terminal of the third switch, the inverting input terminal of the operational amplifier, and the one terminal of the storage capacitor and of which another terminal is connected to the output terminal of the operational amplifier and the other terminal of the storage capacitor,

[Claim 2]

[Claim 3]

[Claim 4]

wherein the non-inverting input terminal of the operational amplifier is connected to the other end of the drive line and the shielding plate. [Claim 5] The charge transfer circuit of claim 1, wherein the X-drive part comprises: a first switch configured to be turned on by a first clock signal and turned off by a second clock signal; and a second switch configured to be turned off by the first clock signal and turned on by the second clock signal. [Claim 6] The charge transfer circuit of claim 1, wherein the X-drive part comprises: a first switch configured to be turned on by a second clock bar signal and turned off by a first clock bar signal; and a second switch configured to be turned off by the second clock bar signal and turned on by the first clock bar signal. [Claim 7] The charge transfer circuit of claim 5, wherein the first clock signal and the second clock signal do not overlap with each other. The charge transfer circuit of claim 1, wherein a preset voltage or a [Claim 8] reset voltage is applied to the voltage input terminal. [Claim 9] A charge transfer circuit for capacitive sensing, the charge transfer circuit comprising: a variable capacitor defined through a sensor plate connected to one end of a drive line and one end of an X-drive line; an X-drive part disposed between a voltage input terminal and another end of the X-drive line opposing the variable capacitor; an active output voltage feedback unit disposed between a voltage output terminal and another end of the drive line of which the one end is connected to the variable capacitor; and a shielding plate connected to an output terminal of the active output voltage feedback unit, wherein the output terminal of the active output voltage feedback unit opposing the one end of the drive line is connected to the other end of the drive line. [Claim 10] The charge transfer circuit of claim 9, wherein the active output voltage feedback unit comprises: a third switch and a fourth switch connected in parallel to the other end of the drive line; a buffer circuit unit connected to one terminal of the third switch opposing the drive line;

> a storage capacitor of which one terminal is connected between the one terminal of the third switch and an input terminal of the buffer circuit unit and of which another terminal is grounded; and a reset switch of which one terminal is connected to the one terminal of the third switch, the input terminal of the buffer circuit unit, and the storage capacitor and of which another terminal is grounded, wherein an output terminal of the buffer circuit unit opposing the third switch is connected to the other end of the drive line.

[Claim 11] The charge transfer circuit of claim 10,

> wherein the third switch is turned off by a first clock signal and turned on by a second clock signal, and wherein the fourth switch is turned on by the first clock signal and

turned off by the second clock signal.

The charge transfer circuit of claim 10, [Claim 12]

> wherein the third switch is turned off by a second clock bar signal and turned on by a first clock bar signal, and

wherein the fourth switch is turned on by the second clock bar signal and turned off by the first clock bar signal.

[Claim 13] The charge transfer circuit of claim 11, wherein the first clock signal and the second clock signal do not overlap with each other.

> The charge transfer circuit of claim 10, wherein the buffer circuit unit is an operational amplifier.

> The charge transfer circuit of claim 14, wherein a non-inverting input terminal of the operational amplifier is connected to the one terminal of the third switch, and an inverting input terminal of the operational amplifier is connected between an output terminal of the operational amplifier and the fourth switch.

A fingerprint recognition device comprising:

a charge transfer circuit for capacitive sensing, the charge transfer circuit comprising:

a variable capacitor defined through a sensor plate connected to one end of a drive line and one end of an X-drive line;

an X-drive part disposed between a voltage input terminal and another end of the X-drive line opposing the variable capacitor;

a switched capacitor integrator disposed between a voltage output terminal and another end of the drive line of which the one end is connected to the variable capacitor; and

a shielding plate connected to a first input terminal of the switched

[Claim 14]

[Claim 15]

[Claim 16]

capacitor integrator, wherein the first input terminal of the switched capacitor integrator is connected to the other end of the drive line; and a bezel of which one end is connected to the one end of the X-drive line and of which another end is directly contactable by a finger.

[Claim 17]

A fingerprint recognition device comprising:

a charge transfer circuit for capacitive sensing, the charge transfer circuit comprising:

a variable capacitor defined through a sensor plate connected to one end of a drive line and one end of an X-drive line;

an X-drive part disposed between a voltage input terminal and another end of the X-drive line opposing the variable capacitor;

an active output voltage feedback unit disposed between a voltage output terminal and another end of the drive line of which the one end is connected to the variable capacitor; and

a shielding plate connected to an output terminal of the active output voltage feedback unit, wherein the output terminal of the active output voltage feedback unit opposing the one end of the drive line is connected to the other end of the drive line; and

a bezel of which one end is connected to the one end of the X-drive line and of which another end is directly contactable by a finger.

The fingerprint recognition device of claim 16, wherein the bezel is made of metal or conductive polymers.

A fingerprint recognition device comprising:

a charge transfer circuit for capacitive sensing, the charge transfer circuit comprising:

a variable capacitor defined through a sensor plate connected to one end of a drive line and one end of an X-drive line;

an X-drive part disposed between a voltage input terminal and another end of the X-drive line opposing the variable capacitor;

a switched capacitor integrator disposed between a voltage output terminal and another end of the drive line of which the one end is connected to the variable capacitor; and

a shielding plate connected to a first input terminal of the switched capacitor integrator, wherein the first input terminal of the switched capacitor integrator is connected to the other end of the drive line; and a top metal of which one end is connected to the one end of the X-drive line and of which another end is contactable by a finger through a passivation layer.

[Claim 18]

[Claim 19]

[Claim 20] A fingerprint recognition device comprising:

a charge transfer circuit for capacitive sensing, the charge transfer circuit comprising:

a variable capacitor defined through a sensor plate connected to one end of a drive line and one end of an X-drive line;

an X-drive part disposed between a voltage input terminal and another end of the X-drive line opposing the variable capacitor;

an active output voltage feedback unit disposed between a voltage output terminal and another end of the drive line of which the one end is connected to the variable capacitor; and

a shielding plate connected to an output terminal of the active output voltage feedback unit, wherein the output terminal of the active output voltage feedback unit opposing the one end of the drive line is connected to the other end of the drive line; and

a top metal of which one end is connected to the one end of the X-drive line and of which another end is contactable by a finger through a passivation layer.

The fingerprint recognition device of claim 19, wherein the top metal is spaced apart from another top metal so that the one end of the top metal is only connected to the one end of the X-drive line and the other end of the top metal is contactable by the finger through the passivation layer.

A fingerprint sensing method comprising:

receiving capacitances of a ridge and a valley of a fingerprint; integrating the received capacitances according to a variable clock; sampling or holding the integrated capacitances;

converting the sampled or held capacitances into digital values; and determining whether a fingerprint part is the ridge or the valley on the basis of the digital values converted according to a difference in the capacitances of the ridge and the valley.

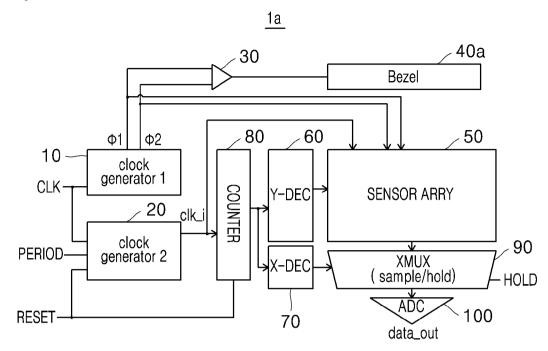
The fingerprint sensing method of claim 22, wherein the integrating the received capacitances according to the variable clock is discrete-time integrating.

[Claim 21]

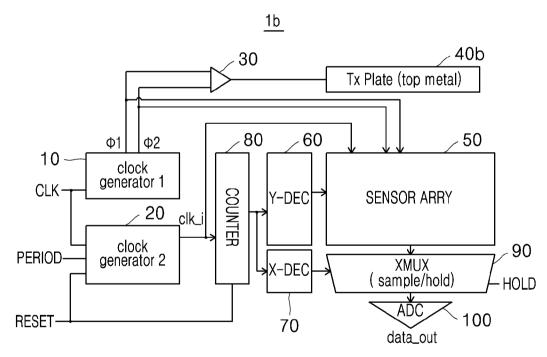
[Claim 22]

[Claim 23]

[Fig. 1]

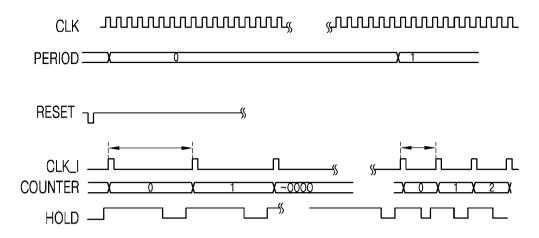


[Fig. 2]

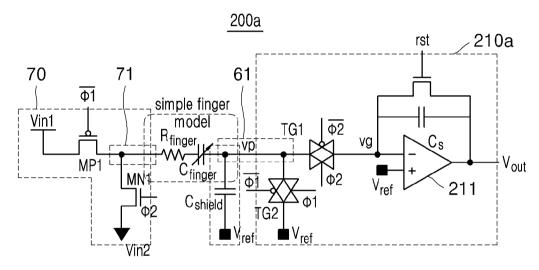


[Fig. 3]  $\begin{array}{c} \Phi 1 \\ \hline \Phi 1 \\ \hline \end{array}$   $\begin{array}{c} \Phi 2 \\ \hline \hline \hline \Phi \overline{2} \\ \end{array}$ 

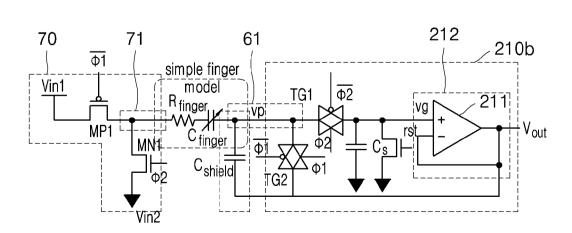




[Fig. 5]

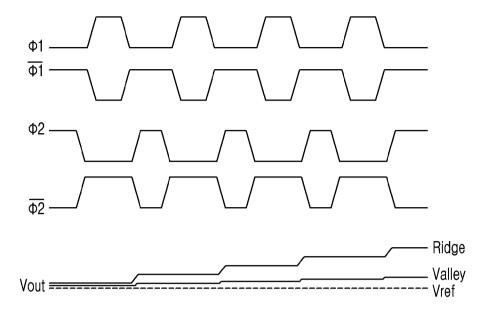


[Fig. 6]

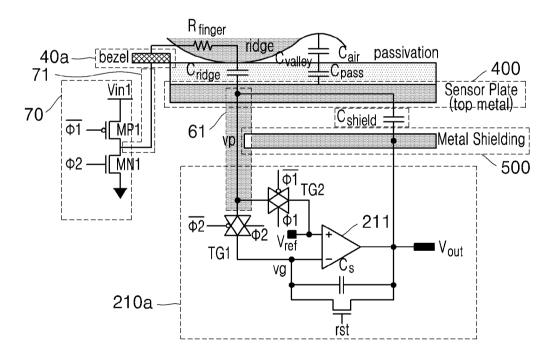


200b

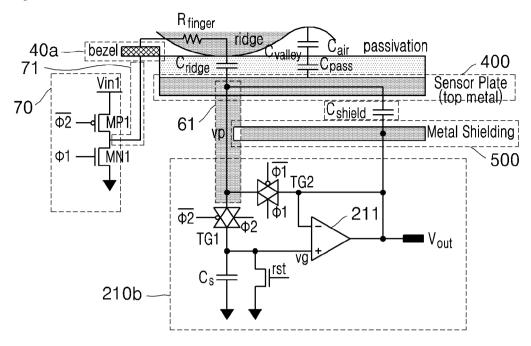




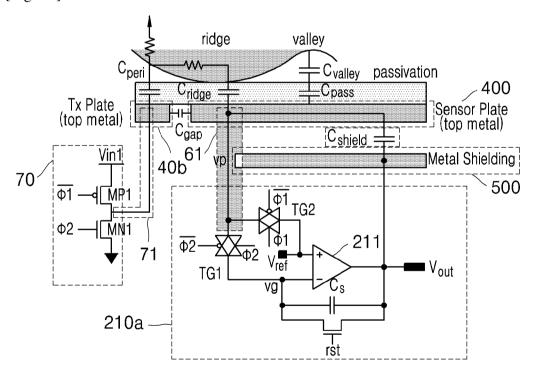
[Fig. 8]



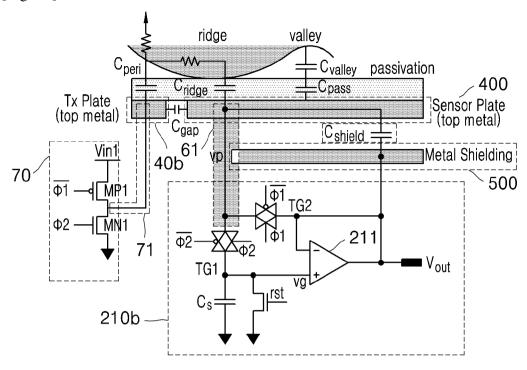
[Fig. 9]



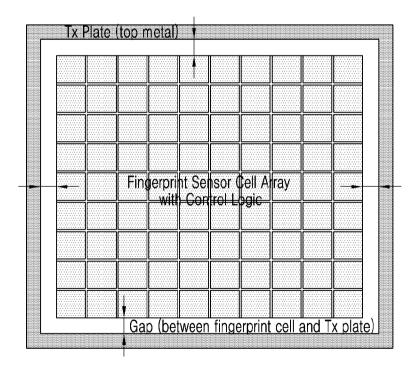
[Fig. 10]



[Fig. 11]



[Fig. 12]



International application No. **PCT/KR2015/011623** 

#### A. CLASSIFICATION OF SUBJECT MATTER

H03K 17/955(2006.01)i, G06K 9/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

#### B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols) H03K 17/955; G06F 3/044; G01R 27/26; G06K 9/00; G09G 3/20; H01L 25/00; G06F 3/041

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: fingerprint, sensor, voltage, drive, capacitor, capacitance, parasitic, polymer, bezel, metal, integrator

#### C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004-0222803 A1 (MARCO TARTAGNI) 11 November 2004 See paragraphs [0019]-[0042] and figures 1-6.	22-23
Y A	see paragraphs [0013] [0042] and Figures 1 0.	1-9,16-21 10-15
Y	US 2008-0069413 A1 (FRANK ROBERT RIEDIJK et al.) 20 March 2008 See paragraphs [0038]-[0058] and figures 1-3.	1-9,16-21
Y	KR 10-2003-0073508 A (HYNIX SEMICONDUCTOR INC.) 19 September 2003 See pages 3-4 and figures 1-5.	4
A	US 2014-0062957 A1 (N-TRIG LTD.) 06 March 2014 See abstract, paragraphs [0119]-[0172] and figures 1A-3.	1-23
A	KR 10-2013-0095427 A (SESIM. LTD.) 28 August 2013 See abstract, paragraphs [0038]-[0050] and figures 11-15.	1-23

	Further documents are listed in the continuation of Box C.		See patent family annex.
*	Special categories of cited documents:	"T"	
"A"	document defining the general state of the art which is not considered to be of particular relevance		date and not in conflict with the application but cited to understand
	1		the principle or theory underlying the invention
"E"	earlier application or patent but published on or after the international	"X"	" document of particular relevance; the claimed invention cannot be
	filing date		considered novel or cannot be considered to involve an inventive
"L"	document which may throw doubts on priority claim(s) or which is		step when the document is taken alone
	cited to establish the publication date of another citation or other	"Y"	" document of particular relevance; the claimed invention cannot be
	special reason (as specified)		considered to involve an inventive step when the document is
"O"	document referring to an oral disclosure, use, exhibition or other		combined with one or more other such documents, such combination
	means		being obvious to a person skilled in the art
"P"	document published prior to the international filing date but later	"&"	
	than the priority date claimed		• •
Date	of the actual completion of the international search	Date	te of mailing of the international search report

Date of the actual completion of the international search	Date of mailing of the international search report		
29 February 2016 (29.02.2016)	29 February 2016 (29.02.2016)		
Name and mailing address of the ISA/KR	Authorized officer		
International Application Division			
Korean Intellectual Property Office	KIM, Sung Gon		
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea			

Telephone No. +82-42-481-8746

Form PCT/ISA/210 (second sheet) (January 2015)

Facsimile No. +82-42-472-7140

### INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

# PCT/KR2015/011623

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004-0222803 A1	11/11/2004	EP 0790479 A1 EP 0790479 B1	20/08/1997 16/01/2002
		EP 0942259 A1 EP 0942259 B1 JP 11-316105 A US 2002-0097059 A1	15/09/1999 10/11/2004 16/11/1999 25/07/2002
		US 2002-0180464 A1 US 6114862 A US 6320394 B1	05/12/2002 05/09/2000 20/11/2001
		US 6362633 B1 US 6437583 B1 US 6496021 B2	26/03/2002 20/08/2002 17/12/2002
		US 6731120 B2 US 6998855 B2	04/05/2004 14/02/2006
US 2008-0069413 A1	20/03/2008	DE 602004017911 D1 EP 1766547 A1 EP 1766547 B1	02/01/2009 28/03/2007 19/11/2008
		JP 04604087 B2 JP 2008-502989 A US 7864992 B2	22/12/2010 31/01/2008 04/01/2011
VD 10 0000 0070500 A	10 /00 /0000	WO 2005-124659 A1	29/12/2005
KR 10-2003-0073508 A US 2014-0062957 A1	19/09/2003 06/03/2014	KR 10-0431750 B1 AT 471501 T	17/05/2004 15/07/2010
05 2011 0002301 M1	00/00/2011	CN 100538292 C CN 101261561 A	09/09/2009 10/09/2008
		CN 102156571 A CN 102156571 B CN 1771430 A	17/08/2011 24/07/2013 10/05/2006
		DE 202004021638 U1 DE 602004027705 D1 EP 1592953 A2	31/12/2009 29/07/2010 09/11/2005
		EP 1592953 A4 EP 1592953 B1	31/12/2008 16/06/2010
		EP 2128580 A1 JP 04540663 B2 JP 2006-517319 A	02/12/2009 08/09/2010 20/07/2006
		KR 10-1060210 B1 KR 10-2005-0101204 A US 2004-155871 A1	29/08/2011 20/10/2005 12/08/2004
		US 2007-171211 A1 US 2008-218494 A1 US 2012-162131 A1	26/07/2007 11/09/2008 28/06/2012
		US 2012-293458 A1 US 2013-113707 A1 US 7372455 B2	22/11/2012 09/05/2013 13/05/2008
		US 7372455 B2 US 7843439 B2	13/05/2008 30/11/2010

### INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

# PCT/KR2015/011623

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 8228311 B2 US 8373677 B2 US 8400427 B2 US 8593433 B2 US 8952930 B2	24/07/2012 12/02/2013 19/03/2013 26/11/2013 10/02/2015
		WO 2004-070396 A2 WO 2004-070396 A3	19/08/2004 14/04/2005
KR 10-2013-0095427 A	28/08/2013	KR 10-1438454 B1	12/09/2014