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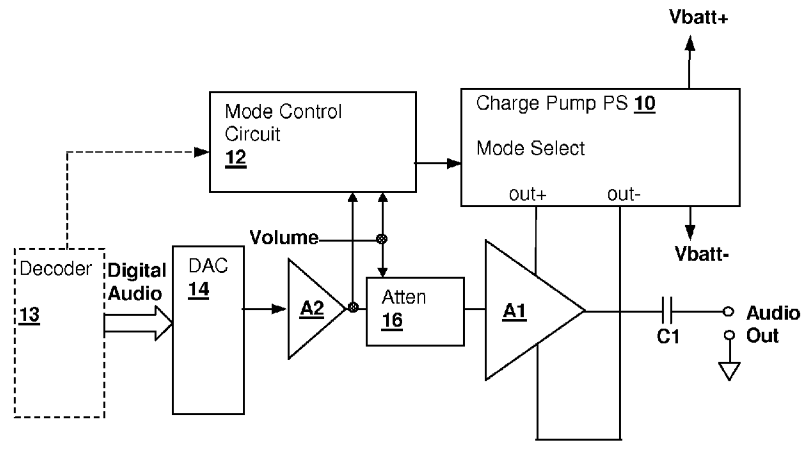

(57) Abstract: An energy-efficient consumer device audio power output stage provides improved battery life and reduced power dissipation. A power supply having a selectable operating mode supplies the power supply rails to the power amplified output stage. The operating mode is controlled in conformity with the audio signal level, which may be determined from a volume control setting of the device and/or from a signal level detector that determines the amplitude of the signal being amplified. The power supply may be a charge pump in which the operating mode uses a capacitive divider to provide for selection of a power supply output voltage that is a rational fraction of the power supply output voltage in a full-voltage operating mode.

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ENERGY-EFFICIENT CONSUMER DEVICE AUDIO POWER OUTPUT STAGE

FIELD OF THE INVENTION

[0001] The present invention relates generally to consumer device audio power output stages, and more specifically, to a audio power stage using a selectable-voltage charge-pump to conserve energy.

BACKGROUND OF THE INVENTION

[0002] In battery-operated consumer audio devices, the power amplifier output, which is generally utilized to drive a pair of headphones or a speaker can be the primary consumer of battery power. In devices having a linear power amplifier for the output stage, power is wasted during low signal level outputs, since the voltage drop across the active output transistor plus the output voltage will be equal to the constant power supply rail voltage.

[0003] Even though the current in the transducer is reduced at low signal amplitudes, more power is still wasted by dissipation in the output transistors than is delivered to the load. Battery power is typically only reduced in linear amplifier circuits by lowering the power supply voltage, which limits the available output power and also may not be possible in some applications in which the power amplifier output also serves as a line output signal that must provide a specified signal level at full signal level, for example +5dBm (15dB over -10dBm) as referenced into a 600 ohm load, which requires a signal swing of $3V_{p-p}$.

[0004] Therefore, it would be desirable to provide a power amplifier circuit for a consumer audio device that has improved efficiency and reduced power dissipation, while maintaining a specified full-signal output level capability.

DISCLOSURE OF THE INVENTION

[0005] The above stated objectives of providing improved efficiency and reduced power dissipation is achieved in a linear power amplifier circuit for a consumer audio device and its method of operation.

[0006] The power amplifier circuit includes a charge pump power supply that has a selectable operating mode, so that in a first mode of operation, the power supply produces a power supply voltage that is a rational fraction of the power supply voltage in a second operating mode. A capacitive voltage divider formed by switching a series combination of capacitors to the input terminals and one of the capacitors to one of the output terminals to provide a fraction of the input voltage at that output terminal. The power supply may be a uni-polar (single-ended) power supply, or may have a bipolar output substantially symmetrical about a reference level, which is generally one of the input power supply terminals.

[0007] The foregoing and other objectives, features, and advantages of the invention will be apparent from the following, more particular, description of the preferred embodiment of the invention, as illustrated in the accompanying drawings.

DESCRIPTION OF THE DRAWINGS

[0008] **Figure 1** is a schematic diagram depicting an audio output stage of a consumer audio device in accordance with an embodiment of the invention.

[0009] **Figure 2** is a schematic diagram depicting a charge-pump power supply **10** of **Figure 1** and in accordance with an embodiment of the invention.

[0010] **Figures 3A-3D** are schematic diagrams depicting the individual charge-pump clock phases for each operating mode of the charge-pump power supply circuit of **Figure 2.**

[0011] **Figure 4** is a schematic diagram depicting an amplifier control circuit in accordance with an embodiment of the invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0012] The present invention encompasses an audio power amplifier stage for a consumer audio device, and a charge-pump power supply for supplying the power supply rails of at least the final power amplifier stage. The voltage of the power supply provided to the final amplifier stage is selectable and is set in conformity with either an expected or actual signal level of the audio signal being amplified, so that at signal amplitudes that do not require the maximum power supply voltage, the power supply voltage is reduced to conserve power. For example, when amplifying a signal having typical maximum amplitude -6dB below occasional peaks referenced at 0dB, the power supply voltage of the final amplifier stage can be reduced by a factor of two during intervals between the above-described peaks, without causing clipping. The result is a potential reduction in power consumption by a factor of four and a reduction in power dissipation by at least that factor over that of an amplifier that does not have a selectable power supply. The charge pump power supply provides a simple selectable-voltage power supply implementation that reduces the power supply voltage by a rational factor, by employing a capacitive divider that divides the input supply voltage and then applies at least one of the divided voltages to the output of the power supply to provide the reduced voltage.

[0013] Referring now to **Figure 1**, a consumer audio device audio output stage is depicted in accordance with an embodiment of the present invention. A digital-to-analog converter (DAC) **14** supplies an analog signal to a first amplifier stage **A2** that is operated from a fixed voltage power supply. The input to DAC **14**

may optionally be provided by a decoder **13**, that decodes a file or stream data source such as an MP3 encoded data stream. The signal at the output of first amplifier stage **A2** is provided to an attenuator **16** that receives a volume control signal and attenuates the signal accordingly. Attenuator **16** may be a digital potentiometer having control provided from a microcontroller or other digital control circuit responsive to a user interface, volume knob encoder or program command, or attenuator **16** may be an analog potentiometer that provides the volume control signal as an output indication from a secondary deck (separate potentiometer circuit coupled to the common shaft or other mechanism) for use in the power supply control algorithms described below. While an attenuator **16** is shown as the volume control mechanism, it is understood that an equivalent volume control may be provided by a programmable resistor in the feedback of amplifier **A2** or another amplifier stage in the signal path. A final power amplifier stage **A2** amplifies the signal received from attenuator **16** and provides an audio output signal, which may operate a speaker, headphone transducer, and/or a line level signal output. A capacitor **C1** may be utilized to couple the output signal to the transducer or line level output, particularly if amplifier **A1** is operated from a unipolar power supply having a quiescent voltage substantially differing from ground.

[0014] The volume control signal is also supplied to a mode control circuit **12** for controlling the output power supply voltage supplied to the power supply rails of power amplifier **A1** in conformity with an expected range of signal levels at the output of power amplifier **A1**, so that power amplifier **A1** will not clip for high (peak) signal levels, but will have a reduced power supply voltage when high (peak) signal levels are not present. Alternatively, or in combination, the output of amplifier **A2** is also provided to mode control circuit **12** so that actual signal levels can be measured by mode control circuit **12** and the power supply voltage of power amplifier **A1** adjusted in conformity with the actual signal level that will be reproduced at the output power amplifier **A1**. In the depicted embodiment, since the volume control is applied after the signal level measurement taken from the output of amplifier **A2**, the volume information is needed even if the signal level is detected by mode control circuit **12**, since mode control circuit must also receive information relating to the amount of gain/attenuation that will be applied to the signal prior to amplification by power amplifier **A1**. Also, an output of decoder **13**, if present, may provide an advance notification to mode control circuit **12** that a peak in signal amplitude will be arriving at DAC **14** and thus provide an early indication that the operating mode needs to be changed if the lower voltage/power operating mode of charge pump power supply **10** is selected.

[0015] Charge pump power supply **10** provides the power supply rail inputs of amplifier **A1** and receives a power supply input, generally from a battery or other power supply, depicted as battery terminal connections **Vbatt+** and **Vbatt-.** Mode control circuit **12** supplies a **Mode Select** signal to charge pump power supply **10**, that selects an operating mode of charge pump power supply **10.** Charge pump power supply **10** provides output power supply rail connections **out+** and **out-** that will have a “full” (maximum) voltage in a first operating mode and a voltage that is a rational fraction of the full voltage in a second operating mode, as selected by mode control circuit, when the audio signal level is low enough or expected to be low enough that clipping will not occur at the output of power amplifier **A1.**

[0016] Referring now to **Figure 2** and additionally with reference to **Figures 3A-3D**, details of charge pump power supply **10** are shown. When the first operating mode (Mode 1) is selected, the **Mode Select** signal is in the logical high ("1") state, and switch **S8** is closed, to apply the **Vbatt+** voltage directly to the **out+** terminal. **Figure 3A** and **Figure 3B** show the circuit connection arrangement for Mode 1 in the first and second clock phases, respectively, omitting open switches and inactive circuit components. Switches **S1**, **S2** and **S4** are open and not activated in the first operating mode, as logical AND gates **AND10** and **AND11** disable the control signals to switches **S1**, **S2** and **S4**, as the inverted **Mode Select** signal provided by inverter **I10** is in a logical low ("0") state. For a single-ended (unipolar) power supply, capacitors **C12**-**C13**, switches **S3**, **S6** and switch **S7** are omitted. As illustrated in **Figures 3A**-**3B**, in Mode 1, the positive power supply voltage at terminal **out+** is supplied directly from the positive input terminal **Vbatt+**.

[0017] To produce the negative output supply voltage in mode 1, the input voltage provided between input terminals **Vbatt+** and **Vbatt-** is inverted by a voltage inverter. In phase one (Φ1) of mode 1, switch **S3** is closed and switch **S6** is closed, which charges capacitor **C12** by connection across input terminals **Vbatt+** and **Vbatt-**, as illustrated in **Figure 3A.** While Figures 3A-3D show polarized capacitors **C10**-**C13** for purposes of clarity, it is understood that polarized capacitors are not required and that non-polarized capacitors can be utilized for capacitors **C10**-**C13.** In phase two (Φ2) of mode 1, switch **S3** and switch **S6** are opened and switch **S5** and switch **S7** are closed, which reverses the terminal of capacitor **C12** applied to the **Vbatt-** input terminal. Switch **S7** applies the terminal of capacitor **C12** that was applied to the **Vbatt-** input terminal in phase one, to the negative output terminal **out-**, as further illustrated by **Figure 3B.** The switching action described above provides a negative voltage at the **out-** terminal with respect to the **Vbatt-** terminal that is substantially equal to the magnitude of the voltage between the **out+** terminal and the **Vbatt-** terminal, which acts as the reference midpoint voltage (ground) at the junction between output capacitors **C11** and **C13.**

[0018] In the second operating mode (Mode 2), which is active when the **Mode Select** signal is in the logical low ("0") state, switch **S8** is opened. In phase one (Φ1) of Mode 2, switches **S1** and **S4** are closed, which apply capacitor **C10** in series with output capacitor **C11** across the **Vbatt+** and **Vbatt-** terminals, as further illustrated in **Figure 3C.** In phase two (Φ2) of Mode 2, switches **S1** and **S4** are opened and switches **S2** and **S5** are closed, which connect capacitor **C10** in parallel with capacitor **C11** as further illustrated in **Figure 3D.** Since the second phase of mode 2 equalizes the voltage on capacitors **C10** and **C11**, the stable operating point of the circuit is such that the input voltage between the **Vbatt+** and **Vbatt-** terminals will be split equally during the charging phase, irrespective of the relative capacitance of **C10** and **C11.** Thus the voltage at the **out+** output terminal in Mode 2 will be half of the voltage across the **Vbatt+** and **Vbatt-** terminals. Other ratios can be constructed by switching more capacitors in series with capacitors **C10** and **C11** during phase one, and connecting them all in parallel during phase two. For example, a voltage of one third of the input battery voltage may be produced by using three capacitors connected alternatively in series across the battery terminals and parallel between the **out+** terminal and the **Vbatt-** terminal.

[0019] The negative supply in the second operating mode (Mode 2) is provided in a manner similar to that of the first operating mode and the connections of capacitor **C12** are shown in **Figure 3B** and **Figure 3D**, as being the same. However, as illustrated in **Figure 3C**, since switch **S8** is open in the second operating mode, during phase one of Mode 2, capacitor **C12** is charged from the **out+** terminal rather than the **Vbatt+** terminal as was shown in **Figure 3A** for Mode 1. Switch **S4** performs the operation of connecting capacitor **C12** to the **out+** terminal, as illustrated in **Figure 3C**, along with the above-described operation of applying capacitor **C10** in series with capacitor **C11** in phase one for the positive power supply and therefore the relative phases between the voltage inverter supplying the **out-** voltage and the circuit supplying the **out+** voltage must be maintained in the depicted configuration. Otherwise, eight switches may be utilized and the common connection between capacitor **C10** and **C12** broken. The additional switch would be provided between capacitor C12 and the **out+** terminal, and would be active in Mode 2, phase 1. It is also possible to further reduce the number of switches from seven to six, by removing switch **S3** and controlling switch **S4** with the unqualified (Φ1) signal. However, the inclusion of switch **S3** reduces the impedance of the power supply path in the first operating mode, which is the highest voltage/current operating mode. Therefore, it is generally advantageous to include switch **S3** in the circuit.

[0020] Referring now to **Figure 4**, details of an amplifier control circuit that can be utilized to implement mode control circuit **12** of **Figure 1** is shown. A signal level detector **30**, which may be an analog peak detection circuit or the output of a digital circuit that indicates the magnitude of the analog signal at some point in the audio signal path, is optionally combined with downstream volume control information, using a multiplier **31**. (If the volume control and signal information are both logarithmic, multiplier **31** is replaced with an adder). A comparator **K1** (or equivalent digital domain comparison), determines whether or not the signal level exceeds a threshold $\mathbf{V_{ref}}$ and if the threshold is exceeded, then the mode control select signal is set to a high logic level to enable operating mode 1 of the charge pump, providing a higher power supply to power amplifier **A1**. Suitable time constants can be provided for signal level detector **30** and hysteresis provided within comparator so that mode 2 is not selected unless the peak level of signal has fallen below the threshold for a predetermined time period and/or voltage hysteresis guard band, to prevent excessive changing of the power supply voltage control.

[0021] As an alternative, signal level detector **30** can be omitted, and the volume control level can be directly compared to a threshold value, to determine the power supply operating mode and thereby the power amplifier supply rail operating voltage. Since the volume control level is a predictor of the expected peak levels that will need to be reproduced by power amplifier **A1**, such control will be sufficient in some applications, in particular, applications in which the maximum signal (peak) level is known a priori, such as when the audio signal is supplied from a digital-to-analog converter integrated within the system.

[0022] An optional circuit that is responsive to voltage peaks when the power supply circuit is in operating mode 2, is provided by a set-reset latch **33**, a delay **32**, and a signal compressor **34.** When the mode control signal transitions from a logical low level (Mode 2) to a logical high level (Mode 1), set-reset latch **33** is set, and remains set until a predetermined time period of delay **32** has expired. The output of set-reset latch **33** is a pulse that activates signal compressor **34** for the predetermined time, which is generally the time required for the power supply rails of power amplifier **A1** to stabilize at the higher power supply rail values of operating mode 1. Signal compressor **34** is inserted in the audio signal path upstream of power amplifier **A1**, and reduces the signal level to avoid clipping until the power supply rails provided to amplifier **A1** are known to be sufficient to support the required output voltage swing without clipping.

[0023] While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form, and details may be made therein without departing from the spirit and scope of the invention.

CLAIMS

WHAT IS CLAIMED IS:

1. An audio amplifier circuit for providing an output signal to an audio transducer, said audio amplifier circuit comprising:

a power amplifier having an audio input for receiving an audio input signal, an audio output for providing said output signal, and a pair of power supply rail connections; and

a charge pump power supply for providing a power supply voltage across said pair of power supply rail connections of said power amplifier, wherein said charge pump power supply has a select input for selecting an operating mode of said power supply, wherein in a first operating mode, said power supply voltage is equal to a first voltage, and wherein in a second operating mode said power supply voltage is substantially equal to a rational fraction of said first voltage.

2. The audio amplifier circuit of Claim 1, wherein in said second operating mode said power supply voltage is substantially equal to half of said first voltage.

3. The audio amplifier of Claim 1, wherein said charge pump power supply has a unipolar power input having a ground terminal and an input voltage terminal, and wherein said power supply voltage is a bipolar output substantially symmetric about a voltage of said ground terminal.

4. The audio amplifier circuit of Claim 1, wherein said charge pump comprises a plurality of capacitors and a switching circuit for switching said capacitors alternatively from a series to a parallel combination, and wherein in response to said select input, a pattern of switching of said switching circuit is altered, whereby a rational relationship between said power supply voltage in said first operating mode and said power supply voltage in second operating mode is provided.

5. The audio amplifier circuit of Claim 1, wherein said charge pump power supply includes a switched-capacitor voltage divider that uses a series-coupling of capacitors in a first switching phase of said second operating mode to produce said rational fraction of said first voltage and couples at least one of said capacitors to at least one of said power supply rail connections in a second switching phase of said second operating mode to apply said rational fraction of said first voltage to said at least one power supply rail connection.

6. The audio amplifier circuit of Claim 1, further comprising a first amplifier stage circuit having an output coupled to said audio input of said power amplifier, wherein said first amplifier stage has a pair of first stage power supply rail connections connected to a fixed voltage power supply, wherein a fixed voltage of said fixed voltage power supply does not change substantially with selection of said operating mode of said power supply.

7. The audio amplifier circuit of Claim 1, further comprising a control circuit for selecting said operating mode in conformity with a volume setting of said audio amplifier circuit.

8. The audio amplifier circuit of Claim 7, wherein said audio amplifier circuit further comprises a potentiometer coupled to said audio input for controlling a magnitude of said output signal, and wherein said control circuit selects said magnitude in conformity with a control level of said potentiometer.

9. The audio amplifier of Claim 8, wherein said potentiometer is a digitally controlled potentiometer, and wherein said control level is determined from a digital control value supplied to said potentiometer.

10. The audio amplifier circuit of Claim 1, further comprising a control circuit for providing a selection signal to said select input in conformity with an amplitude of said audio input, whereby clipping of said power amplifier is prevented when said second operating mode of said charge pump power supply is selected by instead selecting said first operating mode.

11. The audio amplifier circuit of Claim 10, wherein said control circuit generates an indication of an amplitude of said audio input, and wherein said control circuit provides said selection signal to said select input in conformity with said indication of said amplitude of said audio input, whereby said first operating mode is selected when said indication of amplitude indicates that a higher power level is required from said audio output and said second operating mode is selected when said indication of amplitude indicates that a higher power level is not required from said audio output.

12. The audio amplifier circuit of Claim 11, wherein said control circuit comprises a signal level detector for providing said indication of said amplitude by detecting an amplitude of a signal provided to said audio amplifier.

13. The audio amplifier circuit of Claim 12, wherein said audio input is provided from a digital-to-analog converter, and wherein said signal level detector is a digital circuit that compares a digital signal representation coupled to an input of said digital-to-analog converter to a threshold value.

14. The audio amplifier circuit of Claim 1, wherein said charge pump power supply comprises:

a first flyback capacitor; and

a first switching circuit for alternatively coupling said first flyback capacitor in said first operating mode between a positive one of said power supply input terminals and a positive one of said pair of power supply rail connections in first phase and between said pair of power supply input terminals in a second phase, and wherein when said charge pump power supply is in said second operating mode, said first switching circuit couples said positive one of said power supply input terminals to said positive one of said pair of power supply rail connections.

15. The audio amplifier circuit of Claim 14, wherein said charge pump power supply further comprises:

a second flyback capacitor; and

a second switching circuit coupled to said second flyback capacitor for alternatively coupling a first terminal of said second flyback capacitor to positive one of said pair of power supply rail connections and a second terminal of said second flyback capacitor to a negative one of said pair of power supply input terminals in said first phase, and coupling said first terminal of said second flyback capacitor to said negative one of said pair of power supply input terminals and said second terminal of said second flyback capacitor to a negative one of said pair of power supply rail connections in said second phase.

16. The audio amplifier circuit of Claim 15, wherein said first terminal of said second flyback capacitor is connected to a first terminal of said first flyback capacitor.

17. A method of improving efficiency of an amplifier for providing a power output to an audio transducer, said method comprising:

receiving an indication of a magnitude of a signal to be amplified by said amplifier;

selecting an operating mode of a charge pump power supply; and

supplying a power supply voltage to said amplifier from said charge pump in conformity with said selected operating mode, wherein in a first operating mode of said charge pump power supply, said power supply voltage is equal to a first voltage and in a second operating mode of said charge pump power supply, said power supply voltage is substantially equal to a rational fraction of said first voltage.

18. The method of Claim 17, wherein said receiving receives a volume control level corresponding to a gain of a signal path of said signal and wherein said selecting is performed in conformity with a magnitude of said volume control level.

19. The method of Claim 17, wherein said receiving receives an indication of amplitude of said signal, and wherein said selecting is performed in conformity with said indication of magnitude.

20. A charge-pump power supply circuit, comprising:

a pair of power supply input terminals;

a pair of power supply output terminals;

a first flyback capacitor;

a second flyback capacitor; and

a switching circuit for alternatively coupling said first flyback capacitor in a first operating mode between a positive one of said power supply input terminals and a positive one of said power supply output terminals connections in first phase and between said pair of power supply input terminals in a second phase, and wherein when said charge pump power supply is in said second operating mode, said switching circuit couples said positive one of said power supply input terminals to said positive one of said pair of power supply output terminals, and wherein said switching circuit further couples a first terminal of said second flyback capacitor to said positive one of said pair of power supply output terminals and a second terminal of said second flyback capacitor to a negative one of said pair of power supply input terminals in said first phase, and couples said first terminal of said second flyback capacitor to said negative one of said pair of power supply input terminals and said second terminal of said second flyback capacitor to a negative one of said pair of power supply output terminals in said second phase.

21. The power supply circuit of Claim 20, wherein said first terminal of said second flyback capacitor is connected to a first terminal of said first flyback capacitor.

22. The power supply circuit of Claim 20, wherein said switching circuit comprises:

a first switch responsive to selection of said second operating mode, wherein said first switch is connected between said positive one of said power supply output terminals and said positive one of said power supply input terminals;

a second switch responsive in a first phase when said first operating mode is selected, wherein said second switch connects said positive one of said power supply input terminals to a first terminal of said first flyback capacitor;

a third switch responsive in said first phase when said first operating mode is selected, wherein said third switch connects said positive one of said power supply output terminals to a second terminal of said first flyback capacitor;

a fourth switch responsive in a second phase when said first operating mode is selected, wherein said fourth switch connects said negative one of said power supply input terminals to a first terminal of said first flyback capacitor; and

a fifth switch responsive in said second phase when said first operating mode is selected, wherein said fifth switch connects said positive one of said power supply output terminals to a second terminal of said first flyback capacitor.

23. The power supply circuit of Claim 22, further comprising:

a sixth switch responsive in said first phase, wherein said sixth switch connects a negative one of said power supply input terminals to a second terminal of said second flyback capacitor; and

a seventh switch responsive in a second phase, wherein said seventh switch connects said negative one of said power supply input terminals to said second terminal of said second flyback capacitor.

24. The power supply circuit of Claim 22, further comprising an eighth switch responsive in said first phase, wherein said eighth switch connects said positive one of said power supply output terminals to a first terminal of said second flyback capacitor.

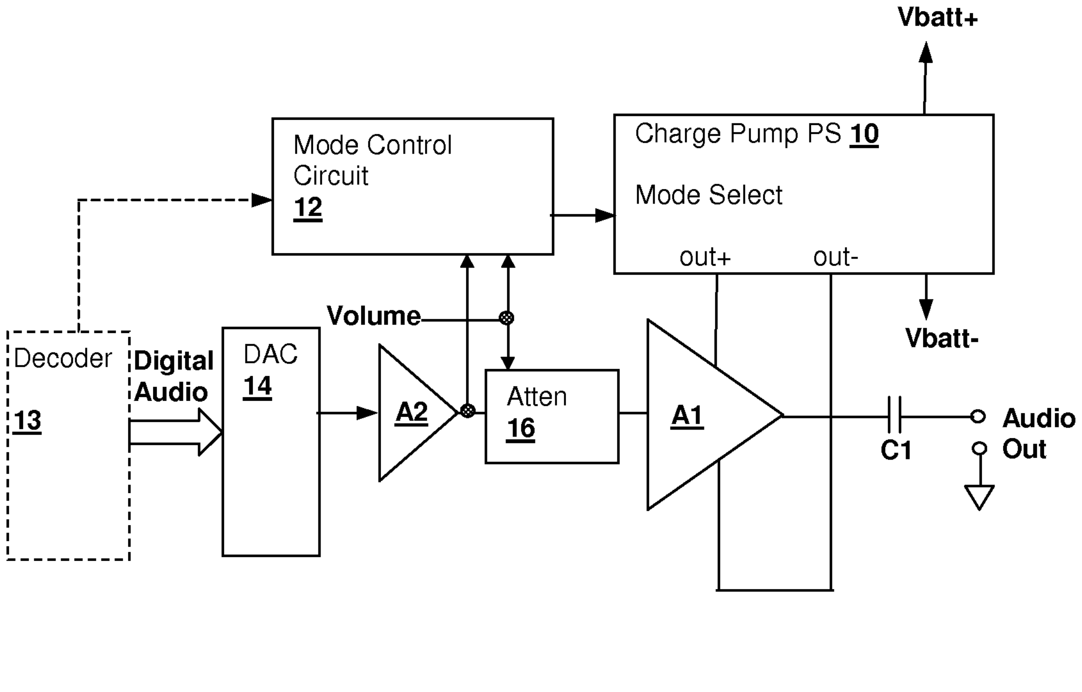
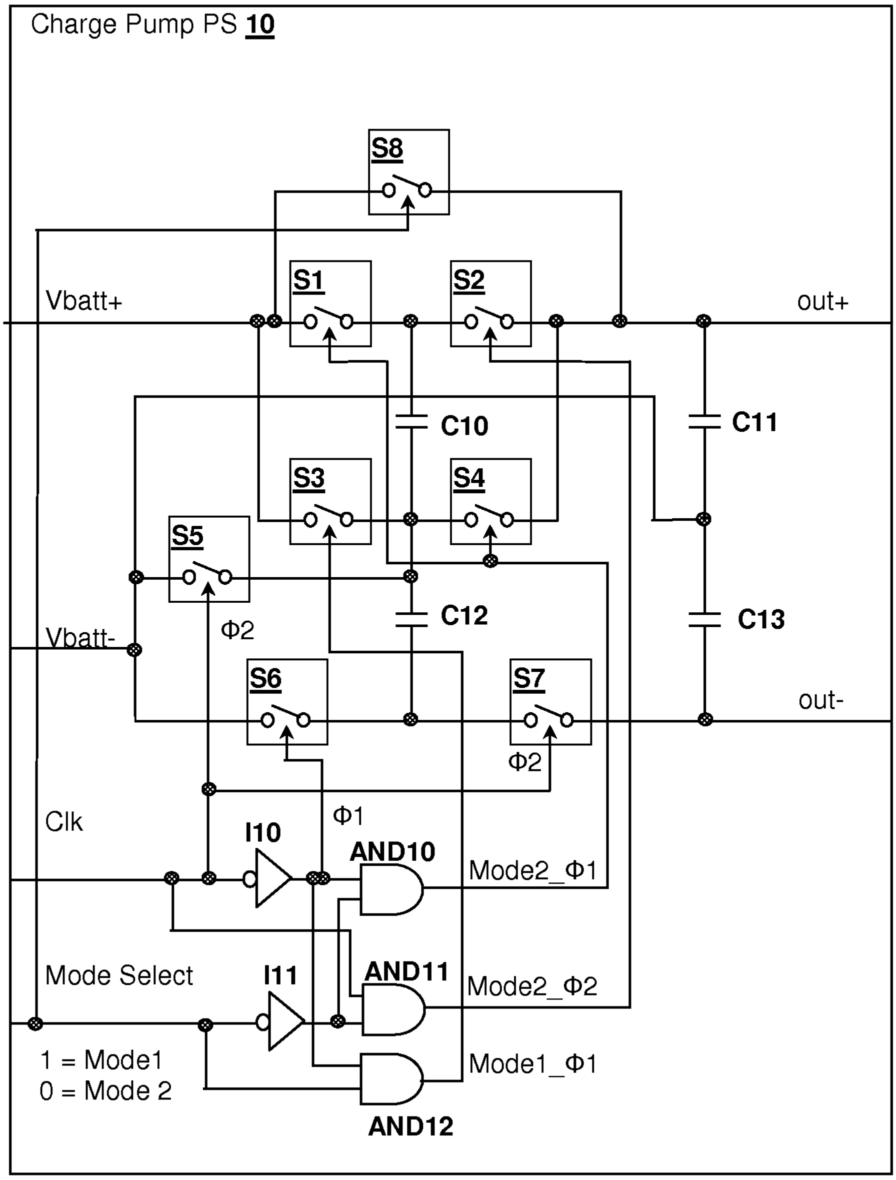

Vbatt+
Mode Control Circuit 12
Charge Pump PS 10
Mode Select
out+
out-
Vbatt-
Volume
Decoder 13
Digital Audio
DAC 14
A2
Atten 16
A1
C1
Audio Out

Fig. 1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S8
S1
S2
Vbatt+
out+
C10
C11
S3
S4
S5
Vbatt-
Φ2
C12
C13
S6
S7
out-
Φ2
Φ1
Clk
I10
AND10
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0 = Mode 2
AND12

Fig. 2

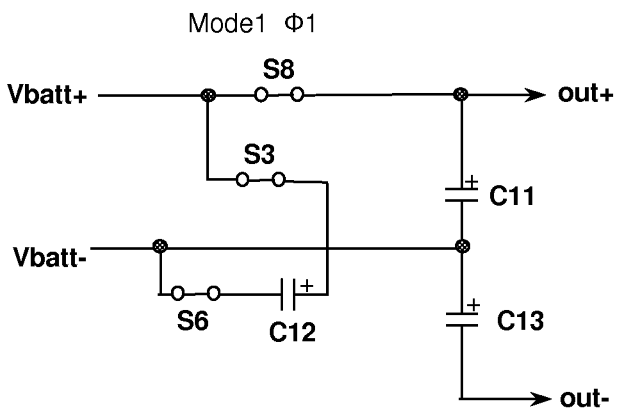

Fig. 3A

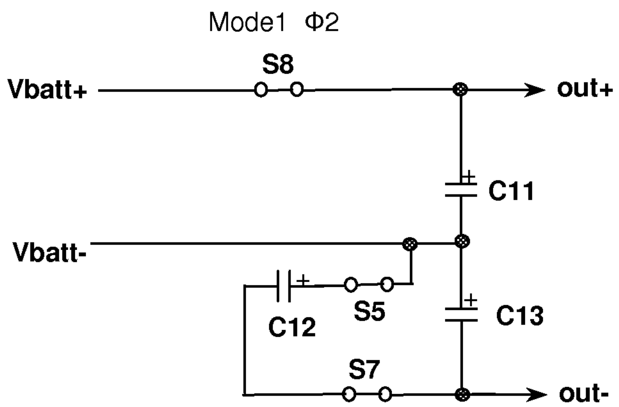

Fig. 3B

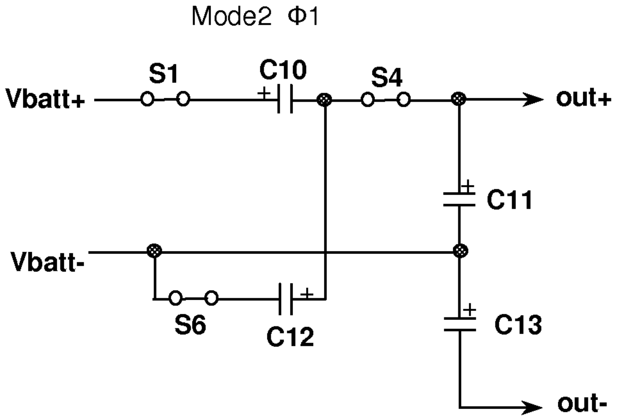

Fig. 3C

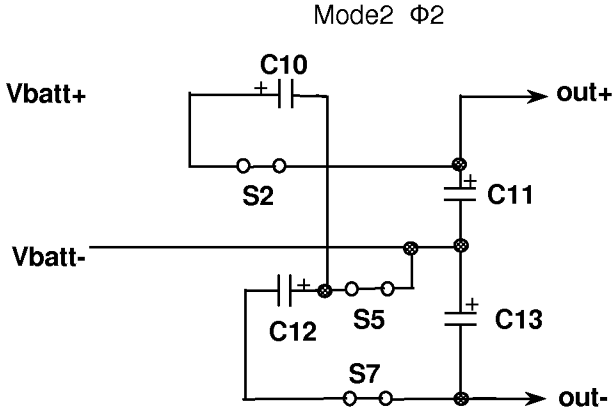

Fig. 3D

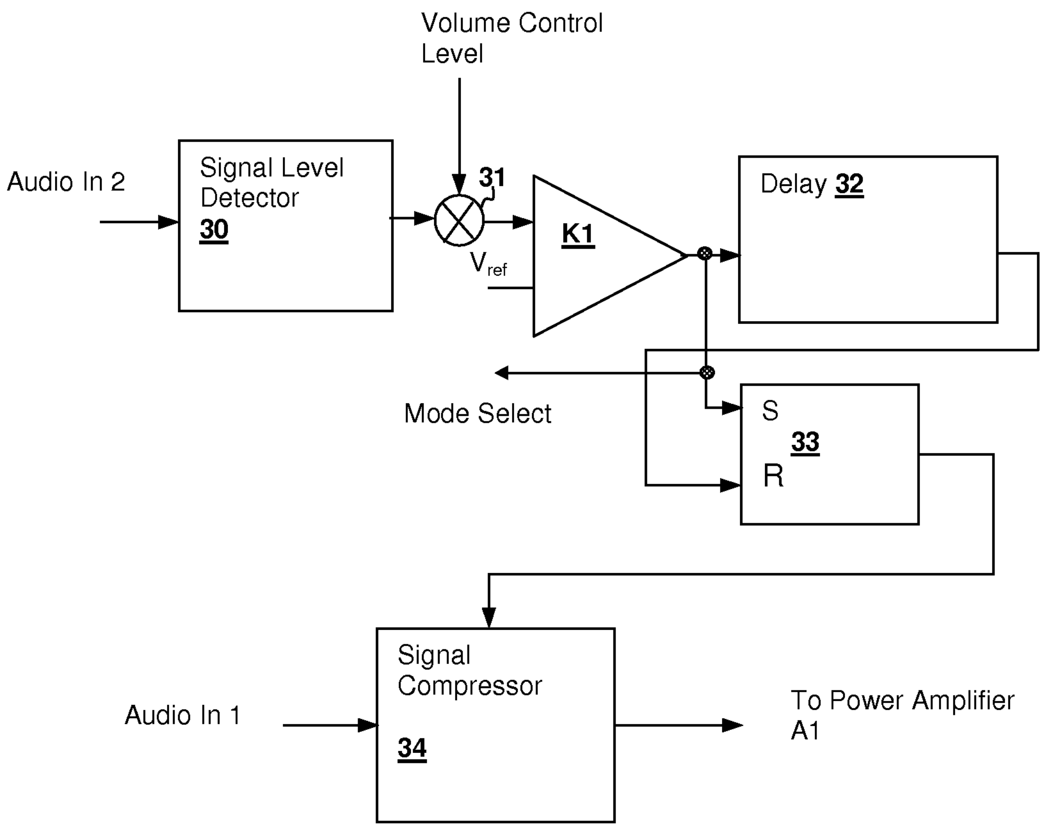
Volume Control
Level
Audio In 2
Signal Level
Detector
30
31
K1
V ref
Delay 32
Mode Select
S
33
R
Signal
Compressor
34
Audio In 1
To Power Amplifier
A1

Fig. 4