(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
04 January 2018 (04.01.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/005385 A1

(51) International Patent Classification:
H01L 31/18 (2006.01) *H01L 31/0236* (2006.01)
H01L 31/0368 (2006.01)

(21) International Application Number:
PCT/US2017/039333

(22) International Filing Date:
26 June 2017 (26.06.2017)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
15/201,324 01 July 2016 (01.07.2016) US

(71) Applicant: **SUNPOWER CORPORATION** [US/US]; 77 Rio Robles, San Jose, California 95134 (US).

(72) Inventors: **HSIA, Benjamin Ian**; 4130 Coriander Terrace, Fremont, California 94538 (US). **BARKHOUSE, David Aaron Randolph**; 1229 Mills Street, Menlo Park, California 94025 (US). **JOHNSON, Todd Richards**; 3868 Willowpark Drive, San Jose, California 95118 (US). **CUDZINOVIC, Michael**; 378 Balsam Avenue, Sunnyvale, California 94085 (US).

(74) Agent: **VINCENT, Lester J.** et al.; BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP, 1279 Oakmead Parkway, Sunnyvale, California 94085 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: PROTECTIVE REGION FOR METALLIZATION OF SOLAR CELLS

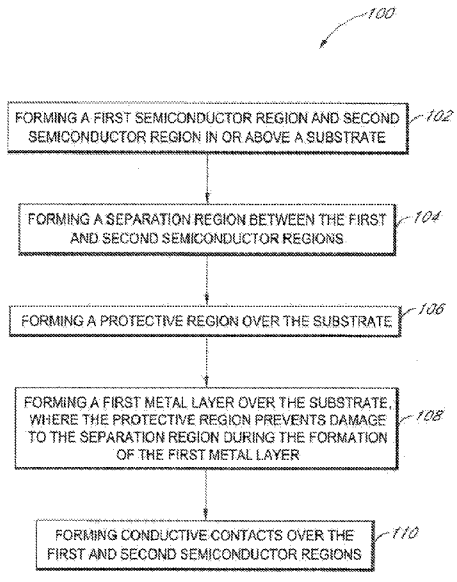

FIG. 1

(57) Abstract: Methods of fabricating a solar cell including metallization techniques and resulting solar cells, are described. In an example, a first and second semiconductor regions can be formed in or above a substrate, where a separation region is disposed between the first and second semiconductor regions. A protective region can be formed over the separation region. A first metal layer can be formed over the substrate, where the protective region prevents and/or inhibits damage to the separation region during the formation of the first metal layer. Conductive contacts can be formed over the first and second semiconductor regions.

WO 2018/005385 A1

[Continued on next page]

Published:
— *with international search report (Art. 21(3))*

PROTECTIVE REGION FOR METALLIZATION OF SOLAR CELLS

BACKGROUND

[0001] Photovoltaic (PV) cells, commonly known as solar cells, are devices for conversion of solar radiation into electrical energy. Generally, solar radiation impinging on the surface of, and entering into, the substrate of a solar cell creates electron and hole pairs in the bulk of the substrate. The electron and hole pairs migrate to p-doped and n-doped regions in the substrate, thereby creating a voltage differential between the doped regions. The doped regions are connected to the conductive regions on the solar cell to direct an electrical current from the cell to an external circuit. When PV cells are combined in an array such as a PV module, the electrical energy collected from all of the PV cells can be combined in series and parallel arrangements to provide power with a certain voltage and current.

[0002] Efficiency is an important characteristic of a solar cell as it is directly related to the capability of the solar cell to generate power. Likewise, efficiency in producing solar cells is directly related to the cost effectiveness of such solar cells. Accordingly, techniques for increasing the efficiency in the manufacture of solar cells, are generally desirable.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Figure 1 illustrates a flow chart representation of an example method for fabricating a solar cell, according to some embodiments.

[0004] Figure 2 illustrates a flow chart representation of an example method for forming conductive contacts for a solar cell, according to some embodiments.

[0005] Figures 3 illustrate a flow chart representation of another example method for forming conductive contacts for a solar cell, according to some embodiments.

[0006] Figure 4 illustrates a stage in solar cell fabrication following formation of semiconductor regions (emitter regions) formed above a substrate of a solar cell, according to some embodiments.

[0007] Figure 5 illustrates the structure of Figure 4 following forming of a protective layer above the substrate, according to some embodiments.

[0008] Figure 6 illustrates the structure of Figure 5 following patterning the protective layer, according to some embodiments.

[0009] Figure 7 illustrates the structure of Figure 6 following forming a first metal layer over the substrate, according to some embodiments.

[0010] Figure 8 illustrates the structure of Figure 6 following heating the substrate, according to some embodiments.

[0011] Figures 9 and 10 illustrate cross-sectional views of example solar cells during a plating process to form conductive contacts, according to some embodiments.

[0012] Figures 11 and 12 illustrate a cross-sectional view of solar cells formed from the method of Figures 1, 2 and 4-10, according to some embodiments.

[0013] Figure 13 illustrates cross-sectional view of example solar cells during a metal-foil based metallization process to form conductive contacts, according to some embodiments.

[0014] Figure 14 illustrates a cross-sectional view of a solar cell formed from the method of Figures 1, 3-8 and 13, according to some embodiments.

DETAILED DESCRIPTION

[0015] The following detailed description is merely illustrative in nature and is not intended to limit the embodiments of the subject matter of the application or uses of such embodiments. As used herein, the word "exemplary" means "serving as an example, instance, or illustration." Any implementation described herein as exemplary is not necessarily to be construed as preferred or advantageous over other implementations. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, brief summary or the following detailed description.

[0016] This specification includes references to "one embodiment" or "an embodiment." The appearances of the phrases "in one embodiment" or "in an embodiment" do not necessarily refer to the same embodiment. Particular features, structures, or characteristics may be combined in any suitable manner consistent with this disclosure.

[0017] Terminology. The following paragraphs provide definitions and/or context for terms found in this disclosure (including the appended claims):

[0018] "Comprising." This term is open-ended. As used in the appended claims, this term does not foreclose additional structure or steps.

[0019] "Configured To." Various units or components may be described or claimed as "configured to" perform a task or tasks. In such contexts, "configured to" is used to connote structure by indicating that the units/components include structure that performs those task or tasks during operation. As such, the unit/component can be said to be configured to perform the task even when the specified unit/component is not currently operational (e.g., is not on/active). Reciting that a unit/circuit/component is "configured to" perform one or more tasks is expressly intended not to invoke 35 U.S.C. §112, sixth paragraph, for that unit/component.

[0020] "First," "Second," etc. As used herein, these terms are used as labels for nouns that they precede, and do not imply any type of ordering (e.g., spatial, temporal, logical, etc.). For example, reference to a "first" semiconductor region does not necessarily imply that this

semiconductor region is the first semiconductor region in a sequence; instead the term "first" is used to differentiate this semiconductor region from another semiconductor region (e.g., a "second" semiconductor region).

[0021] "Based On." As used herein, this term is used to describe one or more factors that affect a determination. This term does not foreclose additional factors that may affect a determination. That is, a determination may be solely based on those factors or based, at least in part, on those factors. Consider the phrase "determine A based on B." While B may be a factor that affects the determination of A, such a phrase does not foreclose the determination of A from also being based on C. In other instances, A may be determined based solely on B.

[0022] "Coupled" – The following description refers to elements or nodes or features being "coupled" together. As used herein, unless expressly stated otherwise, "coupled" means that one element/node/feature is directly or indirectly joined to (or directly or indirectly communicates with) another element/node/feature, and not necessarily mechanically.

[0023] "Inhibit" – As used herein, inhibit is used to describe a reducing or minimizing effect. When a component or feature is described as inhibiting an action, motion, or condition it may completely prevent the result or outcome or future state completely. Additionally, "inhibit" can also refer to a reduction or lessening of the outcome, performance, and/or effect which might otherwise occur. Accordingly, when a component, element, or feature is referred to as inhibiting a result or state, it need not completely prevent or eliminate the result or state.

[0024] In addition, certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as "upper", "lower", "above", and "below" refer to directions in the drawings to which reference is made. Terms such as "front", "back", "rear", "side", "outboard", and "inboard" describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

[0025] In the following description, numerous specific details are set forth, such as specific operations, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known techniques are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure.

[0026] Approaches to prevent and/or inhibit solar cell performance degradation induced during metallization processes are described herein. Embodiments of the present disclosure include the formation of a protective region over portions of a solar cell to prevent and/or inhibit impingement of energetic ions and/or ionizing radiation into the solar cell during a metallization process. In an example, protective regions can be used to inhibit charge carrier lifetime degradation over a trench and/or passivation region of a solar cell during a metal sputter deposition process.

[0027] Methods for metallization of solar cells and the resulting solar cells are also described herein. In the following description, numerous specific details are set forth, such as specific solar cell structures and process flow operations, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known fabrication techniques, such as lithography and patterning techniques, are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be understood that the various embodiments shown in the figures are illustrative representations and are not necessarily drawn to scale.

[0028] Disclosed herein are methods of fabricating solar cells. In an exemplary process flow, Figure 1 illustrates a flowchart 100 listing operations in a method of fabricating a solar cell corresponding to Figures 4-14, according to some embodiments. In various embodiments, the method of Figure 1 can include additional (or fewer) blocks than illustrated. For example, in some embodiments, an optional heating and/or annealing step can be performed after forming a first metal layer over the substrate, at block 108, prior to the formation of conductive contacts at block 110.

[0029] As disclosed herein, a conductive contact can include a metal contact structure formed over a semiconductor region of a solar cell. In an embodiment, the conductive contact can also be referred to as a metal contact. In an example, a conductive contact and/or metal contact can include one or more metal layers. In one example, the conductive contact includes aluminum, titanium tungsten, tungsten, and/or copper, among other metals. Figures 2 and 3 below describe methods of forming conductive contacts.

[0030] Disclosed herein are methods for forming conductive contacts for solar cells. In a one exemplary process flow, Figure 2 illustrates a flowchart 200 listing operations in one method for forming conductive contacts of a solar cell corresponding to Figures 9-12, according to some embodiments.

[0031] Also, disclosed herein is another method for forming conductive contacts for a solar cell. In a an exemplary process flow, Figure 3 illustrates a flowchart 300 listing operations in a patterning process of a solar cell corresponding to Figures 13 and 14, according to some embodiments.

[0032] Embodiments described herein include fabrication of a solar cell 400 according to one or more of the above described approaches. Referring to Figure 4 and corresponding operation 102 of flowchart 100, a first semiconductor region 410 and/or a second semiconductor region 412 can be formed in or above a substrate 406. In an example, as shown in Figure 1, the substrate 406 has disposed there above a first semiconductor region 410 and a second semiconductor region 412. In some examples, the first and second semiconductor regions 410, 412 can be formed in the substrate 406. In an example, the first and second semiconductor regions 410, 412 are emitter regions. In an embodiment, a thin dielectric material 408 can be disposed between the first and second semiconductor region 410, 412 and the substrate 406. In an embodiment, the substrate 406 includes a light-receiving surface 418 on a front side 402 opposite a back side 404 of the solar cell 400.

[0033] In an embodiment, the substrate 406 is a monocrystalline silicon substrate, such as a bulk single crystalline N-type doped silicon substrate. It is to be appreciated, however, that substrate 406 may be a layer, such as a multi-crystalline silicon layer, disposed on a global solar cell substrate. In an embodiment, the thin dielectric layer 408 is a tunneling silicon oxide layer having a thickness of approximately 2 nanometers or less. In one such embodiment, the term "tunneling dielectric layer" refers to a very thin dielectric layer, through which electrical conduction can be achieved. The conduction may be due to quantum tunneling and/or the presence of small regions of direct physical connection through thin spots in the dielectric layer. In one embodiment, the tunneling dielectric layer is or includes a thin silicon oxide layer. In an embodiment, the first and second semiconductor regions 410, 412 are N-type and P-type emitter regions, respectively. In an example, the N-type and P-type emitter regions are formed in the substrate itself, in which case distinct semiconductor regions (such as regions 410 and 412) and the dielectric layer 406 would not be included.

[0034] In an embodiment, the first and second semiconductor regions 410 and 412, respectively, are formed polycrystalline silicon formed by, e.g., using a plasma-enhanced chemical vapor deposition (PECVD) process. In one such embodiment, the first semiconductor region 410 is doped with an N-type impurity, such as phosphorus (e.g., N-type semiconductor region). The second semiconductor region 412 is doped with a P-type impurity, such as boron (e.g., P-type semiconductor region).

[0035] Referring to Figure 4 and corresponding operation 104 of flowchart 100, a separation region 414 can be formed between the first and second semiconductor regions 410, 412. In an embodiment, the separation region 414 is a trench region. In an embodiment, the separation region 414 extends partially into the substrate 406. In one embodiment, the separation region 414 is a passivation region.

[0036] In an embodiment, the light receiving surface 418, is a texturized light-receiving surface, as is depicted in Figure 4. In one embodiment, a hydroxide-based wet etchant is employed to texturize the light receiving surface 418 of the substrate 406 and, possibly, the separation region surface 416 as is also depicted in Figure 4. It is to be appreciated that the timing of the texturizing of the light receiving surface and separation region may vary. For example, the texturizing may be performed before or after the formation of the thin dielectric layer 408. In an embodiment, a texturized surface may be one which has a regular or an irregular shaped surface for scattering incoming light, decreasing the amount of light reflected off of the light receiving surfaces 416, 418 of the solar cell 400. In some embodiments, the light receiving surfaces 416, 418 need not be texturized.

[0037] Solar cell substrates can be susceptible to performance degradation during a solar cell metallization process. In an example, the deposition of a metal seed layer via metal sputtering can involve collision of highly energetic metal species and damaging plasma-induced radiation at the separation region 414 resulting in solar cell performance degradation. Thus, in an embodiment, approaches to prevent and/or inhibit metallization-induced damage at the separation region 414 of the substrate 406 are presented.

[0038] Referring to Figure 5, Figure 6 and corresponding operation 106 of flowchart 100, a protective region is formed over the substrate 406. In an embodiment, the protective region 428 is formed over the separation region 414. In one embodiment, forming the protective region can include forming a blanket protective layer 424 over the substrate 406, as shown in Figure 5, and subsequently patterning the blanket protective layer 424 to form the protective region 428 as shown in Figure 6. In an embodiment, the blanket protective layer 424 includes a polymer. In an example, the blanket protective layer 424 includes a silicone, polymeric silsesquioxane, epoxy or acrylic. In an embodiment, the protective region 428 can include a material which does not include a pigment. In one example, the blanket protective layer 424 can be a blanket polysilicon layer. In one particular embodiment, for example where plated conductive contacts are formed, the protective region 428 can include reflective pigments such as titanium oxide (TiO2). In one particular embodiment, for example where plated conductive contacts are formed, the protective region 428 can include polyimide. In an embodiment, the patterning can include forming a mask

426 over portions 425 of the blanket protective layer 424. In an embodiment, subsequent to forming the mask 426, the patterning can include removing exposed portions 423 of the blanket protective layer 424, where the mask protects portions 425 of the blanket protective layer 424 during the patterning process. Subsequent to patterning, the mask 426 can be removed.

[0039] In an embodiment, the formation of the protective region 428 over the separation region 414 of the solar cell 400 can prevent and/or inhibit impingement of energetic ions and/or ionizing radiation into the solar cell 400 during a subsequent metallization process. In an example, ionizing radiation can include electromagnetic radiation such as in the ultraviolet (UV) and/or x-ray wavelengths. In one example, protective regions 428 can be used to inhibit the impingement of energetic ions and/or ionizing radiation over a trench and/or passivation region 414 of a solar cell 400 during a metal sputter deposition process. In the same example, the protective regions 428 can prevent and/or inhibit charge carrier lifetime loss at the trench and/or passivation region due to the impingement of energetic ions and/or ionizing radiation at those regions.

[0040] In an embodiment, prior to forming the blanket protective layer 424, an intervening layer 420 can be formed over the substrate 406. In an embodiment, the intervening layer 420 can also be referred to as an insulating layer. In one embodiment, the intervening layer 420 includes a back anti-reflective coating (BARC). In an example, the intervening layer 420 includes silicon nitride and/or amorphous silicon. Referring to Figure 5, additional embodiments can include forming of a passivation and/or front anti-reflective coating (ARC) layer 422 on a light-receiving surface 418 at the front side 402 of the substrate 406. In an example, the front anti-reflective coating (ARC) layer 422 can include silicon nitride. It is to be appreciated that the timing of the formation of the intervening layer and/or ARC layers may also vary. For example, subsequent to forming the intervening layer (e.g., a BARC layer) on the back side 404 of the substrate 406, the ARC layer 422 can be formed on the front side 402. In one embodiment, the intervening layer 420 can be formed subsequently after the ARC layer 422. In some embodiments, both the intervening layer 420 and the ARC layer 422 can be formed in a single process (e.g., the same process step).

[0041] Figure 6 illustrates a protective region 428 formed over the separation region 414 of the substrate 406, according to some embodiments. In one embodiment, and as discussed above, the protective region 428 can be formed from patterning a blanket protective layer 424, as described in Figure 5. In an embodiment, other formation and/or patterning processes can be used. In an embodiment, the protective region 428 can formed directly as a pattern, e.g., in contrast to the mask and etching process described above. In an example, the protective region

428 is formed by a printing process. In one example, the protective region 428 is formed by screen printing and/or ink-jet printing. In an embodiment, the protective region 428 includes a polymer. In an example, the protective region 428 includes a silicone, polymeric silsesquoixane, epoxy or acrylic. In an embodiment, the protective region 428 can include a material which does not include a pigment. In an embodiment, the protective region 428 is a dielectric region. In an example, the dielectric region can include silicon oxide. In one embodiment, the protective region 428 is a polysilicon region. In an example, the polysilicon region can be an N-type doped or a P-type doped polysilicon region. In the embodiment where the protective region 428 is a polysilicon region, an insulating layer 420 can insulate the first semiconductor region 410, second semiconductor region 412 and/or the substrate 406 from the protective region 428. In an embodiment, the polysilicon region can be deposited and/or grown. In an embodiment, the protective region 428 includes a material stable at temperatures of at least 300 degrees Celsius. In an example, the protective region 428 includes a material that does not decompose, melt, undergo outgassing or otherwise deteriorate at temperatures of least 300 degrees Celsius. In an embodiment, the protective region 428 can prevent and/or inhibit damage to the separation region 414 at temperatures of at least 300 degrees Celsius. In an example, the formation of a protective region 428 can prevent and/or inhibit impingement of energetic ions and/or ionizing radiation into the solar cell during a metallization process. In an example, ionizing radiation can include electromagnetic radiation such as in the ultraviolet (UV) and/or x-ray wavelengths. In one example, the protective region 428 can be used to inhibit charge carrier lifetime degradation over a trench and/or passivation region of a solar cell during a metal sputter deposition process. In some embodiments, the protective region 428 can prevent and/or inhibit metallization-induced damage at the separation region 414 and/or polysilicon regions of the substrate 406.

[0042] In an embodiment, openings 430 are formed in the intervening layer 420 to accommodate direct contact of a first metal layer to the first and/or second semiconductor regions 410 and 412 (e.g., as shown in Figure 7). In an embodiment, openings are formed in the intervening layer 420 by a patterning process. In an example, a laser ablation, lithography and/or etching process can be performed to form the openings 430. In one embodiment, openings 430 in the intervening layer 420 can be formed prior to forming the protective layer 428 of Figure 5. In an embodiment, the openings 430 in the intervening layer 420 can be formed prior to the formation of the protective region 428 of Figure 6. In some embodiments, the openings 430 in the intervening layer 420 can be formed after to the formation of the protective region 428.

[0043] Referring to Figure 7 and corresponding operation 108 of flowchart 100, a first metal layer 432 is formed over the substrate 406 (which may be referred to as a metal seed layer,

or M1 layer, for the solar cell 400). In an example, forming the first metal layer 432 can include depositing the first metal layer 432 over the substrate 406. In an embodiment, the first metal layer 432 can be formed as an uninterrupted layer over the substrate 406. In an embodiment, the protective region 428 protects the separation region 414 during the formation of the first metal layer 432. In one embodiment, the protective region 428 can prevent and/or inhibit damage to the separation region 414 during the formation of the first metal layer 432. In an example, the protective region 428 prevent and/or inhibit metallization-induced damage at the separation region 414 of the substrate 406. In an embodiment, portions of the first metal layer 432 can contact the first and second semiconductor regions 410, 412 at openings (e.g., openings 430 shown in Figure 6) of the intervening layer 420.

[0044] In an example, the first metal layer 432 is formed from a blanket deposition process. In one example, a sputtering process can be used to form the first metal layer 432. In an embodiment, the protective region 428 protects the separation region 414 during the sputtering process. In one embodiment, the protective region 428 can prevent and/or inhibit damage to the separation region 414 during the sputtering process. In an embodiment, the first metal layer 432 can include one or more metals and/or metal alloys. In an example, the first metal layer 432 can include aluminum, titanium tungsten, tungsten, and/or copper, among other metals.

[0045] In an embodiment, forming the first metal layer 432 can include performing a mask and etching process. In an example, a mask can be formed over portions 436 of the first metal layer. Subsequent to forming the mask, other portions 434 of the first metal layer 432 can be etched to remove the other portions 434 of the first metal layer. Subsequent to etching the first metal layer 432, the mask can be removed.

[0046] In one embodiment, the first metal layer 432 can instead be formed in a pattern, where the first metal layer 432 is formed directly over the first and second semiconductor regions 410, 412 (e.g., not as an uninterrupted layer or in contrast to performing a mask and etching process as described above). In an example, forming the first metal layer 432 can include forming a patterned metal seed layer. In an embodiment, the patterned metal seed layer can be formed in alignment with the first and second semiconductor regions 410, 412.

[0047] Alternative embodiments used in the manufacture of solar cells can include forming the first metal layer 434 without a protective region 428. In this particular embodiment, energetic ions and ionizing radiation can impinge upon separation region 414 of the substrate 406 during metallization processes. In an example, ionizing radiation can include electromagnetic radiation such as in the ultraviolet (UV) and/or x-ray wavelengths. This

metallization-induced damage at the separation region 414 can reduce charge carrier lifetime and cause overall solar cell performance degradation. One way to recover the charge carrier lifetime would be to perform an anneal at high temperatures, in an example, greater than 300 degrees Celsius. In this manner, materials used in the fabrication of the solar cell would be required to be thermally stable at high temperatures, e.g., exposure to greater than 300 degrees Celsius for a duration of 5-30 minutes. In an embodiment, forming the protective region 428, as described above, can eliminate the need for using a subsequent heating and/or annealing process to recover charger carrier lifetime lost subsequent to the formation of the first metal layer 432. In one embodiment, forming the protective region 428 allows for the use of fabrication materials on the solar cell that are thermally stable at temperatures less or equal to 300 degrees Celsius. In an embodiment, using the protective region 428 can allow for performing a reduced heating and/or annealing process subsequent to forming the first metal layer 434. In an example, the reduced heating and/or annealing process can be performed at temperatures less than or equal to 300 degrees Celsius. Figure 8 illustrates performing an optional heating operation subsequent to forming the protective region 428.

[0048] Referring to Figure 8, subsequent to forming the first metal layer 432, the substrate 406 can be heated 435. In an example, the substrate can be heated 435 at temperatures of less than or equal to 300 degrees Celsius. In an embodiment, heating 435 the substrate 406 can include performing an annealing process. Performing an annealing process can reduce contact resistance between the first metal layer 434 and the semiconductor regions 410, 412. In one embodiment, the protective region 428 can prevent and/or inhibit damage during the heating process 435. In an embodiment, the heating 435 need not be performed, where the protective region 428 can prevent and/or inhibit damage to the separation region 414 during the formation of the first metal layer 432 (e.g. during a sputtering process).

[0049] Referring to Figures 9-12, and corresponding operation 110 of flowchart 100, conductive contacts can be formed over the first and second semiconductor regions of the solar cell.

[0050] In an exemplary process flow, Figures 9-12 illustrate cross-sectional views of various stages in one example method for forming conductive contacts for a solar cell, in accordance with an embodiment of the present disclosure. In an embodiment, the method of Figures 9-12 can include performing a plating and etching process. In an exemplary process flow, Figures 13 and 14 illustrate cross-sectional views of various stages in another method for forming conductive contacts for a solar cell, in accordance with an embodiment of the present

disclosure. In an embodiment, the method of Figures 13 and 14 can include performing a metal foil based bonding and etching process.

[0051] In an exemplary process flow, Figure 2 is a flowchart 200 listing operations in one example method for forming conductive contacts for a solar cell corresponding to Figures 9-12, according to some embodiments. As shown, the solar cell of Figures 9-12 have similar reference numbers to elements of the solar cell of Figures 4-8, where like reference numbers refer to similar elements throughout the figures. In an embodiment, the structure of the solar cell of Figures 9-12 is substantially similar to the structure of the solar cell of Figures 4-8, except as described below. Unless otherwise specified below, the numerical indicators used to refer to components in Figures 9-12 are similar to those used to refer to components or features in Figures 4-8 above, except that the index has been incremented by 100. Therefore the description of corresponding portions of Figures 4-8 applies equally to the description of Figure 9-12, except as described below. In various embodiments, the method of Figure 2 can include additional (or fewer) blocks than illustrated. For example, in some embodiments, a mask need not be removed at block 206, where the mask can instead be removed during an etching process at block 208. Accordingly, the exemplary process flow moves from the structure of Figure 8 to the structure of Figure 9.

[0052] Referring to Figure 9 and corresponding operation 202 of flowchart 200, a mask 538 can be formed over a first metal seed layer 532, according to some embodiments. In an embodiment, the mask 538 can protect portions 534 of the first metal layer 532 during a subsequent plating process, while exposed regions 536 can be plated during said plating process. In an embodiment, the mask 538 can be formed by screen printing, inkjet printing, among other printing processes. In one embodiment, the mask 538 can be an etch resist. In one embodiment, the etch resist can be an etch resist 538 commonly used in the fabrication or manufacture of solar cells. In some embodiments, the etch resist 538 is a plating resist.

[0053] Referring to Figure 10 and corresponding operation 204 of flowchart 200, a second metal layer 540 can be plated on exposed portions 536 of the first metal layer 532. In an embodiment, a plating process can be performed to form the second metal layer 540 on exposed portions 536 of the first metal layer 532, where the mask 538 can protect portions 534 of the first metal layer 532 during the plating process (534 shown in Figure 9). In an example, copper, tin, and/or nickel, among other metals, can be plated to exposed portions 536 of the first metal layer 532.

[0054] Referring to Figure 10, Figure 11 and corresponding operation 206 of flowchart 200, the mask 538 of Figure 10 can be removed. In an embodiment, the mask 538 can be

removed using a wet chemical process. In an example, an ink stripping process can be performed to remove the mask 538.

[0055] Referring to Figure 10, Figure 11 and corresponding operation 208 of flowchart 200, the first metal layer 532 of Figure 10 can be patterned to form a first conductive contact 542 and/or second conductive contact 544, respectively. In an embodiment, the patterning includes etching the first metal layer 532 of Figure 10 using one or more etchants. In an embodiment, a hydroxide-based wet etchant can be used. In one example, the etchant can include potassium hydroxide, tetramethylammonium hydroxide, ammonium hydroxide and/or sodium hydroxide. In some embodiments, the etchant can include an etchant having a weight percent of greater than 2% potassium hydroxide. In an embodiment, referring to Figure 10 and subsequent to removing the mask 538, portions 534 of the first metal layer 532 can be etched, where the second metal layer 540 can prevent etching other portions 536 of the first metal layer 532 during the etching process. As shown, the protective region 528 can be left over the separation region 514. In some embodiments, the patterning can include removing the protective region 528. In an example, an etching process can be performed to remove the mask 538 and, subsequently, the protective region 528. In an example, the etching processes discussed above can be used to remove the protective region 528. In an example, Figure 11 shows a solar cell 500 with the protective region 528 and Figure 12 shows a solar cell 500 subsequent to the removal of the protective region 528.

[0056] Referring to Figure 11 and 12, a solar cell 500 is shown fabricated using the methods of Figures 4-11 and corresponding to the operations of the flowcharts 100 and 200 of Figures 1 and 2, respectively. As shown, the solar cell 500 of Figures 11 and 12 have similar reference numbers to elements of the solar cell 400 of Figures 4-8, where like reference numbers refer to similar elements throughout the figures. In an embodiment, the structure of the solar cell 500 of Figures 11 and 12 are substantially similar to the structure of the solar cell 400 of Figures 4-8, except as described above. Unless otherwise specified below, the numerical indicators used to refer to components in Figures 11 and 12 are similar to those used to refer to components or features in Figures 4-10 above, except that the index has been incremented by 100. Therefore the description of corresponding portions of Figures 4-8 applies equally to the description of Figures 11 and 12. In an example, referring to Figures 4-8, Figure 11, and Figure 12, the first and second semiconductor region 410, 412 of Figures 4-8 can correspond to the first and second semiconductor region 510, 512 of Figures 11 and 12. In one example, referring to Figure 8 and Figure 11, the protective region 428 of Figure 8 can correspond to the protective region 528 of Figure 11.

[0057] Referring to Figures 11 and 12, in an embodiment, a solar cell 500 includes a substrate 506. In an embodiment, a first and second semiconductor regions 510, 512 are disposed in (not shown) or above (as shown) the substrate 506. In one embodiment, an intervening layer 520 is in alignment with locations between the first and second semiconductor regions 510 and 512. In an embodiment, the intervening layer 520 includes openings. Referring to Figure 11, in one embodiment, a protective region 528 is disposed over separation regions 514. In an embodiment, the protective regions 528 include a polymer. In an example, the protective region 528 includes a polyimide, silicone, polymeric silsesquioxane, epoxy or acrylic. In an embodiment, a plurality of conductive contact structures 542, 544 are electrically connected to the first and second semiconductor regions 510 and 512. In an embodiment, the conductive contacts 542, 544 include a first metal layer 532 (e.g., a metal seed layer) and a second metal layer 540 (e.g., a plated metal layer). In an embodiment, the conductive contacts 542, 544 can be referred to as plated conductive contacts (e.g., at least a portion of the conductive contacts formed from a plating process). In one particular embodiment, for example where plated conductive contacts are formed, the protective region 428 can include reflective pigments such as titanium oxide (TiO2). In one particular embodiment, for example where plated conductive contacts are formed, the protective region 428 can include polyimide. In an embodiment, the protective regions 528 increase a solar energy absorbance efficiency of the solar cell 500. In one such embodiment, improved back side reflection of IR type wavelength light is achieved. That is, typical losses from IR transmission, in particular as seen the separation region 514 (e.g., textured trenches), may be recovered by using a reflective material on the rear side designed to reflect the longer wavelengths into the cell. Thus, in an embodiment, the protective regions 528 can include a reflective material. In an embodiment, the reflective material can include reflective pigments such as titanium oxide (TiO2) to reflect light, e.g., longer wavelengths, into the cell. In some embodiments, the protective region 528 of Figure 11 is removed as shown in the solar cell 500 of Figure 12.

[0058] In an exemplary process flow, Figure 3 is a flowchart 300 listing operations in another example method for forming conductive contacts for a solar cell corresponding to Figures 13 and 14, according to some embodiments. As shown, the solar cell of Figures 13 and 14 have similar reference numbers to elements of the solar cell of Figures 4-8, where like reference numbers refer to similar elements throughout the figures. In an embodiment, the structure of the solar cell of Figures 13 and 14 are substantially similar to the structure of the solar cell of Figures 4-8, except as described below. Unless otherwise specified below, the numerical indicators used to refer to components in Figures 13 and 14 are similar to those used

to refer to components or features in Figures 4-8 above, except that the index has been incremented by 200. Therefore the description of corresponding portions of Figures 4-8 applies equally to the description of Figures 13 and 14, except as described below. In various embodiments, the method of Figure 3 can include additional (or fewer) blocks than illustrated. For example, in some embodiments, a mask can be formed before patterning at block 306 and subsequently removed after block 306. Accordingly, the exemplary process flow moves from the structure of Figure 8 to the structure of Figure 13.

[0059] Referring to Figure 13 and corresponding operation 302 of flowchart 300, a metal foil 640 is placed over a first metal layer 632. In an embodiment, the metal foil is an aluminum foil. In an embodiment, the metal foil 640 can be pre-patterned and placed over the first and second semiconductor regions 610, 612. In an example, a patterned metal foil can be placed over the first and second semiconductor regions 610, 612. In one example, the patterned metal foil can follow a pattern in alignment with the first and second semiconductor regions 610, 612.

[0060] Referring to Figure 13 and corresponding operation 304 of flowchart 300, the metal foil 640 of Figure 13 is bonded or otherwise joined to the first metal layer 632. In an example, the bonding can include welding the metal foil 640 to the first metal layer 632. In an embodiment, the metal foil 640 is bonded to the first metal layer 632 at weld regions 648. In one such embodiment, the weld regions 648 are formed at locations above the first and second semiconductor regions 610 and 612, as is depicted in Figure 13. In a specific such embodiment, a technique such as, but not limited to, a laser welding process, a thermal compression process or an ultrasonic bonding process is used to bond the metal foil 640 to the first metal layer 632.

[0061] In an embodiment, metal foil 640 is an aluminum (Al) foil having a thickness approximately in the range of 5-100 microns and, preferably, a thickness of less than approximately in the range of 50 microns. In one embodiment, the Al foil is an aluminum alloy foil including aluminum and second element such as, but not limited to, copper, manganese, silicon, magnesium, zinc, tin, lithium, or combinations thereof. In one embodiment, the Al foil is a temper grade foil such as, but not limited to, F-grade (as fabricated), O-grade (full soft), H-grade (strain hardened) or T-grade (heat treated).

[0062] Referring to Figure 14 and corresponding operation 306 of flowchart 300, a patterning process is performed through the metal foil 640 in alignment with the locations between the first and second semiconductor regions 610 and 612 to isolate 650 regions of remaining metal foil 640 in alignment with the first and second semiconductor regions 610 and 612. In one embodiment, additional to preventing and/inhibiting damage to a separation region 614 during the formation of a first metal layer, the protective region 628 can protect, and/or

inhibit, damage to a separation region during the patterning process. In an embodiment, the patterning can include performing a laser ablation process. In an example, the laser ablating through the metal foil 640 involves using a laser having a wavelength. In an embodiment, the protective region 628 can include an opacifying pigment for scattering or absorbing light of the wavelength of the laser. In an embodiment, the laser ablation is performed mask-free; however, in other embodiments, a mask layer is formed on a portion of the metal foil 640 of Figure 13 prior to laser ablating, and is removed subsequent to laser ablating. In an example, a mask can be formed prior to the patterning at block 306 and removed subsequent to the patterning at 306. In the embodiment where a patterned metal foil is used, the patterning process need not be performed.

[0063] Embodiments described herein include fabrication of a solar cell according to one or more of the above described approaches. Referring to Figure 14, in an embodiment, a solar cell 600 includes a substrate 606. A first and second semiconductor regions 610, 612 are disposed in (not shown) or above (as shown) the substrate 606. An intervening layer 620 is in alignment with locations between the first and second semiconductor regions 610 and 612. In an embodiment, the intervening layer 620 includes openings. In one embodiment, a protective regions 628 includes a polymer. In an example, the protective region 628 includes a polyimide, silicone, polymeric silsesquioxane, epoxy or acrylic. A plurality of conductive contact structures 642, 644 are electrically connected to the first and second semiconductor regions 610 and 612. Each conductive contact structure 642, 644 includes a metal foil portion 640 disposed above and in alignment with a corresponding first and second semiconductor regions 610 and 612. In an embodiment, referring particularly to Figure 14, each conductive contact structure 642, 644 further includes a first metal layer 632 (e.g., a metal seed layer) disposed directly between the corresponding one of the first and second semiconductor regions 610 and 612 and the metal foil portion 640. In an embodiment, the first metal layer 632 can contact the first and second semiconductor regions 610, 612 at the openings of the intervening layer 620.

[0064] Referring to Figure 14, in an embodiment, the protective regions 628 increase a solar energy absorbance efficiency of the solar cell 600. In one such embodiment, improved back side reflection of IR type wavelength light is achieved. That is, typical losses from IR transmission, in particular as seen the separation region 614 (e.g., textured trenches), may be recovered by using a reflective material on the rear side designed to reflect the longer wavelengths into the cell. Thus, in an embodiment, the protective regions 628 can include reflective pigments such as titanium oxide (TiO2) to reflect light, e.g., longer wavelengths, into the cell.

[0065] In some embodiments, for example where the protective region 628 includes polysilicon, the protective region 628 can be removed. In one embodiment, the polysilicon region can be removed by a subsequent mask and etch process.

[0066] In an embodiment, although the solar cells 4-14 shown are back-side contact solar cells, the methods and structures described above can be used for front-side contact solar cells.

[0067] Although specific embodiments have been described above, these embodiments are not intended to limit the scope of the present disclosure, even where only a single embodiment is described with respect to a particular feature. Examples of features provided in the disclosure are intended to be illustrative rather than restrictive unless stated otherwise. The above description is intended to cover such alternatives, modifications, and equivalents as would be apparent to a person skilled in the art having the benefit of this disclosure.

[0068] The scope of the present disclosure includes any feature or combination of features disclosed herein (either explicitly or implicitly), or any generalization thereof, whether or not it mitigates any or all of the problems addressed herein. Accordingly, new claims may be formulated during prosecution of this application (or an application claiming priority thereto) to any such combination of features. In particular, with reference to the appended claims, features from dependent claims may be combined with those of the independent claims and features from respective independent claims may be combined in any appropriate manner and not merely in the specific combinations enumerated in the appended claims.

CLAIMS

What is claimed is:

1. A method of fabricating a solar cell, the method comprising:

forming a first and second semiconductor regions in or above a substrate, wherein a separation region is disposed between the first and second semiconductor regions;

forming a polysilicon region over the separation region;

forming an insulating layer between the polysilicon region and substrate, wherein the insulating layer includes openings;

forming a first metal layer over the polysilicon region, insulating layer and within the openings of the insulating layer, wherein the polysilicon region inhibits damage to the separation region during the formation of the first metal layer; and

forming conductive contacts over the first and second semiconductor regions; and

removing the polysilicon region.

2. The method of claim 1, wherein forming the first metal layer comprises performing a sputtering process to form the first metal layer over the polysilicon region, insulating layer and within the openings of the insulating layer, wherein the polysilicon region inhibits damage to the separation region during the sputtering process.

3. The method of claim 1, wherein the separation region is a trench region.

4. The method of claim 1, wherein forming the first metal layer comprises forming a metal seed layer over the polysilicon region, insulating layer and within the openings of the insulating layer.

5. The method of claim 1, wherein forming the first metal layer comprises forming a patterned metal seed layer over the polysilicon region, insulating layer and within the openings of the insulating layer.

6. The method of claim 1, wherein forming the polysilicon region over the separation region comprises depositing the polysilicon region over the separation region.

7. The method of claim 1, wherein forming the polysilicon region over the separation region comprises:

forming a blanket polysilicon layer over the substrate;

forming a mask over portions of the blanket polysilicon layer;

etching exposed portions of the blanket polysilicon layer to form a polysilicon region over the separation region; and

removing the mask.

8. The method of claim 1, wherein forming conductive contacts over the first and second semiconductor regions comprises:

forming a mask over portions of the first metal layer;

plating a second metal layer to exposed portions of the first metal layer;

removing the mask; and

performing an etching process to form conductive contacts over the first and second semiconductor regions.

9. The method of claim 1, wherein forming conductive contacts over the first and second semiconductor regions comprises:

placing a metal foil over the first metal layer;

bonding the metal foil to the first metal layer; and

patterning the metal foil and first metal layer to form conductive contacts over the first and second semiconductor regions.

10. A method of fabricating a solar cell, the method comprising:

forming a first and second semiconductor regions in or above a substrate, wherein a separation region is disposed between the first and second semiconductor regions;

forming a protective region over the separation region;

forming an insulating layer between the protective region and substrate, wherein the insulating layer includes openings;

forming a first metal layer over the protective region, insulating layer and within the openings of the insulating layer, wherein the protective region inhibits damage to the separation region during the formation of the first metal layer;

forming a mask over portions of the first metal layer;

plating a second metal layer to exposed portions of the first metal layer;

removing the mask; and

performing an etching process to form conductive contacts over the first and second semiconductor regions.

11. The method of claim 10, wherein forming a protective region over the separation region comprises forming a protective region thermally stable at temperatures of at less than or equal to 300 degrees Celsius.

12. The method of claim 10, wherein forming the first metal layer comprises performing a sputtering process to form the first metal layer over the protective region, insulating layer and within the openings of the insulating layer, wherein the protective region inhibits damage to the separation region during the sputtering process.

13. The method of claim 10, further comprising:

heating the substrate to a temperature of less than or equal to 300 degrees Celsius, wherein the protective region inhibits damage to the separation region during the heating.

14. The method of claim 10, wherein the separation region is a trench region.

15. The method of claim 10, wherein forming the first metal layer over the protective region, insulating layer and within the openings of the insulating layer comprises forming a metal seed layer over the protective region, insulating layer and within the openings of the insulating layer.

16. The method of claim 10, wherein forming the protective region over the separation region comprises forming a polymer over the separation region.

17. The method of claim 16, wherein forming the polymer over the separation regions comprises forming a polyimide, silicone, polymeric silsesquioxane, epoxy or acrylic over the separation region.

18. A method of fabricating a solar cell, the method comprising:

forming a first and second semiconductor regions in or above a substrate, wherein a separation region is disposed between the first and second semiconductor regions;

forming a protective region over the separation region;

forming an insulating layer between the protective region and substrate, wherein the insulating layer includes openings;

forming a first metal layer over the protective region, insulating layer and within the openings of the insulating layer, wherein the protective region inhibits damage to the separation region during the formation of the first metal layer;

placing a metal foil over the first metal layer;

bonding the metal foil to the first metal layer; and

patterning the metal foil and first metal layer to form conductive contacts over the first and second semiconductor regions.

19. The method of claim 18, wherein forming a protective region over the separation region comprises forming a protective region thermally stable at temperatures of less than or equal to 300 degrees Celsius.

20. The method of claim 18, wherein forming the first metal layer comprises performing a sputtering process to form the first metal layer over the protective region, insulating layer and within the openings of the insulating layer, wherein the protective region inhibits damage to the separation region during the sputtering process.

21. A solar cell comprising:

a first and second semiconductor regions disposed in or above a substrate, wherein a separation region is disposed between the first and second semiconductor regions;

a protective region disposed over the separation region, wherein the protective region comprises a reflective pigments; and

plated conductive contacts disposed over the first and second semiconductor regions.

22. The solar cell of claim 21, wherein the protective region comprises silicone, polyimide, polymeric silsesquoixane, epoxy or acrylic.

23. The solar cell of claim 21, wherein the reflective pigments include titanium oxide (TiO2).

24. The solar cell of claim 21, wherein first semiconductor region is N-type and the second semiconductor region is P-type.

25. The solar cell of claim 21, wherein the first and second semiconductor regions are disposed on a back side of the solar cell.

26. The solar cell of claim 21, wherein the separation region is a trench region.

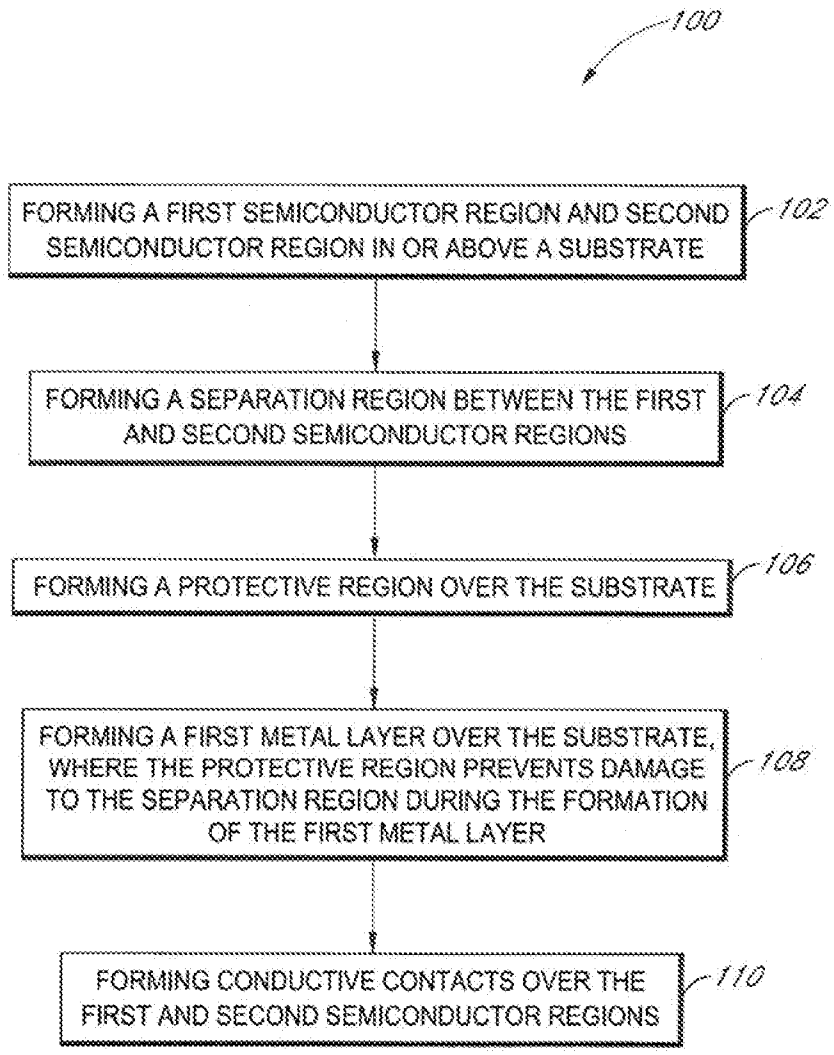
100
FORMING A FIRST SEMICONDUCTOR REGION AND SECOND SEMICONDUCTOR REGION IN OR ABOVE A SUBSTRATE
102
FORMING A SEPARATION REGION BETWEEN THE FIRST AND SECOND SEMICONDUCTOR REGIONS
104
FORMING A PROTECTIVE REGION OVER THE SUBSTRATE
106
FORMING A FIRST METAL LAYER OVER THE SUBSTRATE, WHERE THE PROTECTIVE REGION PREVENTS DAMAGE TO THE SEPARATION REGION DURING THE FORMATION OF THE FIRST METAL LAYER
108
FORMING CONDUCTIVE CONTACTS OVER THE FIRST AND SECOND SEMICONDUCTOR REGIONS
110

FIG. 1

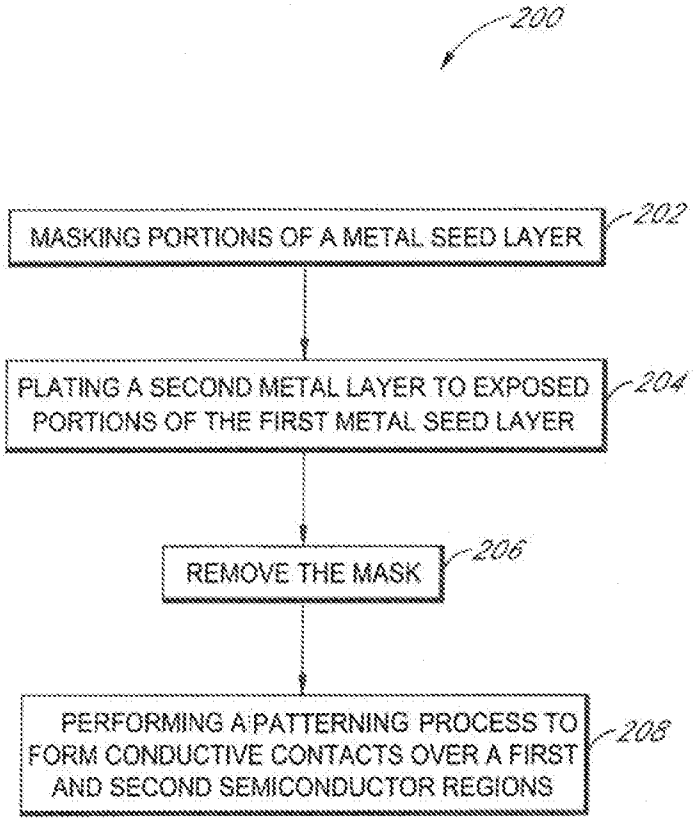
200
MASKING PORTIONS OF A METAL SEED LAYER
202
PLATING A SECOND METAL LAYER TO EXPOSED PORTIONS OF THE FIRST METAL SEED LAYER
204
REMOVE THE MASK
206
PERFORMING A PATTERNING PROCESS TO FORM CONDUCTIVE CONTACTS OVER A FIRST AND SECOND SEMICONDUCTOR REGIONS
208

FIG. 2

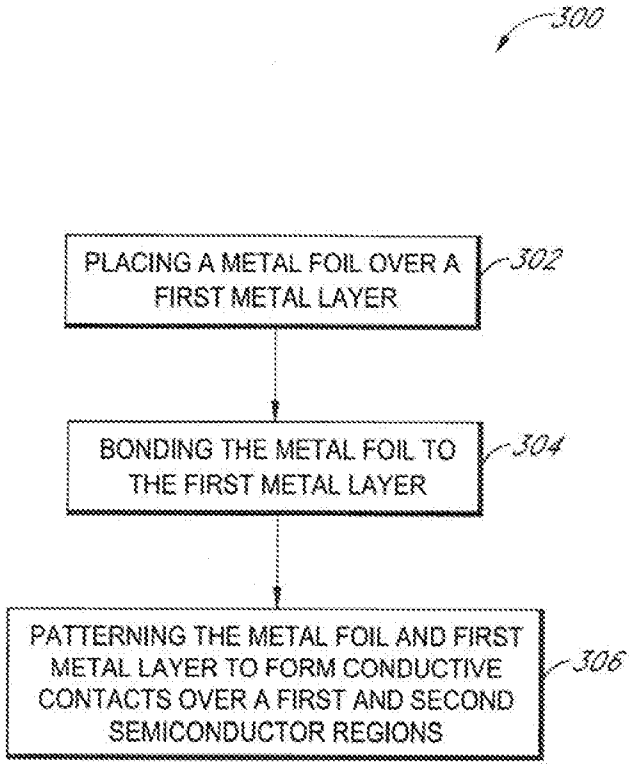
300
PLACING A METAL FOIL OVER A FIRST METAL LAYER
302
BONDING THE METAL FOIL TO THE FIRST METAL LAYER
304
PATTERNING THE METAL FOIL AND FIRST METAL LAYER TO FORM CONDUCTIVE CONTACTS OVER A FIRST AND SECOND SEMICONDUCTOR REGIONS
306

FIG. 3

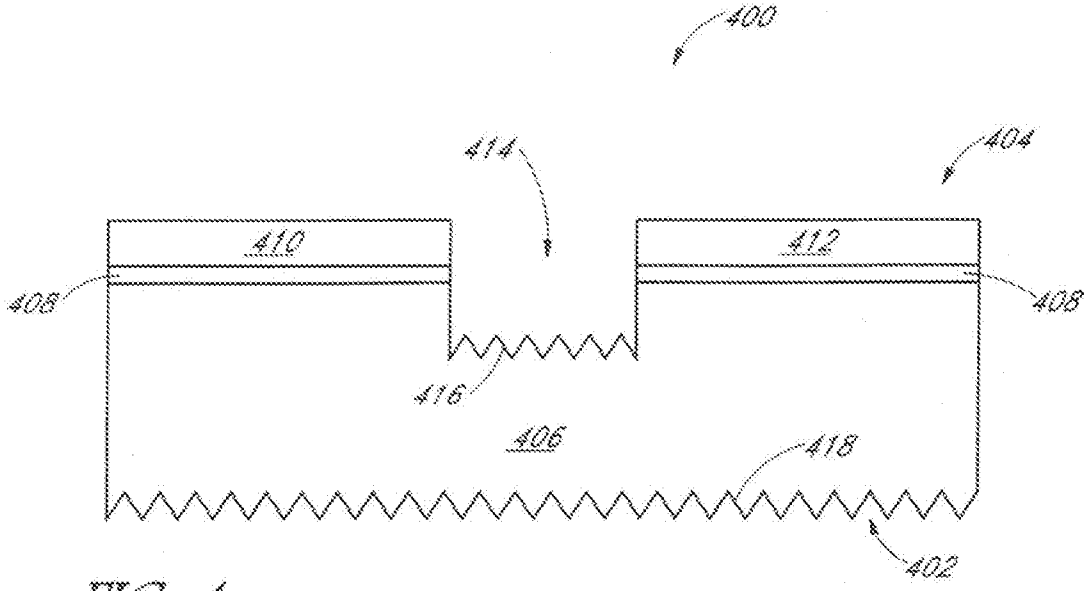
400
414
404
410
412
408
408
416
406
418
402

FIG. 4

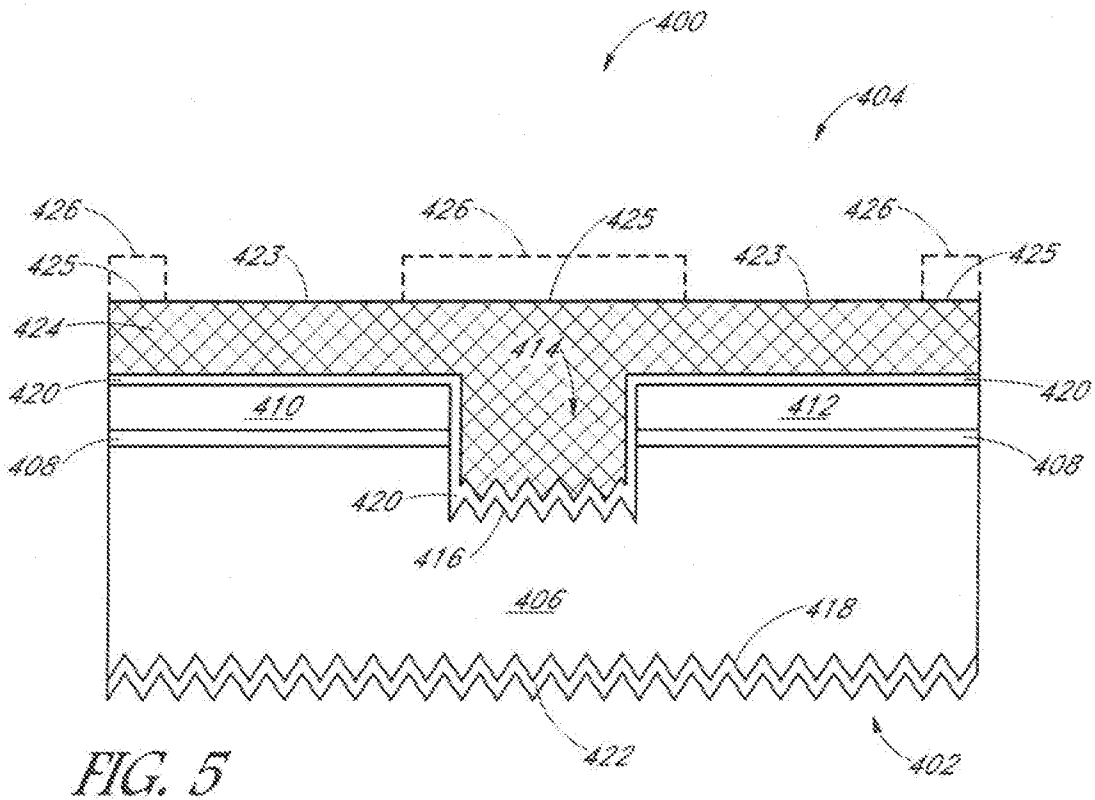
400
404
426
426
425
426
425
425
425
424
414
420
420
410
412
408
408
420
416
406
418
422
402

FIG. 5

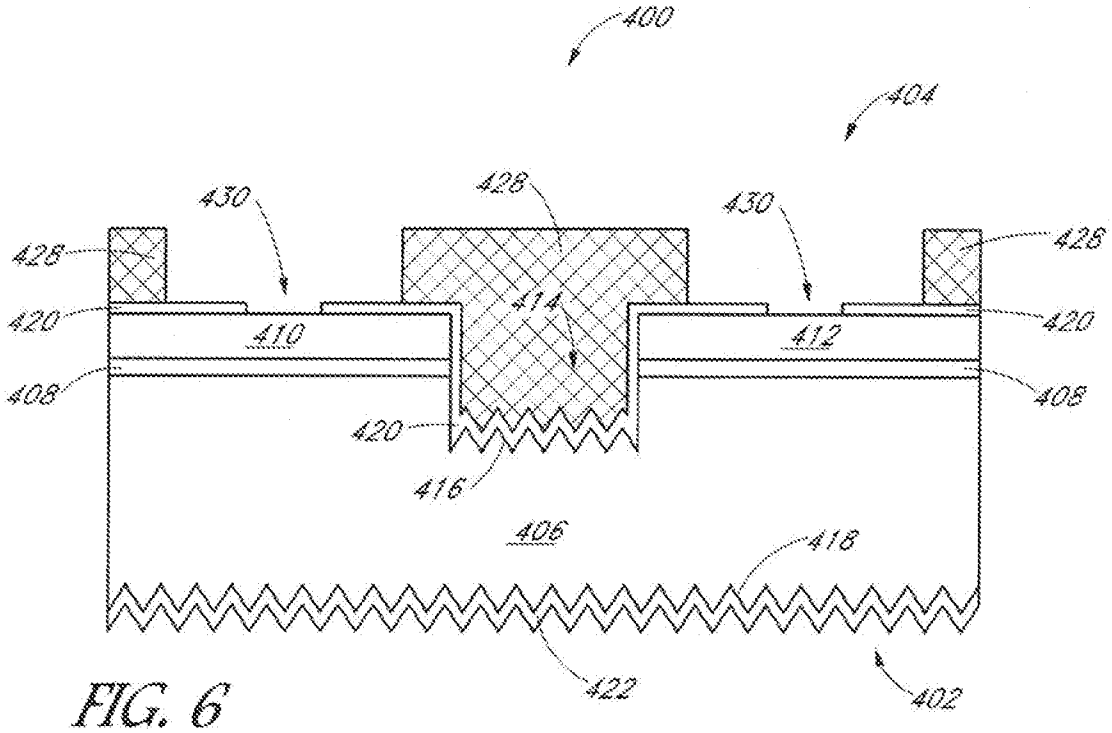
400
404
430
428
430
428
428
420
410
414
412
420
408
408
420
416
406
418
422
402

FIG. 6

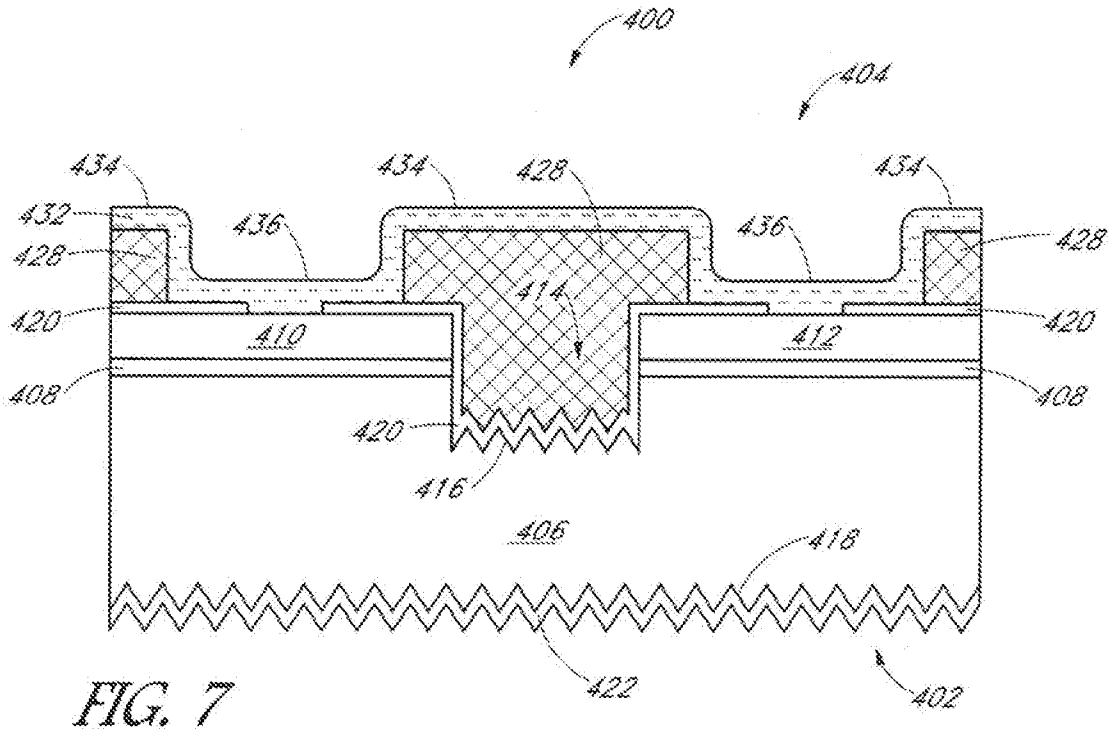
400
404
434
434
428
434
432
436
436
428
428
420
410
414
412
420
408
408
420
416
406
418
422
402

FIG. 7

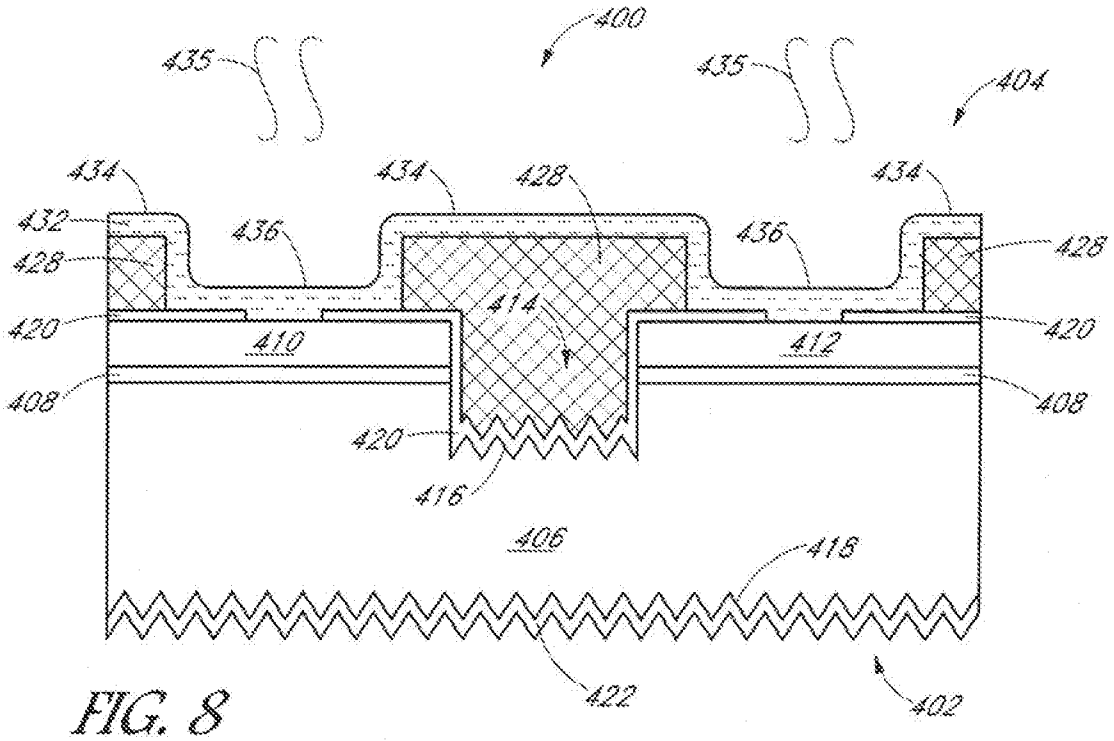
400
435
435
404
434
434
428
434
432
436
436
428
428
420
410
414
412
420
408
408
420
416
406
416
422
402

FIG. 8

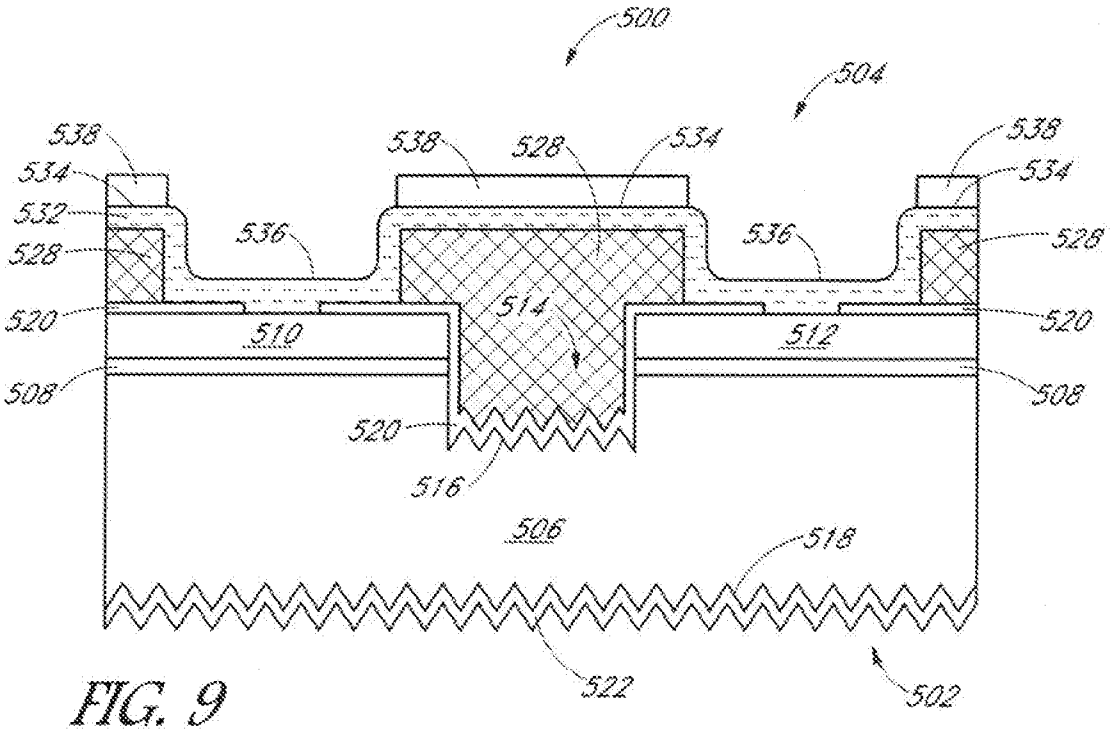
500
504
538
538
528
534
538
534
534
532
536
536
528
528
520
510
514
512
520
508
508
520
516
506
518
522
502

FIG. 9

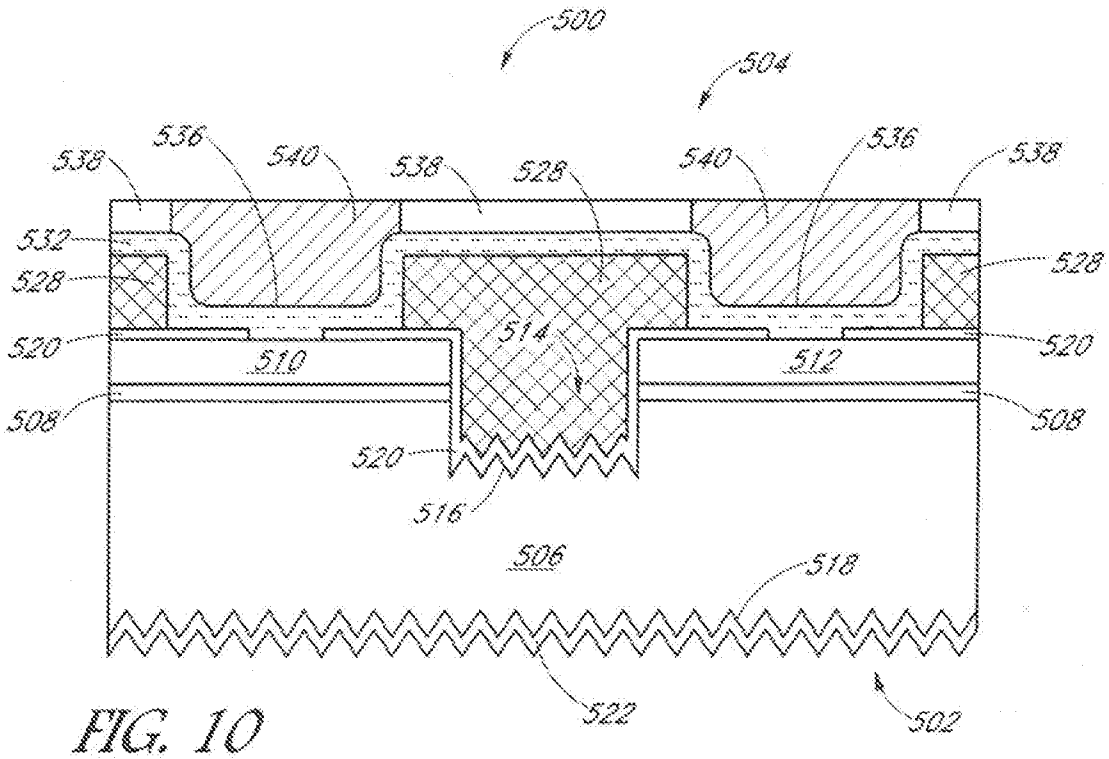
500
504
538
536
540
538
525
540
536
538
532
528
528
520
510
514
512
520
508
508
520
516
506
518
522
502

FIG. 10

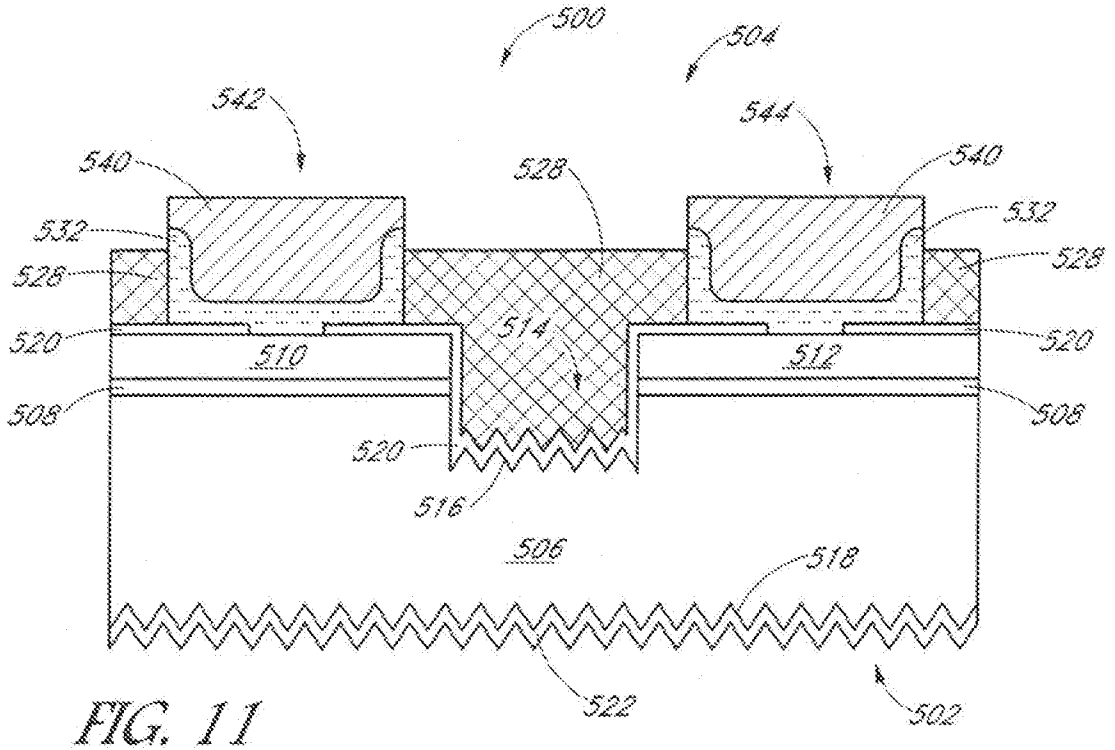
500
504
542
544
540
528
540
532
532
528
525
520
510
514
512
520
508
508
520
516
506
518
522
502

FIG. 11

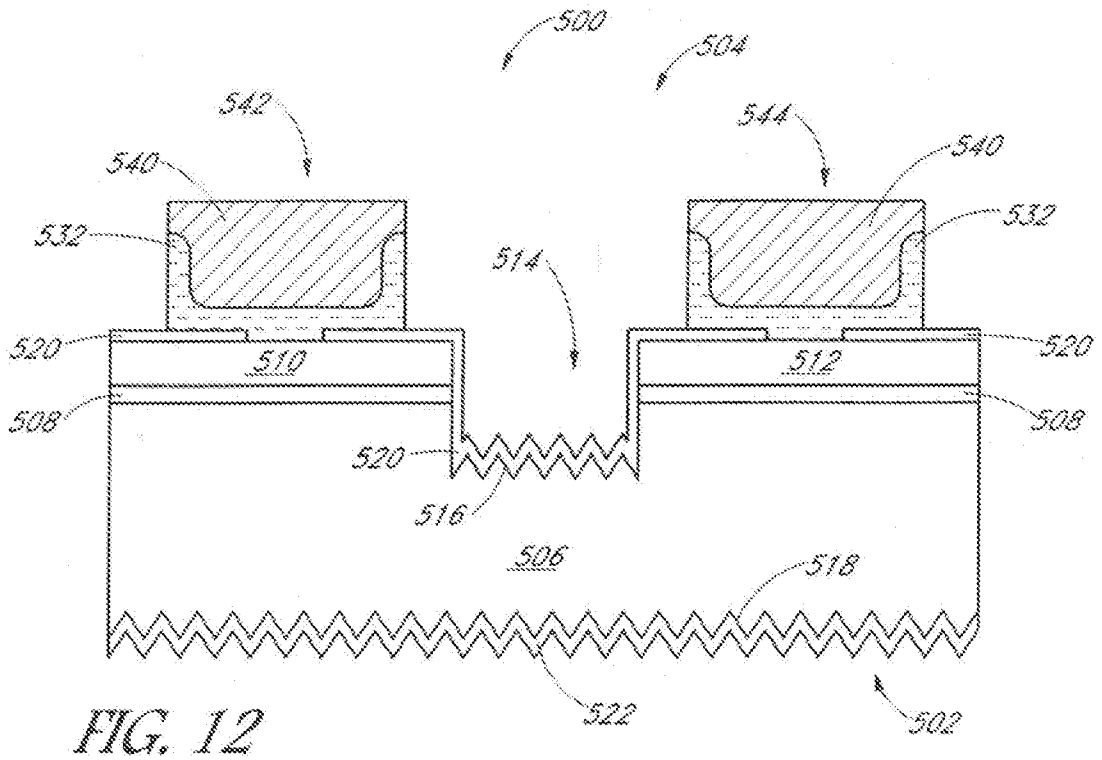
500
504
542
544
540
540
532
532
514
520
510
512
520
508
508
520
516
506
518
522
502

FIG. 12

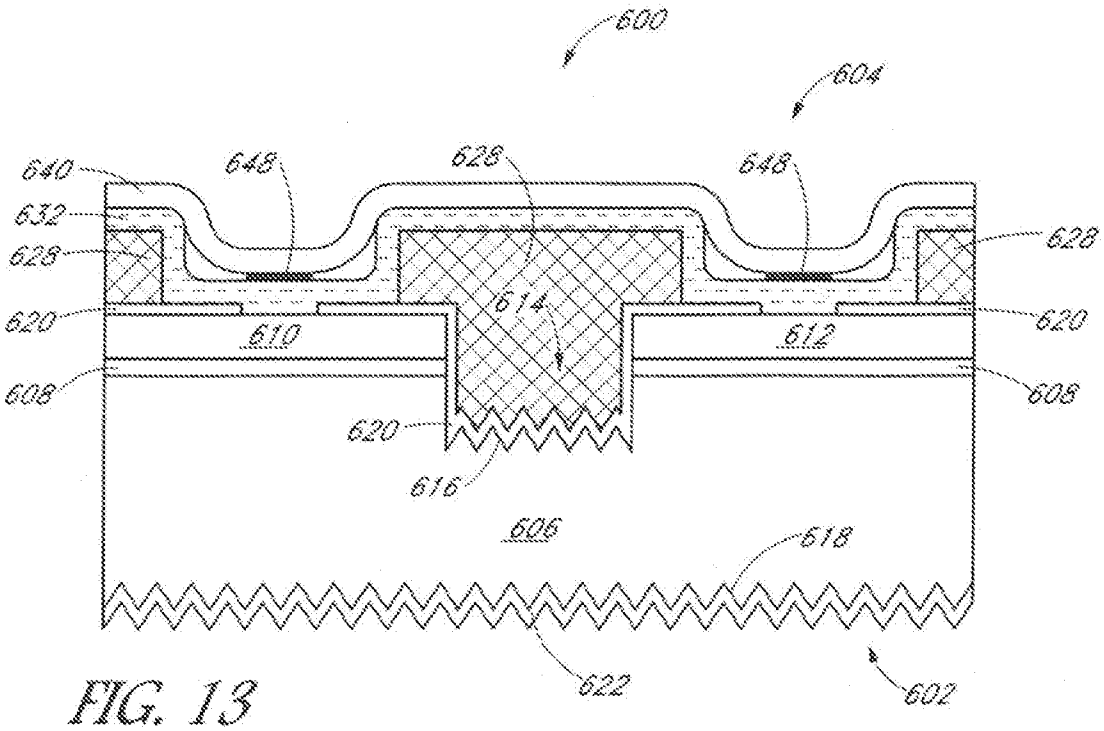
600
604
640
648
628
648
632
628
628
620
614
620
610
612
608
608
620
616
606
618
622
602

FIG. 13

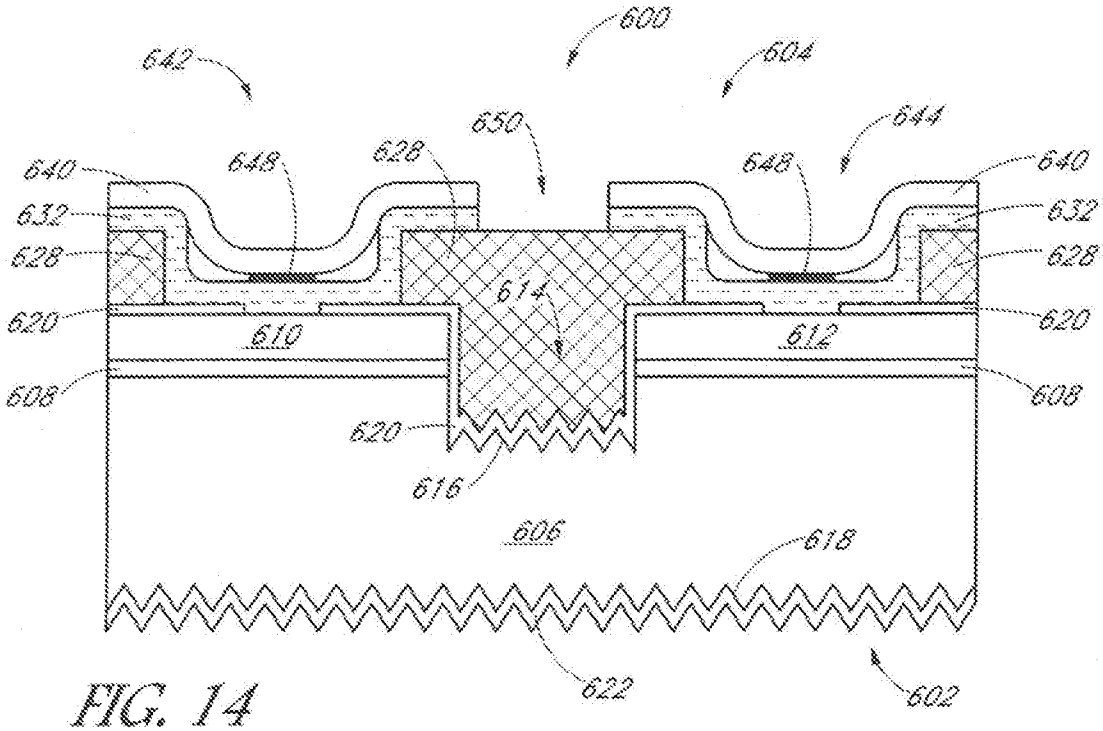
600
642
604
644
650
640
648
628
632
614
610
612
620
608
616
606
618
622
602

FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/039333

A. CLASSIFICATION OF SUBJECT MATTER

H01L 31/18(2006.01)i, H01L 31/0368(2006.01)i, H01L 31/0236(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 31/18; H01L 31/02; H01L 31/0224; H01L 31/065; H01L 31/00; H01L 31/0368; H01L 31/0236

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: solar cell, insulating layer, polysilicon region, trench region, conductive contact, metal layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016-0181447 A1 (TAESEOK KIM et al.) 23 June 2016 See paragraphs [0035]-[0048]; and figures 1A-1F.	21-26
Y		1-20
Y	US 2014-0130854 A1 (SAMSUNG SDI CO., LTD.) 15 May 2014 See paragraphs [0066]-[0068]; and figures 4K-4L.	1-20
Y	US 7339110 B1 (WILLIAM P. MULLIGAN et al.) 04 March 2008 See column 5, lines 16-35; and figures 13-15.	8,10-17
A	US 2015-0280029 A1 (GABRIEL HARLEY et al.) 01 October 2015 See paragraphs [0038]-[0051]; and figures 1A-2.	1-26
A	US 2015-0090329 A1 (SUNPOWER CORPORATION) 02 April 2015 See paragraphs [0015]-[0026]; and figures 1-7.	1-26

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 October 2017 (12.10.2017)	**12 October 2017 (12.10.2017)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
KIM, Seong Woo
Telephone No. +82-42-481-3348

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/039333

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2016-0181447 A1	23/06/2016	US 2017-0179312 A1	22/06/2017
		US 9620661 B2	11/04/2017
US 2014-0130854 A1	15/05/2014	CN 103811572 A	21/05/2014
		EP 2731146 A2	14/05/2014
		EP 2731146 A3	03/09/2014
		JP 2014-096574 A	22/05/2014
		KR 10-2014-0061953 A	22/05/2014
US 7339110 B1	04/03/2008	US 7883343 B1	08/02/2011
		US 7897867 B1	01/03/2011
		US 8399287 B1	19/03/2013
US 2015-0280029 A1	01/10/2015	AU 2015-236206 A1	07/07/2016
		CN 106170870 A	30/11/2016
		DE 112015001529 T5	15/12/2016
		JP 2017-511597 A	20/04/2017
		KR 10-2016-0139008 A	06/12/2016
		TW 201543699 A	16/11/2015
		WO 2015-148571 A1	01/10/2015
US 2015-0090329 A1	02/04/2015	AU 2014-327036 A1	17/12/2015
		CN 105474412 A	06/04/2016
		EP 3050122 A1	03/08/2016
		JP 2016-536808 A	24/11/2016
		KR 10-2016-0061368 A	31/05/2016
		MX 2016003561 A	02/06/2016
		SG 11201601079 A	30/03/2016
		TW 201521220 A	01/06/2015
		US 2016-0343888 A1	24/11/2016
		US 9437756 B2	06/09/2016
		WO 2015-047952 A1	02/04/2015