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(54) **Title:** METHOD FOR FORMING SELF-ALIGNED DUAL SALICIDE IN CMOS TECHNOLOGIES

(57) **Abstract:** A method of fabricating a complementary metal oxide semiconductor (CMOS) device, wherein the method comprises forming a first well region (103) in a semiconductor substrate (102) for accommodation of a first type semiconductor device (130); forming a second well region (104) in the semiconductor substrate (102) for accommodation of a second type semiconductor device (140); shielding the first type semiconductor device (130) with a mask (114); depositing a first metal layer (118) over the second type semiconductor device (140); performing a first salicide formation on the second type semiconductor device (140); removing the mask (114); depositing a second metal layer (123) over the first and second type semiconductor devices (130,140); and performing a second salicide formation on the first type semiconductor device (130). The method requires only one pattern level and it eliminates pattern overlay as it also simplifies the processes to form different suicide material over different devices.

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# INTERNATIONAL SEARCH REPORT

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<b>B. FIELDS SEARCHED</b> Minimum documentation searched (classification system followed by classification symbols) U.S. : 438/199,233,586,664,682,FOR216,FOR187  Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched  Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	Applicant's Admitted Prior Art, Figs. 2 and 3.	1,3,4,6-8 and 10
Y	US 6,787,464 (CHEEK et al.) 7 September 2004 (07.09.2004), Fig. 2C, Col. 5, lines 9-11.	1,3,4,4,6-8 and 10
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
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