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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : G06F 15/66	A1	(11) International Publication Number: WO 92/01995
		(43) International Publication Date: 6 February 1992 (06.02.92)

(21) International Application Number: PCT/US91/05034

(22) International Filing Date: 17 July 1991 (17.07.91)

(30) Priority data:
554,327 19 July 1990 (19.07.90) US

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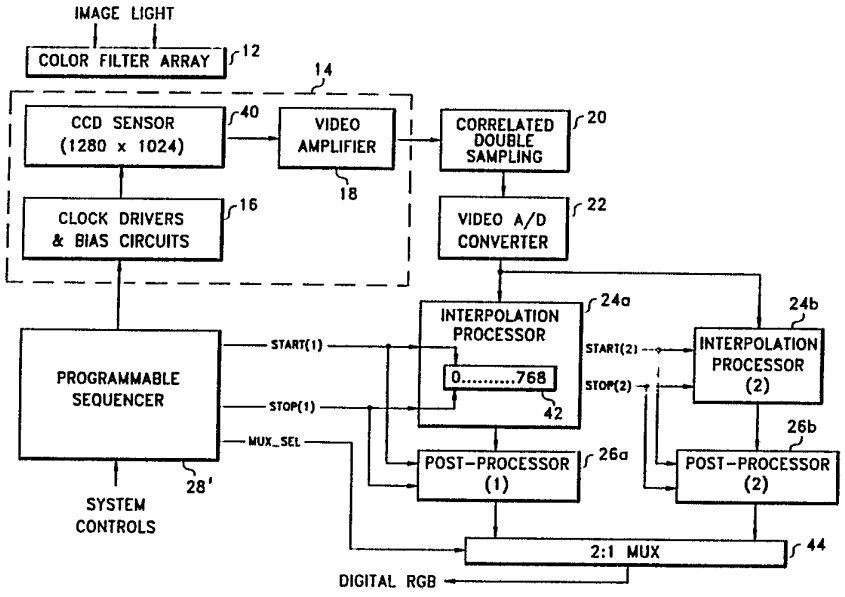
(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB (European patent), GR (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: A DISTRIBUTED DIGITAL SIGNAL PROCESSING SYSTEM USING STANDARD RESOLUTION PROCESSORS FOR A HIGH RESOLUTION SENSOR



(57) Abstract

A digital processing architecture for a high resolution image sensor (40) uses a plurality of like digital processors (24a, 26a, 24b, 26b) for time-divided processing of the output of the sensor (40). Each processor is operational according to start and stop signals from a programmable sequencer (28'). In a preferred embodiment, two sets of processors handle a line resolution of 1024 pixels, one set (24a, 26a) doing the first half of each line and the other set (24b, 26b) doing the second half. This is of particular utility where vertical processing is required, and the full line delays (50, 52) needed are divided into partial resettable delays resident in each of the processors.

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A DISTRIBUTED DIGITAL SIGNAL PROCESSING SYSTEM USING STANDARD RESOLUTION PROCESSORS FOR A HIGH RESOLUTION SENSOR

Technical Field

This invention pertains to a signal processing architecture for an imaging system and, more particularly, to a digital processing circuit utilizing one or more line delays to process the image signals generated by a high resolution image sensor.

Background Art

In order to obtain quality color video images from a one-chip color charge-coupled device (CCD) sensor, a large amount of signal processing is required. Figure 1 shows a known one-chip color CCD imaging system using custom digital video processing circuits. This system is described in detail in "A Digital Color CCD Imaging System Using Custom VLSI Circuits," by K. A. Parulski, L. J. D'Luna, and R. H. Hibbard, IEEE Trans. on Consumer Electronics, Vol. 35, No. 3, August 1989, pp. 382-388. This paper shows how the digital video processing is pipelined and operated at the same pixel rate as the image sensor, so that a framestore is not required. To minimize chip area, the signal processing has been carefully designed so that no multipliers are required.

The color imaging system shown in Figure 1 includes a CCD sensor 10 and a color filter array 12. The color filter array 12 contains a pattern of red, green, and blue filters that provide a single red, green, or blue value for each photosite of the CCD sensor 10. The image sensor 10 is an interline transfer CCD with 570 horizontal by 484 vertical

active pixels (e.g., the Model KAI-0280 sensor manufactured by the Eastman Kodak Co.) that is packaged in a leadless chip carrier which is mounted on a thick film hybrid substrate 14. The hybrid 14 includes the necessary clock drivers and bias circuits 16 and an output amplifier 18. The sensor output is processed by a clamp/sample-and-hold circuit 20 that implements a known correlated double sampling function. The processed sensor output signal is then digitized with a conventional flash A/D converter 22 and input to an interpolation processor 24.

As described in greater detail in the afore-mentioned paper, the interpolation processor 24 clamps the input video to the average sensor optical black reference value, conceals defects by substituting therefor the values of adjacent pixels, interpolates missing luminance pixels, converts to log space to perform gain control and white balance, and then interpolates chrominance values in log space. The latter interpolation is first completed in the vertical direction using on-chip line delays, and then in the horizontal direction using shift and add circuits. The log RGB outputs of the interpolation processor 24 are connected to the inputs of a post processor 26, which performs black level correction for lens flare, a 3 x 3 color matrix correction, gamma correction, and edge-enhancement. The edge enhancement improves the "crispness" of the image by extracting vertical and horizontal high frequency detail from the green channel and then adding the extracted detail back to the RGB signals. For this reason the post-processor 26 includes on-chip line delay in order to provide symmetric three-line vertical enhancement.

System timing is controlled by a programmable sequencer 28, which is described in "The EBS-1, an EPROM-based Sequencer ASIC," by M. D. Brown et al, CICC '88 Technical Digest, pp. 15.6.1-15.6.4, May 1988. A timing generation program allows the sequencer timing to be quickly developed or modified. The sequencer 28 incorporates various pixel and line counters that implement imager read-out functions according to instructions from the system controls, e.g., camera shutter button and the like. The interpolation processor 24 and the post-processor 26 chips include resettable line delays to support signal processing from sensors with up to 768 active photosites per line, making the chips suitable for NTSC, PAL, and CCIR 601 video standards. When applications requiring "higher than video" resolution arise, i.e., requiring a line resolution greater than 768 active photosites, then these "video" custom chips cannot be directly used. Moreover, "higher than video" custom chips devoted to high resolution processing have certain disadvantage since it is difficult to integrate the longer line delays necessary for high resolution processing on a chip of reasonable size.

It is known to provide higher resolution by using two linear sensors with a small overlap between them to scan a large line length (see, e.g., U.S. Patents 4,314,281 and 4,692,812). The main concern of such disclosures is the matching of the line outputs at the crossover point, although the '281 patent provides certain initial signal processing in the two separate output channels, in particular a gain adjustment related to the operating characteristics of each array. In U.S.

Patent No. 4,484,349 a parallel pipeline image processor is described in which an image matrix is partitioned so that contiguous segments of the image can be processed simultaneously by two or more adjacent serial neighborhood processors. A processor as described in the '349 patent would not be suitable for the type of imaging system described in the Parulski et al article without the addition of full image storage, which would be very expensive for high resolution image processing. Consequently, the need exists to incorporate the processor chips 24 and 26 of Figure 1 into a mega-pixel imaging system, particularly one that has the capability of providing vertical interpolation and processing vertically-oriented detail.

Disclosure of Invention

It is an objective of the invention to use the afore-mentioned custom processing chips with resettable line delays described in the aforementioned Parulski et al article with image sensor arrays having line resolution greater than the chips, particularly considering the line delays resident therein, were designed to handle.

The invention is based on the realization that the effect of a full (high resolution) line delay needed for certain vertical processing effects can be obtained by allocating separate processors each with partial line delays to separate segments of the image and then interrupting the process, and the delays therewith, at the segment boundaries. Accordingly, each line of the image sensor is divided into at least a first line section and a second line section and separate processors are allocated to each section. A first processor includes a first partial line delay corresponding to

the length of the first line section, while a second processor includes a second partial line delay corresponding to the second line section. The two processors are then sequenced so that the first processor is operational during the scanning of the first line section and the second processor is operational during the scanning of the second line section. By such sequencing, the two partial line delays form a contiguous delay corresponding to a line of the image sensor, thereby enabling standard resolution processors to be used in a high resolution application.

Brief Description of the Drawings

The invention will be described in relation to the drawings, in which

Figure 1 is a diagram of a known digital signal processing architecture for a standard resolution sensor;

Figure 2 is a diagram of a distributed digital signal processing architecture according to the invention for a high resolution sensor;

Figure 3 is a waveform diagram of several signals involved in the operation of the signal processing architecture of Figure 2; and

Figure 4(A) is an illustration of the type of color filter array requiring vertical interpolation, and Figure 4(B) is an example of a line delay arrangement for use in such vertical interpolation.

Best Mode for Carrying Out the Invention

Since digital processing systems are well known, the present description will be directed in particular to elements forming part of, or cooperating more directly with, the present invention. Elements not specifically shown or

described herein may be selected from those known in the art. In particular, details of the processors 24 and 26, and the sequencer 28, of Figure 1 are provided in the aforementioned IEEE articles by Parulski et al and Brown et al which are incorporated herein by reference for their disclosure of background materials. (The interpolation processor 24 and the post processor 26 are referred to in the Parulski et al article as a "CFA Signal Processor" and "RGB Signal Post-Processor", respectively).

In accordance with the invention, the digital signal processing of the image signals generated by a high resolution sensor 40 can be accomplished with the same interpolation and post-processor chips 24 and 26 as described in Figure 1 by using them in a distributed processing architecture as shown in Figure 2. Since this distributed architecture uses many of the same processing elements as used in the architecture of Figure 1, the same reference characters are used to describe elements that are basically the same (allowing for insubstantial differences, e.g., the color filter array 12 is basically the same although sized to accommodate a higher resolution sensor pattern in Figure 2). The interpolation processor 24 and the post-processor 26 described in Figure 1 require externally supplied start and stop signals for the on-chip line-delays. Such start and stop signals support a range of sensors 10, each having a different number of pixels per line. The line delays, however, process a maximum of 768 pixels/line. Therefore, for an image sensor 40 having less than 1536 pixels/line (i.e., 2x768 pixels), two processor chipsets are required, that

is, interpolation processors 24a and 24b and post-processors 26a and 26b. Thus, the Figure 2 diagram is the preferred architecture for the illustrated sensor 40, having 1280 horizontal pixels by 1024 vertical pixels, such as the model KAF 1300C CCD image sensor manufactured by the Eastman Kodak Co. Clearly, larger image sensor arrays would merely require additional processors. For example, a 4 mega-pixel sensor having 2048 pixels in a line (such as the model KAF-4200 manufactured by the Eastman Kodak Co.) would require three processor sets.

Referring now to Figure 2, the interpolation processor 24a and the post-processor 26a process half the image from the image sensor 40 and the interpolation processor 24b and the post-processor 26b process the other half of the image. For this purpose, the programmable sequencer 28 is programmed (and renumbered in Figure 2 as 28') to produce the waveforms of Figure 3. More specifically, the processors 24a and 26a are started by the signal start(1) at the beginning of each line time (pixel 0) and stopped by the signal stop(1) at about half of each line time (e.g., pixel 640). The processors 24b and 26b are started by the signal start(2) at about half of each line time (e.g., pixel 641) and stopped by the signal stop(2) at the end of each line time (pixel 1280). As shown by a delay element 42 in the interpolation processors 24a and 24b, the waveforms of Figure 3 also serve to start the delay element (signal start(1) or start(2)) at pixel 0 and then to stop the delay element (signal stop(1) or stop(2)) at a selected pixel position up to pixel 768. The half-line output signals from the post-processors 26a and 26b

are then time-division multiplexed into a single RGB output stream by a 2:1 multiplexer 44, which is toggled by the signal mux_sel from the sequencer 28'.

The two sets of processors 24a and 26a, and 24b and 26b, are therefore idle about half of each line time, intermittently starting and stopping pursuant to instructions from the sequencer 28' as a full raster is scanned line-by-line. As long as each processor is capable of processing at the same rate as the sensor read-out, the distributed architecture of Figure 2 can handle the image data in real time. Importantly, the line delays necessary to associate two or more pixels vertically can be performed with the partial line delays inherent in each processor.

Figure 4(A), which shows a small section of a typical color filter array 12, is helpful in understanding the need for vertical interpolation. System chrominance values, that is, color values derived from both R and B pixels, are not present on every line. Therefore, at least one full line delay is provided in order to interpolate, or align, an R and B chrominance value with every pixel position. For example, in Figure 4(B), two line delays 50 and 52 are provided (in, e.g., the interpolation processors 24a and 24b) to align three output values in order to perform vertical interpolation across three lines. Each delay is resettable so as to start (start(0)) at the first pixel position (0) and to stop (stop (n<= 768) at an arbitrary pixel position less than or equal to pixel position 768. In this way each line delay can be exactly configured to handle the portion of the total line allocated to each processor set 24a and 26a, and 24b

and 26b. Although not shown separately, a similar arrangement of resettable line delays can be provided in the post-processors 26a and 26b to provide the necessary pixel values for vertical enhancement. Resettable delay lines are conventionally known; see, for example, Mattausch, H. et al, "A Memory-Based High-Speed Digital Delay Line with a Large Adjustable Length", IEEE Journal of Solid State Circuits, Vol. SC-23, No. 1, pgs. 105-110, Feb. 1988.

While the preceding description illustrates the arbitrary starting and stopping of each processor set 24a and 26a, and 24b and 26b, it is possible in a further embodiment to freely operate the first processor set 24a and 26a and to let the multiplexer 44 effect the sequencing between processor sets. In other words, it is unnecessary to arbitrarily stop the processors 24a and 26a. They are simply started at the beginning of the line and the multiplexer 44 sequences the output signal by switching to the other processors 24b and 26b when they are started. The fact that the processors 24a and 26a continue to operate is of no consequence. In certain situations, this embodiment may be preferred because one reset signal (the stop signal for processors 24a and 26a) can be eliminated. Furthermore, in cases where less than the full line length of the second processor set 24b and 26b is required, it is feasible to start the line delays in the second set at an appropriate pixel location and let them continue to the end of the line (rather than start the line delays at n=0 and stop them at the appropriate pixel location).

What is claimed is:

1. A signal processing system for generating vertically-processed image signals from the scanned output of a two-dimensional image sensor (40), each line of said image sensor being divided into at least a first line section and a second line section, characterized in that said signal processing system comprises:

first processing means (24a, 24b) for processing image signals derived from said first line section, said first processing means including a plurality of first partial line delays (50, 52) corresponding to a plurality of said first line sections;

second processing means (24b, 26b) for processing image signals derived from said second line section, said second processing means including a plurality of second partial line delays (50, 52) corresponding to a plurality of said second line sections; and

means (28') for sequencing the operation of said first and second processing means so that said first processing means (24a, 26a) is operational during the scanning of the first line sections and said second processing means (24b, 26b) is operational during the scanning of the second line sections, said two pluralities of partial line delays (50, 52) thereby forming a contiguous delay useful in the vertical processing of image signals corresponding to plural lines of the image sensor (40).

2. A signal processing system as claimed in claim 1 wherein said partial line delays (50, 52) are resettable line delays, and said sequencing means (28') provides reset signals to said line

delays for starting and stopping each delay in correspondence to the length of each line section.

3. A signal processing system as claimed in claim 1 wherein the sensor (40) is a color sensor that does not provide full chroma information in each line and said partial line delays (50, 52) in said first and second processing means (24a, 26a, 24b, 26b) are used to vertically interpolate chroma information.

4. A signal processing system as claimed in claim 1 wherein said first and second processing means (24a, 26a, 24b, 26b) perform an enhancement operation and said partial line delays are used to generate vertically-enhanced detail.

5. A signal processing system as claimed in claim 1 further including a multiplexer (44) to provide a time-divided sequence of the outputs of said first and second processing means (24a, 26a, 24b, 26b).

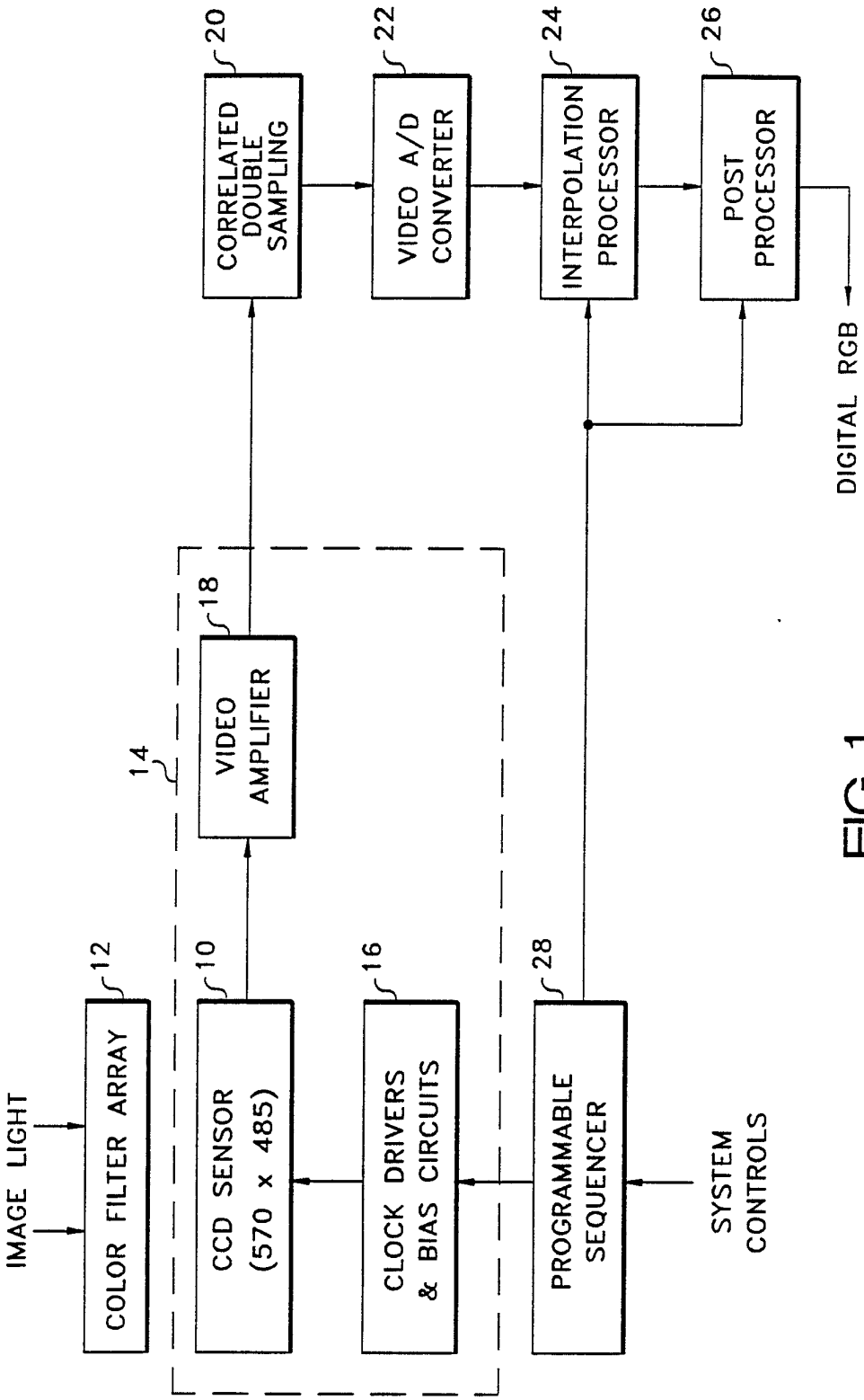

FIG. 1
(PRIOR ART)

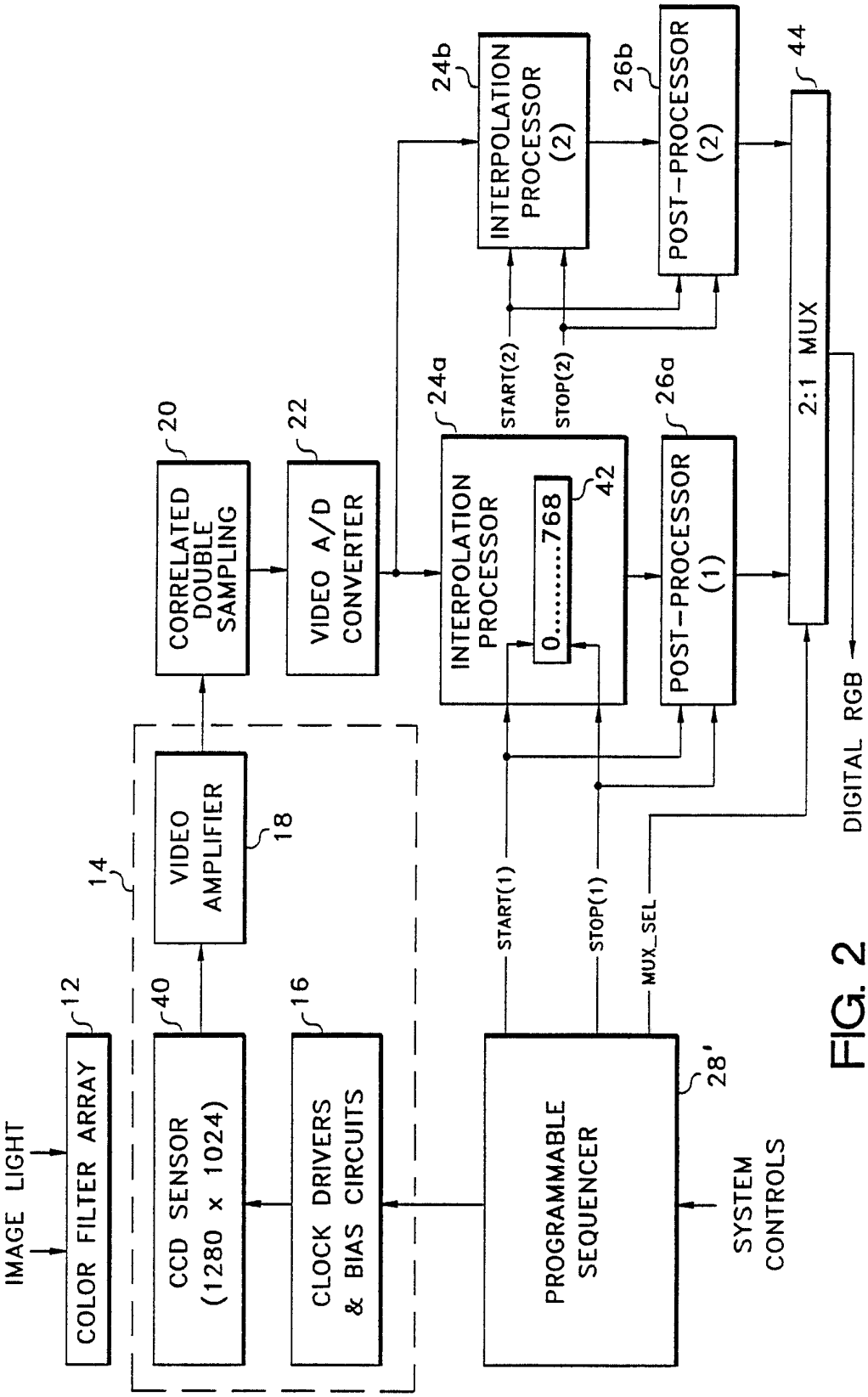
IMAGE LIGHT
COLOR FILTER ARRAY
12
CCD SENSOR (1280 x 1024)
40
CLOCK DRIVERS & BIAS CIRCUITS
16
14
VIDEO AMPLIFIER
18
CORRELATED DOUBLE SAMPLING
20
VIDEO A/D CONVERTER
22
INTERPOLATION PROCESSOR
24a
0.....768
42
INTERPOLATION PROCESSOR (2)
24b
START(2)
STOP(2)
POST-PROCESSOR (1)
26a
POST-PROCESSOR (2)
26b
2:1 MUX
44
DIGITAL RGB
START(1)
STOP(1)
MUX_SEL
PROGRAMMABLE SEQUENCER
28'
SYSTEM CONTROLS

FIG. 2

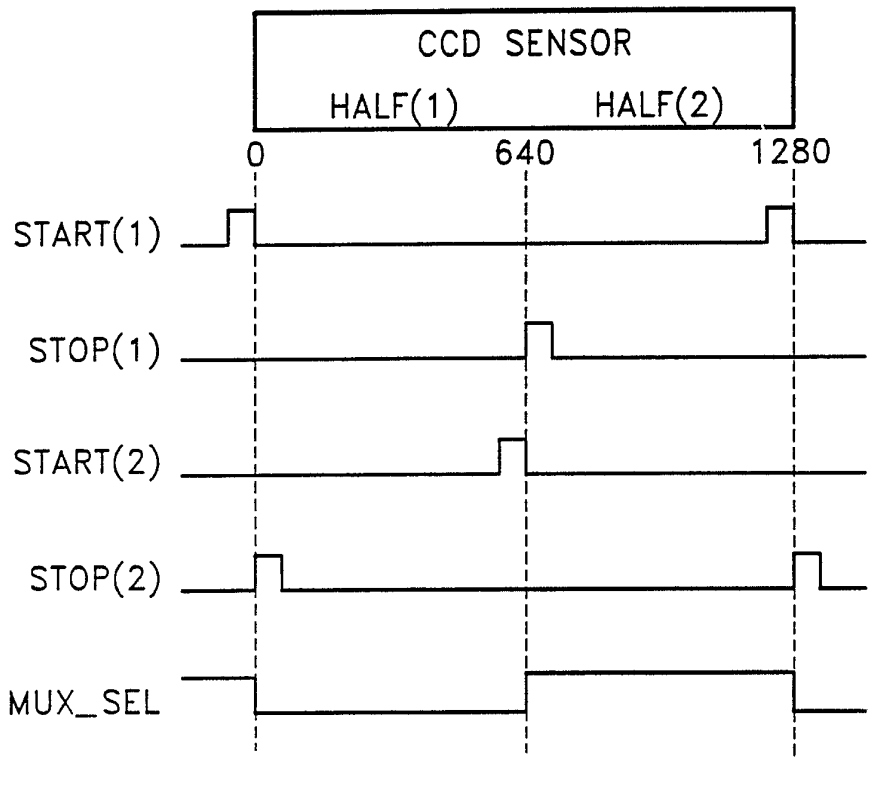
CCD SENSOR
HALF(1)
HALF(2)
0
640
1280
START(1)
STOP(1)
START(2)
STOP(2)
MUX_SEL

FIG. 3

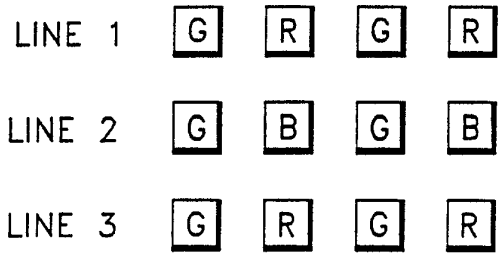
LINE 1
G
R
G
R
LINE 2
G
B
G
B
LINE 3
G
R
G
R

FIG. 4A

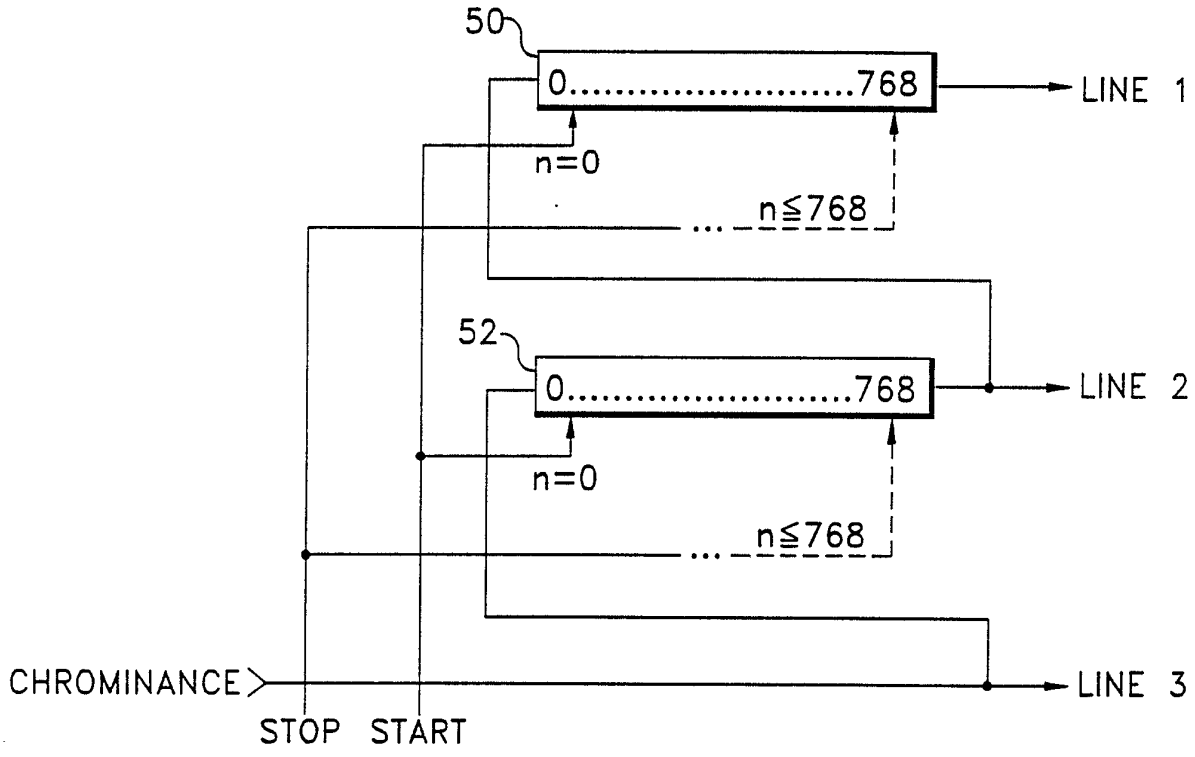
50
0.....768
LINE 1
n=0
n≦768
52
0.....768
LINE 2
n=0
n≦768
CHROMINANCE
LINE 3
STOP
START

FIG. 4B

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 91/05034

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC5: G 06 F 15/66

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
IPC5	G 06 F, H 04 N

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category *	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
A	IEEE Transactions on Consumer Electronics, vol. 35, No. 3, August 1989,(Rochester, N.Y.) K.A. Parulski et al: "A DIGITAL COLOR CCD IMAGING SYSTEM USING CUSTOM VLSI CIRCUITS ", see page 382 - page 388 refered to in the description --	1-5
A	JOURNAL OF SOLID-STATE CIRCUITS, vol. 23, No. 1, February 1988, Hans-Jürgen Mattausch et al: "A Memory-Based High-Speed Digital Delay Line with a Large Adjustable Length ", see page 105 - page 110 refered to in the description --	1-5

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
2nd December 1991	13. 12. 91
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	Daniella van der Haas

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
A	US, A, 4380046 (LAI-WO FUNG) 12 April 1983, see column 1, line 14 - column 2, line 5 --	1-5
A	US, A, 4692812 (S. HIRAHARA ET AL) 8 September 1987, refered to in the description --	1-5
A	US, A, 4314281 (D. G. WIGGINS ET AL) 2 February 1982, refered to in the description --	1-5
A	US, A, 4873515 (C. M. DICKSON ET AL) 10 October 1989, see figures 2,4,6 --	1-5
A	US, A, 4484349 (D. L. MCCUBBREY) 20 November 1984, refered to in the description --	1-5

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. PCT/US 91/05034

SA 50088

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 4380046	12/04/83	NONE	
US-A- 4692812	08/09/87	DE-A-C- 3610271	16/10/86
		JP-A- 61219258	29/09/86
		JP-A- 62101170	11/05/87
US-A- 4314281	02/02/82	CA-A- 1162640	21/02/84
		CA-A- 1181841	29/01/85
		EP-A-B- 0027372	22/04/81
		JP-A- 56062481	28/05/81
US-A- 4873515	10/10/89	NONE	
US-A- 4484349	20/11/84	NONE	