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(54) Title: HOLD-UP TIME ENHANCEMENT CIRCUIT FOR LLC RESONANT CONVERTER

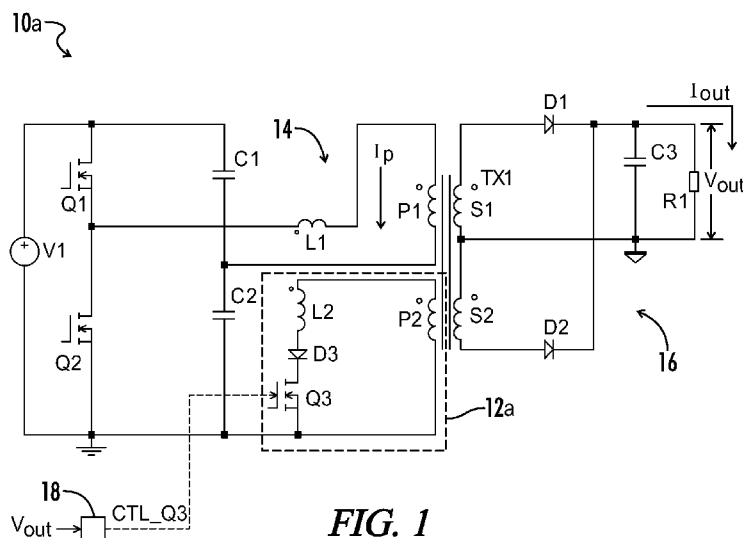


FIG. 1

(57) Abstract: An open loop half-bridge LLC power converter includes circuitry to reliably increase hold-up time without sacrificing efficiency. An LLC resonant circuit (14) includes resonant inductance, a primary transformer winding, and resonant capacitance. An auxiliary circuit includes an auxiliary transformer winding, an inductor, and a third switching element coupled in series. A controller is coupled across a voltage sensor to determine a holdup time condition. In a "normal" operating condition the controller (18) generates switch driver signals to turn OFF the third switching element (Q3) and disable the auxiliary circuit, and in a hold-up time condition the controller (18) turns ON the third switching element (Q3) and enables the auxiliary circuit wherein the output voltage is increased via current supplied from the auxiliary winding. In various embodiments the auxiliary winding may be an auxiliary primary or secondary, or a secondary to an auxiliary primary winding of a second transformer.

DESCRIPTION**HOLD-UP TIME ENHANCEMENT CIRCUIT FOR LLC RESONANT
CONVERTER****TECHNICAL FIELD**

[0001] The present invention relates generally to power converters. More particularly, the present invention relates to gain enhancement circuitry for LLC resonant power converters wherein a hold-up time may be increased with minimal effect on efficiency.

BACKGROUND ART

[0002] As market requirements for high efficiency have become more demanding, LLC resonant converters have correspondingly grown in popularity due to their high efficiency performance and their ability to achieve high power density. The 80 Plus Platinum certification standard requires greater than 94% efficiency at half load (50%) conditions. The 80 Plus Titanium standard requires 96% efficiency at half load conditions.

[0003] However, there is a trade-off between the high efficiency and long hold-up time performance in a resonant converter. Generally speaking, the hold-up time of a converter is the amount of time (typically in milliseconds) that a power converter can continue to generate output within a specified range after an input power interruption. Efficiency can be increased significantly with, for example, an increase in magnetizing inductance to reduce switching losses. However, the hold-up time will consequently decrease by a significant amount as well. And likewise, efficiency may be sacrificed for long hold-up time performance.

[0004] One solution that is known in the art for maintaining high efficiency performance while achieving long hold-up time is to increase the bulk capacitance. However, this results in problems of low power density and also higher cost.

[0005] It would therefore be desirable to provide power converters with circuitry for balancing high efficiency and long hold-up time, while addressing the power density issues which would otherwise result from solutions in power converters as are presently known to those of skill in the art.

DISCLOSURE OF THE INVENTION

[0006] An open loop half-bridge LLC resonant power converter according to one aspect of the present invention includes circuitry to reliably increase hold-up time without increasing bulk capacitance or sacrificing efficiency.

[0007] In an exemplary embodiment, an LLC resonant circuit includes resonant inductance, a primary transformer winding, and resonant capacitance. An auxiliary circuit includes an auxiliary transformer winding, an inductor, and a third switching element coupled in series. A controller is coupled across a voltage sensor and effective thereby to determine a holdup time condition. In a “normal” operating condition the controller generates switch driver signals to turn OFF the third switching element and disable the auxiliary circuit, and in a hold-up time condition the controller turns ON the third switching element and enables the auxiliary circuit.

[0008] Generally stated, when the auxiliary circuit is enabled, current flows through the second inductor and the current is further coupled to the main transformer, wherein the gain of the resonant converter is increased and the output voltage maintained for a lower bulk voltage. Hence, increasing the hold-up time and maintaining high efficiency is achieved without requiring a larger, more expensive bulk capacitor in accordance with an objective of the present invention.

[0009] In some embodiments the auxiliary winding may be an auxiliary primary winding of the transformer.

[0010] In other embodiments the auxiliary winding may be an auxiliary secondary winding of the transformer.

[0011] In still other embodiments the converter may further include a second transformer having a primary winding coupled in parallel with the primary winding of the first transformer, and the auxiliary winding of the hold-up circuit may be an auxiliary primary winding of the second transformer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Fig. 1 is a circuit block diagram representing an exemplary LLC resonant converter with a first embodiment of a gain enhancement circuit according to the present invention.

[0013] Figs. 2(a), 2(b), 2(c), 2(d) are graphical illustrations representing exemplary results from a simulation performed on the embodiment of Fig. 1.

[0014] Fig. 3 is a circuit block diagram representing the exemplary LLC resonant converter of Fig. 1 with a second embodiment of a gain enhancement circuit according to the present invention.

[0015] Fig. 4 is a circuit block diagram representing the exemplary LLC resonant converter of Fig. 1 with a third embodiment of a gain enhancement circuit according to the present invention.

[0016] Fig. 5 is a circuit block diagram representing the exemplary LLC resonant converter of Fig. 1 with a fourth embodiment of a gain enhancement circuit according to the present invention.

[0017] Fig. 6 is a circuit block diagram representing the exemplary LLC resonant converter of Fig. 1 with a fifth embodiment of a gain enhancement circuit according to the present invention.

[0018] Fig. 7 is a circuit block diagram representing the exemplary LLC resonant converter of Fig. 1 with a sixth embodiment of a gain enhancement circuit according to the present invention.

[0019] Fig. 8 is a circuit block diagram representing the exemplary LLC resonant converter of Fig. 1 with a seventh embodiment of a gain enhancement circuit according to the present invention.

[0020] Fig. 9 is a circuit block diagram representing the exemplary LLC resonant converter of Fig. 1 with an eighth embodiment of a gain enhancement circuit according to the present invention.

[0021] Fig. 10 is a circuit block diagram representing the exemplary LLC resonant converter of Fig. 1 with a ninth embodiment of a gain enhancement circuit according to the present invention.

[0022] Fig. 11 is a circuit block diagram representing the exemplary LLC resonant converter of Fig. 1 with a tenth embodiment of a gain enhancement circuit according to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0023] Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context dictates otherwise. The meanings identified below do not necessarily limit the terms, but merely provide illustrative examples for the terms. The meaning of “a,” “an,” and “the” may include plural references, and the meaning of “in” may include “in” and “on.” The phrase “in one embodiment,” as used herein does not necessarily refer to the same embodiment, although it may.

[0024] The term “coupled” means at least either a direct electrical connection between the connected items or an indirect connection through one or more passive or active intermediary devices.

[0025] The term “circuit” means at least either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function.

[0026] The term “signal” as used herein may include any meanings as may be understood by those of ordinary skill in the art, including at least an electric or magnetic representation of current, voltage, charge, temperature, data or a state of one or more memory locations as expressed on one or more transmission mediums, and generally capable of being transmitted, received, stored, compared, combined or otherwise manipulated in any equivalent manner.

[0027] The terms “switching element” and “switch” may be used interchangeably and may refer herein to at least: a variety of transistors as known in the art (including but not limited to FET, BJT, IGBT, JFET, etc.), a switching diode, a silicon controlled rectifier (SCR), a diode for alternating current (DIAC), a triode for alternating current (TRIAC), a mechanical single pole/double pole switch (SPDT), or electrical, solid state or reed relays. Where either a field effect transistor (FET) or a bipolar junction transistor (BJT) may be employed as an embodiment of a transistor, the scope of the terms “gate,” “drain,” and “source” includes “base,” “collector,” and “emitter,” respectively, and vice-versa.

[0028] The terms “power converter” and “converter” unless otherwise defined with respect to a particular element may be used interchangeably herein and with reference to at least DC-DC, DC-AC, AC-DC, buck, buck-boost, boost, half-bridge, full-bridge, H-bridge or various other forms of power conversion or inversion as known to one of skill in the art.

[0029] Terms such as “providing,” “processing,” “supplying,” “determining,” “calculating” or the like may refer at least to an action of a computer system, computer program, signal processor, logic or alternative analog or digital electronic device that may be transformative of signals represented as physical quantities, whether automatically or manually initiated.

[0030] The terms “controller,” “control circuit” and “control circuitry” as used herein may refer to a processor-readable and non-transitory medium such as may be embodied by or included within a general microprocessor, application specific integrated circuit (ASIC), microcontroller, or the like as may be designed and programmed to cause specific functions as further defined herein to be performed upon execution by a processing unit, either alone or in combination with a field

programmable gate array or various alternative blocks of discrete circuitry as known in the art.

[0031] Referring generally to Figs. 1-11, various embodiments of an LLC resonant power converter with hold-up time enhancement circuitry according to the present invention may now be described. Where the various figures may describe embodiments sharing various common elements and features with other embodiments, similar elements and features are given the same reference numerals and redundant description thereof may be omitted below.

[0032] For example, each of Figs. 1-11 refer generally to a common configuration for an LLC resonant power converter 10, with the individual figures referring more particularly to embodiments that vary depending on the position and configuration of a hold-up time enhancement circuit 12 according to the present invention. Generally stated, an exemplary such power converter 10 may include a power source V1 which may typically be, for example, the output from a power factor correction (PFC) circuit, but may be any form of DC input as would be known to those of skill in the art. At least a first pair of switching elements Q1, Q2 are coupled in series across the input power terminals of the power source V1 to define a half bridge configuration. An LLC resonant circuit 14 is defined by a resonant inductor L1, a magnetizing inductance in the primary winding P1 of a main transformer TX1, and resonant capacitors C1, C2.

[0033] An output circuit 16 may be defined by secondary windings S1, S2 of the main transformer TX1. Opposing ends of the secondary windings S1, S2 are coupled via diodes D1, D2 to a first end of output capacitor C3 defining a first output terminal. A center tap between the secondary windings S1, S2 is coupled to a second end of the output capacitor C3 defining a second output terminal. Other configurations of the output circuit 16 may certainly be contemplated within the scope of the present invention, but the center tapped winding configuration may be desirable to increase the efficiency of the converter.

[0034] A voltage sensor R1 is coupled to a controller 18 whereby the controller may monitor an appropriate status of the power converter and determine the presence of a hold-up time condition. The sensor R1 may be positioned in any of various locations throughout the power converter circuit 10, whether proximate the output circuit, the input power source, or the like, and may further take various forms. As but one alternative example, an output inductor (not shown) may be coupled along the first branch of the output circuit between the diode D1 and the output capacitor C3,

with nodes on opposing sides of the output inductor being coupled to the controller via, for example, a resistive network.

[0035] Referring more particularly now to Fig. 1, in a particular embodiment of the power converter 10a according to the present invention, a hold-up time enhancement circuit 12a includes an auxiliary primary winding P2, an auxiliary inductor L2, a diode D3 and an auxiliary switching element Q3 coupled in series. The auxiliary switching element Q3 is driven on and off by signals provided from the controller 18.

[0036] During a normal condition (i.e., wherein the input power is ON or as may for example be determined by comparison of the input voltage to a predetermined threshold), the controller 18 turns off (or maintains off) the auxiliary switching element Q3, either by disabling control signals to the gate of the switching element Q3 or by reducing the magnitude of the control signals to below the internal threshold for the switch Q3.

[0037] However, when there is a temporary failure in the input power source, or any equivalent condition that would prompt the voltage across the bulk capacitor to drop (e.g., below the predetermined threshold), the controller 18 is programmed to thereby identify the presence of a hold-up time condition, and subsequently generates control signals to turn on the auxiliary switching element Q3.

[0038] Alternatively, the controller 18 may continuously provide drive signals to the auxiliary switching element Q3, the drive signals of a voltage corresponding inversely to the detected signals from the voltage sensor. The auxiliary switching element Q3 is only turned on when its gate-source voltage exceeds the internal threshold voltage for the switch Q3, which may correspond by design approximately to the desired point based on the voltage drop across the bulk capacitor.

[0039] The auxiliary winding P2 is coupled with voltage from primary winding P1 having a value approximately proportional to the turn ratio of P2 and P1. When the auxiliary switching element Q3 is turned on, this voltage acts on the auxiliary inductor L2 and a current sourced through the auxiliary inductor L2 is further coupled to the primary winding P1. The additional current on the primary winding increases P1 the gain of the LLC resonant converter, and the output voltage is maintained for an extended hold-up time.

[0040] Referring generally to the graphical diagrams represented in Fig. 2, an exemplary operation of the embodiment in Fig. 1 is now described. Component values may be as follows:

resonant inductance (L1) = 27uH;

resonant capacitance (C1, C2) = 22nF

main transformer (TX1) = gapped to 150uH;

turn ratio for main transformer (TX1) = P1:P2:S1:S2 = 15:5:1:1;

output voltage (Vout) = 14V

output current/ load (Iout) = 55A

[0041] When the signal CTL_Q3 is provided in Fig. 2(d), it may be demonstrated that the primary resonant current I_p increases and the voltage swing across the resonant capacitors V_{c_res} becomes larger. Hence, the total converter gain is boosted and a longer hold-up time is achieved. Note that the output voltage Vout further increased from 14V to 20V in this exemplary operation.

[0042] In various embodiments as described herein, it may be further possible to boost converter efficiency by increasing the magnetization inductance to reduce switching losses on the auxiliary switching element Q3.

[0043] In another exemplary embodiment of the LLC converter 10b as represented in Fig. 3, a hold-up time enhancement circuit 12b of the present invention may alternatively be located on the secondary side of the circuit. More particularly, the auxiliary winding may alternatively be an auxiliary secondary winding S3. Otherwise, the configuration and operation of the embodiment 10b of Fig. 3 would be substantially identical to that of the embodiment 10a of Fig. 1 and as described in more detail above.

[0044] In another exemplary embodiment of the LLC converter 10c as represented in Fig. 4, a hold-up time enhancement circuit 12c of the present invention may be coupled to a second transformer TX2. A primary winding P21 of the second transformer TX2 is a magnetizing inductance coupled in parallel with the magnetizing inductance of the primary winding P11 of the first transformer TX1, and an auxiliary winding of the hold-up time enhancement circuit 12c is a secondary winding S21 with respect to the primary winding P21. Otherwise, the configuration and operation of the embodiment 10c of Fig. 4 would be substantially identical to that of the embodiment 10a of Fig. 1 and as described in more detail above.

[0045] In another exemplary embodiment of the LLC converter 10d as represented in Fig. 5, a hold-up time enhancement circuit 12d of the present invention may be located on the secondary side of the circuit in similar fashion to that of the embodiment 10b in Fig. 3, wherein the auxiliary winding may be an auxiliary secondary winding S3, but one end of the auxiliary winding S3 is now coupled to the output voltage rather than to the secondary ground, or otherwise stated is now coupled to a first output voltage terminal rather than a second output voltage terminal as in Fig. 3. Otherwise, the configuration and operation of the embodiment 10d of Fig. 5 would be substantially identical to that of the embodiment 10a of Fig. 1 and as described in more detail above.

[0046] In another exemplary embodiment of the LLC converter 10e as represented in Fig. 6, a hold-up time enhancement circuit 12e of the present invention may be coupled to a second transformer TX2 in similar fashion to that of embodiment 12c in Fig. 4, wherein a primary winding P21 of the second transformer TX2 is a magnetizing inductance coupled in parallel with the magnetizing inductance of primary winding P11 of the first transformer TX1, and an auxiliary winding of the hold-up time enhancement circuit 12e is a secondary S21 with respect to the primary winding P21. The primary difference of note is that one end of the auxiliary winding S21 is coupled to the output voltage rather than to primary circuit ground as in Fig. 4. Otherwise, the configuration and operation of the embodiment 10c of Fig. 4 would be substantially identical to that of the embodiment 10a of Fig. 1 and as described in more detail above.

[0047] Referring now to Fig. 7, an embodiment of the hold-up time enhancement circuit 12f may be positioned again in the primary side of the circuit, but now including a diode bridge D4, D5, D6, D7 coupled between the auxiliary winding P2 and the auxiliary switching element Q3.

[0048] Referring to Fig. 8, another embodiment of the hold-up time enhancement circuit 12g may have substantially the same configuration as that of Fig. 7, with the exception of the circuit 12g being positioned on the secondary side of the main transformer TX1.

[0049] Referring to Fig. 9, another embodiment of the hold-up time enhancement circuit 12h may have substantially the same configuration as that of Fig. 7, with the exception of the circuit 12h being positioned with respect to a second transformer TX2.

[0050] Referring to Fig. 10, another embodiment of the hold-up time enhancement circuit 12i may include first and second auxiliary switching elements Q3, Q4. The controller 18 provides control signals to each of the auxiliary switching elements Q3, Q4 during a hold-up time condition to perform substantially the same operation as in the configurations described above, namely, sourcing current through the auxiliary inductor L2 to provide such current to the primary winding P1 and further to generate a higher output voltage V_{out} .

[0051] The embodiment of a hold-up time enhancement circuit 12j as represented in Fig. 11 is substantially the same as the embodiment 12i in Fig. 11, except that it is now positioned in the secondary side of the circuit 10j.

[0052] The previous detailed description has been provided for the purposes of illustration and description. Thus, although there have been described particular embodiments of the present invention of a new and useful “Hold-up Time Enhancement Circuit for LLC Resonant Converter,” it is not intended that such references be construed as limitations upon the scope of this invention except as set forth in the following claims.

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CLAIMS

What is claimed is:

1. A power conversion system comprising:
 - first and second switching elements coupled in series across first and second power input terminals;
 - an LLC resonant circuit coupled between the first and second switching elements and comprising a first inductor, a primary winding of a transformer, and one or more resonant capacitors;
 - an output circuit comprising one or more secondary transformer windings and a bulk capacitor coupled across first and second output terminals;
 - a voltage sensor;
 - a hold-up time enhancement circuit further comprising an auxiliary primary winding of the transformer, a second inductor coupled on a first end to the auxiliary transformer winding, and a third switching element coupled to a second end of the second inductor;
 - a controller coupled to the voltage sensor and effective to determine a holdup time condition based on a voltage across the voltage sensor;
 - the controller is further effective in a first operating mode associated with a normal condition to generate switch driver signals to turn OFF the third switching element and disable the hold-up time enhancement circuit; and
 - the controller is further effective in a second operating mode associated with a hold-up time condition to generate switch driver signals to turn ON the third switching element and enable the holdup time enhancement circuit wherein the output voltage is increased via current supplied from the auxiliary winding.
2. The system of claim 1, wherein the auxiliary winding is coupled on a first end to the second inductor and on a second end to circuit ground and the third switching element is coupled on a first end to the second inductor and on a second end to circuit ground.
3. The system of claim 2, further comprising a fourth switching element coupled between the second end of the auxiliary winding and circuit ground.
4. The system of claim 2, the hold-up time enhancement circuit further comprising a diode having an anode coupled to the second end of the second inductor and a cathode coupled to the first end of the third switching element.

5. The system of claim 1, the hold-up time enhancement circuit further comprising first and second diodes in each of first and second branches of a diode bridge, the anodes of each of the first diodes are coupled to circuit ground, the cathodes of each of the second diodes are coupled to the first end of the second inductor, and opposing ends of the auxiliary winding are coupled between the first and second diodes of the first and second branches, respectively.
6. The system of claim 1, the output circuit comprising first and second secondary windings coupled in series, opposing ends of the secondary windings coupled to the first output terminal, and a center tap between the secondary windings coupled to the second output terminal.
7. A power conversion system comprising:
first and second switching elements coupled in series across first and second power input terminals;
an LLC resonant circuit coupled between the first and second switching elements and comprising a first inductor, a primary winding of a transformer, and one or more resonant capacitors;
an output circuit comprising one or more secondary transformer windings, and a bulk capacitor coupled across first and second output terminals;
a voltage sensing circuit;
a hold-up time enhancement circuit further comprising an auxiliary secondary winding of the transformer, a second inductor coupled on a first end to the auxiliary transformer winding, and a third switching element coupled to a second end of the second inductor; and
a controller coupled to the voltage sensor and effective to determine a holdup time condition based on a voltage across the voltage sensor,
the controller is further effective in a first operating mode associated with a normal condition to generate switch driver signals to turn OFF the third switching element and disable the hold-up time enhancement circuit, and
the controller is further effective in a second operating mode associated with a hold-up time condition to generate switch driver signals to turn ON the third switching element and enable the holdup time enhancement circuit wherein the output voltage is increased via current supplied from the auxiliary winding.

8. The system of claim 7, wherein the auxiliary winding is coupled on a first end to the second inductor and on a second end to the second output terminal, further wherein the third switching element is coupled on a first end to the second inductor and on a second end to the second output terminal.
9. The system of claim 8, further comprising a fourth switching element coupled between the second end of the auxiliary winding and the second output terminal.
10. The system of claim 7, the hold-up time enhancement circuit further comprising a diode having an anode coupled to the second end of the second inductor and a cathode coupled to the first end of the third switching element.
11. The system of claim 7, the hold-up time enhancement circuit further comprising first and second diodes in each of first and second branches of a diode bridge,
the anodes of each of the first diodes are coupled to the second output terminal,
the cathodes of each of the second diodes are coupled to the first end of the second inductor, and
opposing ends of the auxiliary winding are coupled between the first and second diodes of the first and second branches, respectively.
12. The system of claim 7, the output circuit comprising first and second secondary windings coupled in series, opposing ends of the secondary windings coupled to the first output terminal, and a center tap between the secondary windings coupled to the second output terminal.
13. The system of claim 12, wherein the auxiliary winding is coupled on a first end to the second inductor and on a second end to the first output terminal, further wherein the third switching element is coupled on a first end to the second inductor and on a second end to the second output terminal.
14. A power conversion system comprising:
first and second switching elements coupled in series across first and second power input terminals;
an LLC resonant circuit coupled between the first and second switching elements and comprising a first inductor, a primary winding of a first transformer, and one or more resonant capacitors;
a primary winding of a second transformer coupled in parallel with the primary winding of the first transformer;

an output circuit comprising one or more secondary transformer windings of the first transformer and a bulk capacitor coupled across first and second output terminals;

a voltage sensor;

a hold-up time enhancement circuit further comprising a secondary winding of the second transformer as an auxiliary winding, a second inductor coupled on a first end to the auxiliary winding, and a third switching element coupled to a second end of the second inductor; and

a controller coupled to the voltage sensor and effective to determine a holdup time condition based on a voltage across the voltage sensor,

the controller is further effective in a first operating mode associated with a normal condition to generate switch driver signals to turn OFF the third switching element and disable the hold-up time enhancement circuit, and

the controller is further effective in a second operating mode associated with a hold-up time condition to generate switch driver signals to turn ON the third switching element and enable the holdup time enhancement circuit wherein the output voltage is increased via current supplied from the auxiliary winding.

15. The system of claim 14, wherein the auxiliary winding is coupled on a first end to the second inductor and on a second end to circuit ground, further wherein the third switching element is coupled on a first end to the second inductor and on a second end to circuit ground.

16. The system of claim 15, further comprising a fourth switching element coupled between the second end of the auxiliary winding and circuit ground.

17. The system of claim 15, the hold-up time enhancement circuit further comprising a diode having an anode coupled to the second end of the second inductor and a cathode coupled to the first end of the third switching element.

18. The system of claim 17, the output circuit comprising first and second secondary windings coupled in series, opposing ends of the secondary windings coupled to the first output terminal, and a center tap between the secondary windings coupled to the second output terminal.

19. The system of claim 18, wherein the auxiliary winding is coupled on a first end to the second inductor and on a second end to the first output terminal, further wherein the third switching element is coupled on a first end to the second inductor and on a second end to circuit ground.

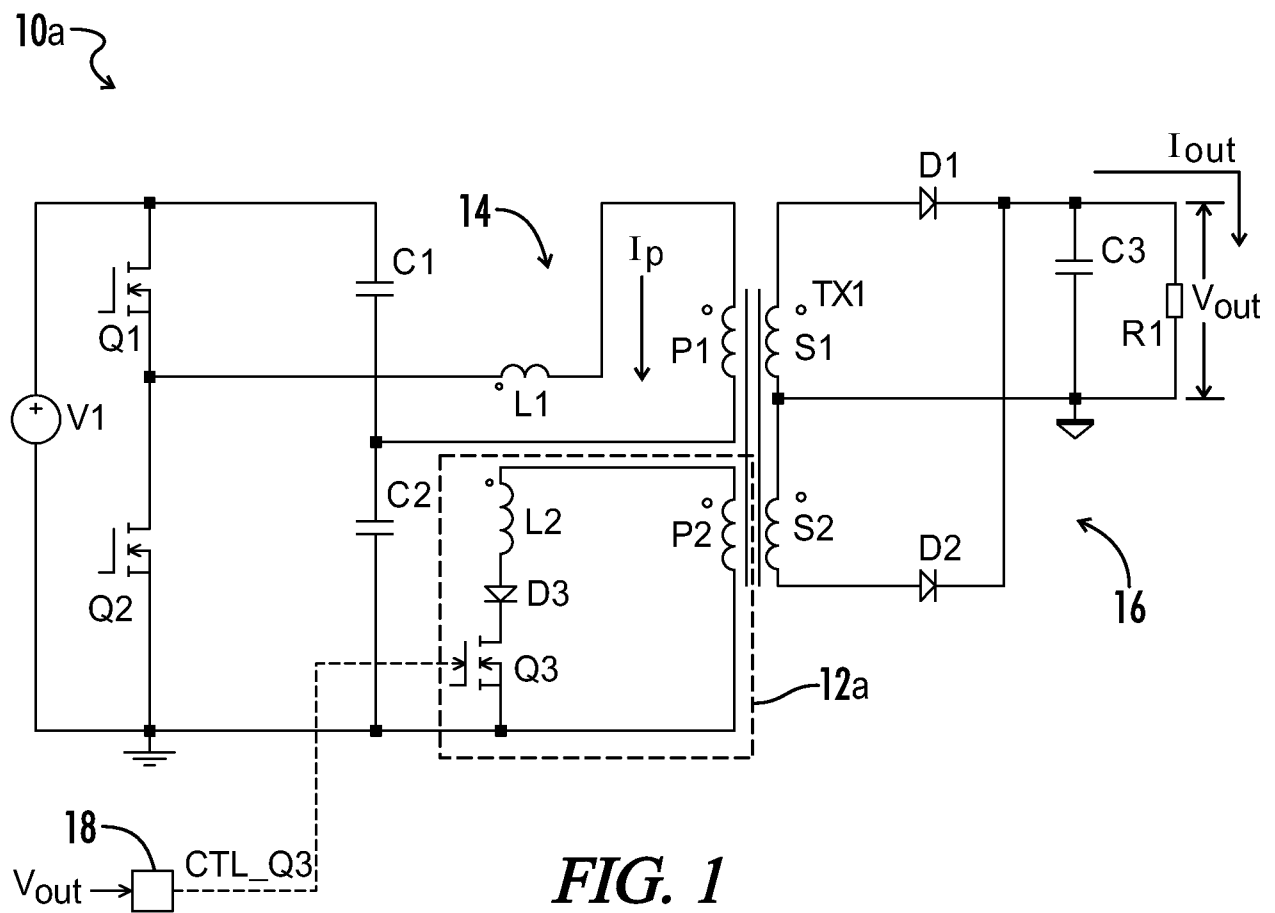
20. The system of claim 14, the hold-up time enhancement circuit further comprising first and second diodes in each of first and second branches of a diode bridge,

the anodes of each of the first diodes coupled to circuit ground,

the cathodes of each of the second diodes coupled to the first end of the second inductor, and

opposing ends of the auxiliary winding coupled between the first and second diodes of the first and second branches, respectively.

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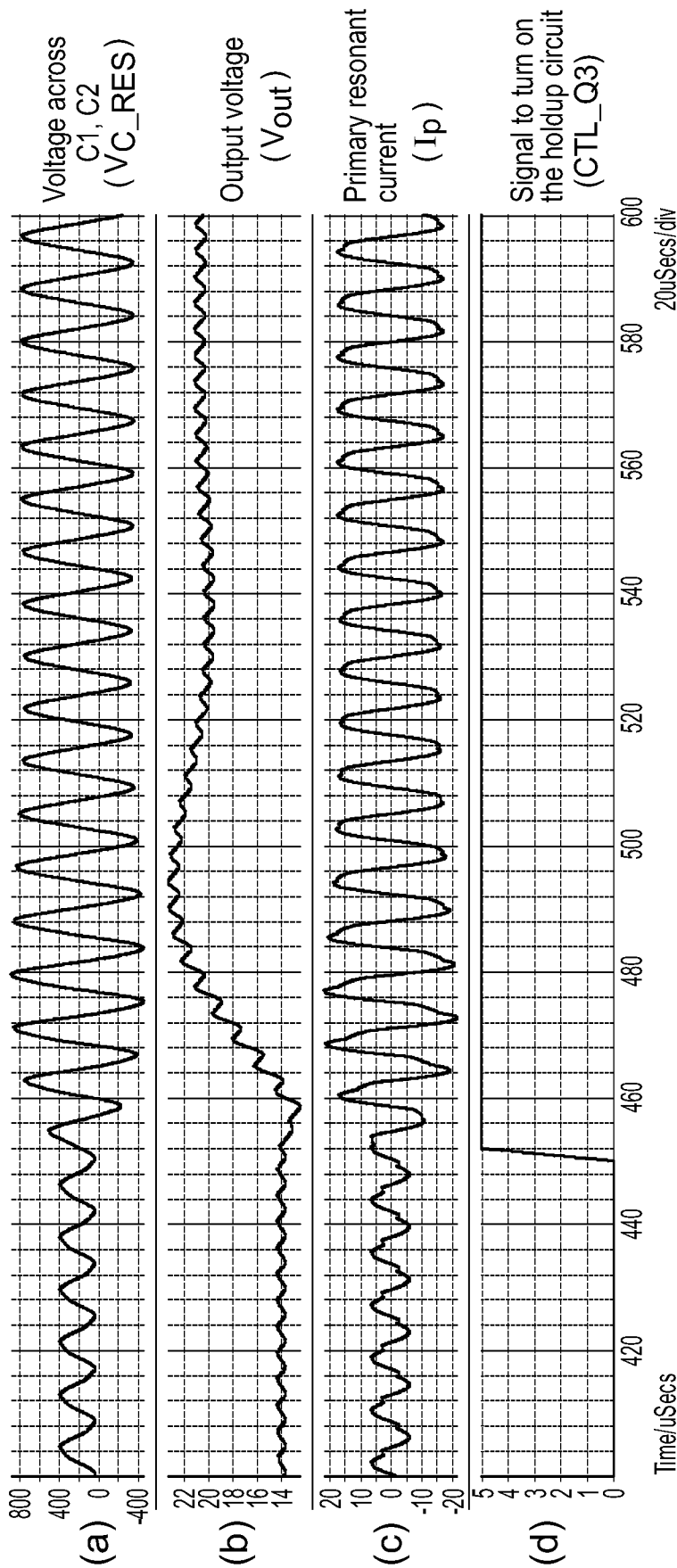


FIG. 2

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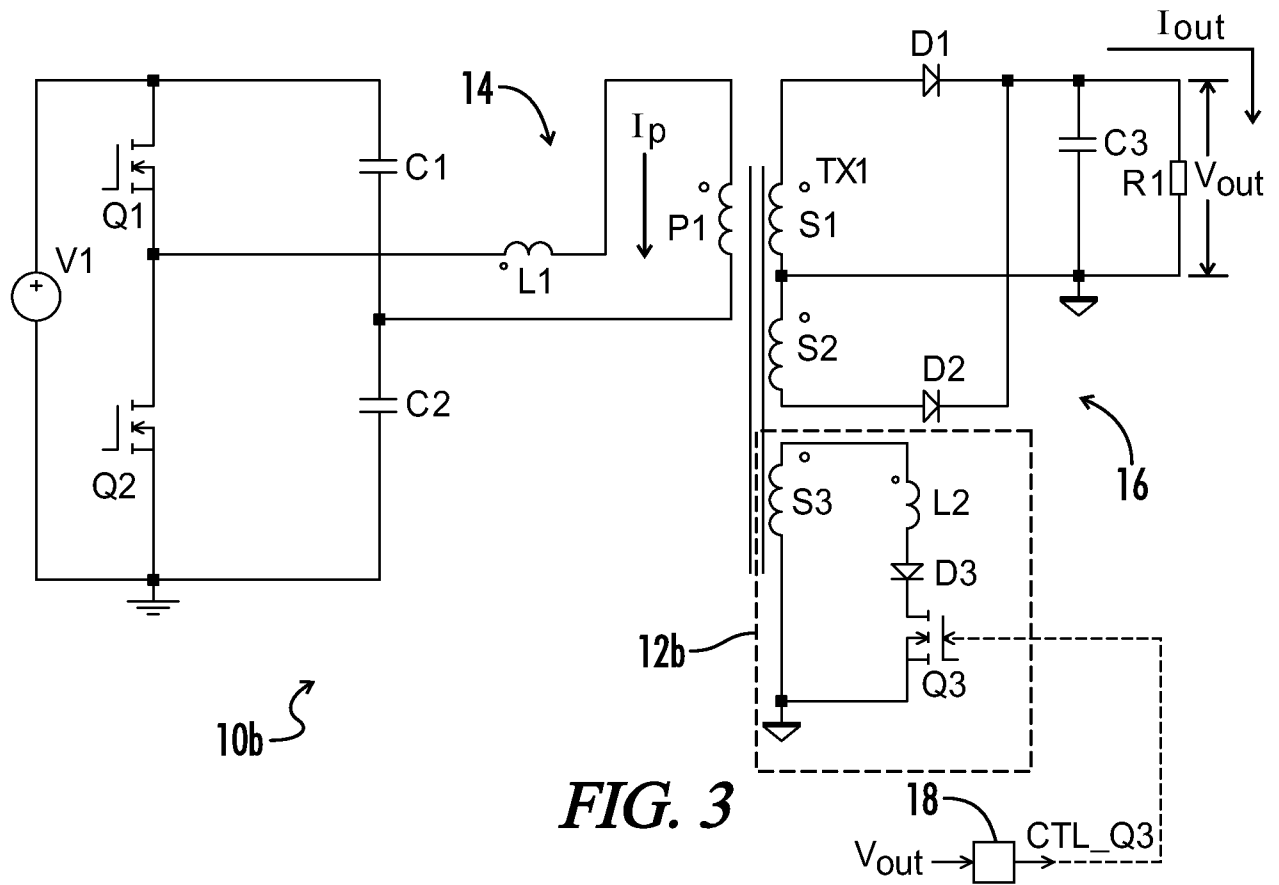


FIG. 3

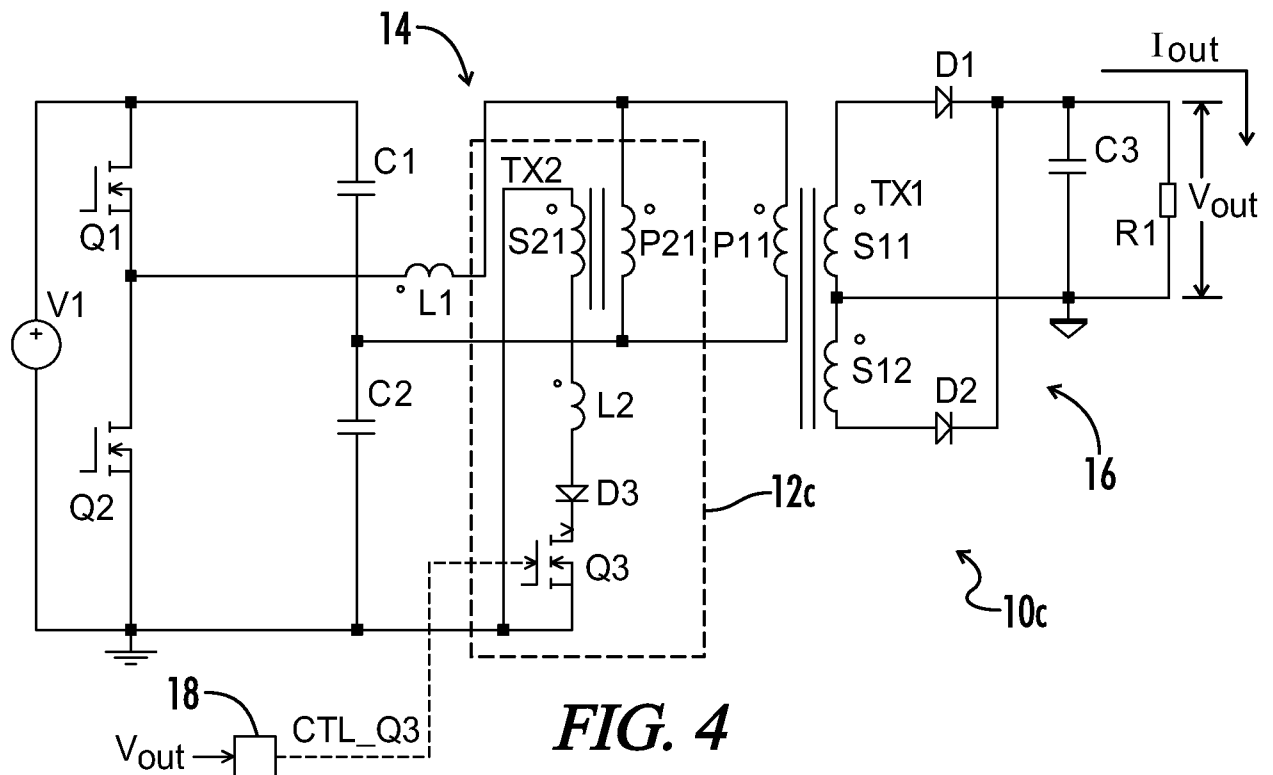


FIG. 4

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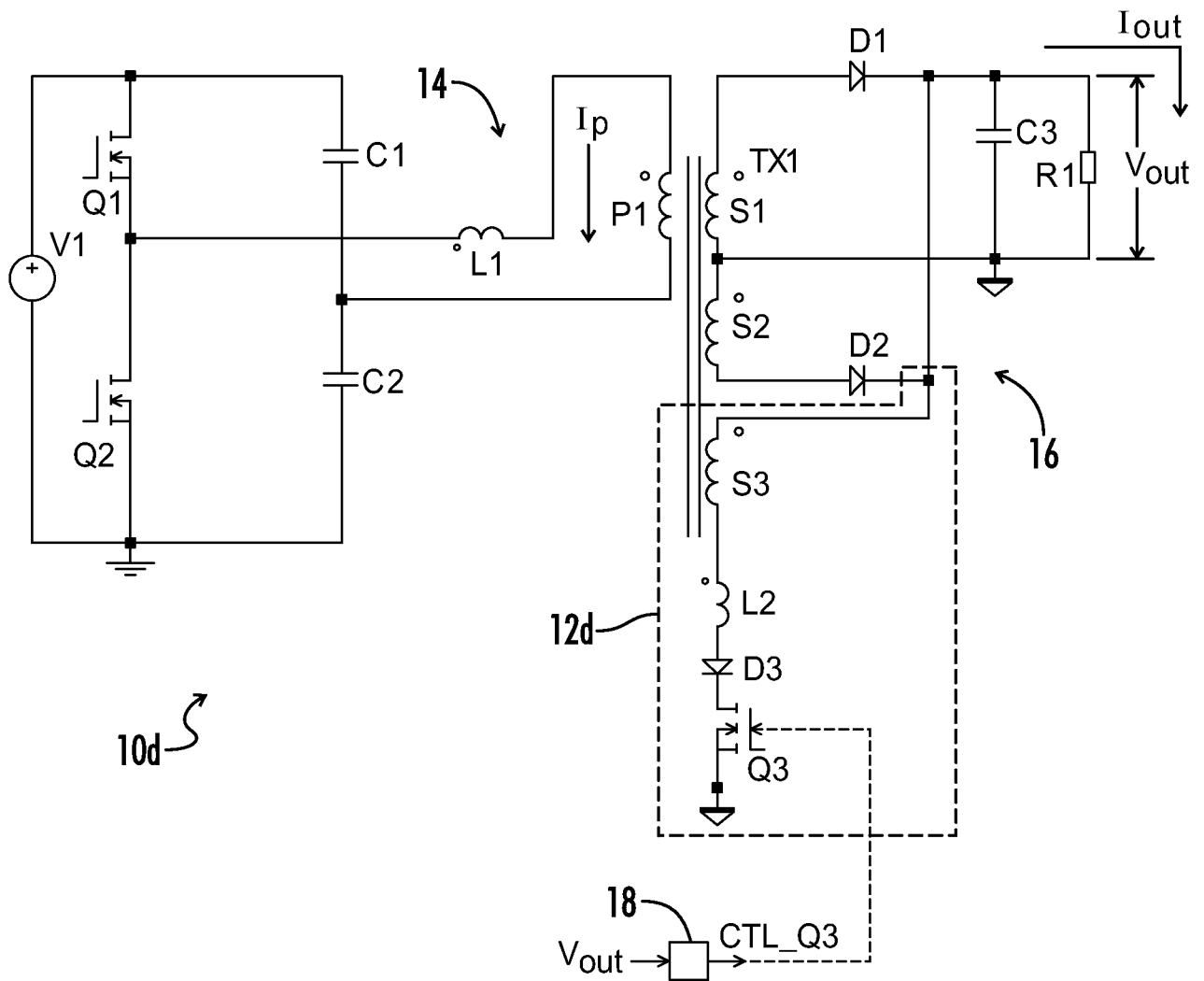


FIG. 5

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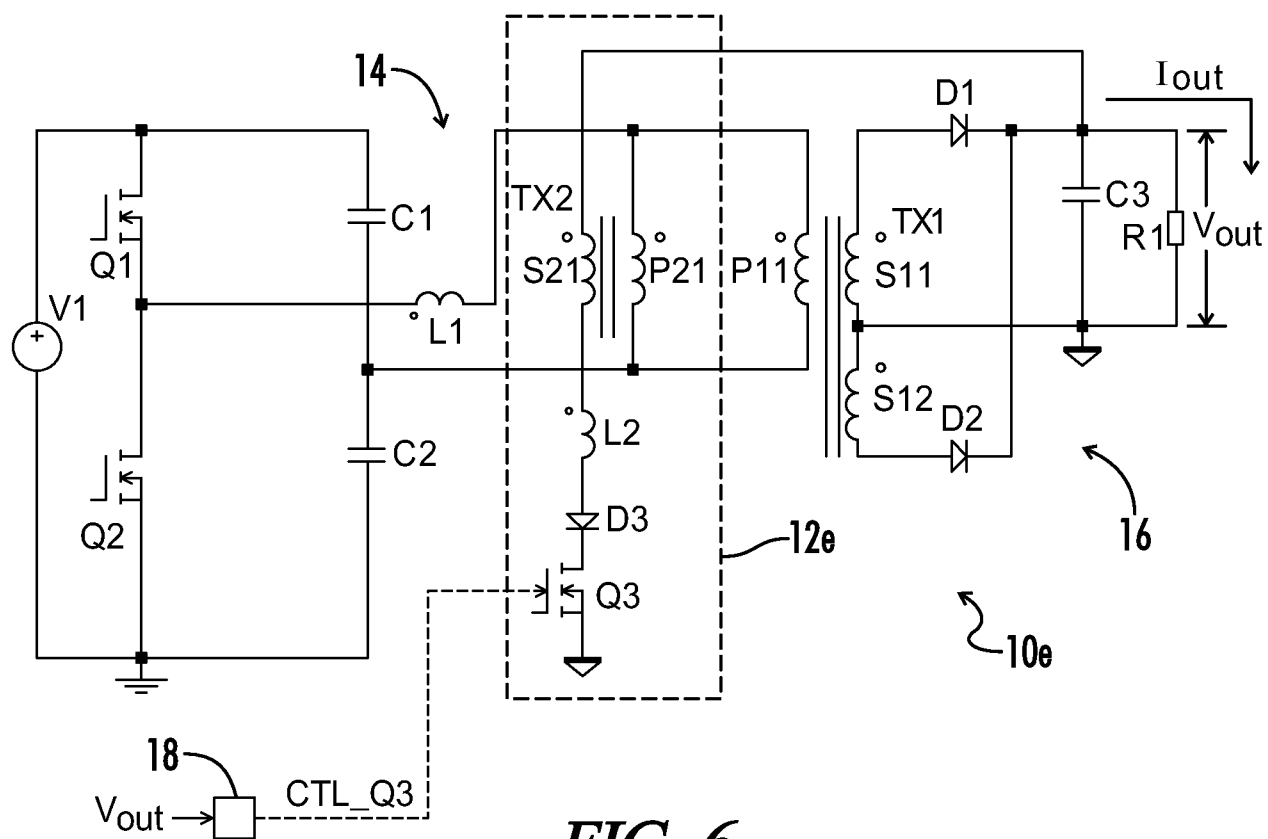


FIG. 6

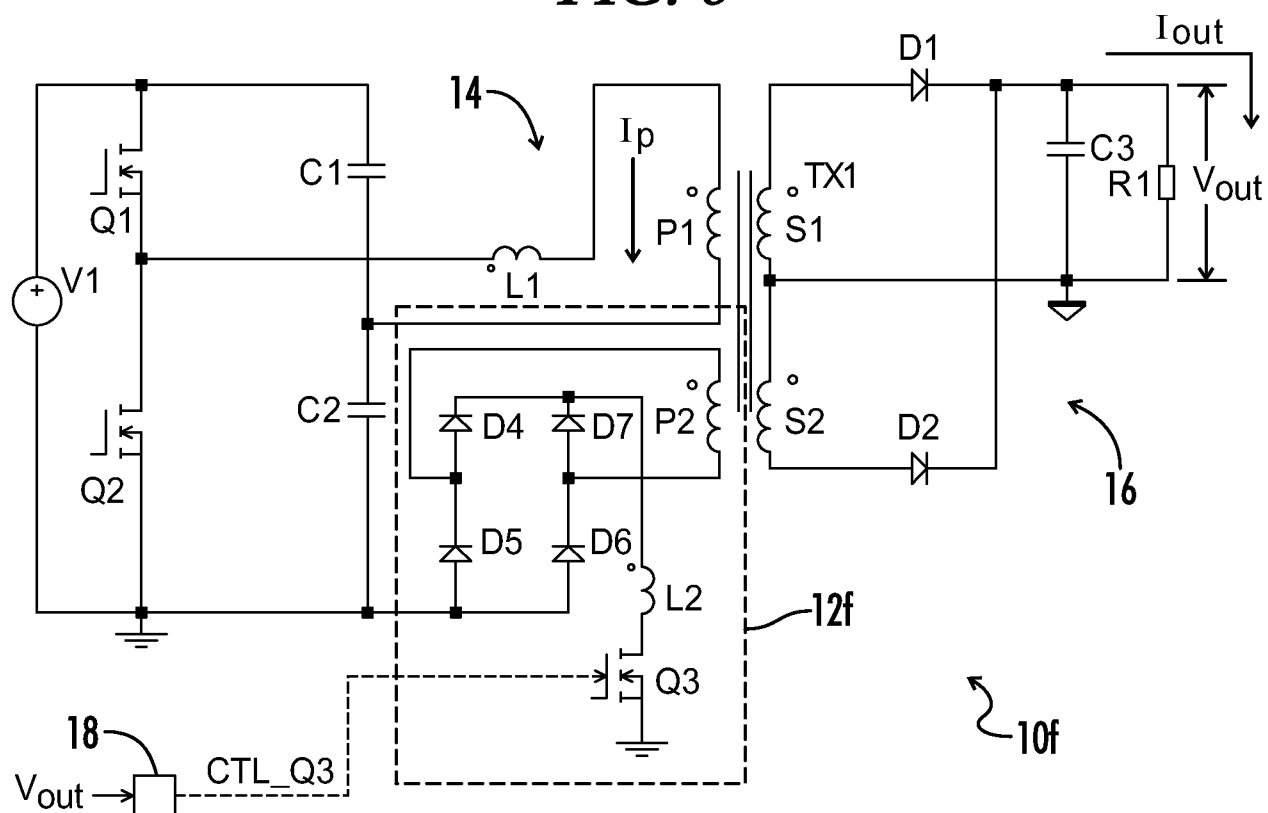


FIG. 7

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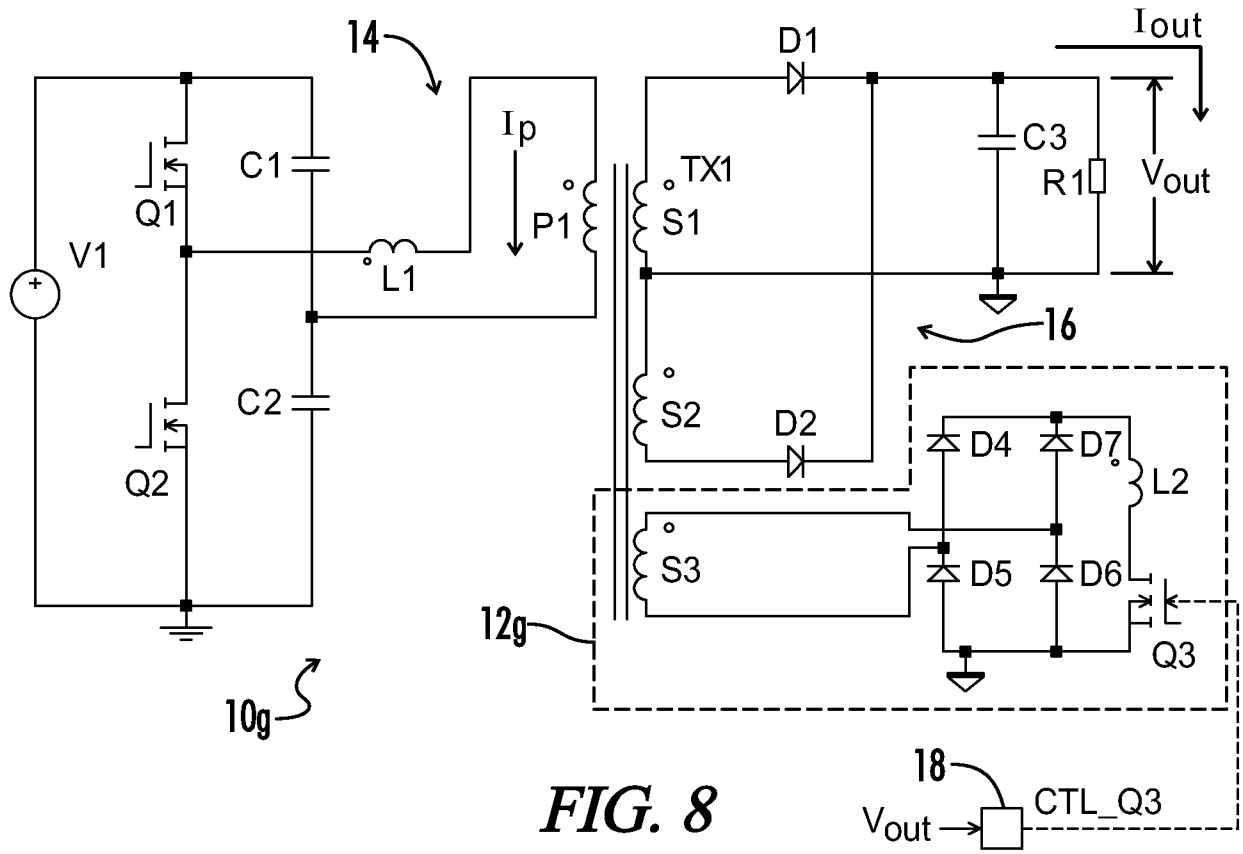


FIG. 8

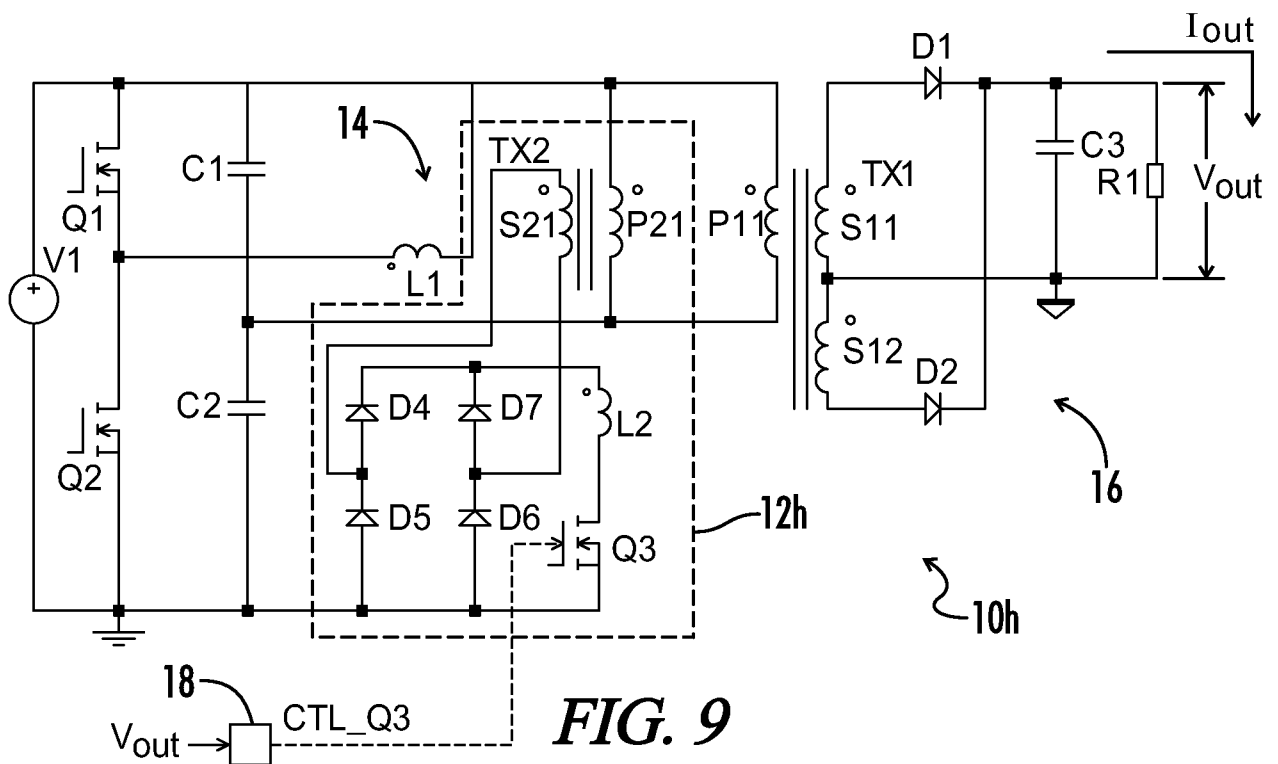
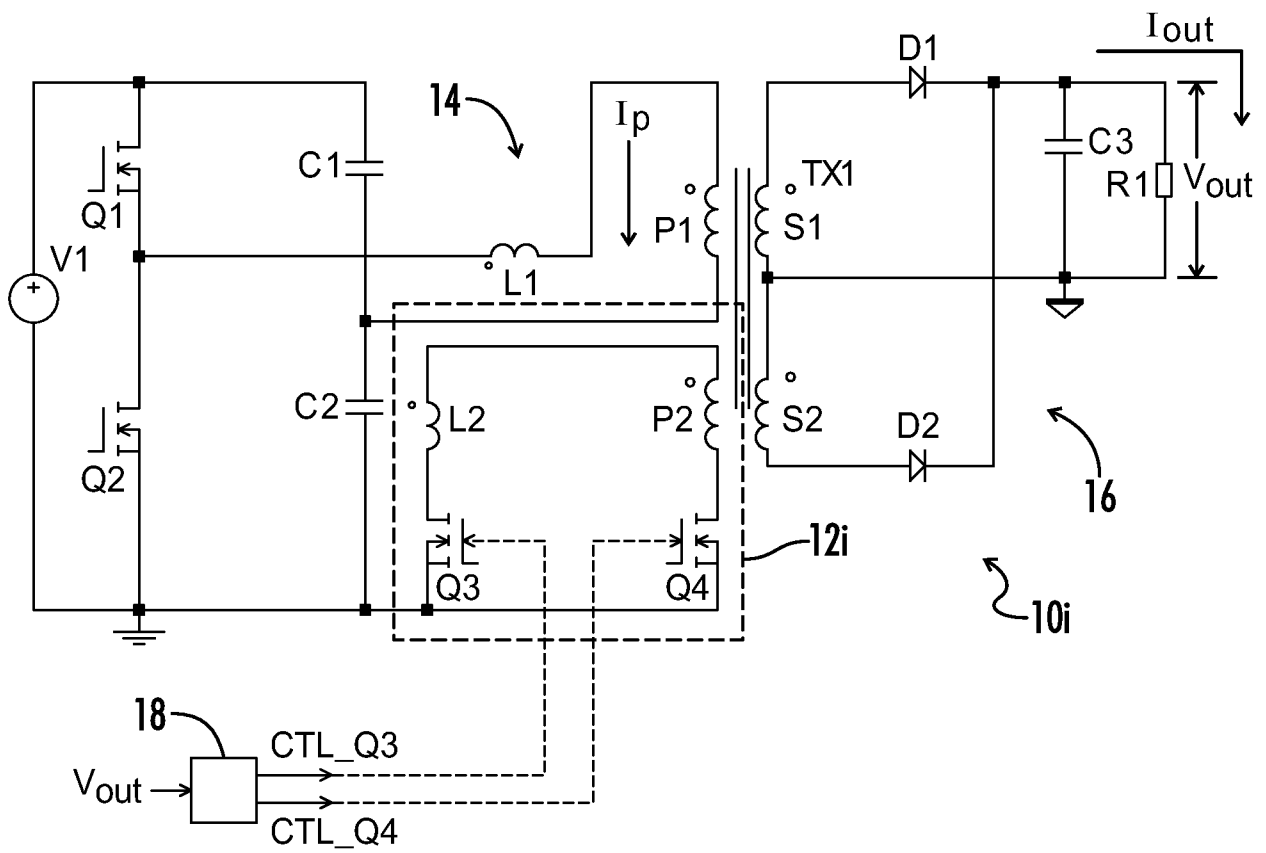
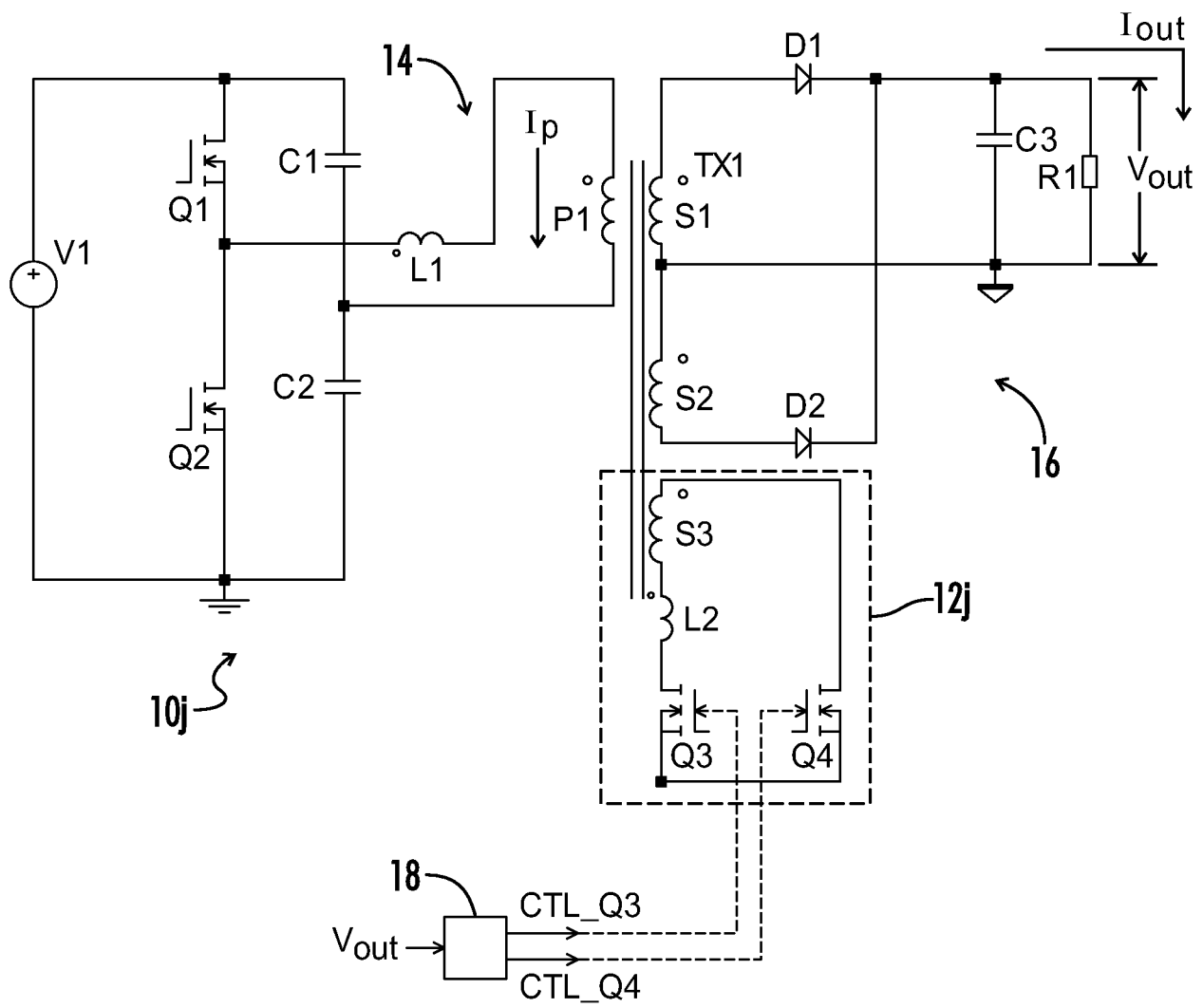


FIG. 9

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**FIG. 10**

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**FIG. 11**

A. CLASSIFICATION OF SUBJECT MATTER**H02M 3/28(2006.01)i, H02M 3/24(2006.01)i, H02M 3/22(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M 3/28; H02M 3/335; H02J 17/00; H02M 3/24; H02M 3/22

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: converter, resonant, hold-up, inductor, capacitor, auxiliary circuit, efficiency, mode

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010-0182803 A1 (ZHANGHE NAN et al.) 22 July 2010 See paragraphs [0031]-[0032], claim 1 and figures 9, 11.	1-20
A	JP 2002-159175 A (DENSEI LAMBDA K.K.) 31 May 2002 See abstract, paragraphs [0021]-[0023] and figures 1-2.	1-20
A	JP 2000-166236 A (NEC HOME ELECTRONICS LTD.) 16 June 2000 See abstract, paragraphs [0009]-[0013] and figures 1-2.	1-20
A	US 2007-0115700 A1 (NIGEL SPRINGETT) 24 May 2007 See paragraphs [0052]-[0059] and figures 3-5.	1-20
A	WO 2011-063108 A2 (ACCESS BUSINESS GROUP INTERNATIONAL LLC et al.) 26 May 2011 See paragraphs [0047]-[0059], claims 1-2 and figures 3-5.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

25 July 2013 (25.07.2013)

Date of mailing of the international search report

26 July 2013 (26.07.2013)

Name and mailing address of the ISA/KR

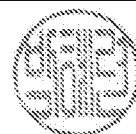
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/036130

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010-0182803 A1	22/07/2010	None	
JP 2002-159175 A	31/05/2002	JP 4591861 B2	01/12/2010
JP 2000-166236 A	16/06/2000	None	
US 2007-0115700 A1	24/05/2007	CN 1988071 A	27/06/2007
		EP 1783788 A2	09/05/2007
		EP 1783788 A3	25/03/2009
WO 2011-063108 A2	26/05/2011	CN 102714430 A	03/10/2012
		KR 10-2012-0112462 A	11/10/2012
		TW 201145748 A	16/12/2011
		US 2011-0115303 A1	19/05/2011
		WO 2011-063108 A3	03/05/2012