



(51) International Patent Classification:

H01L 29/778 (2006.01) H01L 29/66 (2006.01)
H01L 29/12 (2006.01) H01L 29/80 (2006.01)

(21) International Application Number:

PCT/US2016/036327

(22) International Filing Date:

08 June 2016 (08.06.2016)

(25) Filing Language:

English

(26) Publication Language:

English

(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054-1549 (US).

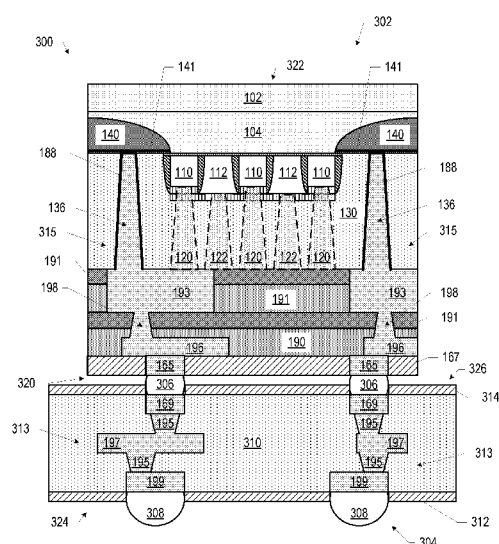
(72) Inventors: ROBERTS, Jeanette M.; 17898 NW Pumpkin Ridge Road, North Plains, Oregon 97133 (US). PIL-LARISSETTY, Ravi; 1330 SW 3rd Avenue, Apt. 1103, Portland, Oregon 97201 (US). MICHALAK, David J.; 1511 SW Park Avenue, Apt 811, Portland, Oregon 97201 (US). YOSCOVITS, Zachary R.; 16145 NW Schendel Avenue, Unit 21B, Beaverton, Oregon 97006 (US). CLARKE, James S.; 5676 NW 204th Place, Portland, Oregon 97229 (US). ELSHERBINI, Adel A.; 300 North Gila Springs Blvd, Chandler, Arizona 85226 (US).

(74) Agent: ZAGER, Laura A.; Patent Capital Group, 2816 Lago Vista Lane, Rockwall, TX 75032 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: QUANTUM DOT DEVICE PACKAGES



Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *of inventorship (Rule 4.17(iv))*

Published:

- *with international search report (Art. 21(3))*

QUANTUM DOT DEVICE PACKAGES

Background

[0001] Quantum computing refers to the field of research related to computation systems that use quantum mechanical phenomena to manipulate data. These quantum mechanical phenomena, such as superposition (in which a quantum variable can simultaneously exist in multiple different states) and entanglement (in which multiple quantum variables have related states irrespective of the distance between them in space or time), do not have analogs in the world of classical computing, and thus cannot be implemented with classical computing devices.

Brief Description of the Drawings

[0002] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0003] FIGS. 1-3 are cross-sectional views of a quantum dot device, in accordance with various embodiments.

[0004] FIGS. 4-25 illustrate various example stages in the manufacture of a quantum dot device, in accordance with various embodiments.

[0005] FIGS. 26-28 are cross-sectional views of various examples of quantum well stacks that may be used in a quantum dot device, in accordance with various embodiments.

[0006] FIGS. 29-35 illustrate example base/fin arrangements that may be used in a quantum dot device, in accordance with various embodiments.

[0007] FIGS. 36-38 illustrate various example stages in the manufacture of alternative gate arrangements that may be included in a quantum dot device, in accordance with various embodiments.

[0008] FIG. 39 illustrates an embodiment of a quantum dot device having multiple groups of gates on a single fin, in accordance with various embodiments.

[0009] FIGS. 40-44 illustrate various alternative stages in the manufacture of a quantum dot device, in accordance with various embodiments.

[0010] FIG. 45 illustrates an example alternative stage in the manufacture of a quantum dot device, in accordance with various embodiments.

[0011] FIGS. 46-47 illustrate detail views of various embodiments of a doped region in a quantum dot device.

[0012] FIGS. 48-51 illustrate various quantum dot device packages, in accordance with various embodiments.

[0013] FIGS. 52-61 illustrate various stages in the manufacture of a package substrate for a quantum dot device package, in accordance with various embodiments.

[0014] FIGS. 62-67 illustrate various alternative stages in the manufacture of a package substrate for a quantum dot device package, in accordance with various embodiments.

[0015] FIGS. 68A and 68B are top views of a wafer and dies that may include any of the quantum dot devices disclosed herein.

[0016] FIG. 69 is a cross-sectional side view of a device assembly that may include any of the quantum dot device packages disclosed herein.

[0017] FIG. 70 is a flow diagram of an illustrative method of manufacturing a quantum dot device package, in accordance with various embodiments.

[0018] FIGS. 71-72 are flow diagrams of illustrative methods of operating a quantum dot device, in accordance with various embodiments.

[0019] FIG. 73 is a block diagram of an example quantum computing device that may include any of the quantum dot devices disclosed herein, in accordance with various embodiments.

Detailed Description

[0020] Disclosed herein are quantum dot device packages, as well as related computing devices and methods. For example, in some embodiments, a quantum dot device package may include a die having a quantum dot device, wherein the quantum dot device includes a quantum well stack, gates disposed above the quantum well stack, and conductive pathways coupled between associated ones of the gates and conductive contacts of the die. The quantum dot device package may also include a package substrate, wherein conductive contacts are disposed on the package substrate, and first level interconnects are disposed between the die and the package substrate, coupling the conductive contacts of the die with associated conductive contacts of the package substrate.

[0021] The quantum dot devices disclosed herein may enable the formation of quantum dots to serve as quantum bits ("qubits") in a quantum computing device, as well as the control of these quantum dots to perform quantum logic operations. Unlike previous approaches to quantum dot formation and manipulation, various embodiments of the quantum dot devices disclosed herein provide strong spatial localization of the quantum dots (and therefore good control over quantum dot interactions and manipulation), good scalability in the number of quantum dots included in the device, and/or design flexibility in making electrical connections to the quantum dot devices to integrate the quantum dot devices in larger computing devices.

[0022] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical

changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0023] Various operations may be described as multiple discrete actions or operations in turn in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0024] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. As used herein, the notation "A/B/C" means (A), (B), and/or (C).

[0025] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale. As used herein, a "high-k dielectric" refers to a material having a higher dielectric constant than silicon oxide.

[0026] FIGS. 1-3 are cross-sectional views of a quantum dot device 100, in accordance with various embodiments. In particular, FIG. 2 illustrates the quantum dot device 100 taken along the section A-A of FIG. 1 (while FIG. 1 illustrates the quantum dot device 100 taken along the section C-C of FIG. 2), and FIG. 3 illustrates the quantum dot device 100 taken along the section B-B of FIG. 1 with a number of components not shown to more readily illustrate how the gates 106/108 may be patterned (while FIG. 1 illustrates a quantum dot device 100 taken along the section D-D of FIG. 3). Although FIG. 1 indicates that the cross-section illustrated in FIG. 2 is taken through the fin 104-1, an analogous cross section taken through the fin 104-2 may be identical, and thus the discussion of FIG. 2 refers generally to the "fin 104."

[0027] The quantum dot device 100 may include a base 102 and multiple fins 104 extending away from the base 102. The base 102 and the fins 104 may include a substrate and a quantum well stack (not shown in FIGS. 1-3, but discussed below with reference to the substrate 144 and the quantum

well stack 146), distributed in any of a number of ways between the base 102 and the fins 104. The base 102 may include at least some of the substrate, and the fins 104 may each include a quantum well layer of the quantum well stack (discussed below with reference to the quantum well layer 152). Examples of base/fin arrangements are discussed below with reference to the base fin arrangements 158 of FIGS. 29-35.

[0028] Although only two fins, 104-1 and 104-2, are shown in FIGS. 1-3, this is simply for ease of illustration, and more than two fins 104 may be included in the quantum dot device 100. In some embodiments, the total number of fins 104 included in the quantum dot device 100 is an even number, with the fins 104 organized into pairs including one active fin 104 and one read fin 104, as discussed in detail below. When the quantum dot device 100 includes more than two fins 104, the fins 104 may be arranged in pairs in a line (e.g., $2N$ fins total may be arranged in a $1 \times 2N$ line, or a $2 \times N$ line) or in pairs in a larger array (e.g., $2N$ fins total may be arranged as a $4 \times N/2$ array, a $6 \times N/3$ array, etc.). The discussion herein will largely focus on a single pair of fins 104 for ease of illustration, but all the teachings of the present disclosure apply to quantum dot devices 100 with more fins 104.

[0029] As noted above, each of the fins 104 may include a quantum well layer (not shown in FIGS. 1-3, but discussed below with reference to the quantum well layer 152). The quantum well layer included in the fins 104 may be arranged normal to the z -direction, and may provide a layer in which a two-dimensional electron gas (2DEG) may form to enable the generation of a quantum dot during operation of the quantum dot device 100, as discussed in further detail below. The quantum well layer itself may provide a geometric constraint on the z -location of quantum dots in the fins 104, and the limited extent of the fins 104 (and therefore the quantum well layer) in the y -direction may provide a geometric constraint on the y -location of quantum dots in the fins 104. To control the x -location of quantum dots in the fins 104, voltages may be applied to gates disposed on the fins 104 to adjust the energy profile along the fins 104 in the x -direction and thereby constrain the x -location of quantum dots within quantum wells (discussed in detail below with reference to the gates 106/108). The dimensions of the fins 104 may take any suitable values. For example, in some embodiments, the fins 104 may each have a width 162 between 10 and 30 nanometers. In some embodiments, the fins 104 may each have a height 164 between 200 and 400 nanometers (e.g., between 250 and 350 nanometers, or equal to 300 nanometers).

[0030] The fins 104 may be arranged in parallel, as illustrated in FIGS. 1 and 3, and may be spaced apart by an insulating material 128, which may be disposed on opposite faces of the fins 104. The insulating material 128 may be a dielectric material, such as silicon oxide. For example, in some embodiments, the fins 104 may be spaced apart by a distance 160 between 100 and 250 microns.

[0031] Multiple gates may be disposed on each of the fins 104. In the embodiment illustrated in FIG. 2, three gates 106 and two gates 108 are shown as distributed on the top of the fin 104. This particular number of gates is simply illustrative, and any suitable number of gates may be used. Additionally, as discussed below with reference to FIG. 39, multiple groups of gates (like the gates illustrated in FIG. 2) may be disposed on the fin 104.

[0032] As shown in FIG. 2, the gate 108-1 may be disposed between the gates 106-1 and 106-2, and the gate 108-2 may be disposed between the gates 106-2 and 106-3. Each of the gates 106/108 may include a gate dielectric 114; in the embodiment illustrated in FIG. 2, the gate dielectric 114 for all of the gates 106/108 is provided by a common layer of gate dielectric material. In other embodiments, the gate dielectric 114 for each of the gates 106/108 may be provided by separate portions of gate dielectric 114 (e.g., as discussed below with reference to FIGS. 40-44). In some embodiments, the gate dielectric 114 may be a multilayer gate dielectric (e.g., with multiple materials used to improve the interface between the fin 104 and the corresponding gate metal). The gate dielectric 114 may be, for example, silicon oxide, aluminum oxide, or a high-k dielectric, such as hafnium oxide. More generally, the gate dielectric 114 may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of materials that may be used in the gate dielectric 114 may include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, tantalum oxide, tantalum silicon oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric 114 to improve the quality of the gate dielectric 114.

[0033] Each of the gates 106 may include a gate metal 110 and a hardmask 116. The hardmask 116 may be formed of silicon nitride, silicon carbide, or another suitable material. The gate metal 110 may be disposed between the hardmask 116 and the gate dielectric 114, and the gate dielectric 114 may be disposed between the gate metal 110 and the fin 104. Only one portion of the hardmask 116 is labeled in FIG. 2 for ease of illustration. In some embodiments, the gate metal 110 may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or niobium titanium nitride. In some embodiments, the hardmask 116 may not be present in the quantum dot device 100 (e.g., a hardmask like the hardmask 116 may be removed during processing, as discussed below). The sides of the gate metal 110 may be substantially parallel, as shown in FIG. 2, and insulating spacers 134 may be disposed on the sides of the gate metal 110 and the hardmask 116. As illustrated in FIG. 2, the spacers 134 may be thicker closer to the fin 104 and

thinner farther away from the fin 104. In some embodiments, the spacers 134 may have a convex shape. The spacers 134 may be formed of any suitable material, such as a carbon-doped oxide, silicon nitride, silicon oxide, or other carbides or nitrides (e.g., silicon carbide, silicon nitride doped with carbon, and silicon oxynitride). The gate metal 110 may be any suitable metal, such as titanium nitride.

[0034] Each of the gates 108 may include a gate metal 112 and a hardmask 118. The hardmask 118 may be formed of silicon nitride, silicon carbide, or another suitable material. The gate metal 112 may be disposed between the hardmask 118 and the gate dielectric 114, and the gate dielectric 114 may be disposed between the gate metal 112 and the fin 104. In the embodiment illustrated in FIG. 2, the hardmask 118 may extend over the hardmask 116 (and over the gate metal 110 of the gates 106), while in other embodiments, the hardmask 118 may not extend over the gate metal 110 (e.g., as discussed below with reference to FIG. 45). In some embodiments, the gate metal 112 may be a different metal from the gate metal 110; in other embodiments, the gate metal 112 and the gate metal 110 may have the same material composition. In some embodiments, the gate metal 112 may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or niobium titanium nitride. In some embodiments, the hardmask 118 may not be present in the quantum dot device 100 (e.g., a hardmask like the hardmask 118 may be removed during processing, as discussed below).

[0035] The gate 108-1 may extend between the proximate spacers 134 on the sides of the gate 106-1 and the gate 106-2, as shown in FIG. 2. In some embodiments, the gate metal 112 of the gate 108-1 may extend between the spacers 134 on the sides of the gate 106-1 and the gate 106-2. Thus, the gate metal 112 of the gate 108-1 may have a shape that is substantially complementary to the shape of the spacers 134, as shown. Similarly, the gate 108-2 may extend between the proximate spacers 134 on the sides of the gate 106-2 and the gate 106-3. In some embodiments in which the gate dielectric 114 is not a layer shared commonly between the gates 108 and 106, but instead is separately deposited on the fin 104 between the spacers 134 (e.g., as discussed below with reference to FIGS. 40-44), the gate dielectric 114 may extend at least partially up the sides of the spacers 134, and the gate metal 112 may extend between the portions of gate dielectric 114 on the spacers 134. The gate metal 112, like the gate metal 110, may be any suitable metal, such as titanium nitride.

[0036] The dimensions of the gates 106/108 may take any suitable values. For example, in some embodiments, the z-height 166 of the gate metal 110 may be between 40 and 75 nanometers (e.g., approximately 50 nanometers); the z-height of the gate metal 112 may be in the same range. In embodiments like the ones illustrated in FIGS. 2, 38, and 45, the z-height of the gate metal 112 may

be greater than the z-height of the gate metal 110. In some embodiments, the length 168 of the gate metal 110 (i.e., in the x-direction) may be between 20 and 40 nanometers (e.g., 30 nanometers). In some embodiments, the distance 170 between adjacent ones of the gates 106 (e.g., as measured from the gate metal 110 of one gate 106 to the gate metal 110 of an adjacent gate 106 in the x-direction, as illustrated in FIG. 2) may be between 40 and 60 nanometers (e.g., 50 nanometers). In some embodiments, the thickness 172 of the spacers 134 may be between 1 and 10 nanometers (e.g., between 3 and 5 nanometers, between 4 and 6 nanometers, or between 4 and 7 nanometers). The length of the gate metal 112 (i.e., in the x-direction) may depend on the dimensions of the gates 106 and the spacers 134, as illustrated in FIG. 2. As indicated in FIG. 1, the gates 106/108 on one fin 104 may extend over the insulating material 128 beyond their respective fins 104 and towards the other fin 104, but may be isolated from their counterpart gates by the intervening insulating material 130 and spacers 134.

[0037] As shown in FIG. 2, the gates 106 and 108 may be alternately arranged along the fin 104 in the x-direction. During operation of the quantum dot device 100, voltages may be applied to the gates 106/108 to adjust the potential energy in the quantum well layer (not shown) in the fin 104 to create quantum wells of varying depths in which quantum dots 142 may form. Only one quantum dot 142 is labeled with a reference numeral in FIGS. 2 and 3 for ease of illustration, but five are indicated as dotted circles in each fin 104. The location of the quantum dots 142 in FIG. 2 is not intended to indicate a particular geometric positioning of the quantum dots 142. The spacers 134 may themselves provide "passive" barriers between quantum wells under the gates 106/108 in the quantum well layer, and the voltages applied to different ones of the gates 106/108 may adjust the potential energy under the gates 106/108 in the quantum well layer; decreasing the potential energy may form quantum wells, while increasing the potential energy may form quantum barriers.

[0038] The fins 104 may include doped regions 140 that may serve as a reservoir of charge carriers for the quantum dot device 100. For example, an n-type doped region 140 may supply electrons for electron-type quantum dots 142, and a p-type doped region 140 may supply holes for hole-type quantum dots 142. In some embodiments, an interface material 141 may be disposed at a surface of a doped region 140, as shown. The interface material 141 may facilitate electrical coupling between a conductive contact (e.g., a conductive via 136, as discussed below) and the doped region 140. The interface material 141 may be any suitable metal-semiconductor ohmic contact material; for example, in embodiments in which the doped region 140 includes silicon, the interface material 141 may include nickel silicide, aluminum silicide, titanium silicide, molybdenum silicide, cobalt silicide, tungsten silicide, or platinum silicide (e.g., as discussed below with reference to FIGS. 22-23). In some embodiments, the interface material 141 may be a non-silicide compound, such as titanium

nitride. In some embodiments, the interface material 141 may be a metal (e.g., aluminum, tungsten, or indium).

[0039] The quantum dot devices 100 disclosed herein may be used to form electron-type or hole-type quantum dots 142. Note that the polarity of the voltages applied to the gates 106/108 to form quantum wells/barriers depend on the charge carriers used in the quantum dot device 100. In embodiments in which the charge carriers are electrons (and thus the quantum dots 142 are electron-type quantum dots), apply negative voltages applied to a gate 106/108 may increase the potential barrier under the gate 106/108, and apply positive voltages applied to a gate 106/108 may decrease the potential barrier under the gate 106/108 (thereby forming a potential well in which an electron-type quantum dot 142 may form). In embodiments in which the charge carriers are holes (and thus the quantum dots 142 are hole-type quantum dots), apply positive voltages applied to a gate 106/108 may increase the potential barrier under the gate 106/108, and apply negative voltages applied to a gate 106 and 108 may decrease the potential barrier under the gate 106/108 (thereby forming a potential well in which a hole-type quantum dot 142 may form). The quantum dot devices 100 disclosed herein may be used to form electron-type or hole-type quantum dots.

[0040] Voltages may be applied to each of the gates 106 and 108 separately to adjust the potential energy in the quantum well layer under the gates 106 and 108, and thereby control the formation of quantum dots 142 under each of the gates 106 and 108. Additionally, the relative potential energy profiles under different ones of the gates 106 and 108 allow the quantum dot device 100 to tune the potential interaction between quantum dots 142 under adjacent gates. For example, if two adjacent quantum dots 142 (e.g., one quantum dot 142 under a gate 106 and another quantum dot 142 under a gate 108) are separated by only a short potential barrier, the two quantum dots 142 may interact more strongly than if they were separated by a taller potential barrier. Since the depth of the potential wells/height of the potential barriers under each gate 106/108 may be adjusted by adjusting the voltages on the respective gates 106/108, the differences in potential between adjacent gates 106/108 may be adjusted, and thus the interaction tuned.

[0041] In some applications, the gates 108 may be used as plunger gates to enable the formation of quantum dots 142 under the gates 108, while the gates 106 may be used as barrier gates to adjust the potential barrier between quantum dots 142 formed under adjacent gates 108. In other applications, the gates 108 may be used as barrier gates, while the gates 106 are used as plunger gates. In other applications, quantum dots 142 may be formed under all of the gates 106 and 108, or under any desired subset of the gates 106 and 108.

[0042] Conductive vias and lines may make contact with the gates 106/108, and to the doped regions 140, to enable electrical connection to the gates 106/108 and the doped regions 140 to be

made in desired locations. As shown in FIGS. 1-3, the gates 106 may extend away from the fins 104, and conductive vias 120 may contact the gates 106 (and are drawn in dashed lines in FIG. 2 to indicate their location behind the plane of the drawing). The conductive vias 120 may extend through the hardmask 116 and the hardmask 118 to contact the gate metal 110 of the gates 106. The gates 108 may extend away from the fins 104, and conductive vias 122 may contact the gates 108 (also drawn in dashed lines in FIG. 2 to indicate their location behind the plane of the drawing). The conductive vias 122 may extend through the hardmask 118 to contact the gate metal 112 of the gates 108. Conductive vias 136 may contact the interface material 141 and may thereby make electrical contact with the doped regions 140. The quantum dot device 100 may include further conductive vias and/or lines (not shown) to make electrical contact to the gates 106/108 and/or the doped regions 140, as desired. The conductive vias and lines included in a quantum dot device 100 may include any suitable materials, such as copper, tungsten (deposited, e.g., by CVD), or a superconductor (e.g., aluminum, tin, titanium nitride, niobium titanium nitride, tantalum, niobium, or other niobium compounds such as niobium tin and niobium germanium).

[0043] During operation, a bias voltage may be applied to the doped regions 140 (e.g., via the conductive vias 136 and the interface material 141) to cause current to flow through the doped regions 140. When the doped regions 140 are doped with an n-type material, this voltage may be positive; when the doped regions 140 are doped with a p-type material, this voltage may be negative. The magnitude of this bias voltage may take any suitable value (e.g., between 0.25 volts and 2 volts).

[0044] The conductive vias 120, 122, and 136 may be electrically isolated from each other by an insulating material 130. The insulating material 130 may be any suitable material, such as an interlayer dielectric (ILD). Examples of the insulating material 130 may include silicon oxide, silicon nitride, aluminum oxide, carbon-doped oxide, and/or silicon oxynitride. As known in the art of integrated circuit manufacturing, conductive vias and lines may be formed in an iterative process in which layers of structures are formed on top of each other. In some embodiments, the conductive vias 120/122/136 may have a width that is 20 nanometers or greater at their widest point (e.g., 30 nanometers), and a pitch of 80 nanometers or greater (e.g., 100 nanometers). In some embodiments, conductive lines (not shown) included in the quantum dot device 100 may have a width that is 100 nanometers or greater, and a pitch of 100 nanometers or greater. The particular arrangement of conductive vias shown in FIGS. 1-3 is simply illustrative, and any electrical routing arrangement may be implemented.

[0045] As discussed above, the structure of the fin 104-1 may be the same as the structure of the fin 104-2; similarly, the construction of gates 106/108 on the fin 104-1 may be the same as the

construction of gates 106/108 on the fin 104-2. The gates 106/108 on the fin 104-1 may be mirrored by corresponding gates 106/108 on the parallel fin 104-2, and the insulating material 130 may separate the gates 106/108 on the different fins 104-1 and 104-2. In particular, quantum dots 142 formed in the fin 104-1 (under the gates 106/108) may have counterpart quantum dots 142 in the fin 104-2 (under the corresponding gates 106/108). In some embodiments, the quantum dots 142 in the fin 104-1 may be used as "active" quantum dots in the sense that these quantum dots 142 act as qubits and are controlled (e.g., by voltages applied to the gates 106/108 of the fin 104-1) to perform quantum computations. The quantum dots 142 in the fin 104-2 may be used as "read" quantum dots in the sense that these quantum dots 142 may sense the quantum state of the quantum dots 142 in the fin 104-1 by detecting the electric field generated by the charge in the quantum dots 142 in the fin 104-1, and may convert the quantum state of the quantum dots 142 in the fin 104-1 into electrical signals that may be detected by the gates 106/108 on the fin 104-2. Each quantum dot 142 in the fin 104-1 may be read by its corresponding quantum dot 142 in the fin 104-2. Thus, the quantum dot device 100 enables both quantum computation and the ability to read the results of a quantum computation.

[0046] The quantum dot devices 100 disclosed herein may be manufactured using any suitable techniques. FIGS. 4-25 illustrate various example stages in the manufacture of the quantum dot device 100 of FIGS. 1-3, in accordance with various embodiments. Although the particular manufacturing operations discussed below with reference to FIGS. 4-25 are illustrated as manufacturing a particular embodiment of the quantum dot device 100, these operations may be applied to manufacture many different embodiments of the quantum dot device 100, as discussed herein. Any of the elements discussed below with reference to FIGS. 4-25 may take the form of any of the embodiments of those elements discussed above (or otherwise disclosed herein).

[0047] FIG. 4 illustrates a cross-sectional view of an assembly 200 including a substrate 144. The substrate 144 may include any suitable semiconductor material or materials. In some embodiments, the substrate 144 may include a semiconductor material. For example, the substrate 144 may include silicon (e.g., may be formed from a silicon wafer).

[0048] FIG. 5 illustrates a cross-sectional view of an assembly 202 subsequent to providing a quantum well stack 146 on the substrate 144 of the assembly 200 (FIG. 4). The quantum well stack 146 may include a quantum well layer (not shown) in which a 2DEG may form during operation of the quantum dot device 100. Various embodiments of the quantum well stack 146 are discussed below with reference to FIGS. 26-28.

[0049] FIG. 6 illustrates a cross-sectional view of an assembly 204 subsequent to forming fins 104 in the assembly 202 (FIG. 5). The fins 104 may extend from a base 102, and may be formed in the

assembly 202 by patterning and then etching the assembly 202, as known in the art. For example, a combination of dry and wet etch chemistry may be used to form the fins 104, and the appropriate chemistry may depend on the materials included in the assembly 202, as known in the art. At least some of the substrate 144 may be included in the base 102, and at least some of the quantum well stack 146 may be included in the fins 104. In particular, the quantum well layer (not shown) of the quantum well stack 146 may be included in the fins 104. Example arrangements in which the quantum well stack 146 and the substrate 144 are differently included in the base 102 and the fins 104 are discussed below with reference to FIGS. 29-35.

[0050] FIG. 7 illustrates a cross-sectional view of an assembly 206 subsequent to providing an insulating material 128 to the assembly 204 (FIG. 6). Any suitable material may be used as the insulating material 128 to electrically insulate the fins 104 from each other. As noted above, in some embodiments, the insulating material 128 may be a dielectric material, such as silicon oxide.

[0051] FIG. 8 illustrates a cross-sectional view of an assembly 208 subsequent to planarizing the assembly 206 (FIG. 7) to remove the insulating material 128 above the fins 104. In some embodiments, the assembly 206 may be planarized using a chemical mechanical polishing (CMP) technique.

[0052] FIG. 9 is a perspective view of at least a portion of the assembly 208, showing the fins 104 extending from the base 102 and separated by the insulating material 128. The cross-sectional views of FIGS. 4-8 are taken parallel to the plane of the page of the perspective view of FIG. 9. FIG. 10 is another cross-sectional view of the assembly 208, taken along the dashed line along the fin 104-1 in FIG. 9. The cross-sectional views illustrated in FIGS. 11-25 are taken along the same cross-section as FIG. 10.

[0053] FIG. 11 is a cross-sectional view of an assembly 210 subsequent to forming a gate stack 174 on the fins 104 of the assembly 208 (FIGS. 8-10). The gate stack 174 may include the gate dielectric 114, the gate metal 110, and a hardmask 116. The hardmask 116 may be formed of an electrically insulating material, such as silicon nitride or carbon-doped nitride.

[0054] FIG. 12 is a cross-sectional view of an assembly 212 subsequent to patterning the hardmask 116 of the assembly 210 (FIG. 11). The pattern applied to the hardmask 116 may correspond to the locations for the gates 106, as discussed below. The hardmask 116 may be patterned by applying a resist, patterning the resist using lithography, and then etching the hardmask (using dry etching or any appropriate technique).

[0055] FIG. 13 is a cross-sectional view of an assembly 214 subsequent to etching the assembly 212 (FIG. 12) to remove the gate metal 110 that is not protected by the patterned hardmask 116 to form the gates 106. In some embodiments, as illustrated in FIG. 13, the gate dielectric 114 may remain

after the etched gate metal 110 is etched away; in other embodiments, the gate dielectric 114 may also be etched during the etching of the gate metal 110. Examples of such embodiments are discussed below with reference to FIGS. 40-44.

[0056] FIG. 14 is a cross-sectional view of an assembly 216 subsequent to providing spacer material 132 on the assembly 214 (FIG. 13). The spacer material 132 may include any of the materials discussed above with reference to the spacers 134, for example, and may be deposited using any suitable technique. For example, the spacer material 132 may be a nitride material (e.g., silicon nitride) deposited by sputtering.

[0057] FIG. 15 is a cross-sectional view of an assembly 218 subsequent to etching the spacer material 132 of the assembly 216 (FIG. 14), leaving spacers 134 formed of the spacer material 132 on the sides of the gates 106 (e.g., on the sides of the hardmask 116 and the gate metal 110). The etching of the spacer material 132 may be an anisotropic etch, etching the spacer material 132 "downward" to remove the spacer material 132 on top of the gates 106 and in some of the area between the gates 106, while leaving the spacers 134 on the sides of the gates 106. In some embodiments, the anisotropic etch may be a dry etch.

[0058] FIG. 16 is a cross-sectional view of an assembly 220 subsequent to providing the gate metal 112 on the assembly 218 (FIG. 15). The gate metal 112 may fill the areas between adjacent ones of the gates 106, and may extend over the tops of the gates 106.

[0059] FIG. 17 is a cross-sectional view of an assembly 222 subsequent to planarizing the assembly 220 (FIG. 16) to remove the gate metal 112 above the gates 106. In some embodiments, the assembly 220 may be planarized using a CMP technique. Some of the remaining gate metal 112 may fill the areas between adjacent ones of the gates 106, while other portions 150 of the remaining gate metal 112 may be located "outside" of the gates 106.

[0060] FIG. 18 is a cross-sectional view of an assembly 224 subsequent to providing a hardmask 118 on the planarized surface of the assembly 222 (FIG. 17). The hardmask 118 may be formed of any of the materials discussed above with reference to the hardmask 116, for example.

[0061] FIG. 19 is a cross-sectional view of an assembly 226 subsequent to patterning the hardmask 118 of the assembly 224 (FIG. 18). The pattern applied to the hardmask 118 may extend over the hardmask 116 (and over the gate metal 110 of the gates 106, as well as over the locations for the gates 108 (as illustrated in FIG. 2). The hardmask 118 may be non-coplanar with the hardmask 116, as illustrated in FIG. 19. The hardmask 118 illustrated in FIG. 19 may thus be a common, continuous portion of hardmask 118 that extends over all of the hardmask 116. Examples of embodiments in which the hardmask 118 is not disposed over the entirety of the hardmask 116 are discussed below

with reference to FIGS. 36-38 and 45. The hardmask 118 may be patterned using any of the techniques discussed above with reference to the patterning of the hardmask 116, for example.

[0062] FIG. 20 is a cross-sectional view of an assembly 228 subsequent to etching the assembly 226 (FIG. 19) to remove the portions 150 that are not protected by the patterned hardmask 118 to form the gates 108. Portions of the hardmask 118 may remain on top of the hardmask 116, as shown. The operations performed on the assembly 226 may include removing any gate dielectric 114 that is "exposed" on the fin 104, as shown. The excess gate dielectric 114 may be removed using any suitable technique, such as chemical etching or silicon bombardment.

[0063] FIG. 21 is a cross-sectional view of an assembly 230 subsequent to doping the fins 104 of the assembly 228 (FIG. 20) to form doped regions 140 in the portions of the fins 104 "outside" of the gates 106/108. The type of dopant used to form the doped regions 140 may depend on the type of quantum dot desired, as discussed above. In some embodiments, the doping may be performed by ion implantation. For example, when the quantum dot 142 is to be an electron-type quantum dot 142, the doped regions 140 may be formed by ion implantation of phosphorous, arsenic, or another n-type material. When the quantum dot 142 is to be a hole-type quantum dot 142, the doped regions 140 may be formed by ion implantation of boron or another p-type material. An annealing process that activates the dopants and causes them to diffuse farther into the fins 104 may follow the ion implantation process. The depth of the doped regions 140 may take any suitable value; for example, in some embodiments, the doped regions 140 may extend into the fin 104 to a depth 115 between 500 and 1000 Angstroms.

[0064] The outer spacers 134 on the outer gates 106 may provide a doping boundary, limiting diffusion of the dopant from the doped regions 140 into the area under the gates 106/108. As shown, the doped regions 140 may extend under the adjacent outer spacers 134. In some embodiments, the doped regions 140 may extend past the outer spacers 134 and under the gate metal 110 of the outer gates 106, may extend only to the boundary between the outer spacers 134 and the adjacent gate metal 110, or may terminate under the outer spacers 134 and not reach the boundary between the outer spacers 134 and the adjacent gate metal 110. Examples of such embodiments are discussed below with reference to FIGS. 46 and 47. The doping concentration of the doped regions 140 may, in some embodiments, be between $10^{17}/\text{cm}^3$ and $10^{20}/\text{cm}^3$.

[0065] FIG. 22 is a cross-sectional side view of an assembly 232 subsequent to providing a layer of nickel or other material 143 over the assembly 230 (FIG. 21). The nickel or other material 143 may be deposited on the assembly 230 using any suitable technique (e.g., a plating technique, chemical vapor deposition, or atomic layer deposition).

[0066] FIG. 23 is a cross-sectional side view of an assembly 234 subsequent to annealing the assembly 232 (FIG. 22) to cause the material 143 to interact with the doped regions 140 to form the interface material 141, then removing the unreacted material 143. When the doped regions 140 include silicon and the material 143 includes nickel, for example, the interface material 141 may be nickel silicide. Materials other than nickel may be deposited in the operations discussed above with reference to FIG. 22 in order to form other interface materials 141, including titanium, aluminum, molybdenum, cobalt, tungsten, or platinum, for example. More generally, the interface material 141 of the assembly 234 may include any of the materials discussed herein with reference to the interface material 141.

[0067] FIG. 24 is a cross-sectional view of an assembly 236 subsequent to providing an insulating material 130 on the assembly 234 (FIG. 23). The insulating material 130 may take any of the forms discussed above. For example, the insulating material 130 may be a dielectric material, such as silicon oxide. The insulating material 130 may be provided on the assembly 234 using any suitable technique, such as spin coating, chemical vapor deposition (CVD), or plasma-enhanced CVD (PECVD). In some embodiments, the insulating material 130 may be polished back after deposition, and before further processing.

[0068] FIG. 25 is a cross-sectional view of an assembly 238 subsequent to forming, in the assembly 236 (FIG. 24), conductive vias 120 through the insulating material 130 (and the hardmasks 116 and 118) to contact the gate metal 110 of the gates 106, conductive vias 122 through the insulating material 130 (and the hardmask 118) to contact the gate metal 112 of the gates 108, and conductive vias 136 through the insulating material 130 to contact the interface material 141 of the doped regions 140. Further conductive vias and/or lines may be formed on the assembly 238 using conventional interconnect techniques, if desired. The resulting assembly 238 may take the form of the quantum dot device 100 discussed above with reference to FIGS. 1-3. In some embodiments, the assembly 236 may be planarized to remove the hardmasks 116 and 118, then additional insulating material 130 may be provided on the planarized surface before forming the conductive vias 120, 122, and 136; in such an embodiment, the hardmasks 116 and 118 would not be present in the quantum dot device 100.

[0069] As discussed above, the base 102 and the fin 104 of a quantum dot device 100 may be formed from a substrate 144 and a quantum well stack 146 disposed on the substrate 144. The quantum well stack 146 may include a quantum well layer in which a 2DEG may form during operation of the quantum dot device 100. The quantum well stack 146 may take any of a number of forms, several of which are illustrated in FIGS. 26-28. The various layers in the quantum well stacks 146 discussed below may be grown on the substrate 144 (e.g., using epitaxial processes).

[0070] FIG. 26 is a cross-sectional view of a quantum well stack 146 including only a quantum well layer 152. The quantum well layer 152 may be disposed on the substrate 144 (e.g., as discussed above with reference to FIG. 5), and may be formed of a material such that, during operation of the quantum dot device 100, a 2DEG may form in the quantum well layer 152 proximate to the upper surface of the quantum well layer 152. The gate dielectric 114 of the gates 106/108 may be disposed on the upper surface of the quantum well layer 152 (e.g., as discussed above with reference to FIG. 11). In some embodiments, the quantum well layer 152 of FIG. 26 may be formed of intrinsic silicon, and the gate dielectric 114 may be formed of silicon oxide; in such an arrangement, during use of the quantum dot device 100, a 2DEG may form in the intrinsic silicon at the interface between the intrinsic silicon and the silicon oxide. Embodiments in which the quantum well layer 152 of FIG. 26 is formed of intrinsic silicon may be particularly advantageous for electron-type quantum dot devices 100. In some embodiments, the quantum well layer 152 of FIG. 26 may be formed of intrinsic germanium, and the gate dielectric 114 may be formed of germanium oxide; in such an arrangement, during use of the quantum dot device 100, a 2DEG may form in the intrinsic germanium at the interface between the intrinsic germanium and the germanium oxide. Such embodiments may be particularly advantageous for hole-type quantum dot devices 100. In some embodiments, the quantum well layer 152 may be strained, while in other embodiments, the quantum well layer 152 may not be strained. The thicknesses (i.e., z-heights) of the layers in the quantum well stack 146 of FIG. 26 may take any suitable values. For example, in some embodiments, the thickness of the quantum well layer 152 (e.g., intrinsic silicon or germanium) may be between 0.8 and 1.2 microns.

[0071] FIG. 27 is a cross-sectional view of a quantum well stack 146 including a quantum well layer 152 and a barrier layer 154. The quantum well stack 146 may be disposed on a substrate 144 (e.g., as discussed above with reference to FIG. 5) such that the barrier layer 154 is disposed between the quantum well layer 152 and the substrate 144. The barrier layer 154 may provide a potential barrier between the quantum well layer 152 and the substrate 144. As discussed above with reference to FIG. 26, the quantum well layer 152 of FIG. 27 may be formed of a material such that, during operation of the quantum dot device 100, a 2DEG may form in the quantum well layer 152 proximate to the upper surface of the quantum well layer 152. For example, in some embodiments in which the substrate 144 is formed of silicon, the quantum well layer 152 of FIG. 27 may be formed of silicon, and the barrier layer 154 may be formed of silicon germanium. The germanium content of this silicon germanium may be 20-80% (e.g., 30%). In some embodiments in which the quantum well layer 152 is formed of germanium, the barrier layer 154 may be formed of silicon germanium (with a germanium content of 20-80% (e.g., 70%)). The thicknesses (i.e., z-heights) of the layers in the

quantum well stack 146 of FIG. 27 may take any suitable values. For example, in some embodiments, the thickness of the barrier layer 154 (e.g., silicon germanium) may be between 0 and 400 nanometers. In some embodiments, the thickness of the quantum well layer 152 (e.g., silicon or germanium) may be between 5 and 30 nanometers.

[0072] FIG. 28 is a cross-sectional view of a quantum well stack 146 including a quantum well layer 152 and a barrier layer 154-1, as well as a buffer layer 176 and an additional barrier layer 154-2. The quantum well stack 146 may be disposed on the substrate 144 (e.g., as discussed above with reference to FIG. 5) such that the buffer layer 176 is disposed between the barrier layer 154-1 and the substrate 144. The buffer layer 176 may be formed of the same material as the barrier layer 154, and may be present to trap defects that form in this material as it is grown on the substrate 144. In some embodiments, the buffer layer 176 may be grown under different conditions (e.g., deposition temperature or growth rate) from the barrier layer 154-1. In particular, the barrier layer 154-1 may be grown under conditions that achieve fewer defects than the buffer layer 176. In some embodiments in which the buffer layer 176 includes silicon germanium, the silicon germanium of the buffer layer 176 may have a germanium content that varies from the substrate 144 to the barrier layer 154-1; for example, the silicon germanium of the buffer layer 176 may have a germanium content that varies from zero percent at the silicon substrate 144 to a nonzero percent (e.g., 30%) at the barrier layer 154-1. The thicknesses (i.e., z-heights) of the layers in the quantum well stack 146 of FIG. 28 may take any suitable values. For example, in some embodiments, the thickness of the buffer layer 176 (e.g., silicon germanium) may be between 0.3 and 4 microns (e.g., 0.3-2 microns, or 0.5 microns). In some embodiments, the thickness of the barrier layer 154-1 (e.g., silicon germanium) may be between 0 and 400 nanometers. In some embodiments, the thickness of the quantum well layer 152 (e.g., silicon or germanium) may be between 5 and 30 nanometers (e.g., 10 nanometers). The barrier layer 154-2, like the barrier layer 154-1, may provide a potential energy barrier around the quantum well layer 152, and may take the form of any of the embodiments of the barrier layer 154-1. In some embodiments, the thickness of the barrier layer 154-2 (e.g., silicon germanium) may be between 25 and 75 nanometers (e.g., 32 nanometers).

[0073] As discussed above with reference to FIG. 27, the quantum well layer 152 of FIG. 28 may be formed of a material such that, during operation of the quantum dot device 100, a 2DEG may form in the quantum well layer 152 proximate to the upper surface of the quantum well layer 152. For example, in some embodiments in which the substrate 144 is formed of silicon, the quantum well layer 152 of FIG. 28 may be formed of silicon, and the barrier layer 154-1 and the buffer layer 176 may be formed of silicon germanium. In some such embodiments, the silicon germanium of the buffer layer 176 may have a germanium content that varies from the substrate 144 to the barrier

layer 154-1; for example, the silicon germanium of the buffer layer 176 may have a germanium content that varies from zero percent at the silicon substrate 144 to a nonzero percent (e.g., 30%) at the barrier layer 154-1. The barrier layer 154-1 may in turn have a germanium content equal to the nonzero percent. In other embodiments, the buffer layer 176 may have a germanium content equal to the germanium content of the barrier layer 154-1, but may be thicker than the barrier layer 154-1 so as to absorb the defects that arise during growth. The barrier layer 154-2, like the barrier layer 154-1, may provide a potential energy barrier around the quantum well layer 152, and may take the form of any of the embodiments of the barrier layer 154-1. In some embodiments of the quantum well stack 146 of FIG. 28, the buffer layer 176 and/or the barrier layer 154-2 may be omitted.

[0074] The substrate 144 and the quantum well stack 146 may be distributed between the base 102 and the fins 104 of the quantum dot device 100, as discussed above. This distribution may occur in any of a number of ways. For example, FIGS. 29-35 illustrate example base/fin arrangements 158 that may be used in a quantum dot device 100, in accordance with various embodiments.

[0075] In the base/fin arrangement 158 of FIG. 29, the quantum well stack 146 may be included in the fins 104, but not in the base 102. The substrate 144 may be included in the base 102, but not in the fins 104. When the base/fin arrangement 158 of FIG. 29 is used in the manufacturing operations discussed with reference to FIGS. 5-6, the fin etching may etch through the quantum well stack 146, and stop when the substrate 144 is reached.

[0076] In the base/fin arrangement 158 of FIG. 30, the quantum well stack 146 may be included in the fins 104, as well as in a portion of the base 102. A substrate 144 may be included in the base 102 as well, but not in the fins 104. When the base/fin arrangement 158 of FIG. 30 is used in the manufacturing operations discussed with reference to FIGS. 5-6, the fin etching may etch partially through the quantum well stack 146, and stop before the substrate 144 is reached. FIG. 31 illustrates a particular embodiment of the base/fin arrangement 158 of FIG. 30. In the embodiment of FIG. 31, the quantum well stack 146 of FIG. 28 is used; the fins 104 include the barrier layer 154-1, the quantum well layer 152, and the barrier layer 154-2, while the base 102 includes the buffer layer 176 and the substrate 144.

[0077] In the base/fin arrangement 158 of FIG. 32, the quantum well stack 146 may be included in the fins 104, but not the base 102. The substrate 144 may be partially included in the fins 104, as well as in the base 102. When the base/fin arrangement 158 of FIG. 32 is used in the manufacturing operations discussed with reference to FIGS. 5-6, the fin etching may etch through the quantum well stack 146 and into the substrate 144 before stopping. FIG. 33 illustrates a particular embodiment of the base/fin arrangement 158 of FIG. 32. In the embodiment of FIG. 33, the quantum well stack 146

of FIG. 28 is used; the fins 104 include the quantum well stack 146 and a portion of the substrate 144, while the base 102 includes the remainder of the substrate 144.

[0078] Although the fins 104 have been illustrated in many of the preceding figures as substantially rectangular with parallel sidewalls, this is simply for ease of illustration, and the fins 104 may have any suitable shape (e.g., shape appropriate to the manufacturing processes used to form the fins 104). For example, as illustrated in the base/fin arrangement 158 of FIG. 34, in some embodiments, the fins 104 may be tapered. In some embodiments, the fins 104 may taper by 3-10 nanometers in x-width for every 100 nanometers in z-height (e.g., 5 nanometers in x-width for every 100 nanometers in z-height). When the fins 104 are tapered, the wider end of the fins 104 may be the end closest to the base 102, as illustrated in FIG. 34. FIG. 35 illustrates a particular embodiment of the base/fin arrangement 158 of FIG. 34. In FIG. 35, the quantum well stack 146 is included in the tapered fins 104 while a portion of the substrate 144 is included in the tapered fins and a portion of the substrate 144 provides the base 102.

[0079] In the embodiment of the quantum dot device 100 illustrated in FIG. 2, the z-height of the gate metal 112 of the gates 108 may be approximately equal to the sum of the z-height of the gate metal 110 and the z-height of the hardmask 116, as shown. Also in the embodiment of FIG. 2, the gate metal 112 of the gates 108 may not extend in the x-direction beyond the adjacent spacers 134. In other embodiments, the z-height of the gate metal 112 of the gates 108 may be greater than the sum of the z-height of the gate metal 110 and the z-height of the hardmask 116, and in some such embodiments, the gate metal 112 of the gates may extend beyond the spacers 134 in the x-direction. FIGS. 36-38 illustrate various example stages in the manufacture of alternative gate arrangements that may be included in a quantum dot device 100, in accordance with various embodiments.

[0080] FIG. 36 illustrates an assembly 242 subsequent to providing the gate metal 112 and a hardmask 118 on the assembly 218 (FIG. 15). The assembly 242 may be similar to the assembly 224 of FIG. 18 (and may be formed using any of the techniques discussed above with reference to FIGS. 16-18), but may include additional gate metal 112 between the hardmask 116 and the hardmask 118, of any desired thickness. In some embodiments, the gate metal 112 may be planarized prior to provision of the hardmask 118, but the hardmask 118 may still be spaced away from the hardmask 116 in the z-direction by the gate metal 112, as shown in FIG. 36.

[0081] FIG. 37 illustrates an assembly 244 subsequent to patterning the hardmask 118 of the assembly 242 (FIG. 36). The pattern applied to the hardmask 118 may include the locations for the gates 108, as discussed below. The hardmask 118 may be non-coplanar with the hardmask 116, as

illustrated in FIG. 36, and may extend "over" at least a portion of the hardmask 116 (and thus over the gate metal 110 of the gates 106).

[0082] FIG. 38 illustrates an assembly 246 subsequent to etching the assembly 244 (FIG. 37) to remove the portions 150 that are not protected by the patterned hardmask 118 to form the gates 108. The gate metal 112 of the gates 106 may extend "over" the hardmask 116 of the gates 108, and may be electrically insulated from the gate metal 110 by the hardmask 116. In the embodiment illustrated in FIG. 38, the z-height of the gate metal 112 of the gates 108 may be greater than the sum of the z-height of the gate metal 110 and the z-height of the hardmask 116 of the gates 106. Additionally, the gate metal 112 of the gates 108 may extend beyond the spacers 134 in the x-direction, as shown. Further manufacturing operations may be performed on the assembly 246, as discussed above with reference to FIGS. 21-25.

[0083] As noted above, a single fin 104 may include multiple groups of gates 106/108, spaced apart along the fin by a doped region 140. FIG. 39 is a cross-sectional view of an example of such a quantum dot device 100 having multiple groups of gates 180 on a single fin 104, in accordance with various embodiments. Each of the groups 180 may include gates 106/108 (not labeled in FIG. 39 for ease of illustration) that may take the form of any of the embodiments of the gates 106/108 discussed herein. A doped region 140 (and its interface material 141) may be disposed between two adjacent groups 180 (labeled in FIG. 39 as groups 180-1 and 180-2), and may provide a common reservoir for both groups 180. In some embodiments, this "common" doped region 140 may be electrically contacted by a single conductive via 136. The particular number of gates 106/108 illustrated in FIG. 39, and the particular number of groups 180, is simply illustrative, and a fin 104 may include any suitable number of gates 106/108 arranged in any suitable number of groups 180.

[0084] As discussed above with reference to FIGS. 1-3, in some embodiments in which the gate dielectric 114 is not a layer shared commonly between the gates 108 and 106, but instead is separately deposited on the fin 104 between the spacers 134, the gate dielectric 114 may extend at least partially up the sides of the spacers 134, and the gate metal 112 may extend between the portions of gate dielectric 114 on the spacers 134. FIGS. 40-44 illustrate various alternative stages in the manufacture of such an embodiment of a quantum dot device 100, in accordance with various embodiments. In particular, the operations illustrated in FIGS. 40-44 may take the place of the operations illustrated in FIGS. 13-15.

[0085] FIG. 40 is a cross-sectional view of an assembly 248 subsequent to etching the assembly 212 (FIG. 12) to remove the gate metal 110, and the gate dielectric 114 that is not protected by the patterned hardmask 116, to form the gates 106.

[0086] FIG. 41 is a cross-sectional view of an assembly 250 subsequent to providing spacer material 132 on the assembly 248 (FIG. 40). The deposition of the spacer material 132 may take any of the forms discussed above with reference to FIG. 14, for example.

[0087] FIG. 42 is a cross-sectional view of an assembly 252 subsequent to etching the spacer material 132 of the assembly 250 (FIG. 41), leaving spacers 134 formed of the spacer material 132 on the sides of the gates 106 (e.g., on the sides of the hardmask 116, the gate metal 110, and the gate dielectric 114). The etching of the spacer material 132 may take any of the forms discussed above with reference to FIG. 15, for example.

[0088] FIG. 43 is a cross-sectional view of an assembly 254 subsequent to providing a gate dielectric 114 on the fin 104 between the gates 106 of the assembly 252 (FIG. 42). In some embodiments, the gate dielectric 114 provided between the gates 106 of the assembly 252 may be formed by atomic layer deposition (ALD) and, as illustrated in FIG. 43, may cover the exposed fin 104 between the gates 106, and may extend onto the adjacent spacers 134.

[0089] FIG. 44 is a cross-sectional view of an assembly 256 subsequent to providing the gate metal 112 on the assembly 254 (FIG. 43). The gate metal 112 may fill the areas between adjacent ones of the gates 106, and may extend over the tops of the gates 106, as shown. The provision of the gate metal 112 may take any of the forms discussed above with reference to FIG. 16, for example. The assembly 256 may be further processed as discussed above with reference to FIGS. 17-25.

[0090] As discussed above with reference to FIG. 19, in some embodiments, the pattern applied to the hardmask 118 (used for patterning the gates 108) may not result in a common, continuous portion of hardmask 118 that extends over all of the hardmask 116. One such example was discussed above with reference to FIGS. 36-38, and another example of such an embodiment is illustrated in FIG. 45. In particular, FIG. 45 is a cross-sectional view of an assembly 258 in which the hardmask 118 of the assembly 224 (FIG. 18) is not patterned to extend over the gates 106, but instead is patterned so as not to extend over the gate metal 110. The assembly 258 may be further processed as discussed above with reference to FIGS. 20-25 (e.g., etching away the excess portions 150, etc.). In some embodiments, the hardmasks 116 and 118 may remain in the quantum dot device 100 as part of the gates 106/108, while in other embodiments, the hardmasks 116 and 118 may be removed.

[0091] As discussed above with reference to FIGS. 2 and 21, the outer spacers 134 on the outer gates 106 may provide a doping boundary, limiting diffusion of the dopant from the doped regions 140 into the area under the gates 106/108. In some embodiments, the doped regions 140 may extend past the outer spacers 134 and under the outer gates 106. For example, as illustrated in FIG. 46, the doped region 140 may extend past the outer spacers 134 and under the outer gates 106 by a

distance 182 between 0 and 10 nanometers. In some embodiments, the doped regions 140 may not extend past the outer spacers 134 toward the outer gates 106, but may instead "terminate" under the outer spacers 134. For example, as illustrated in FIG. 47, the doped regions 140 may be spaced away from the interface between the outer spacers 134 and the outer gates 106 by a distance 184 between 0 and 10 nanometers. The interface material 141 is omitted from FIGS. 46 and 47 for ease of illustration.

[0092] In some embodiments, the quantum dot device 100 may be included in a die and coupled to a package substrate to form a quantum dot device package. For example, FIG. 48 illustrates a quantum dot device package 300 in which a quantum dot device 100 is included in a die 302, and the die 302 is coupled to a package substrate 304. The particular quantum dot device 100 illustrated in FIG. 48 may take the form of the quantum dot device 100 illustrated in FIG. 2, but any of the quantum dot devices 100 disclosed herein may be included in a die (e.g., the die 302), and coupled to a package substrate (e.g., the package substrate 304). In particular, any number of fins 104, gates 106/108, doped regions 140, and other components discussed herein with reference to the quantum dot device 100 may be included in the die 302.

[0093] The die 302 may include a first face 320 and an opposing second face 322. The base 102 and the fin 104 may be proximate to the second face 322, and conductive pathways 315 from the doped regions 140, and the gates 106/108, may extend from these elements to conductive contacts 165 disposed at the first face 320. The conductive pathways 315 may include conductive vias (e.g., the conductive vias 120/122/136), conductive lines, and/or any combination of conductive vias and lines. For example, FIG. 48 illustrates an embodiment in which the conductive pathways 315 (extending between the doped regions 140 and associated conductive contacts 165) include the conductive vias 136, conductive lines 193, conductive vias 198, and conductive lines 196. More or fewer structures may be included in the conductive pathways 315, and analogous conductive pathways 315 may be provided between ones of the conductive contacts 165 and the gates 106/108. In some embodiments, conductive lines of the die 302 (and the package substrate 304, discussed below) may extend into and out of the plane of the drawing, providing conductive pathways to route electrical signals to and/or from various elements in the die 302.

[0094] The conductive vias and/or lines that provide the conductive pathways in the die 302 may be formed using any suitable techniques. Examples of such techniques may include subtractive fabrication techniques, additive or semi-additive fabrication techniques, single Damascene fabrication techniques, dual Damascene fabrication techniques, or any other suitable technique. In some embodiments, layers of oxide material 190 and layers of nitride material 191 may insulate various structures in the conductive pathways 315 from proximate structures, and/or may serve as

etch stops during fabrication. In some embodiments, an adhesion layer 188 may be disposed between conductive material and proximate insulating material of the die 302 to improve mechanical adhesion between the conductive material and the insulating material; for example, FIG. 48 illustrates an adhesion layer 188 between the conductive material in the conductive vias 136 and the proximate insulating material 130.

[0095] The conductive vias 120/122/136 may be referred to as part of the "device layer" of the quantum dot device 100, which may also include the gates 106/108 and the doped regions 140. The conductive lines 193 may be referred to as a Metal 1 or "M1" interconnect layer, and may couple the conductive vias 120/122/136 to other interconnect structures. The conductive vias 198 and the conductive lines 196 may be referred to as a Metal 2 or "M2" interconnect layer, and may be formed directly on the M1 interconnect layer. Although the different conductive vias and lines in FIG. 48 (and other figures herein) are not delineated with lines (and are instead illustrated as a continuous structure), conductive vias and lines that are in conductive contact may or may not be structurally and/or materially contiguous. The same is true for conductive vias/lines and conductive contacts that are in conductive contact.

[0096] A solder resist material 167 (e.g., a polyimide or similar material) may be disposed around the conductive contacts 165, and in some embodiments, may extend onto the conductive contacts 165. The solder resist material 167 may be a polyimide or similar material, or may be any appropriate type of packaging solder resist material. In some embodiments, the solder resist material 167 may be a liquid or dry film material including photoimageable polymers. In some embodiments, the solder resist material 167 may be non-photoimageable (and openings therein, such as those discussed below, may be formed using laser drilling or masked etch techniques). The conductive contacts 165 may provide the contacts to couple other components (e.g., a package substrate 304, as discussed below, or another component) to the conductive pathways 315 in the quantum dot device 100, and may be formed of any suitable conductive material (e.g., a superconducting material). For example, solder bonds may be formed on the one or more conductive contacts 165 to mechanically and/or electrically couple the die 302 with another component (e.g., a circuit board), as discussed below. The conductive contacts 165 illustrated in FIG. 48 take the form of bond pads, but other first level interconnect structures may be used (e.g., posts) to route electrical signals to/from the die 302, as discussed below.

[0097] Having first level interconnects 306 disposed between the first face 320 of the die 302 and the second face 326 of the package substrate 304 (e.g., using solder bumps as part of flip chip packaging techniques) may enable the quantum dot device package 300 to achieve a smaller footprint and higher die-to-package-substrate connection density than could be achieved using

conventional wirebond techniques (in which conductive contacts between the die 302 and the package substrate 304 are constrained to be located on the periphery of the die 302). For example, a die 302 having a square first face 320 with side length N may be able to form $4N$ wirebond interconnects to the package substrate 304, versus N^2 flip chip interconnects (utilizing the entire "full field" surface area of the first face 320). Additionally, in some applications, wirebond interconnects may generate unacceptable amounts of heat that may damage or otherwise interfere with the performance of the quantum dot device 100. Using solder bumps as the first level interconnects 306 may enable the quantum dot device package 300 to have much lower parasitic inductance relative to using wirebonds to couple the die 302 and the package substrate 304, which may result in an improvement in signal integrity for high speed signals communicated between the die 302 and the package substrate 304.

[0098] The package substrate 304 may include a first face 324 and an opposing second face 326. Conductive contacts 199 may be disposed at the first face 324, and conductive contacts 169 may be disposed at the second face 326. Solder resist material 314 may be disposed around the conductive contacts 169, and solder resist material 312 may be disposed around the conductive contacts 199; the solder resist materials 314 and 312 may take any of the forms discussed above with reference to the solder resist material 167. In some embodiments, the solder resist material 312 and/or the solder resist material 314 may be omitted. Conductive pathways 313 may extend through insulating material 310 between the first face 324 and the second face 326 of the package substrate 304, electrically coupling various ones of the conductive contacts 199 to various ones of the conductive contacts 169, in any desired manner. The insulating material 310 may be a dielectric material (e.g., an ILD), and may take the form of any of the embodiments of the insulating material 130 disclosed herein, for example. The conductive pathways 313 may include one or more conductive vias 195, and/or one or more conductive lines 197, for example.

[0099] In some embodiments, the package substrate 304 may be or may otherwise include a silicon interposer, and the conductive pathways 313 may be through-silicon vias. Silicon may have a desirably low coefficient of thermal expansion compared with other dielectric materials that may be used for the insulating material 310, and thus may limit the degree to which the package substrate 304 expands and contracts during temperature changes relative to such other materials (e.g., polymers having higher coefficients of thermal expansion). A silicon interposer may also help the package substrate 304 achieve a desirably small line width and maintain high connection density to the die 302.

[0100] Limiting differential expansion and contraction may help preserve the mechanical and electrical integrity of the quantum dot device package 300 as the quantum dot device package 300 is

fabricated (and exposed to higher temperatures) and used in a cooled environment (and exposed to lower temperatures). In some embodiments, thermal expansion and contraction in the package substrate 304 may be managed by maintaining an approximately uniform density of the conductive material in the package substrate 304 (so that different portions of the package substrate 304 expand and contract uniformly), using reinforced dielectric materials as the insulating material 310 (e.g., dielectric materials with silicon dioxide fillers), or utilizing stiffer materials as the insulating material 310 (e.g., a prepreg material including glass cloth fibers).

[0101] The conductive contacts 165 of the die 302 may be electrically coupled to the conductive contacts 169 of the package substrate 304 via first level interconnects 306. In some embodiments, the first level interconnects 306 may include solder bumps or balls (as illustrated in FIG. 48); for example, the first level interconnects 306 may be flip chip (or controlled collapse chip connection, C4) bumps disposed initially on the die 302 or on the package substrate 304. Second level interconnects 308 (e.g., solder balls or other types of interconnects) may couple the conductive contacts 199 on the first face 324 of the package substrate 304 to another component, such as a circuit board (not shown). Examples of arrangements of electronics packages that may include an embodiment of the quantum dot device package 300 are discussed below with reference to FIG. 69. The die 302 may be brought in contact with the package substrate 304 using a pick-and-place apparatus, for example, and a reflow or thermal compression bonding operation may be used to couple the die 302 to the package substrate 304 via the first level interconnects 306.

[0102] The combination of the conductive pathways and the proximate insulating material (e.g., the insulating material 130, the oxide material 190, and the nitride material 191) in the die 302 may provide an interlayer dielectric (ILD) stack of the die 302. As noted above, interconnect structures may be arranged within the quantum dot device 100 to route electrical signals according to a wide variety of designs (in particular, the arrangement is not limited to the particular configuration of interconnect structures depicted in FIG. 48 or any of the other accompanying figures, and may include more or fewer interconnect structures). During operation of the quantum dot device 100, electrical signals (such as power and/or input/output (I/O) signals) may be routed to and/or from the gates 106/108 and/or the doped regions 140 of the quantum dot device 100 through the interconnects provided by the conductive vias 120/122/136 and additional conductive vias and/or lines, and through the conductive pathways of the package substrate 304.

[0103] Example superconducting materials that may be used for the structures in the conductive pathways 313 (discussed below) and 315, and/or conductive contacts of the die 302 and/or the package substrate 304, may include aluminum, niobium, tin, titanium, osmium, zinc, molybdenum, tantalum, vanadium, or composites of such materials (e.g., niobium-titanium, niobium-aluminum, or

niobium-tin). In some embodiments, the conductive contacts 165, 169, and/or 199 may include aluminum, and the first level interconnects 306 and/or the second level interconnects 308 may include an indium-based solder.

[0104] The conductive contacts 165, 169, and/or 199 may include multiple layers of material that may be selected to serve different purposes. In some embodiments, the conductive contacts 165, 169, and/or 199 may be formed of aluminum, and may include a layer of gold (e.g., with a thickness of less than 1 micron) between the aluminum and the adjacent interconnect to limit the oxidation of the surface of the contacts and improve the adhesion with adjacent solder. In some embodiments, the conductive contacts 165, 169, and/or 199 may be formed of aluminum, and may include a layer of a barrier metal such as nickel, as well as a layer of gold, wherein the layer of barrier metal is disposed between the aluminum and the layer of gold, and the layer of gold is disposed between the barrier metal and the adjacent interconnect. In such embodiments, the gold may protect the barrier metal surface from oxidation before assembly, and the barrier metal may limit the diffusion of solder from the adjacent interconnects into the aluminum.

[0105] In some embodiments, the structures and materials in the quantum dot device 100 may be damaged if the quantum dot device 100 is exposed to the high temperatures that are common in conventional integrated circuit processing (e.g., greater than 100 degrees Celsius, or greater than 200 degrees Celsius). In particular, on embodiments in which the first level interconnects 306 include solder, the solder may be a low-temperature solder (e.g., a solder having a melting point below 100 degrees Celsius) so that it can be melted to couple the conductive contacts 165 and the conductive contacts 169 without having to expose the die 302 to higher temperatures and risk damaging the quantum dot device 100. Examples of solders that may be suitable include indium-based solders (e.g., solders including indium alloys). When low-temperature solders are used, however, these solders may not be fully solid during handling of the quantum dot device package 300 (e.g., at room temperature or temperatures between room temperature and 100 degrees Celsius), and thus the solder of the first level interconnects 306 alone may not reliably mechanically couple the die 302 and the package substrate 304 (and thus may not reliably electrically couple the die 302 and the package substrate 304). In some such embodiments, the quantum dot device package 300 may further include a mechanical stabilizer to maintain mechanical coupling between the die 302 and the package substrate 304, even when solder of the first level interconnects 306 is not solid.

[0106] Any suitable mechanical stabilizer may be used to maintain mechanical coupling between the die 302 and the package substrate 304. For example, FIG. 49 is a detailed view of a portion of the quantum dot device package 300 of FIG. 48, further including an underfill material 316 disposed

between the first face 320 of the die 302 and the second face 326 of the package substrate 304. As shown in FIG. 49, in some embodiments, the underfill material 316 may wet the edge of the die 302 to improve the mechanical contact between the underfill material 316 and the die 302, and to minimize edge cracks. After the underfill material 316 is provisioned between the die 302 and the package substrate 304, it may be cured to allow it to set for a period of time, or by exposing it to heat or another energy source. The underfill material 316 may be, for example, an epoxy-based material.

[0107] FIG. 50 is a detailed view of a portion of the quantum dot device package 300 of FIG. 48, further including a corner glue 318 disposed between corners (and/or edges) of the first face 320 of the die 302 and the second face 326 of the package substrate 304. The corner glue 318 may be, for example, an epoxy-based material, but may be more viscous than an underfill material (e.g., the underfill material 316), and thus may not flow under the bulk of the die 302, but may remain at the corners (and/or edges). As illustrated in FIG. 50, in some embodiments, the outer surface of the corner glue 318 may angle relative to the second face 326 of the package substrate 304.

[0108] FIG. 51 is a view of the quantum dot device package 300 of FIG. 48, further including an overmold material 328 disposed around the die 302 and in contact with the second face 326 of the package substrate 304. In some embodiments, the overmold material 328 may be disposed over the second face 322 of the die 302 (e.g., as shown); in other embodiments, the overmold material 328 may not extend over the second face 322. In some embodiments, the overmold material 328 may fully or partially extend between the die 302 and the package substrate 304 (e.g., as shown); in other embodiments, the overmold material 328 may not extend between the die 302 and the package substrate 304.

[0109] In some embodiments, various combinations of the mechanical stabilizers illustrated in FIGS. 49-51 may be used. For example, an underfill material 316 and an overmold material 328 may both be included in a quantum dot device package 300. In some such embodiments, a common material may provide both the underfill material 316 and the overmold material 328. Other mechanical stabilizers may also be included in a quantum dot device package 300. For example, a metallic or plastic pre-formed cover cap may be disposed on the die 302 and attached to the die 302 and the package substrate 304 with an adhesive.

[0110] A package substrate 304 for a quantum dot device package 300 may be manufactured using any suitable technique. For example, FIGS. 52-61 illustrate various stages in the manufacture of a package substrate for a quantum dot device package, in accordance with various embodiments. FIGS. 52-61 illustrate example operations in a subtractive manufacturing process, while FIGS. 62-67, discussed below, illustrate example operations in a semi-additive manufacturing process.

[0111] FIG. 52 is a cross-sectional view of an assembly 260 including a carrier 330. The carrier 330 may provide mechanical support during manufacture, and may be formed of any suitable material (e.g., a metal sheet, a dielectric material, or a reinforced dielectric material).

[0112] FIG. 53 is a cross-sectional view of an assembly 262 subsequent to providing a conductive material 332 on the carrier 330 of the assembly 260 (FIG. 52). The conductive material 332 may, in some embodiments, be a superconducting material (e.g., any of the superconducting materials discussed herein). The conductive material 332 may be provided on the carrier 330 to any desired thickness using any suitable technique (e.g., sputtering, electroplating, electroless plating, lamination, etc.).

[0113] FIG. 54 is a cross-sectional view of an assembly 264 subsequent to patterning the conductive material 332 of the assembly 262 (FIG. 53) to form the conductive contacts 199. The conductive material 332 may be patterned using any suitable technique. For example, the conductive material 332 may be patterned by providing a mask material (e.g., by lamination, spin coating, or slit coating), patterning the mask material (e.g., by photolithography, laser direct imaging, electron beam lithography, etc.), etching the conductive material 332 in accordance with the patterned mask material (e.g., using wet or dry etching), and removing the remaining mask material).

[0114] FIG. 55 is a cross-sectional view of an assembly 266 subsequent to providing an insulating material 310 on the assembly 264 (FIG. 54). The insulating material 310 may be provided using any suitable technique (e.g., lamination or spin coating), and may cover the conductive contacts 199. The insulating material 310 may be, for example, a dielectric material, as discussed above.

[0115] FIG. 56 is a cross-sectional view of an assembly 268 subsequent to forming cavities 334 in the insulating material 310 of the assembly 266 (FIG. 55). The cavities 334 may extend down to the conductive contacts 199. In some embodiments, the cavities 334 may be tapered so as to be narrower proximate to the conductive contacts 199, as shown. The cavities 334 may be formed using any suitable technique (e.g., laser or mechanical drilling, or using photolithography for photoimageable insulating material 310). In some embodiments, the cavities 334 may be drill holes.

[0116] FIG. 57 is a cross-sectional view of an assembly 270 subsequent to providing a conductive material 336 on the assembly 268 (FIG. 56). The conductive material 336 may be a same conductive material as the conductive material 332, or may be a different conductive material. In some embodiments, the conductive material 336 may be a superconducting material. The conductive material 336 may include portions that fill the cavities 334 to provide the conductive vias 195, and a portion 338 that extends beyond the cavities 334. The conducting material 336 may be provided using any of the techniques discussed above with reference to FIG. 53.

[0117] FIG. 58 is a cross-sectional view of an assembly 272 subsequent to patterning the portion 338 of the conductive material 336 of the assembly 270 (FIG. 57) to form the conductive lines 197. The portion 338 may be patterned using any suitable technique (e.g., any of the techniques discussed above with reference to FIG. 54).

[0118] FIG. 59 is a cross-sectional view of an assembly 274 subsequent to forming conductive contacts 169 and additional conductive vias 195 on the assembly 272 (FIG. 58). The conductive contacts 169 and additional conductive vias 195 may be formed by repeating the operations discussed above with reference to FIGS. 55-58, as appropriate, and may be insulated by additional insulating material 310.

[0119] FIG. 60 is a cross-sectional view of an assembly 276 subsequent to providing and patterning the solder resist material 314 on the face of the assembly 274 (FIG. 59) proximate to the conductive contacts 169. The solder resist material 314 may be provided using any suitable technique (e.g., lamination or spin coating), and may be patterned using any suitable technique (e.g., photolithography). In particular, the patterned solder resist material 314 may include openings 346 that expose the conductive contacts 169.

[0120] FIG. 61 is a cross-sectional view of an assembly 278 subsequent to removing the carrier 330 from the assembly 276 (FIG. 60) and providing and patterning the solder resist material 312 on the face of the assembly 278 proximate to the conductive contacts 199. In particular, the patterned solder resist material 312 may include openings 348 that expose the conductive contacts 199. The solder resist material 312 may be provided and patterned using any of the techniques discussed above with reference to the solder resist material 314 of FIG. 60. The assembly 278 may take the form of the package substrate 304 illustrated in FIG. 48.

[0121] In some embodiments of the manufacturing process illustrated in FIGS. 52-61, an adhesion material may be disposed between the insulating material 310 and adjacent conductive material. For example, a layer of titanium may be provided (e.g., by sputtering) between the insulating material 310 and the conductive material of the conductive pathways 313 (e.g., a superconducting material) to improve the interface between the two. In other embodiments, a layer of sputtered or spray-coated organic adhesion promoter (e.g., a copolyamide-based promoter) may be provided between the insulating material 310 and adjacent conductive material. In some embodiments, the surface of the insulating material 310 may be mechanically or chemically roughened before deposition of conductive material (e.g., a superconducting material) to improve adhesion. In some embodiments, the insulating material 310 (e.g., a dielectric material) may include adhesion promoters, which may be activated at the surface of the insulating material 310 (prior to deposition of the conductive material) using an etching, plasma treatment, or laser process.

[0122] In some embodiments, additive manufacturing operations may be used instead of, or in addition to, the subtractive techniques illustrated in FIGS. 52-61. For example, FIGS. 62-67 illustrate various alternative semi-additive stages in the manufacture of a package substrate for a quantum dot device package, in accordance with various embodiments.

[0123] FIG. 62 is a cross-sectional view of an assembly 280 subsequent to providing a seed layer 340 on the carrier 330 of the assembly 260 (FIG. 52). The seed layer 340 may, in some embodiments, be a superconducting material (e.g., any of the superconducting materials discussed herein), and may serve as a thin seed layer for a subsequent electroplating operation (discussed below with reference to FIG. 63). The seed layer 340 may be provided on the carrier 330 to any desired thickness using any suitable technique (e.g., sputtering). In some embodiments, the seed layer 340 may be formed of tin or aluminum.

[0124] FIG. 63 is a cross-sectional view of an assembly 282 subsequent to providing a patterned mask material 342 on the seed layer 340 of the assembly 280 (FIG. 62). The patterned mask material 342 may be formed by depositing the mask material 342 using any suitable technique, and then patterning the mask material 342 to form cavities 343 that extend down to the seed layer 340 (e.g., using any of the techniques discussed above with reference to FIG. 54).

[0125] FIG. 64 is a cross-sectional view of an assembly 284 subsequent to electroplating conductive material 344 on the assembly 282 (FIG. 63). The seed layer 340 of the assembly 282 (FIG. 63) may serve as the starting point for the electroplating. In some embodiments, the electroplated conductive material 344 may extend over the mask material 342; in such embodiments, this "express" conductive material 344 may be polished back to form the assembly 284. In some embodiments, the conductive material 344 may be tin or aluminum.

[0126] FIG. 65 is a cross-sectional view of an assembly 286 subsequent to removing the mask material 342 from the assembly 284 (FIG. 64). The conductive material 344 may include recessed portions 350 (which may only include the material of the seed layer 340 disposed under the patterned mask material 342) and projecting portions 352 (which may include the seed layer 340 and the additional electroplated conductive material 344 grown in the cavities 343 of the patterned mask material 342).

[0127] FIG. 66 is a cross-sectional view of an assembly 288 subsequent to etching the conductive material 344 of the assembly 286 (FIG. 65) to remove a desired thickness of the conductive material 344. In particular, the conductive material 344 may be etched until the recessed portions 350 are removed, and the thickness of the projecting portions 352 have been reduced by a corresponding amount. The remaining conductive material 344 may provide the conductive contacts 199.

[0128] FIG. 67 is a cross-sectional view of an assembly 290 subsequent to providing and patterning an insulating material 310 on the assembly 288 (FIG. 66). The insulating material 310 may be provided using any of the techniques discussed above with reference to FIG. 55, for example, and may be patterned with cavities 334 in accordance with any of the techniques discussed above with reference to FIG. 56. As discussed above with reference to FIG. 56, the cavities 334 may extend down to the conductive contacts 199 (and may be used to form the conductive vias 195). The conductive vias 195, and additional vias, lines, and contacts, may be built up on the assembly 290 to form the package substrate 304 by repeating the operations of FIGS. 62-67. In some embodiments, adjacent vias and lines may be formed separately (e.g., in a Damascene process) or at the same time (e.g., in a dual Damascene process).

[0129] The subtractive techniques discussed with reference to FIGS. 52-61 may be advantageously used when the materials or structures of the package substrate 304 (and the first level interconnects 306 and the die 302) may be damaged by exposure to the high temperatures typically used in semi-additive processes like those discussed with reference to FIGS. 62-67. For example, certain sputtering processes may operate at relatively high temperatures, as do certain electroplating and etching baths (although some may be operated at lower temperature at the expense of throughput). Additionally, if a desired conductive material (e.g., a superconducting material) is relatively "easy" to etch, but difficult to electroplate, subtractive techniques may be advantageous. However, semi-additive techniques may enable smaller feature sizes in the package substrate 304, so the appropriate manufacturing techniques may be application dependent.

[0130] In some embodiments, some or all of the operations discussed above for manufacturing a package substrate 304 may be performed on both "sides" of the package substrate 304 (e.g., forming the first surface 324 and the second surface 326) substantially simultaneously. Such an approach may be used with coreless package substrates 304, for example, and may achieve higher throughput (and thus reduce manufacturing cost). Examples of operations that may be performed on both sides of a package substrate 304 simultaneously may include wet etching, photoresist development, and electroplating, among others.

[0131] In some embodiments, the quantum dot device package 300 may be a cored package, one in which the package substrate 304 is built on a carrier material (not shown) that remains in the package substrate 304. In such embodiments, the carrier material may be a dielectric material that is part of the insulating material 310; laser vias or other through-holes may be made through the carrier material to allow conductive pathways 313 to extend between the first surface 324 and the second surface 326.

[0132] FIGS. 68A-B are top views of a wafer 6800 and dies 6802 that may be formed from the wafer 6800; the dies 6801 may be included in any of the quantum dot device packages (e.g., the quantum dot device package 300) disclosed herein. The wafer 6800 may include semiconductor material and may include one or more dies 6802 having conventional and quantum dot device elements formed on a surface of the wafer 6800. Each of the dies 6802 may be a repeating unit of a semiconductor product that includes any suitable conventional and/or quantum dot device. After the fabrication of the semiconductor product is complete, the wafer 6800 may undergo a singulation process in which each of the dies 6802 is separated from one another to provide discrete "chips" of the semiconductor product. A die 6802 may include one or more quantum dot devices 100 and/or supporting circuitry to route electrical signals to the quantum dot devices 100 (e.g., interconnects including the conductive vias 120/122/136 and other conductive vias and lines), as well as any other IC components. In some embodiments, the wafer 6800 or the die 6802 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 6802. For example, a memory array formed by multiple memory devices may be formed on a same die 6802 as a processing device (e.g., the processing device 2002 of FIG. 73) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0133] FIG. 69 is a cross-sectional side view of a device assembly 6900 that may include any of the embodiments of the quantum dot device packages 300 disclosed herein. The device assembly 6900 includes a number of components disposed on a circuit board 6902. The device assembly 6900 may include components disposed on a first face 6940 of the circuit board 6902 and an opposing second face 6942 of the circuit board 6902; generally, components may be disposed on one or both faces 6940 and 6942.

[0134] In some embodiments, the circuit board 6902 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 6902. In other embodiments, the circuit board 6902 may be a package substrate or flexible board.

[0135] The IC device assembly 6900 illustrated in FIG. 69 includes a package-on-interposer structure 6936 coupled to the first face 6940 of the circuit board 6902 by coupling components 6916. The coupling components 6916 may electrically and mechanically couple the package-on-interposer structure 6936 to the circuit board 6902, and may include solder balls (as shown in FIG. 69), male

and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0136] The package-on-interposer structure 6936 may include a package 6920 coupled to an interposer 6904 by coupling components 6918. The coupling components 6918 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 6916. For example, the coupling components 6918 may be the second level interconnects 308. Although a single package 6920 is shown in FIG. 69, multiple packages may be coupled to the interposer 6904; indeed, additional interposers may be coupled to the interposer 6904. The interposer 6904 may provide an intervening substrate used to bridge the circuit board 6902 and the package 6920. The package 6920 may be a quantum dot device package 300 or may be a conventional IC package, for example. In some embodiments, the package 6920 may take the form of any of the embodiments of the quantum dot device package 300 disclosed herein, and may include a quantum dot device die 302 coupled to a package substrate 304 (e.g., by flip chip connections). Generally, the interposer 6904 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 6904 may couple the package 6920 (e.g., a die) to a ball grid array (BGA) of the coupling components 6916 for coupling to the circuit board 6902. In the embodiment illustrated in FIG. 69, the package 6920 and the circuit board 6902 are attached to opposing sides of the interposer 6904; in other embodiments, the package 6920 and the circuit board 6902 may be attached to a same side of the interposer 6904. In some embodiments, three or more components may be interconnected by way of the interposer 6904.

[0137] The interposer 6904 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some embodiments, the interposer 6904 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 6904 may include metal interconnects 6908 and vias 6910, including but not limited to through-silicon vias (TSVs) 6906. The interposer 6904 may further include embedded devices 6914, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 6904. The package-on-interposer structure 6936 may take the form of any of the package-on-interposer structures known in the art.

[0138] The device assembly 6900 may include a package 6924 coupled to the first face 6940 of the circuit board 6902 by coupling components 6922. The coupling components 6922 may take the form of any of the embodiments discussed above with reference to the coupling components 6916, and the package 6924 may take the form of any of the embodiments discussed above with reference to the package 6920. The package 6924 may be a quantum dot device package 300 or may be a conventional IC package, for example. In some embodiments, the package 6924 may take the form of any of the embodiments of the quantum dot device package 300 disclosed herein, and may include a quantum dot device die 302 coupled to a package substrate 304 (e.g., by flip chip connections).

[0139] The device assembly 6900 illustrated in FIG. 69 includes a package-on-package structure 6934 coupled to the second face 6942 of the circuit board 6902 by coupling components 6928. The package-on-package structure 6934 may include a package 6926 and a package 6932 coupled together by coupling components 6930 such that the package 6926 is disposed between the circuit board 6902 and the package 6932. The coupling components 6928 and 6930 may take the form of any of the embodiments of the coupling components 6916 discussed above, and the packages 6926 and 6932 may take the form of any of the embodiments of the package 6920 discussed above. Each of the packages 6926 and 6932 may be a quantum dot device package 300 or may be a conventional IC package, for example. In some embodiments, one or both of the packages 6926 and 6932 may take the form of any of the embodiments of the quantum dot device package 300 disclosed herein, and may include a quantum dot device die 302 coupled to a package substrate 304 (e.g., by flip chip connections).

[0140] As noted above, any suitable techniques may be used to manufacture the quantum dot devices 100 and the quantum dot device packages 300 disclosed herein. FIG. 70 is a flow diagram of an illustrative method 1000 of manufacturing a quantum dot device package, in accordance with various embodiments. Although the operations discussed below with reference to the method 1000 are illustrated in a particular order and depicted once each, these operations may be repeated or performed in a different order (e.g., in parallel), as suitable. Additionally, various operations may be omitted, as suitable. Various operations of the method 1000 may be illustrated with reference to one or more of the embodiments discussed above, but the method 1000 may be used to manufacture any suitable quantum dot device package (including any suitable ones of the embodiments disclosed herein).

[0141] At 1002, conductive contacts on a die may be coupled to conductive contacts on a package substrate through first level interconnects disposed between the die and the package substrate. The die may include a quantum well stack, multiple gates disposed above the quantum well stack, and

conductive pathways within the die to electrically couple the gates with the conductive contacts on the die. For example, a die 302 may include a quantum well stack 146, multiple gates 106/108, and conductive pathways (including, e.g., the conductive vias 120/122) electrically coupling the gates 106/108 with the conductive contacts 185 on the die 302 (e.g., as discussed above with reference to FIG. 48).

[0142] At 1004, a mechanical stabilizer may be provided to the die and package substrate. For example, an underfill material 316, a corner glue 318, and/or an overmold material 328 may be provided to the assembly of the die 302 and the package substrate 304 (e.g., as discussed above with reference to FIGS. 48-51).

[0143] A number of techniques are disclosed herein for operating a quantum dot device 100 in a quantum dot device package 300. FIGS. 71-72 are flow diagrams of particular illustrative methods 1020 and 1040, respectively, of operating a quantum dot device in a quantum dot device package, in accordance with various embodiments. Although the operations discussed below with reference to the methods 1020 and 1040 are illustrated in a particular order and depicted once each, these operations may be repeated or performed in a different order (e.g., in parallel), as suitable. Additionally, various operations may be omitted, as suitable. Various operations of the methods 1020 and 1040 may be illustrated with reference to one or more of the embodiments discussed above, but the methods 1020 and 1040 may be used to operate any suitable quantum dot device (including any suitable ones of the embodiments disclosed herein).

[0144] Turning to the method 1020 of FIG. 71, at 1022, electrical signals may be provided to one or more gates on a first quantum well stack region to cause a first quantum dot to form in the first quantum well stack region. The electrical signals may be provided to the one or more gates on the first quantum well stack region by providing electrical signals to conductive contacts on a package substrate to which the die is coupled by any of the first level interconnects disclosed herein (e.g., flip chip interconnects). For example, one or more voltages may be applied to the gates 106/108 on a fin 104-1 of a quantum dot device 100 coupled to a package substrate 304 via first level interconnects 306 to cause at least one quantum dot 142 to form in the fin 104-1.

[0145] At 1024, electrical signals may be provided to one or more gates on a second quantum well stack region to cause a second quantum dot to form in the second quantum well stack region. For example, one or more voltages may be applied to the gates 106/108 on a fin 104-2 to cause at least one quantum dot 142 to form in the fin 104-2.

[0146] At 1026, a quantum state of the first quantum dot may be sensed with the second quantum dot. For example, a quantum dot 142 in the fin 104-2 (the "read" fin) may sense the quantum state of a quantum dot 142 in the fin 104-1 (the "active" fin).

[0147] Turning to the method 1040 of FIG. 72, at 1042, an electrical signal may be applied to a first gate disposed above a quantum well stack region to cause a first quantum dot to form in a first quantum well in the quantum well stack region under the first gate. A conductive pathway to the first gate may extend through a first level interconnect disposed between the quantum well stack region and a package substrate. For example, a voltage may be applied to the gate 108-1 disposed on a fin 104 in a quantum dot device 100 to cause a first quantum dot 142 to form in the quantum well layer 152 in the fin 104 under the gate 108-1. The voltage may be applied to the gate 108-1 through a conductive pathway 313 in the package substrate 304, a first level interconnect 306, and a conductive pathway 315 in the quantum dot device 100.

[0148] At 1044, an electrical signal may be applied to a second gate disposed above the quantum well stack region to cause a second quantum dot to form in a second quantum well in the quantum well stack region under the second gate. A conductive pathway to the second gate may extend through a first level interconnect disposed between the quantum well stack region and the package substrate. For example, a voltage may be applied to the gate 108-2 disposed on the fin 104 to cause a second quantum dot 142 to form in the quantum well layer 152 in the fin 104 under the gate 108-2. The voltage may be applied to the gate 108-2 through a conductive pathway 313 in the package substrate 304, a first level interconnect 306, and a conductive pathway 315 in the quantum dot device 100.

[0149] At 1046, an electrical signal may be applied to a third gate disposed above the quantum well stack region to (1) cause a third quantum dot to form in a third quantum well in the quantum well stack region under the third gate or (2) provide a potential barrier between the first quantum well and the second quantum well. A conductive pathway to the third gate may extend through a first level interconnect disposed between the quantum well stack region and the package substrate. For example, a voltage may be applied to the gate 106-2 to (1) cause a third quantum dot 142 to form in the quantum well layer 152 in the fin 104 (e.g., when the gate 106-2 acts as a "plunger" gate) or (2) provide a potential barrier between the first quantum well (under the gate 108-1) and the second quantum well (under the gate 108-2) (e.g., when the gate 106-2 acts as a "barrier" gate). The voltage may be applied to the gate 106-2 through a conductive pathway 313 in the package substrate 304, a first level interconnect 306, and a conductive pathway 315 in the quantum dot device 100.

[0150] FIG. 73 is a block diagram of an example quantum computing device 2000 that may include any of the quantum dot devices disclosed herein (e.g., any of the quantum dot device packages disclosed herein). A number of components are illustrated in FIG. 73 as included in the quantum computing device 2000, but any one or more of these components may be omitted or duplicated, as

suitable for the application. In some embodiments, some or all of the components included in the quantum computing device 2000 may be attached to one or more printed circuit boards (e.g., a motherboard), and may be included in a quantum dot device package 300. In some embodiments, various ones of these components may be fabricated onto a single system-on-a-chip (SoC) die. Additionally, in various embodiments, the quantum computing device 2000 may not include one or more of the components illustrated in FIG. 73, but the quantum computing device 2000 may include interface circuitry for coupling to the one or more components. For example, the quantum computing device 2000 may not include a display device 2006, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 2006 may be coupled. In another set of examples, the quantum computing device 2000 may not include an audio input device 2024 or an audio output device 2008, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 2024 or audio output device 2008 may be coupled.

[0151] The quantum computing device 2000 may include a processing device 2002 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 2002 may include a quantum processing device 2026 (e.g., one or more quantum processing devices), and a non-quantum processing device 2028 (e.g., one or more non-quantum processing devices). The quantum processing device 2026 may include one or more of the quantum dot devices 100 disclosed herein, and may perform data processing by performing operations on the quantum dots that may be generated in the quantum dot devices 100, and monitoring the result of those operations. For example, as discussed above, different quantum dots may be allowed to interact, the quantum states of different quantum dots may be set or transformed, and the quantum states of quantum dots may be read (e.g., by another quantum dot). The quantum processing device 2026 may be a universal quantum processor, or specialized quantum processor configured to run one or more particular quantum algorithms. In some embodiments, the quantum processing device 2026 may execute algorithms that are particularly suitable for quantum computers, such as cryptographic algorithms that utilize prime factorization, encryption/decryption, algorithms to optimize chemical reactions, algorithms to model protein folding, etc. The quantum processing device 2026 may also include support circuitry to support the processing capability of the quantum processing device 2026, such as input/output channels, multiplexers, signal mixers, quantum amplifiers, and analog-to-digital converters.

[0152] As noted above, the processing device 2002 may include a non-quantum processing device 2028. In some embodiments, the non-quantum processing device 2028 may provide peripheral logic to support the operation of the quantum processing device 2026. For example, the non-quantum processing device 2028 may control the performance of a read operation, control the performance of a write operation, control the clearing of quantum bits, etc. The non-quantum processing device 2028 may also perform conventional computing functions to supplement the computing functions provided by the quantum processing device 2026. For example, the non-quantum processing device 2028 may interface with one or more of the other components of the quantum computing device 2000 (e.g., the communication chip 2012 discussed below, the display device 2006 discussed below, etc.) in a conventional manner, and may serve as an interface between the quantum processing device 2026 and conventional components. The non-quantum processing device 2028 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices.

[0153] The quantum computing device 2000 may include a memory 2004, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the states of qubits in the quantum processing device 2026 may be read and stored in the memory 2004. In some embodiments, the memory 2004 may include memory that shares a die with the non-quantum processing device 2028. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM).

[0154] The quantum computing device 2000 may include a cooling apparatus 2030. The cooling apparatus 2030 may maintain the quantum processing device 2026 at a predetermined low temperature during operation to reduce the effects of scattering in the quantum processing device 2026. This predetermined low temperature may vary depending on the setting; in some embodiments, the temperature may be 5 degrees Kelvin or less. In some embodiments, the non-quantum processing device 2028 (and various other components of the quantum computing device 2000) may not be cooled by the cooling apparatus 2030, and may instead operate at room temperature. The cooling apparatus 2030 may be, for example, a dilution refrigerator, a helium-3 refrigerator, or a liquid helium refrigerator.

[0155] In some embodiments, the quantum computing device 2000 may include a communication chip 2012 (e.g., one or more communication chips). For example, the communication chip 2012 may

be configured for managing wireless communications for the transfer of data to and from the quantum computing device 2000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0156] The communication chip 2012 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 1402.11 family), IEEE 1402.16 standards (e.g., IEEE 1402.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 1402.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 1402.16 standards. The communication chip 2012 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 2012 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 2012 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 2012 may operate in accordance with other wireless protocols in other embodiments. The quantum computing device 2000 may include an antenna 2022 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0157] In some embodiments, the communication chip 2012 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 2012 may include multiple communication chips. For instance, a first communication chip 2012 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 2012 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 2012 may be dedicated to

wireless communications, and a second communication chip 2012 may be dedicated to wired communications.

[0158] The quantum computing device 2000 may include battery/power circuitry 2014. The battery/power circuitry 2014 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the quantum computing device 2000 to an energy source separate from the quantum computing device 2000 (e.g., AC line power).

[0159] The quantum computing device 2000 may include a display device 2006 (or corresponding interface circuitry, as discussed above). The display device 2006 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0160] The quantum computing device 2000 may include an audio output device 2008 (or corresponding interface circuitry, as discussed above). The audio output device 2008 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0161] The quantum computing device 2000 may include an audio input device 2024 (or corresponding interface circuitry, as discussed above). The audio input device 2024 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0162] The quantum computing device 2000 may include a global positioning system (GPS) device 2018 (or corresponding interface circuitry, as discussed above). The GPS device 2018 may be in communication with a satellite-based system and may receive a location of the quantum computing device 2000, as known in the art.

[0163] The quantum computing device 2000 may include an other output device 2010 (or corresponding interface circuitry, as discussed above). Examples of the other output device 2010 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0164] The quantum computing device 2000 may include an other input device 2020 (or corresponding interface circuitry, as discussed above). Examples of the other input device 2020 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0165] The quantum computing device 2000, or a subset of its components, may have any appropriate form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal

computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device.

[0166] The following paragraphs provide examples of various ones of the embodiments disclosed herein.

[0167] Example 1 is a quantum dot device package, including: a die having a first face and an opposing second face, wherein the die includes a quantum dot device, and the quantum dot device includes a quantum well stack, a plurality of gates disposed above the quantum well stack, and a plurality of conductive pathways coupled between associated ones of the plurality of gates and conductive contacts at a first face of the die; a package substrate having a first face and an opposing second face, wherein conductive contacts are disposed at the second face of the package substrate; and first level interconnects disposed between the first face of the die and the second face of the package substrate, coupling the conductive contacts at the first face of the die with associated conductive contacts at the second face of the package substrate.

[0168] Example 2 may include the subject matter of Example 1, and may further specify that the package substrate includes a silicon interposer.

[0169] Example 3 may include the subject matter of any of Examples 1-2, and may further specify that the plurality of conductive pathways are first conductive pathways, the conductive contacts disposed at the second face of the package substrate are second conductive contacts, and the package substrate further includes first conductive contacts disposed at the first face of the package substrate and second conductive pathways between the first conductive contacts and associated second conductive contacts.

[0170] Example 4 may include the subject matter of Example 3, and may further specify that the second conductive pathways include a superconducting material.

[0171] Example 5 may include the subject matter of Example 4, and may further specify that the second conductive pathways include aluminum or tin.

[0172] Example 6 may include the subject matter of any of Examples 4-5, and may further specify that the package substrate includes a dielectric material and titanium disposed between at least some of the dielectric material and the conductive pathways.

[0173] Example 7 may include the subject matter of any of Examples 1-6, and may further specify that the first level interconnects include a solder, and the solder includes indium.

[0174] Example 8 may include the subject matter of any of Examples 1-7, and may further specify that the first level interconnects include a solder, and the solder includes bismuth or gallium.

[0175] Example 9 may include the subject matter of any of Examples 1-8, and may further specify that the first level interconnects include a solder having a melting point that is less than 100 degrees Celsius.

[0176] Example 10 may include the subject matter of Example 9, and may further include an underfill material disposed between the first face of the die and the second face of the package substrate, wherein the underfill material is disposed around at least some of the first level interconnects.

[0177] Example 11 may include the subject matter of any of Examples 9-10, and may further include an adhesive disposed between the first face of the die and the second face of the package substrate, wherein the first face of the die has corners, and the adhesive is disposed proximate to the corners.

[0178] Example 12 may include the subject matter of any of Examples 1-11, and may further specify that individual conductive contacts disposed at the second face of the package substrate include a layer of gold in contact with an associated individual first level interconnect.

[0179] Example 13 may include the subject matter of Example 12, and may further specify that individual conductive contacts disposed at the second face of the package substrate include a layer of nickel arranged such that the layer of gold is disposed between the layer of nickel and the associated individual first level interconnect.

[0180] Example 14 may include the subject matter of Example 12, and may further specify that the layer of gold is disposed on aluminum such that the layer of gold is disposed between the aluminum and the associated individual first level interconnect.

[0181] Example 15 may include the subject matter of any of Examples 1-14, and may further specify that the quantum well stack is included in a fin that extends away from a base.

[0182] Example 16 may include the subject matter of Example 15, and may further specify that insulating material is disposed on opposing faces of the fin.

[0183] Example 17 may include the subject matter of any of Examples 15-16, and may further specify that the quantum well stack is a first quantum well stack, the fin is a first fin, the plurality of gates is a first plurality of gates, the plurality of conductive pathways is a first plurality of conductive pathways, and the quantum dot device further includes: a second quantum well stack included in a second fin, a second plurality of gates disposed above the second quantum well stack, and a second plurality of conductive pathways coupled between associated ones of the second plurality of gates and conductive contacts at a first face of the die.

[0184] Example 18 may include the subject matter of Example 17, and may further specify that the first and second fins are spaced apart by an insulating material.

[0185] Example 19 may include the subject matter of any of Examples 1-18, and may further specify that the quantum well stack is a first quantum well stack region, the plurality of gates is a first plurality of gates, the plurality of conductive pathways is a first plurality of interconnects, and the quantum dot device further includes: a second quantum well stack region, a second plurality of gates disposed above the second quantum well stack region, and a second plurality of conductive pathways coupled between associated ones of the second plurality of gates and conductive contacts at the first face of the die.

[0186] Example 20 may include the subject matter of Example 19, and may further specify that the first quantum well stack region includes an active quantum dot region and the second quantum well stack region includes a read quantum dot region.

[0187] Example 21 is a method of operating a quantum dot device, including: providing electrical signals to one or more gates on a first quantum well stack region to cause a first quantum dot to form in the first quantum well stack region, wherein the first quantum well stack region is included in a die, and providing electrical signals to the one or more gates on the first quantum well stack region includes providing electrical signals to conductive contacts on a package substrate to which the die is coupled by flip chip contacts; providing electrical signals to one or more gates on a second quantum well stack region to cause a second quantum dot to form in the second quantum well stack region, wherein the second quantum well stack region is included in the die; and sensing a quantum state of the first quantum dot with the second quantum dot.

[0188] Example 22 may include the subject matter of Example 21, and may further specify that the package substrate is coupled to a circuit board via second level interconnects, and the electrical signals are provided to the package substrate from the circuit board through the second level interconnects.

[0189] Example 23 may include the subject matter of any of Examples 21-22, and may further specify that providing the electrical signals to the one or more gates on the first quantum well stack region comprises applying a voltage to a first gate of the one or more gates to cause the first quantum dot to form in the first quantum well stack region under the first gate.

[0190] Example 24 may include the subject matter of any of Examples 21-23, and may further specify that sensing the quantum state of the first quantum dot with the second quantum dot comprises sensing a spin state of the first quantum dot with the second quantum dot.

[0191] Example 25 may include the subject matter of any of Examples 21-24, and may further include: providing the electrical signals to the one or more gates on the first quantum well stack region to cause a third quantum dot to form in the first quantum well stack region; and prior to

sensing the quantum state of the first quantum dot with the second quantum dot, allowing the first and third quantum dots to interact.

[0192] Example 26 may include the subject matter of Example 25, and may further specify that allowing the first and third quantum dots to interact comprises providing the electrical signals to the one or more gates on the first quantum well stack regions to control interaction between the first and third quantum dots.

[0193] Example 27 may include the subject matter of any of Examples 21-26, and may further specify that the first and second quantum well stack regions are included in different, parallel fins.

[0194] Example 28 is a method of manufacturing a quantum dot device package, including: coupling conductive contacts of a die to conductive contacts on a package substrate through first level interconnects disposed between the die and the package substrate, wherein the die includes a quantum well stack, multiple gates disposed above the quantum well stack, and conductive pathways within the die to electrically couple the gates with the conductive contacts on the die; and providing a mechanical stabilizer to the die and the package substrate.

[0195] Example 29 may include the subject matter of Example 28, and may further specify that providing the mechanical stabilizer includes providing an underfill material between the die and the package substrate.

[0196] Example 30 may include the subject matter of any of Examples 28-29, and may further specify that providing the mechanical stabilizer includes providing a corner glue between the die and the package substrate.

[0197] Example 31 may include the subject matter of any of Examples 28-30, and may further specify that providing the mechanical stabilizer includes providing an overmold material around the die on the package substrate.

[0198] Example 32 may include the subject matter of any of Examples 28-31, and may further include manufacturing the package substrate.

[0199] Example 33 may include the subject matter of Example 32, wherein the package substrate includes conductive pathways in contact with the conductive contacts on the package substrate, and the conductive pathways include a superconducting material.

[0200] Example 34 may include the subject matter of any of Examples 28-33, and may further include manufacturing the die.

[0201] Example 35 may include the subject matter of Example 34, and may further specify that manufacturing the die includes: providing the quantum well stack on a substrate; removing at least some of the quantum well stack to form fins in the quantum well stack; providing an insulating material between the fins; and forming gates on top of the fins.

[0202] Example 36 may include the subject matter of any of Examples 28-35, and may further specify that the first level interconnects include solder having a melting point below 100 degrees Celsius.

[0203] Example 37 is a quantum computing device, including: a quantum processing device, wherein the quantum processing device includes a die coupled to a package substrate by first level interconnects disposed between the die and the package substrate, wherein the die includes an active quantum well stack region with multiple gates disposed thereon and a read quantum well stack region with multiple gates disposed thereon; a non-quantum processing device, coupled to the quantum processing device at least partially via the package substrate, to control electrical signals applied to the gates disposed on the active quantum well stack region; and a memory device to store data generated by the gates disposed on the read quantum well stack region during operation of the quantum processing device.

[0204] Example 38 may include the subject matter of Example 37, and may further include a cooling apparatus to maintain a temperature of the quantum processing device below 5 degrees Kelvin.

[0205] Example 39 may include the subject matter of Example 38, and may further specify that the cooling apparatus includes a dilution refrigerator.

[0206] Example 40 may include the subject matter of Example 38, and may further specify that the cooling apparatus includes a liquid helium refrigerator.

[0207] Example 41 may include the subject matter of any of Examples 37-40, and may further specify that the memory device is to store instructions for a quantum computing algorithm to be executed by the quantum processing device.

[0208] Example 42 may include the subject matter of any of Examples 37-41, and may further specify that the package substrate includes conductive pathways formed of a superconducting material.

[0209] Example 43 may include the subject matter of any of Examples 37-42, and may further specify that the package substrate includes a silicon interposer.

Claims:

1. A quantum dot device package, comprising:
a die having a first face and an opposing second face, wherein the die includes a quantum dot device, and the quantum dot device includes:
 - a quantum well stack,
 - a plurality of gates disposed above the quantum well stack, and
 - a plurality of conductive pathways coupled between associated ones of the plurality of gates and conductive contacts at a first face of the die;a package substrate having a first face and an opposing second face, wherein conductive contacts are disposed at the second face of the package substrate; and
first level interconnects disposed between the first face of the die and the second face of the package substrate, coupling the conductive contacts at the first face of the die with associated conductive contacts at the second face of the package substrate.
2. The quantum dot device package of claim 1, wherein the package substrate includes a silicon interposer.
3. The quantum dot device package of claim 1, wherein the plurality of conductive pathways are first conductive pathways, the conductive contacts disposed at the second face of the package substrate are second conductive contacts, and the package substrate further includes first conductive contacts disposed at the first face of the package substrate and second conductive pathways between the first conductive contacts and associated second conductive contacts.
4. The quantum dot device package of claim 3, wherein the second conductive pathways include a superconducting material.
5. The quantum dot device package of claim 4, wherein the second conductive pathways include aluminum or tin.
6. The quantum dot device package of claim 4, wherein the package substrate includes a dielectric material and titanium disposed between at least some of the dielectric material and the conductive pathways.
7. The quantum dot device package of any of claims 1-6, wherein the first level interconnects include a solder, and the solder includes indium.
8. The quantum dot device package of any of claims 1-6, wherein the first level interconnects include a solder, and the solder includes bismuth or gallium.
9. The quantum dot device package of any of claims 1-6, wherein the first level interconnects include a solder having a melting point that is less than 100 degrees Celsius.

10. The quantum dot device package of any of claims 1-6, wherein the quantum well stack is included in a fin that extends away from a base.

11. The quantum dot device package of claim 10, wherein the quantum well stack is a first quantum well stack, the fin is a first fin, the plurality of gates is a first plurality of gates, the plurality of conductive pathways is a first plurality of conductive pathways, and the quantum dot device further comprises:

a second quantum well stack included in a second fin,

a second plurality of gates disposed above the second quantum well stack, and

a second plurality of conductive pathways coupled between associated ones of the second plurality of gates and conductive contacts at a first face of the die.

12. The quantum dot device package of claim 11, wherein the first and second fins are spaced apart by an insulating material.

13. The quantum dot device package of any of claims 1-6, wherein the quantum well stack is a first quantum well stack region, the plurality of gates is a first plurality of gates, the plurality of conductive pathways is a first plurality of interconnects, and the quantum dot device further comprises:

a second quantum well stack region,

a second plurality of gates disposed above the second quantum well stack region, and

a second plurality of conductive pathways coupled between associated ones of the second plurality of gates and conductive contacts at the first face of the die.

14. A method of operating a quantum dot device, comprising:

providing electrical signals to one or more gates on a first quantum well stack region to cause a first quantum dot to form in the first quantum well stack region, wherein the first quantum well stack region is included in a die, and providing electrical signals to the one or more gates on the first quantum well stack region includes providing electrical signals to conductive contacts on a package substrate to which the die is coupled by flip chip contacts;

providing electrical signals to one or more gates on a second quantum well stack region to cause a second quantum dot to form in the second quantum well stack region, wherein the second quantum well stack region is included in the die; and

sensing a quantum state of the first quantum dot with the second quantum dot.

15. The method of claim 14, wherein the package substrate is coupled to a circuit board via second level interconnects, and the electrical signals are provided to the package substrate from the circuit board through the second level interconnects.

16. The method of any of claims 14-15, wherein sensing the quantum state of the first quantum dot with the second quantum dot comprises sensing a spin state of the first quantum dot with the second quantum dot.
17. A method of manufacturing a quantum dot device package, comprising:
coupling conductive contacts of a die to conductive contacts on a package substrate through first level interconnects disposed between the die and the package substrate, wherein the die includes a quantum well stack, multiple gates disposed above the quantum well stack, and conductive pathways within the die to electrically couple the gates with the conductive contacts on the die; and providing a mechanical stabilizer to the die and the package substrate.
18. The method of claim 17, wherein providing the mechanical stabilizer includes providing an underfill material between the die and the package substrate.
19. The method of claim 17, wherein providing the mechanical stabilizer includes providing a corner glue between the die and the package substrate.
20. The method of claim 17, wherein providing the mechanical stabilizer includes providing an overmold material around the die on the package substrate.
21. The method of any of claims 17-20, further comprising:
manufacturing the package substrate.
22. The method of any of claims 17-20, wherein the first level interconnects include solder having a melting point below 100 degrees Celsius.
23. A quantum computing device, comprising:
a quantum processing device, wherein the quantum processing device includes a die coupled to a package substrate by first level interconnects disposed between the die and the package substrate, wherein the die includes an active quantum well stack region with multiple gates disposed thereon and a read quantum well stack region with multiple gates disposed thereon;
a non-quantum processing device, coupled to the quantum processing device at least partially via the package substrate, to control electrical signals applied to the gates disposed on the active quantum well stack region; and
a memory device to store data generated by the gates disposed on the read quantum well stack region during operation of the quantum processing device.
24. The quantum computing device of claim 23, wherein the memory device is to store instructions for a quantum computing algorithm to be executed by the quantum processing device.
25. The quantum computing device of any of claims 23-24, wherein the package substrate includes conductive pathways formed of a superconducting material.

1/25

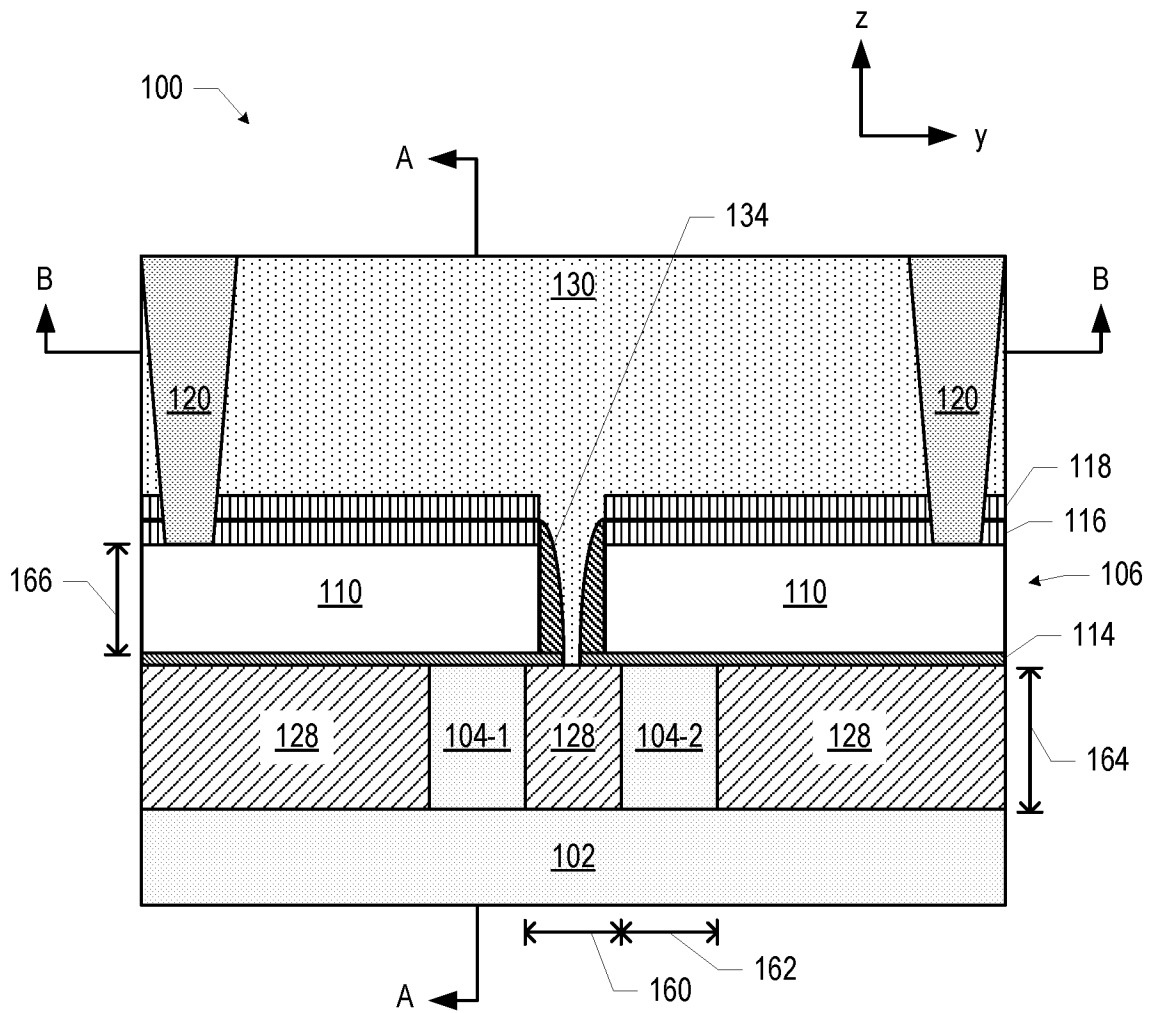


FIG. 1

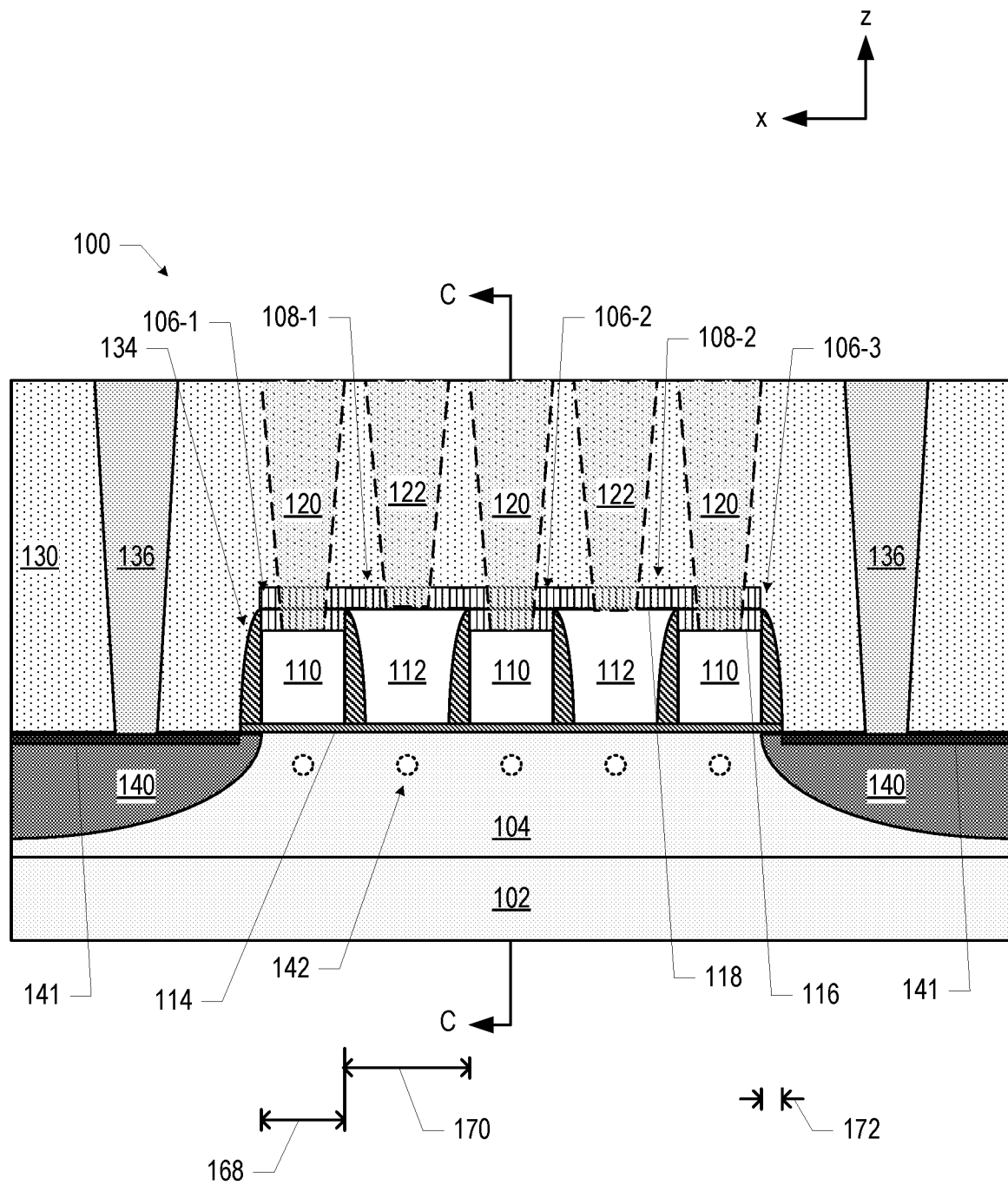


FIG. 2

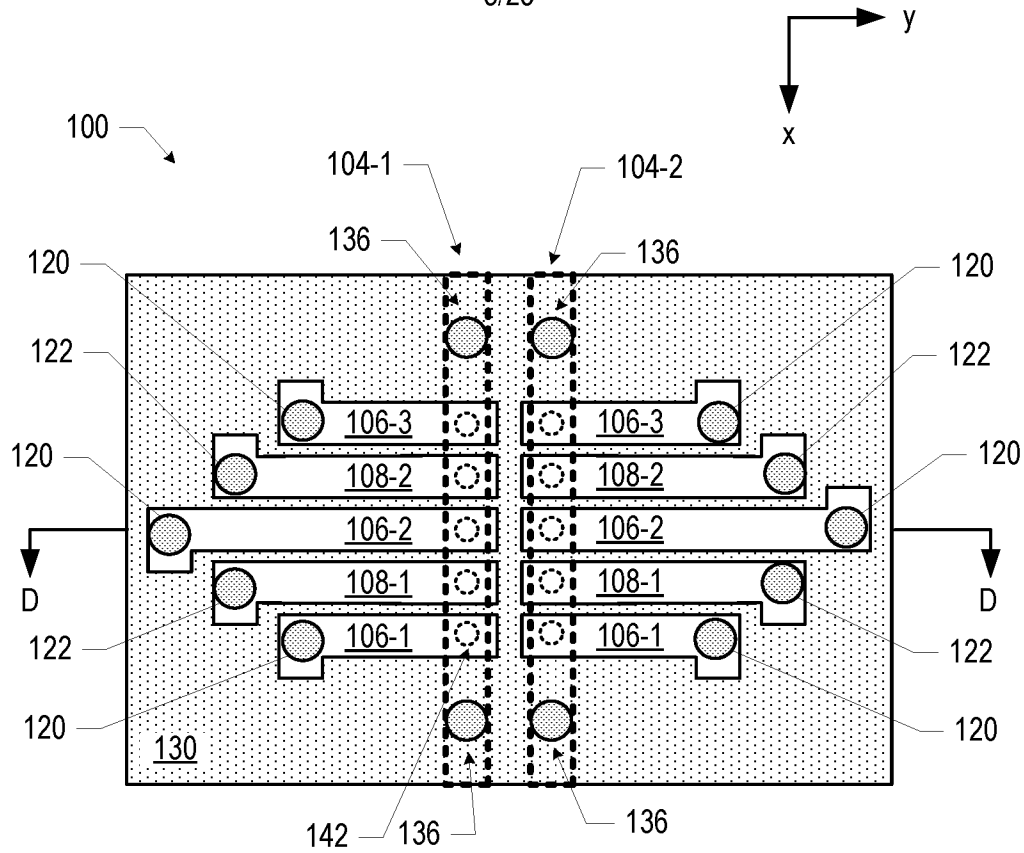


FIG. 3

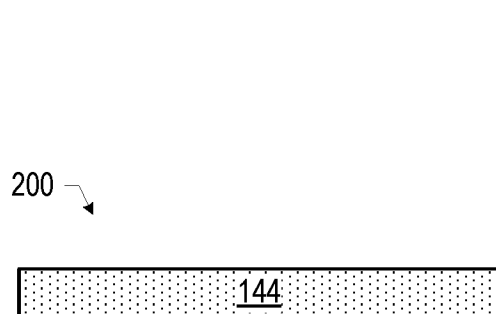


FIG. 4

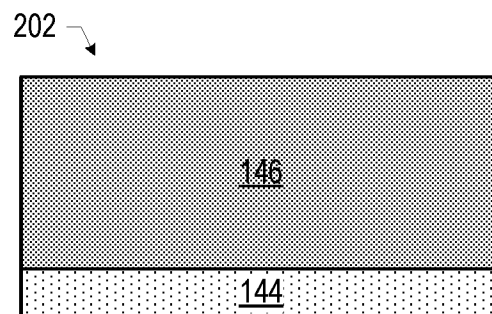


FIG. 5

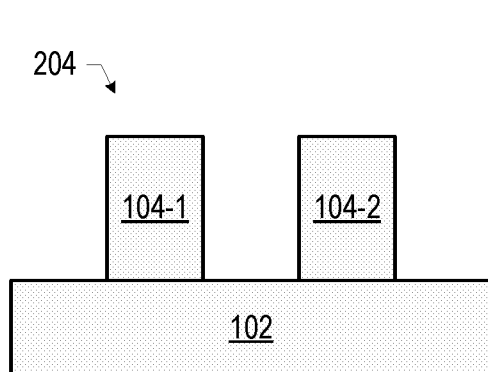


FIG. 6

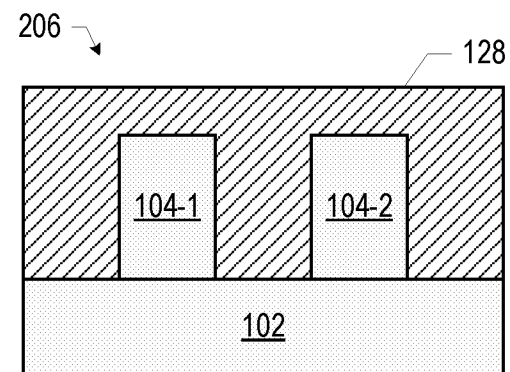


FIG. 7

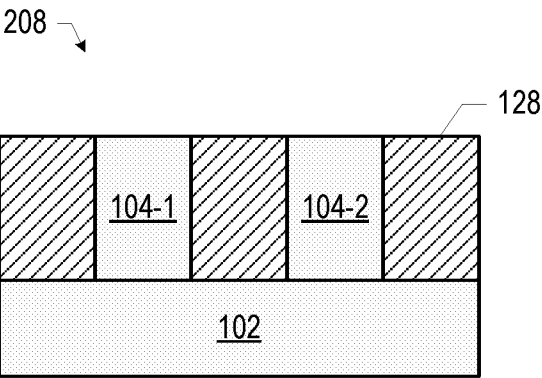


FIG. 8

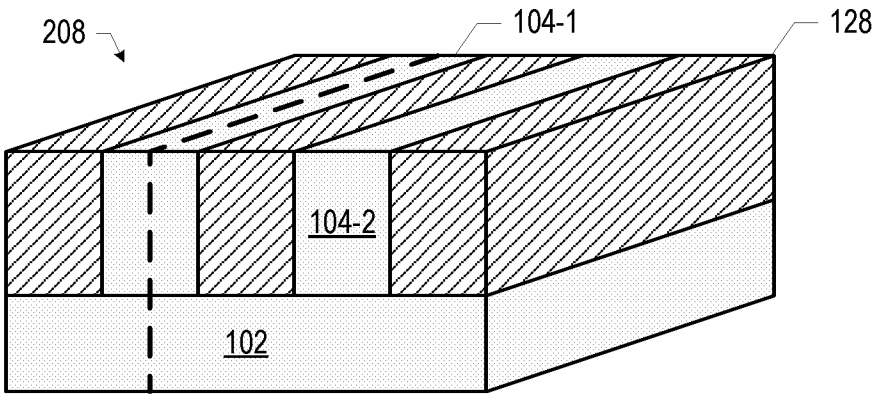


FIG. 9

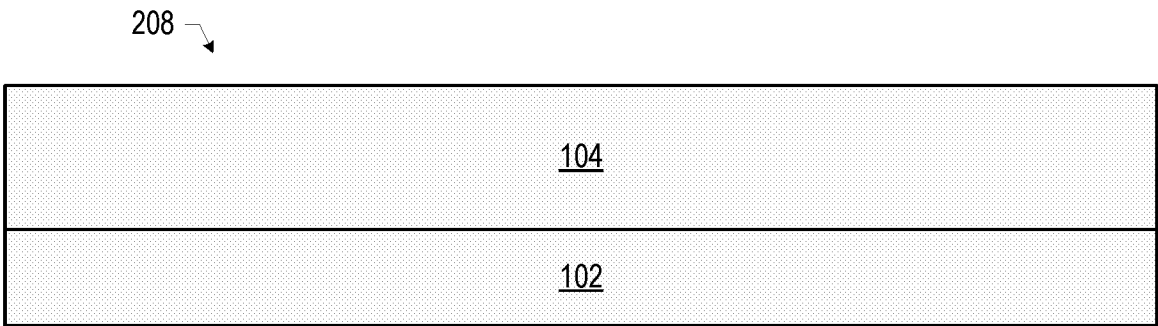


FIG. 10

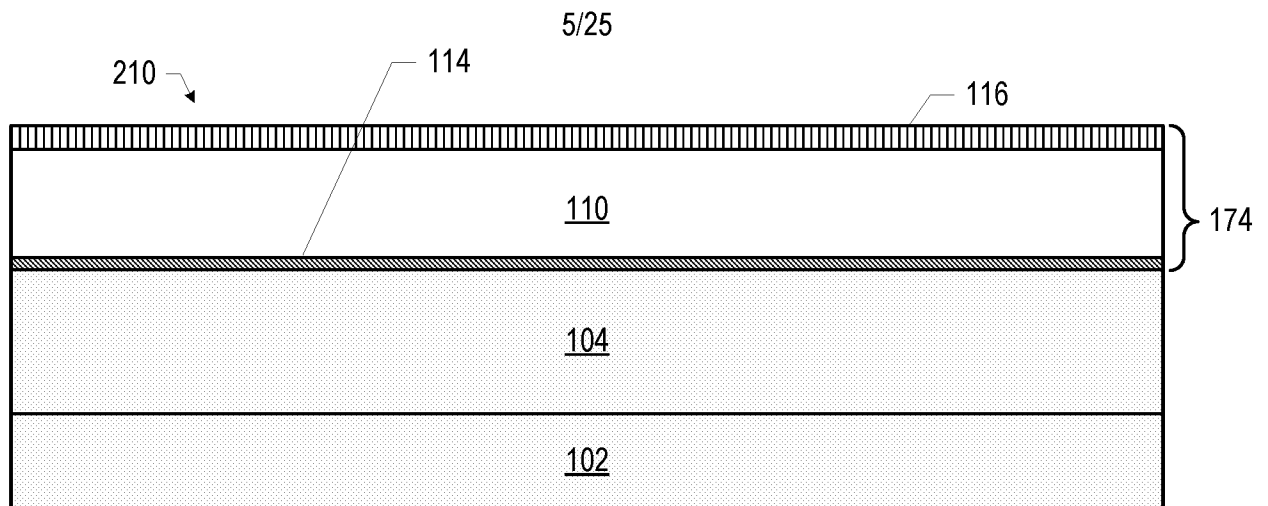


FIG. 11

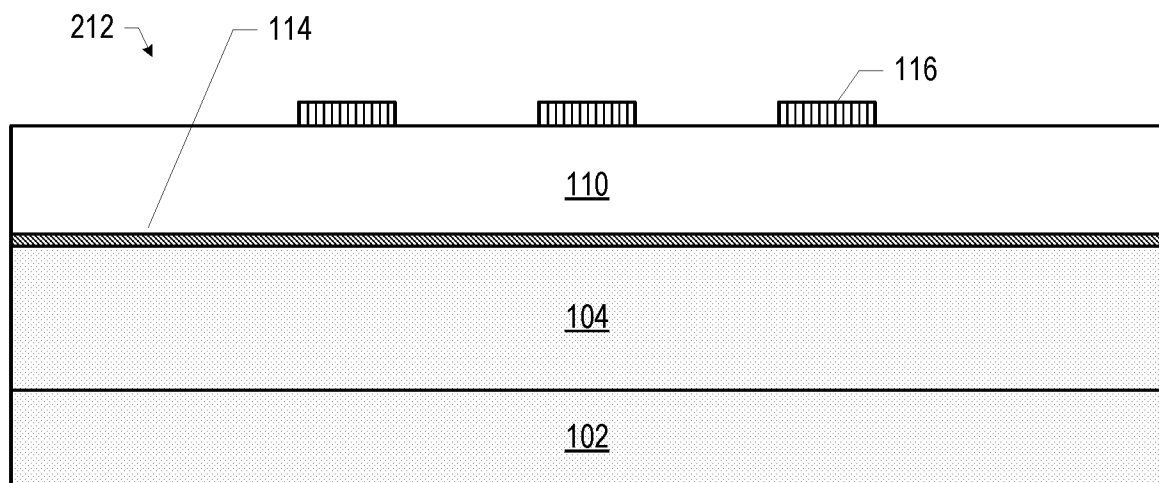


FIG. 12

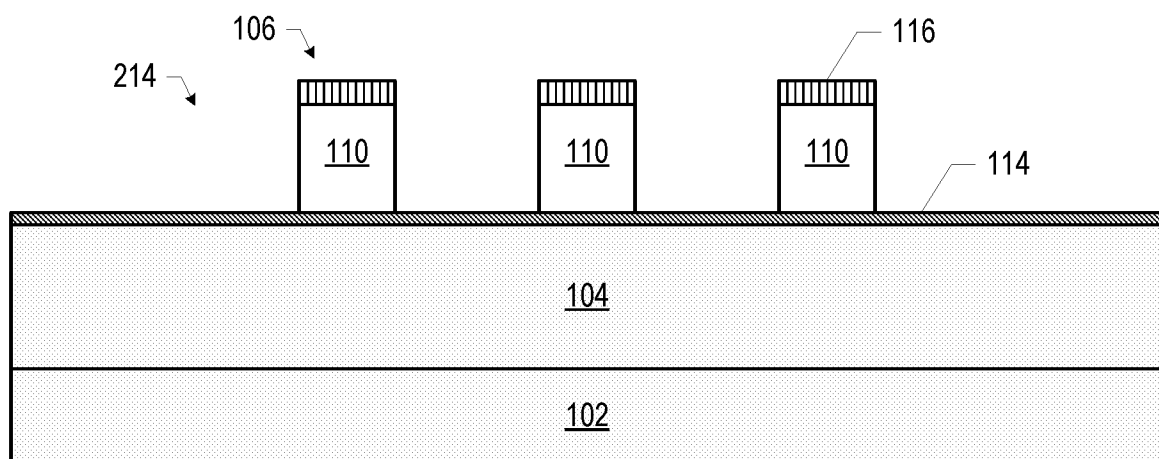


FIG. 13

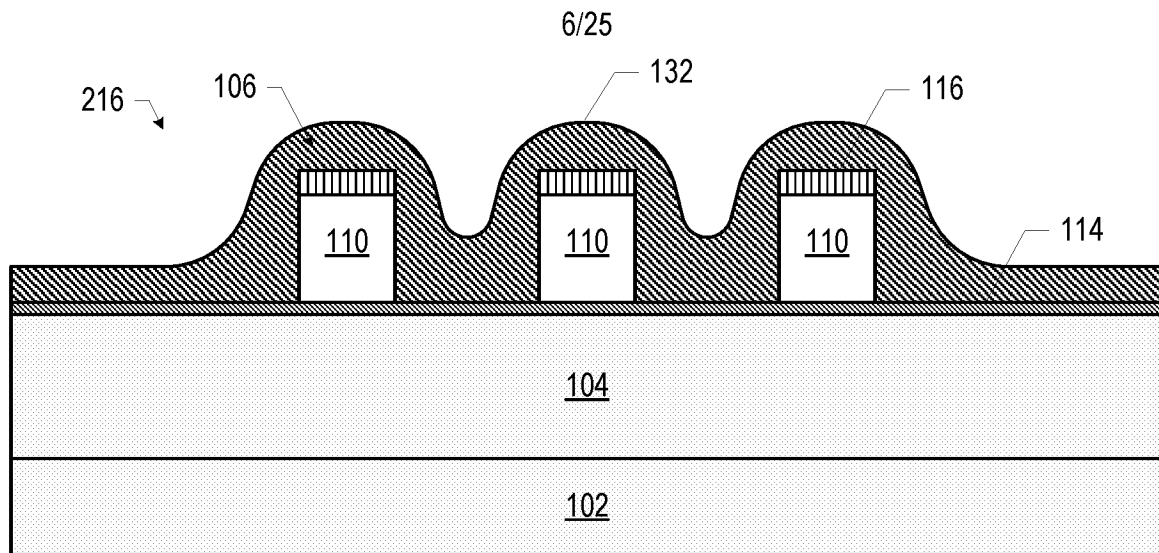


FIG. 14

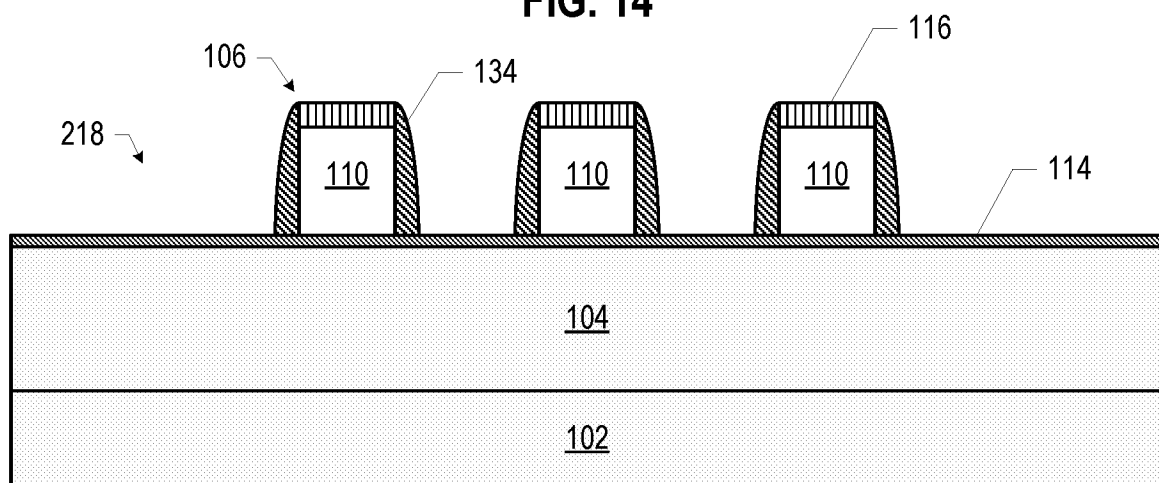


FIG. 15

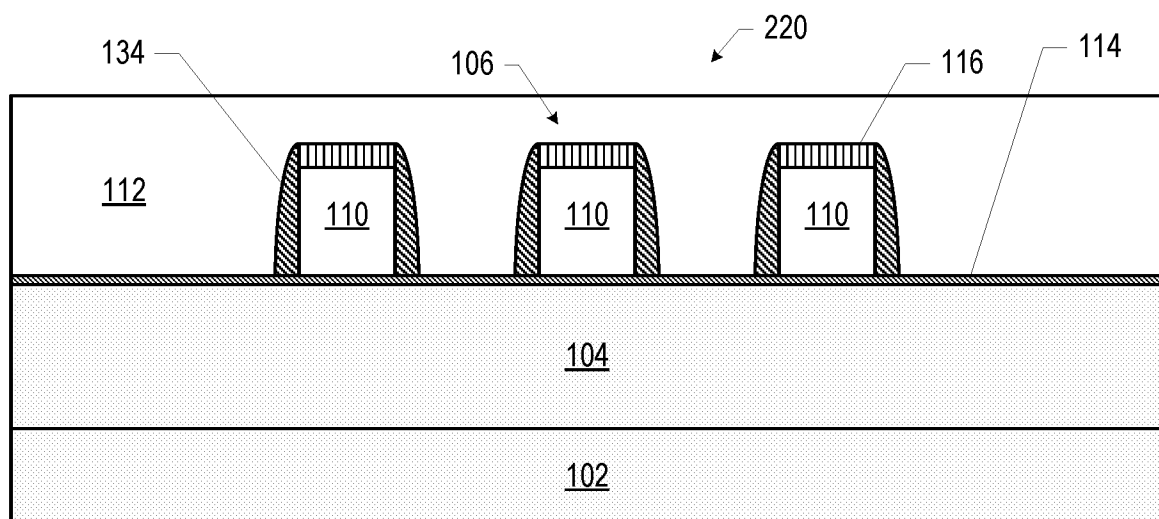


FIG. 16

7/25

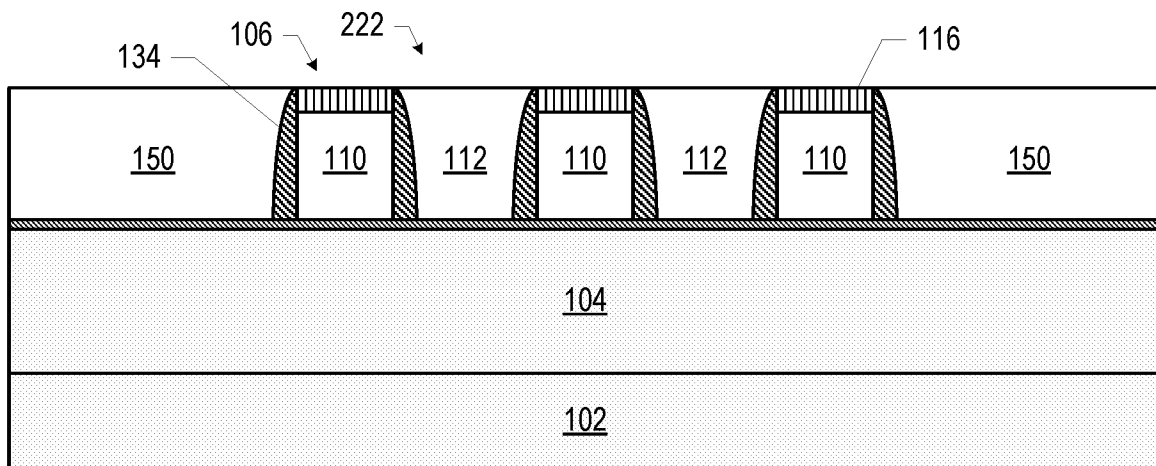


FIG. 17

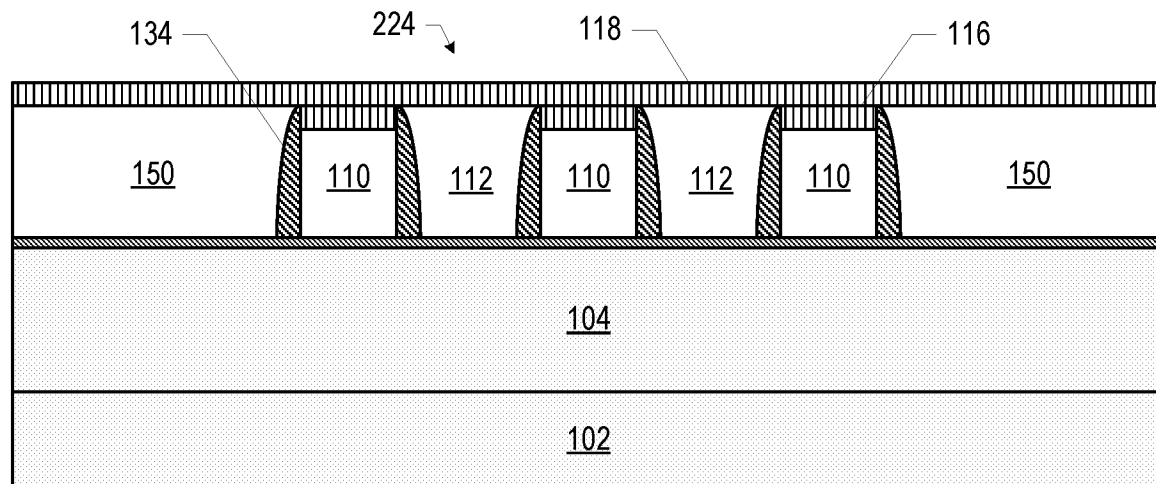


FIG. 18

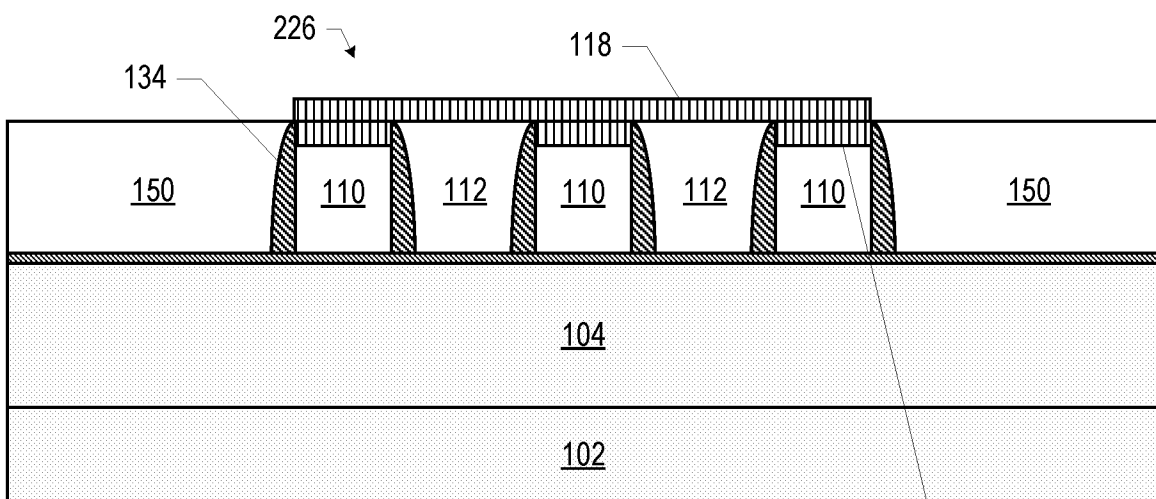


FIG. 19

8/25

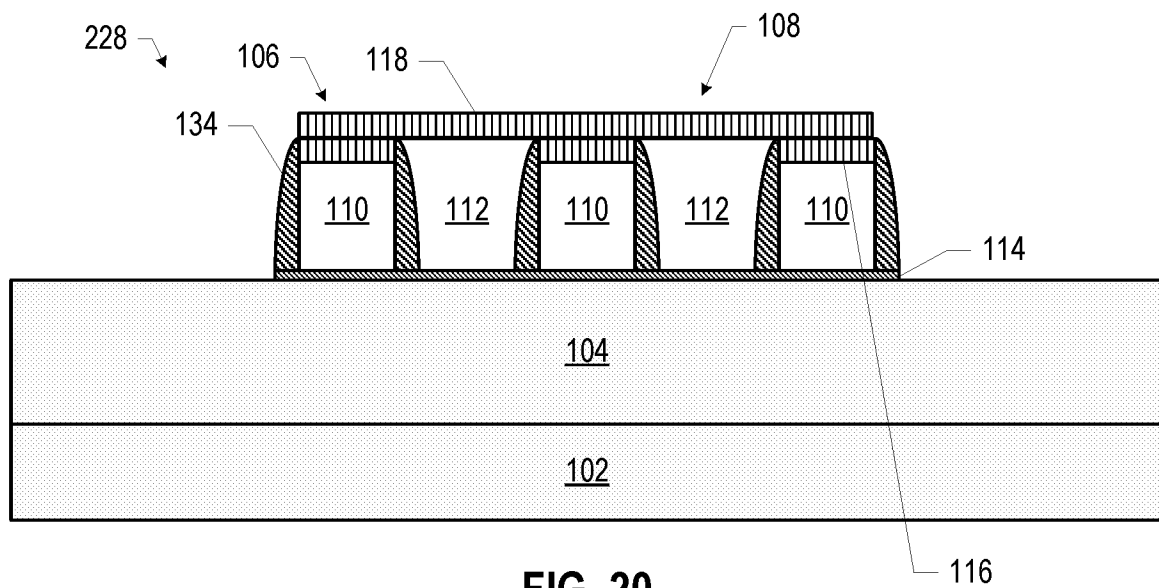


FIG. 20

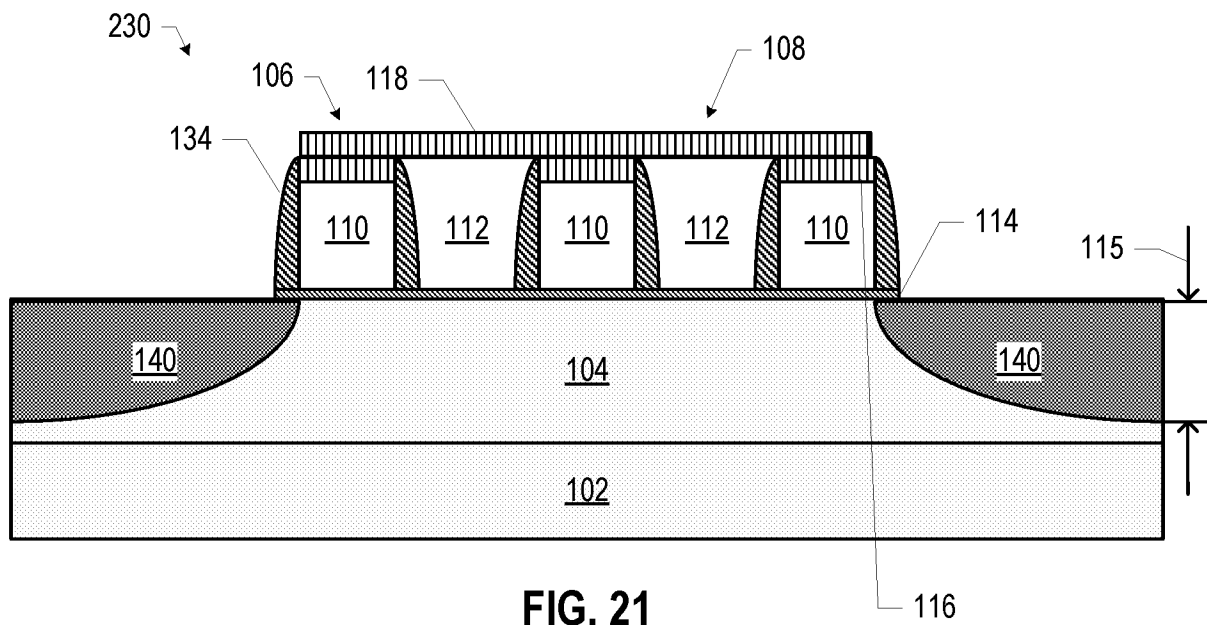


FIG. 21

9/25

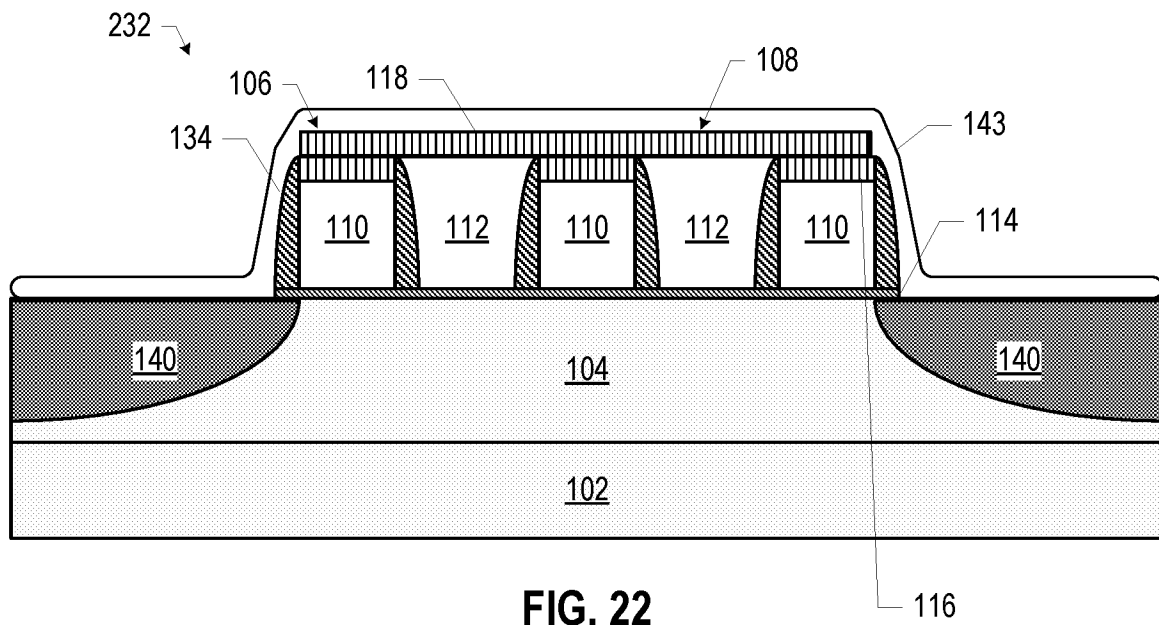


FIG. 22

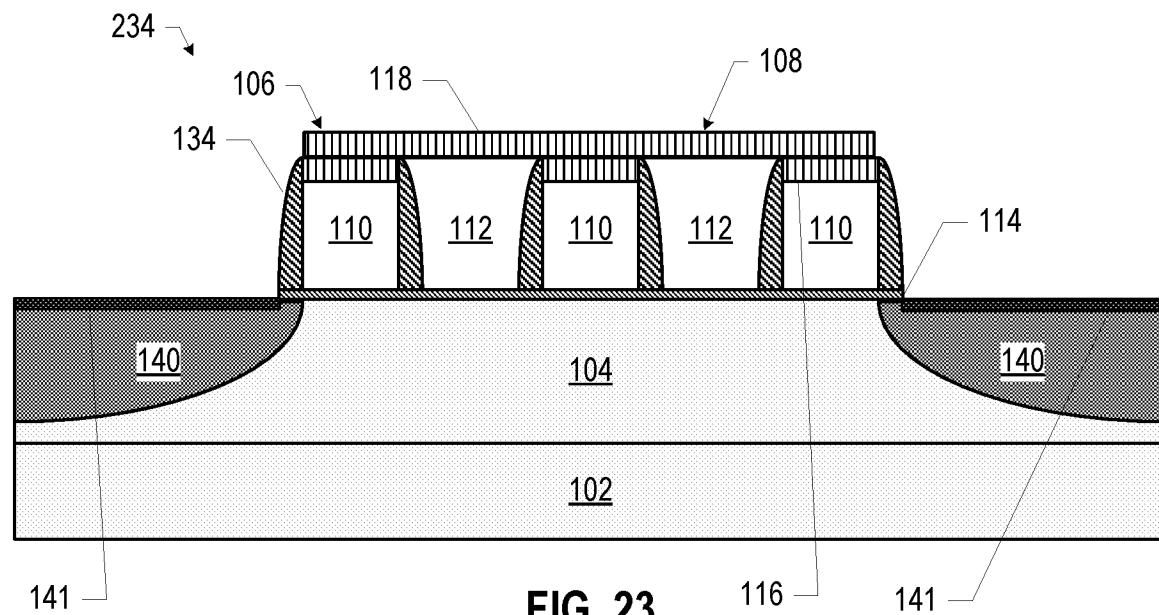
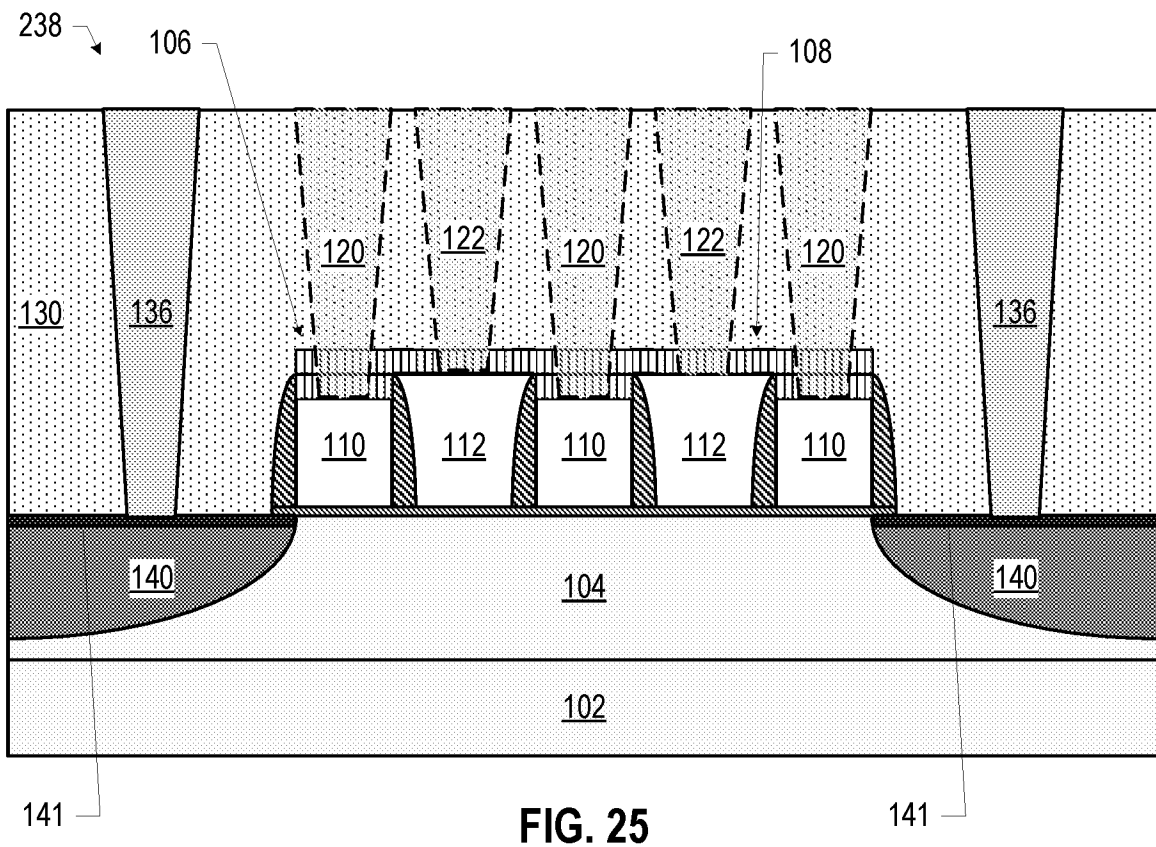
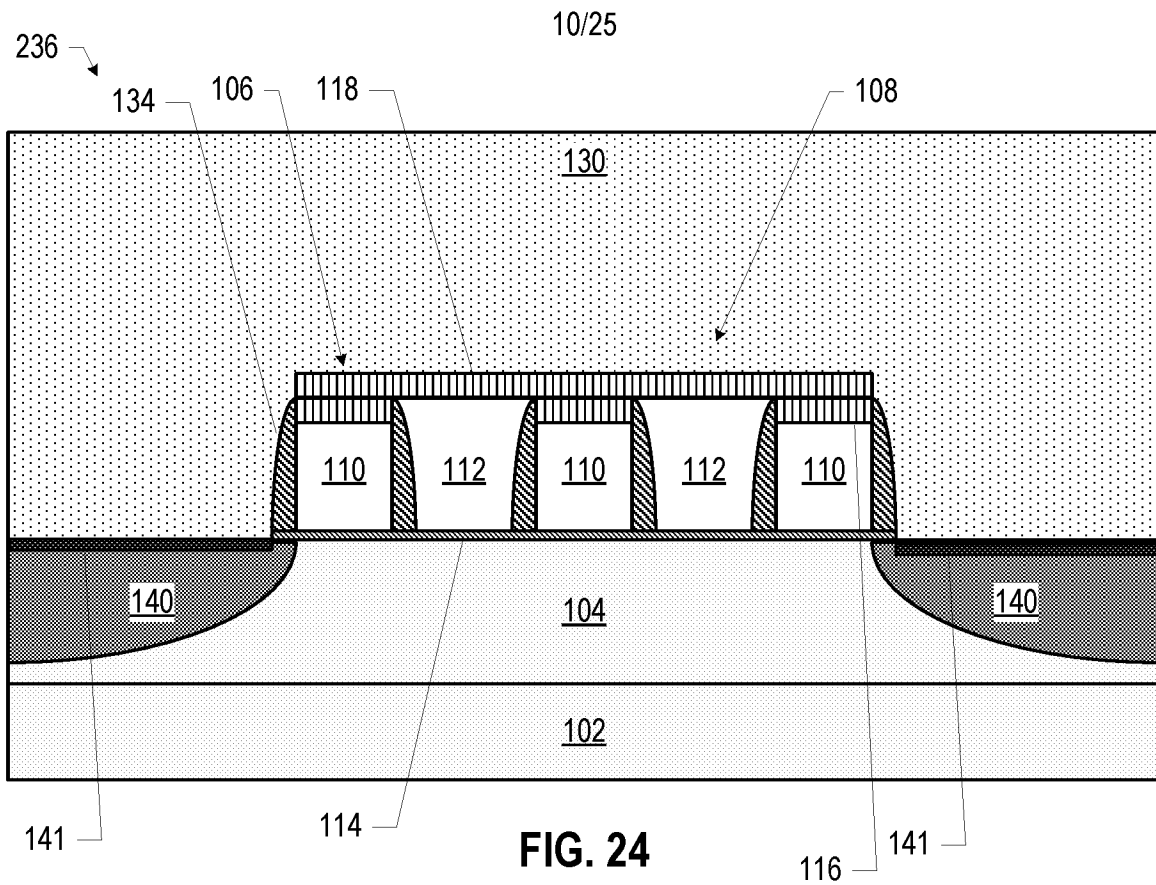


FIG. 23



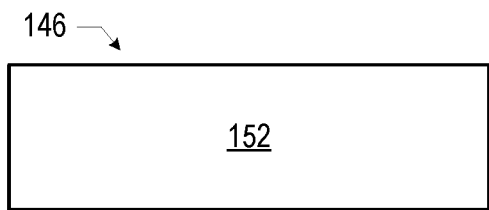


FIG. 26

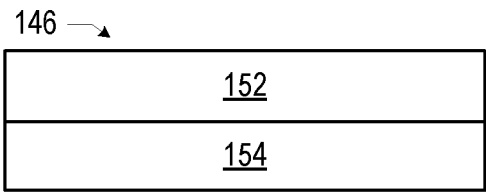
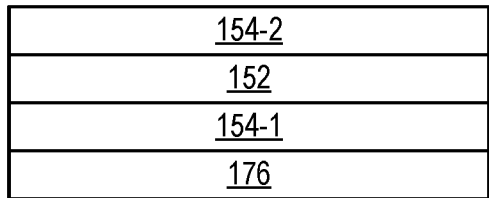


FIG. 27



146 →

FIG. 28

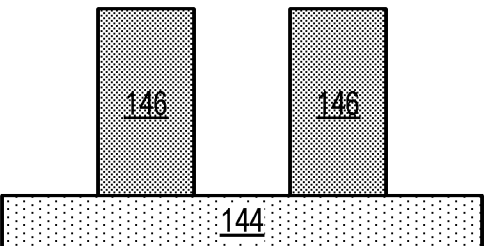


FIG. 29

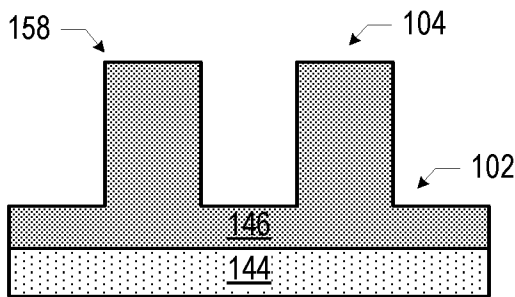


FIG. 30

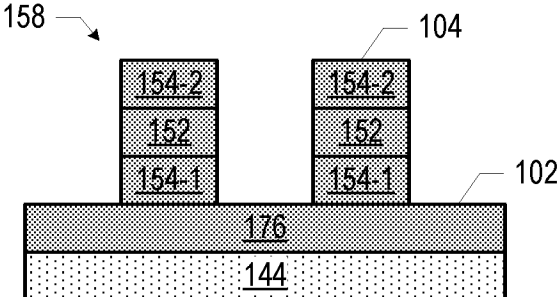


FIG. 31

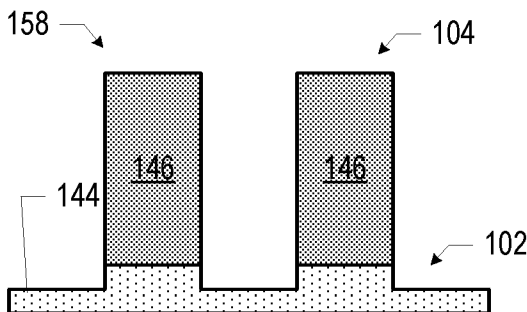


FIG. 32

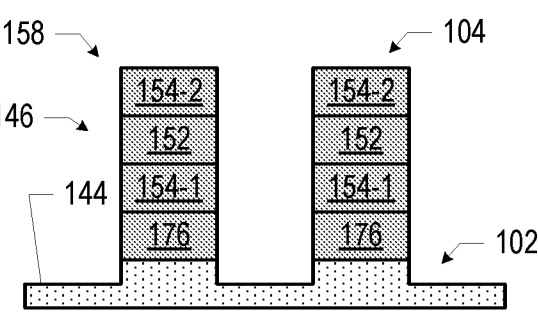


FIG. 33

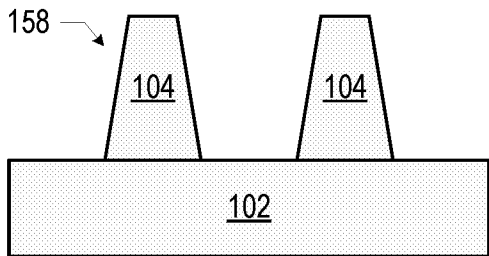


FIG. 34

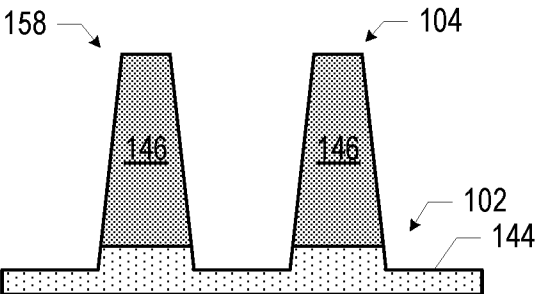


FIG. 35

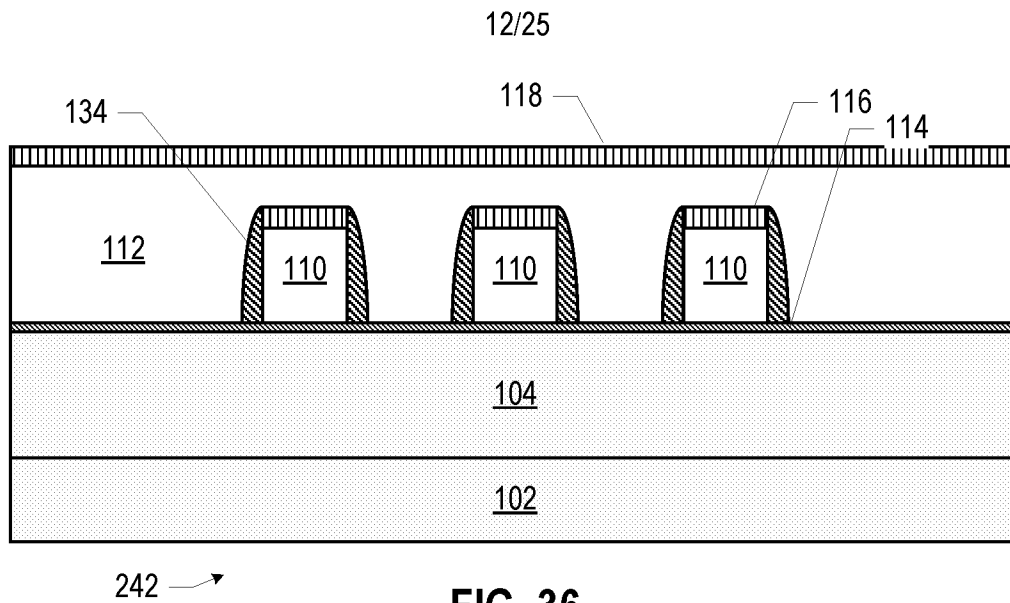


FIG. 36

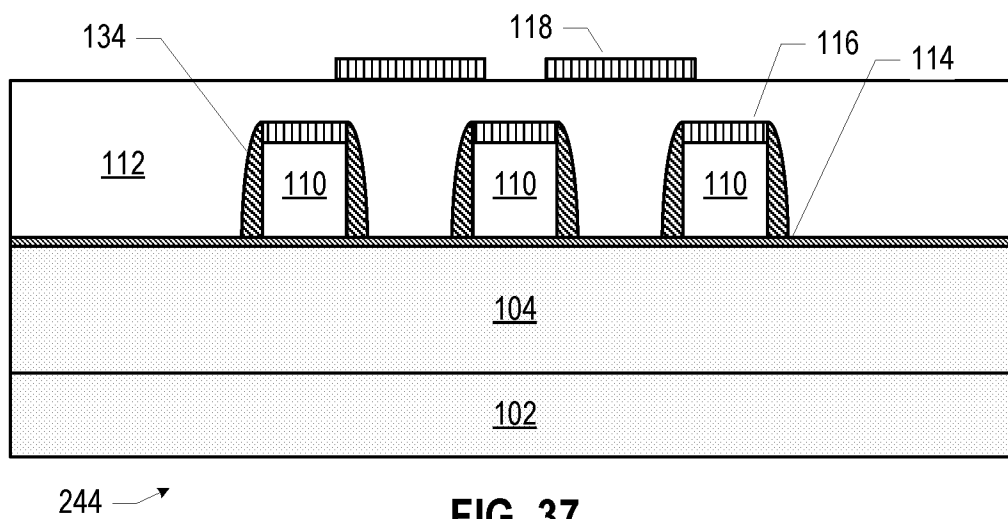


FIG. 37

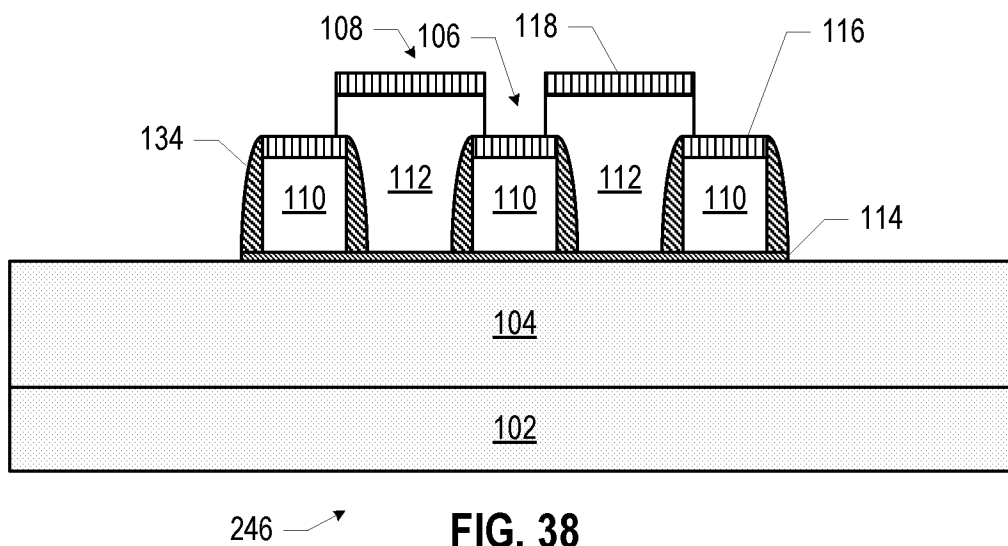


FIG. 38

13/25

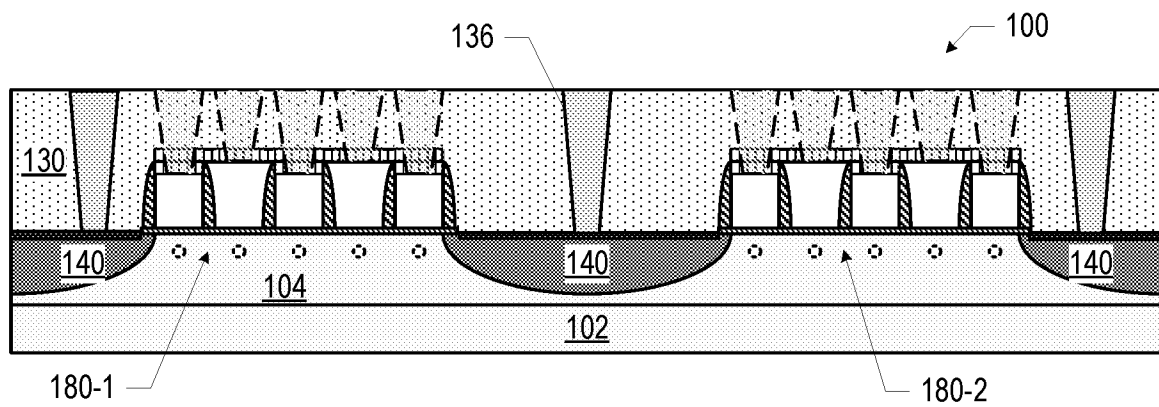


FIG. 39

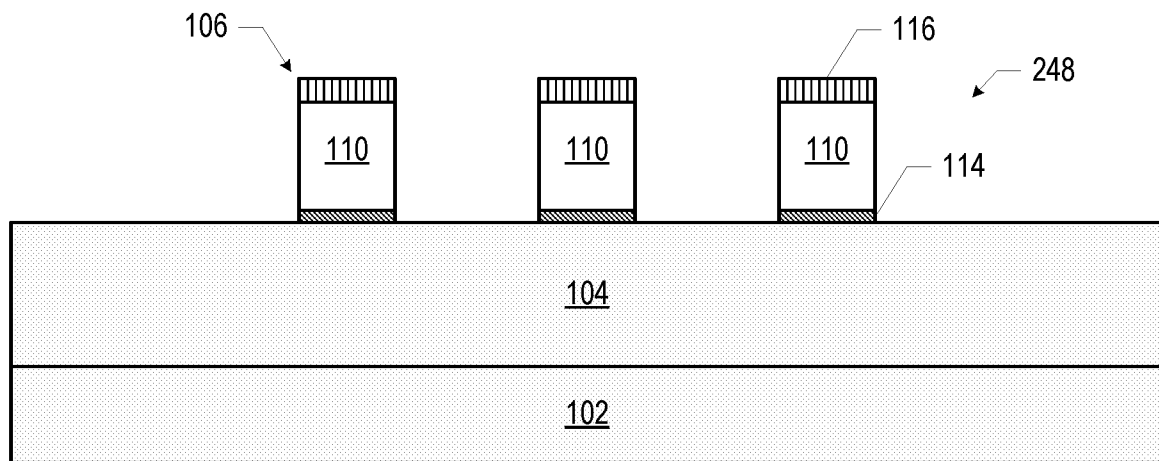


FIG. 40

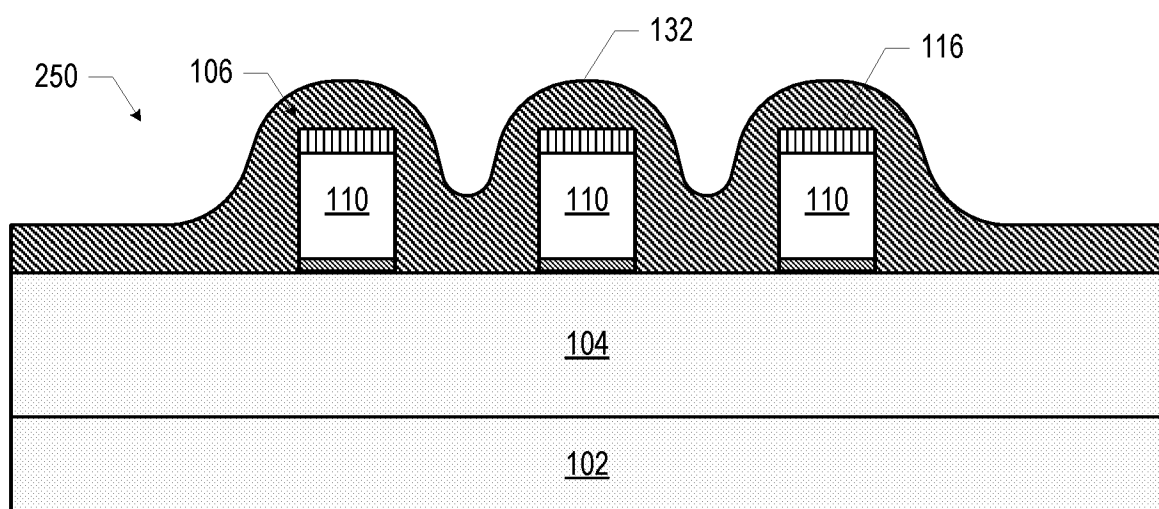


FIG. 41

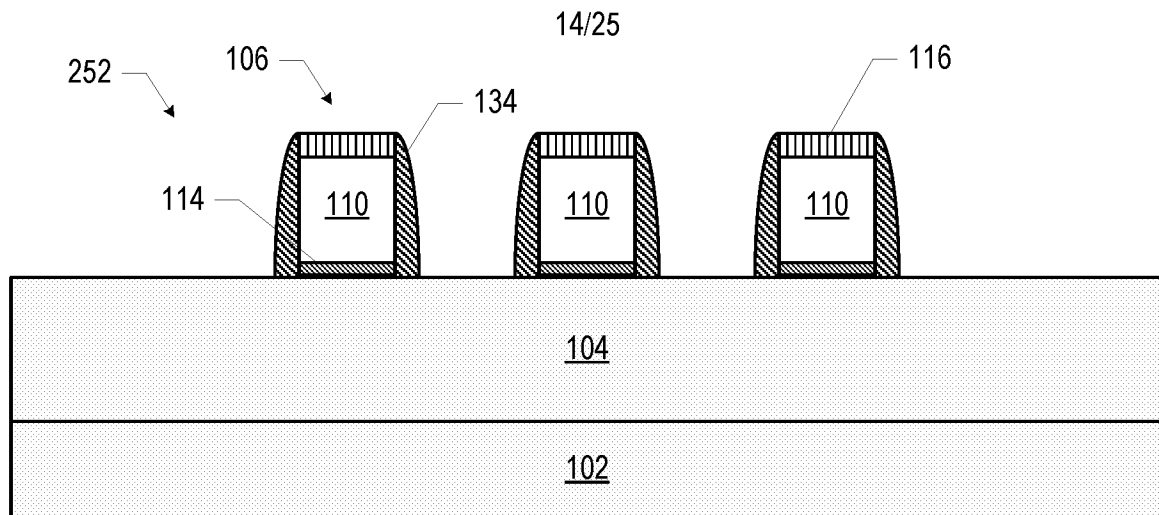


FIG. 42

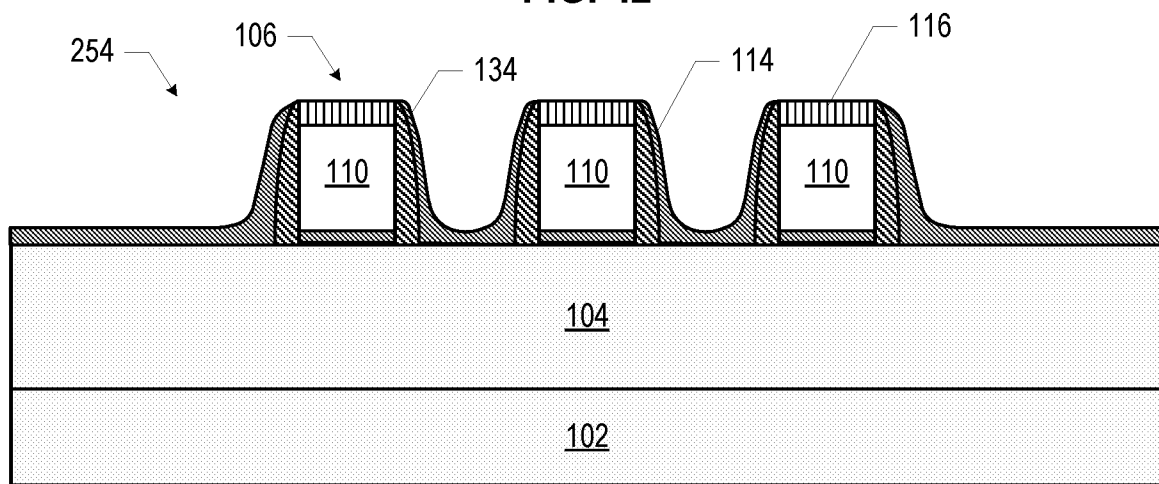


FIG. 43

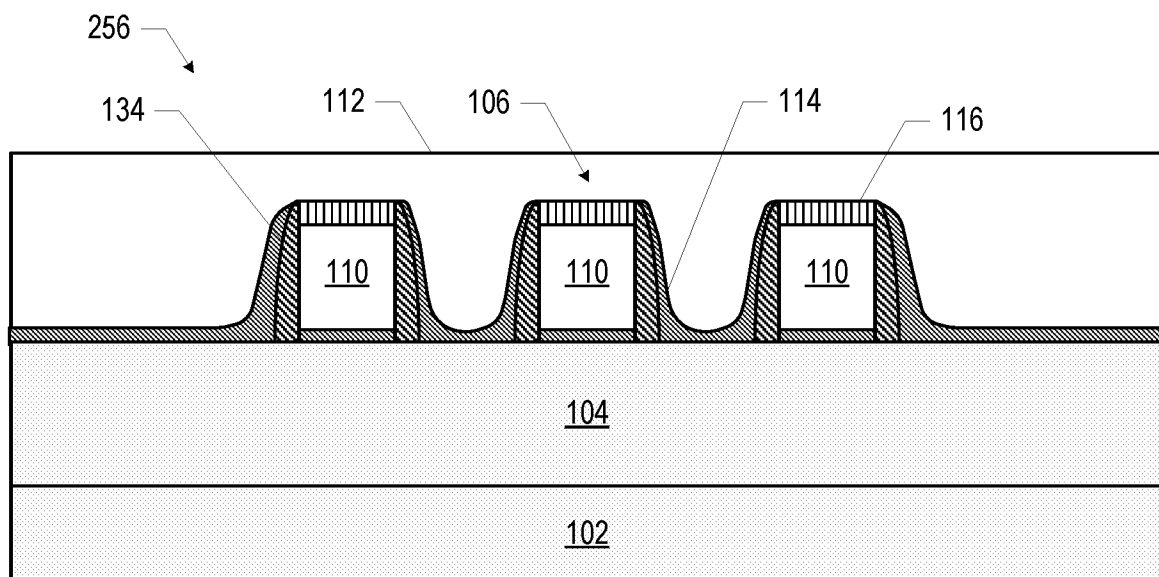


FIG. 44

15/25

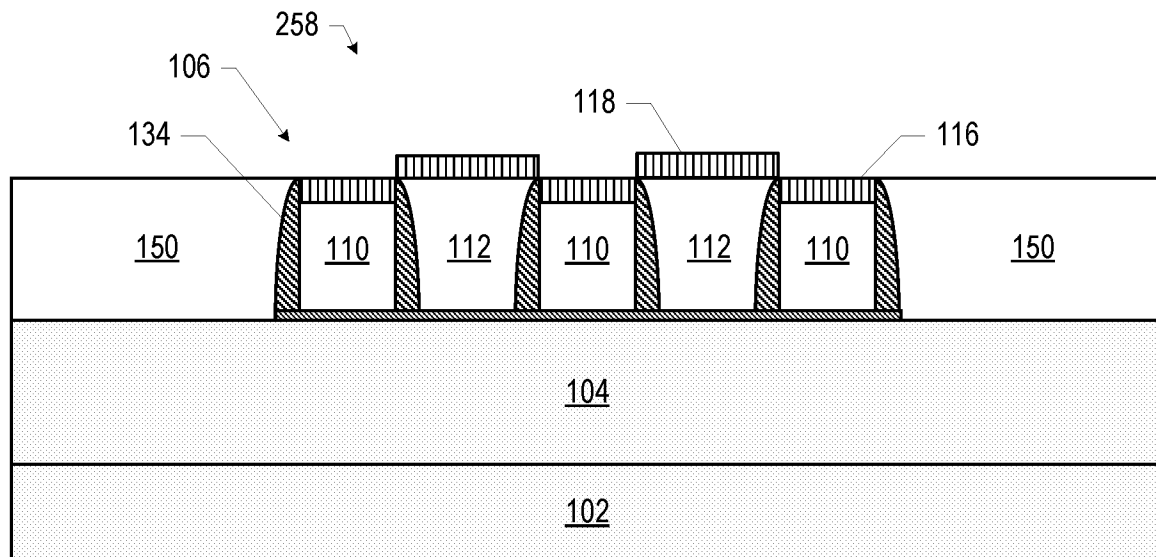


FIG. 45

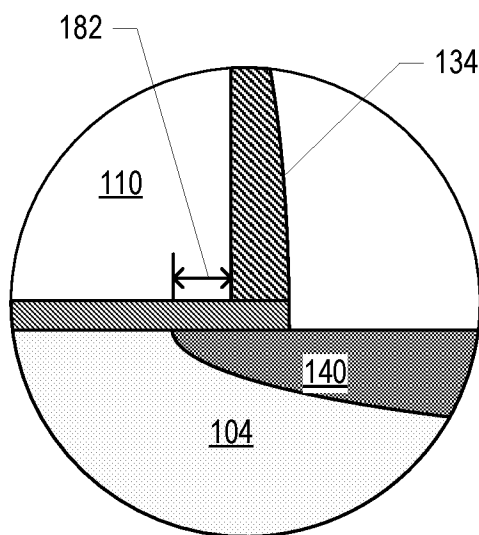


FIG. 46

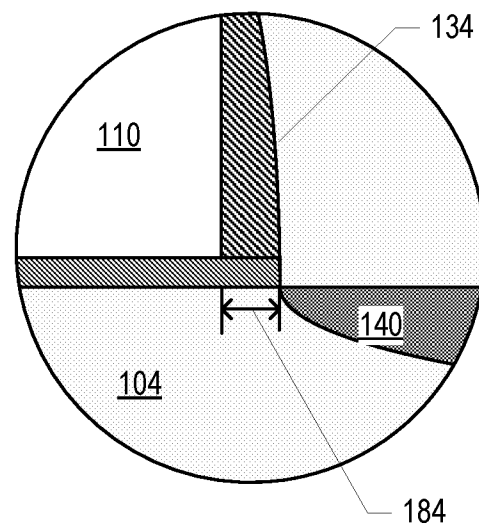


FIG. 47

16/25

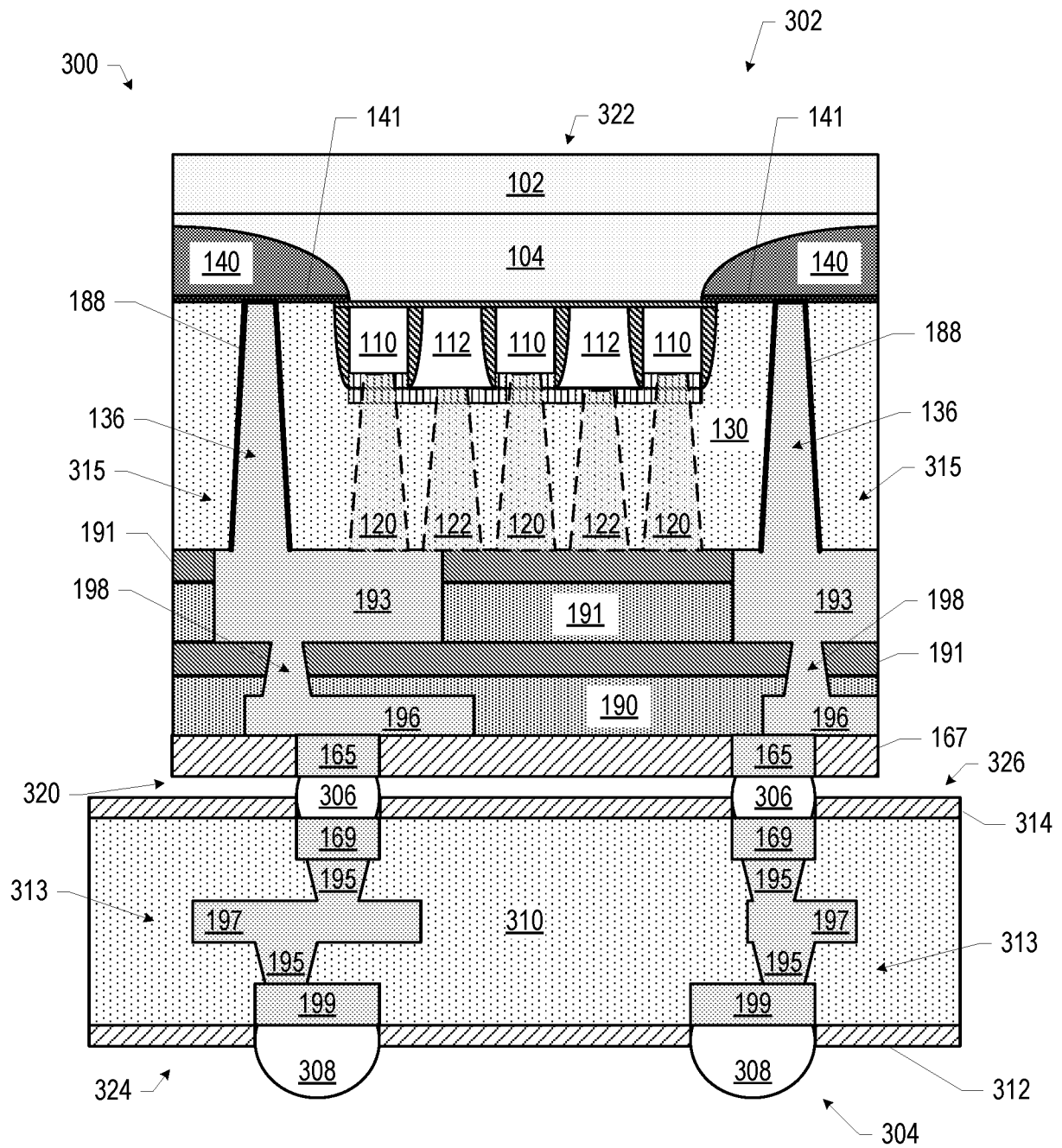


FIG. 48

17/25

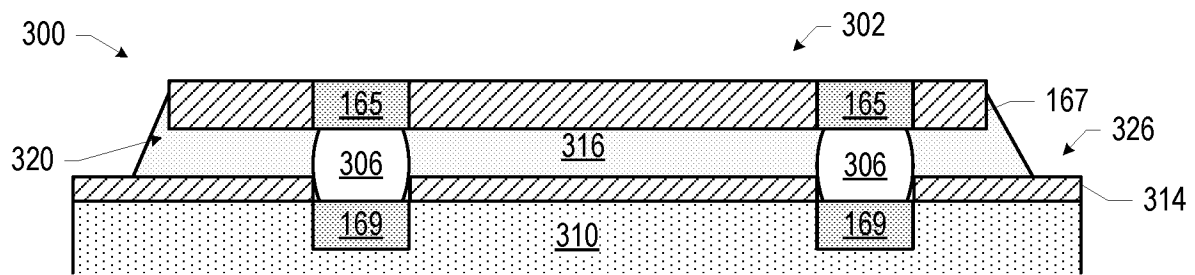


FIG. 49

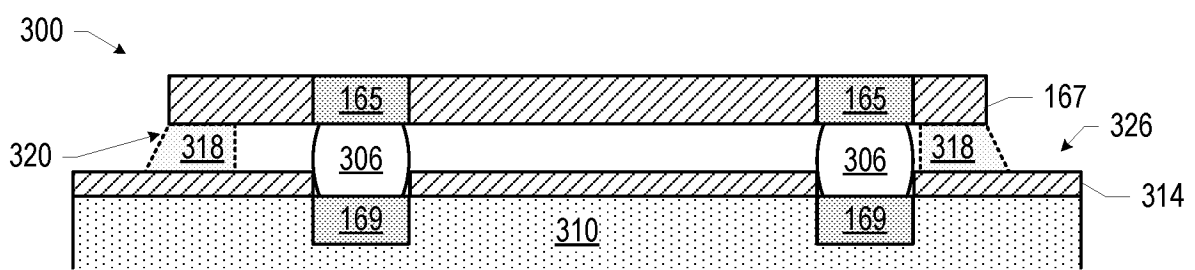


FIG. 50

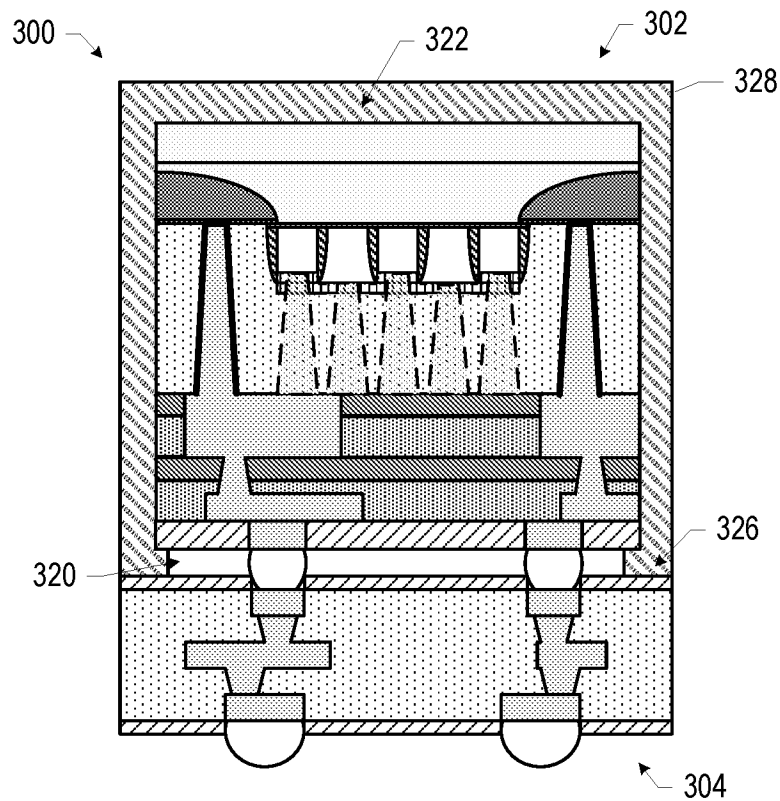


FIG. 51

260 ↘

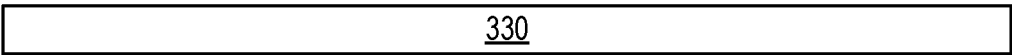


FIG. 52

262 ↘

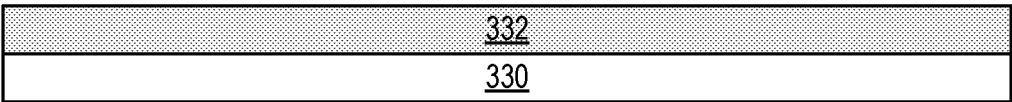


FIG. 53

264 ↘

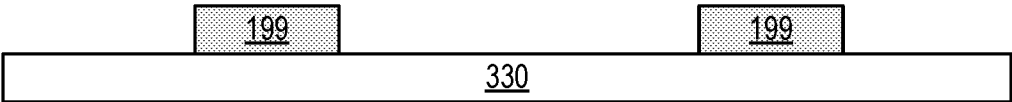


FIG. 54

266 ↘

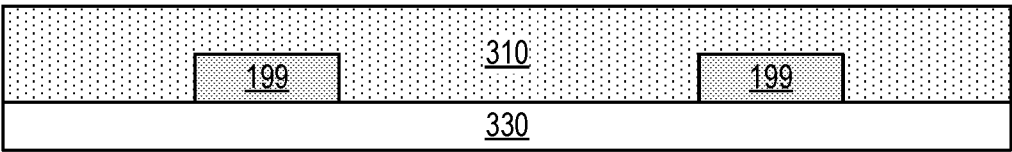


FIG. 55

19/25

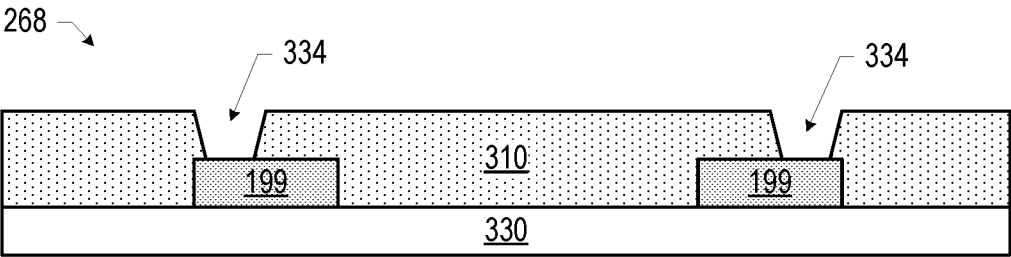


FIG. 56

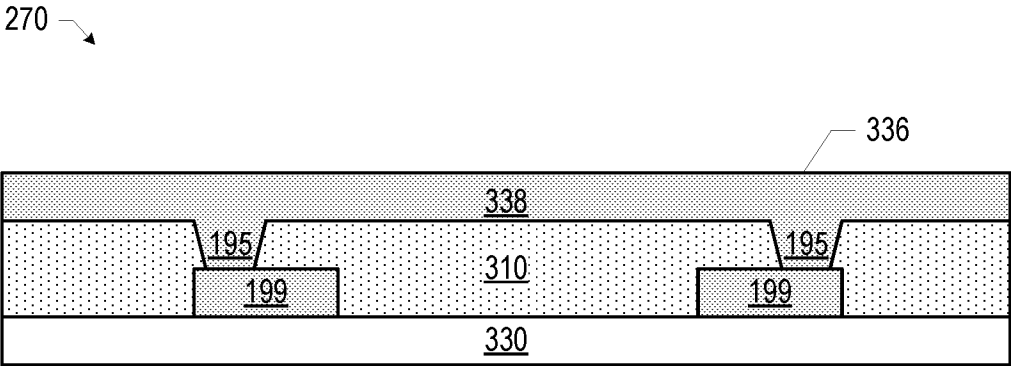


FIG. 57

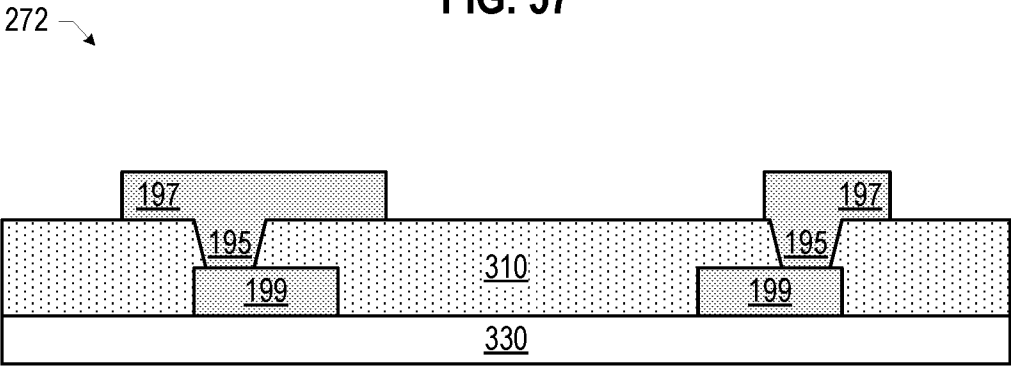


FIG. 58

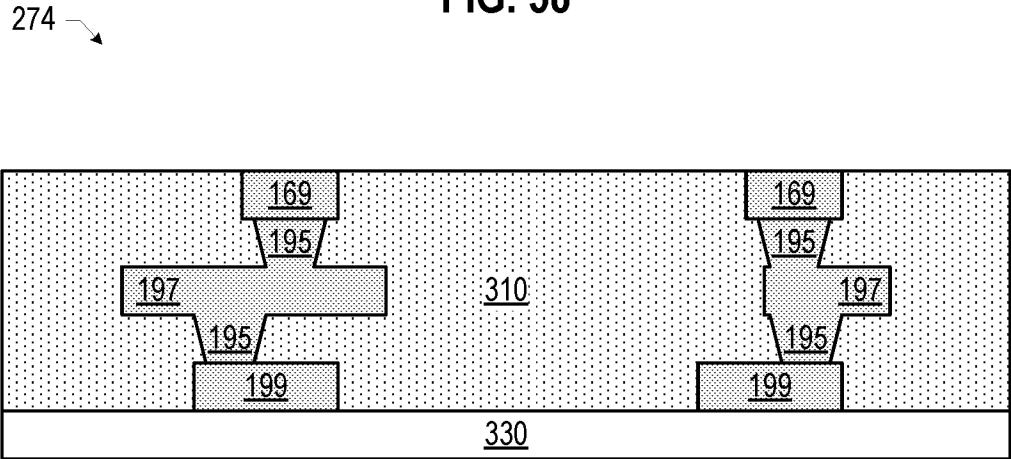


FIG. 59

20/25

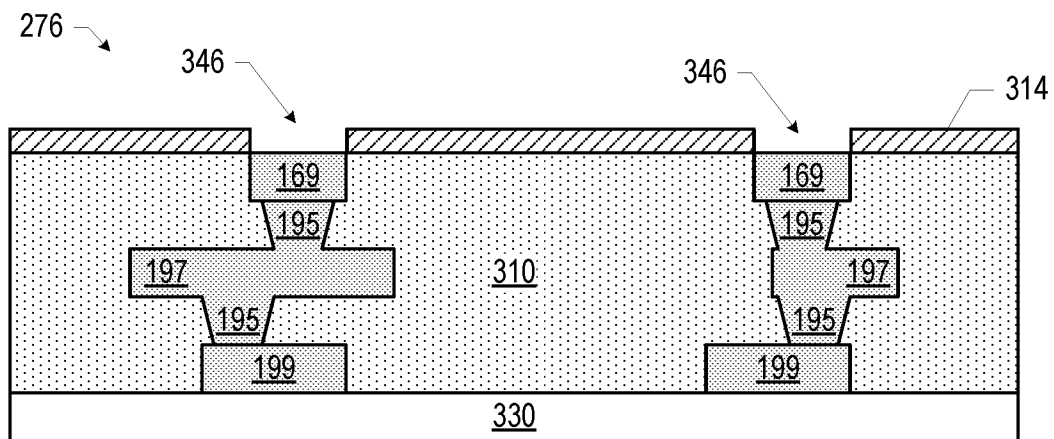


FIG. 60

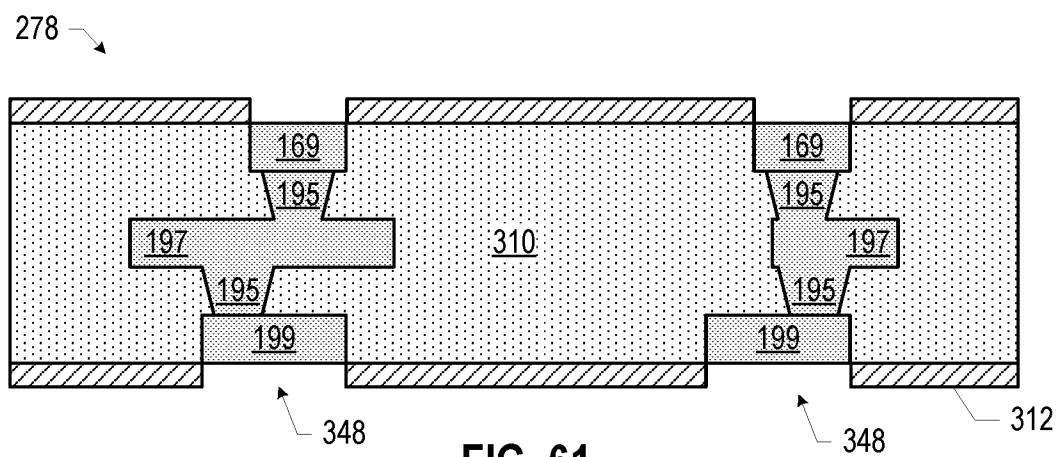


FIG. 61

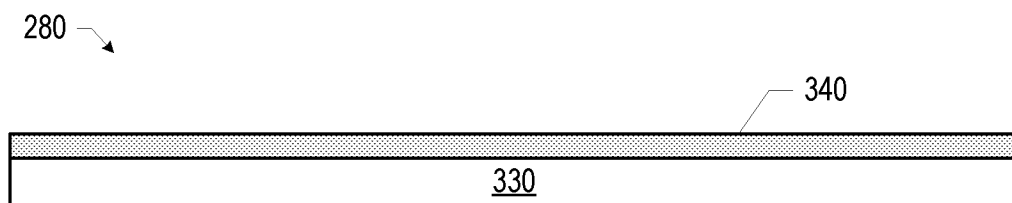


FIG. 62

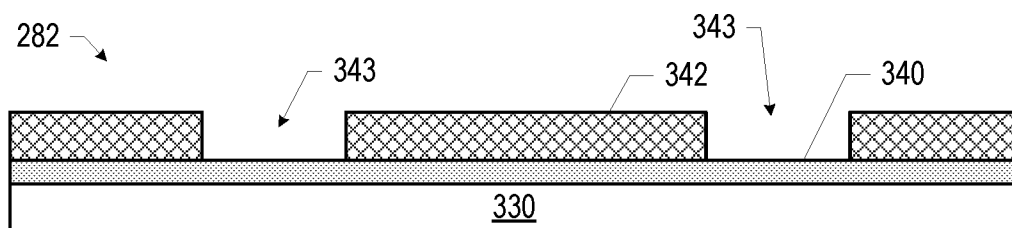


FIG. 63

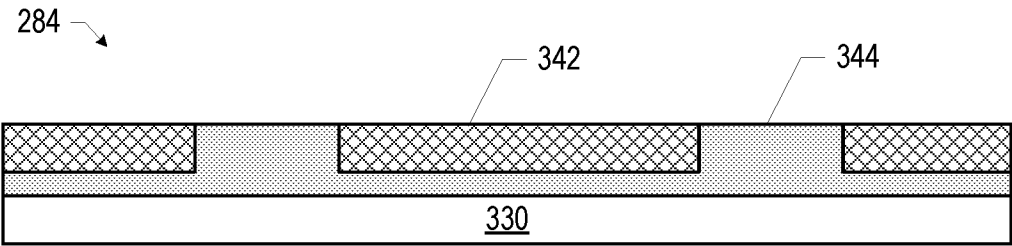


FIG. 64

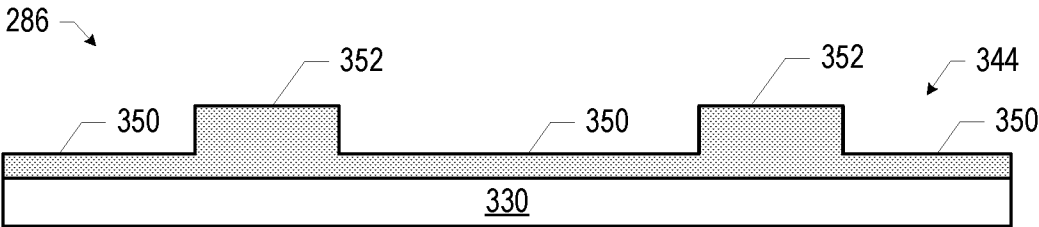


FIG. 65

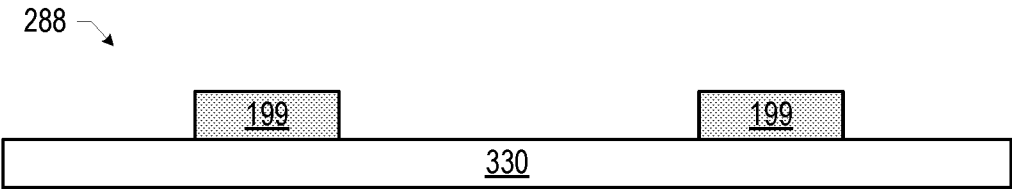


FIG. 66

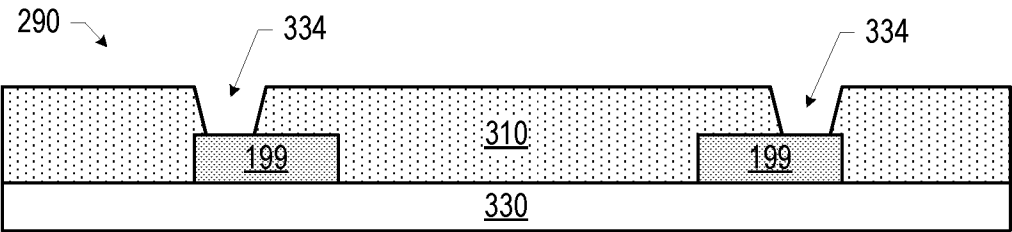


FIG. 67

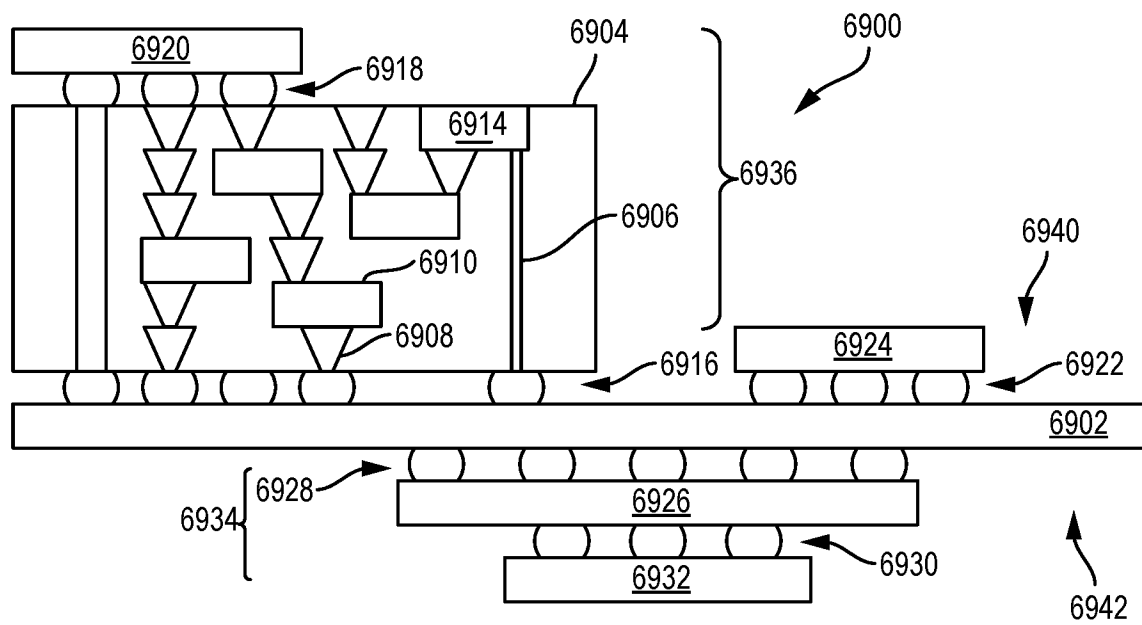
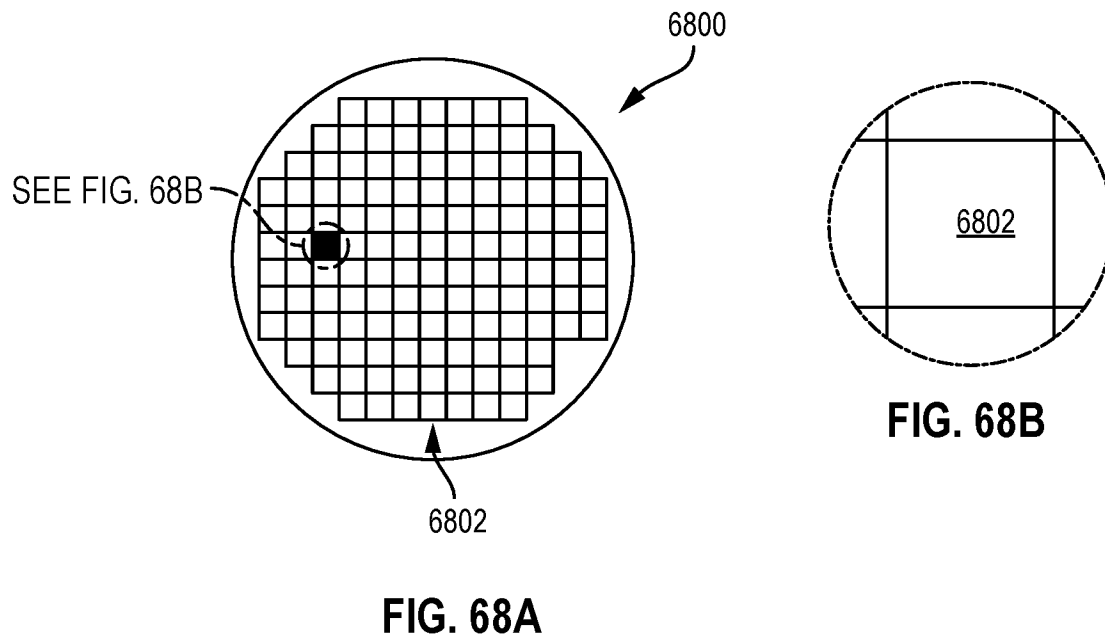
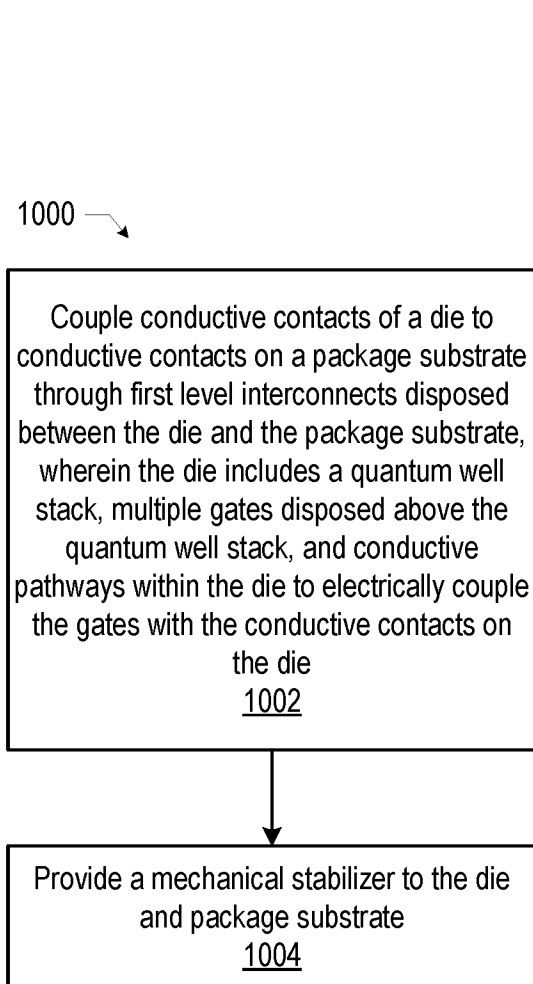
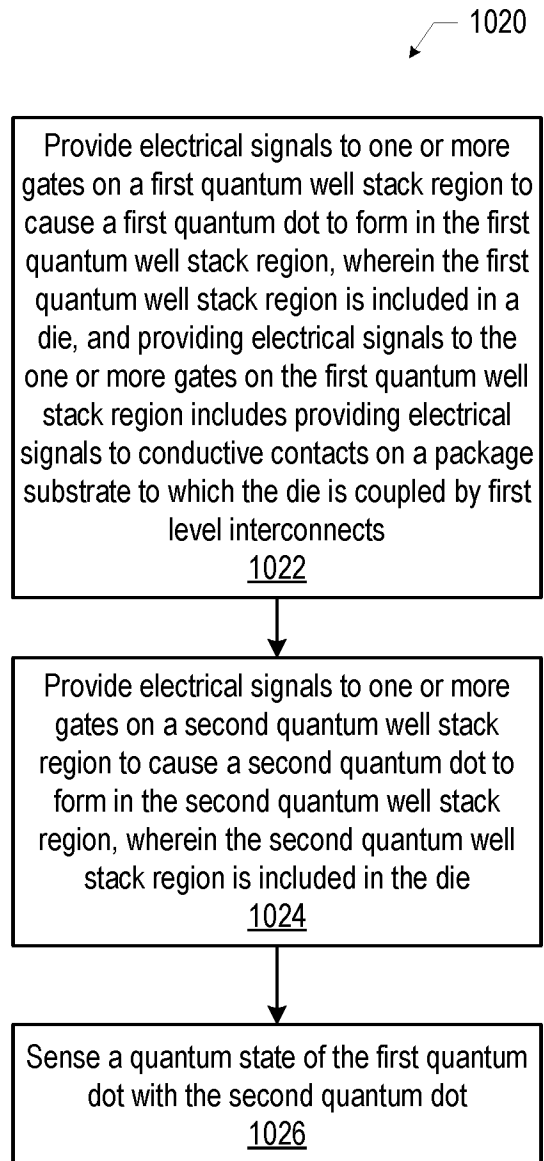


FIG. 69

**FIG. 70****FIG. 71**

24/25

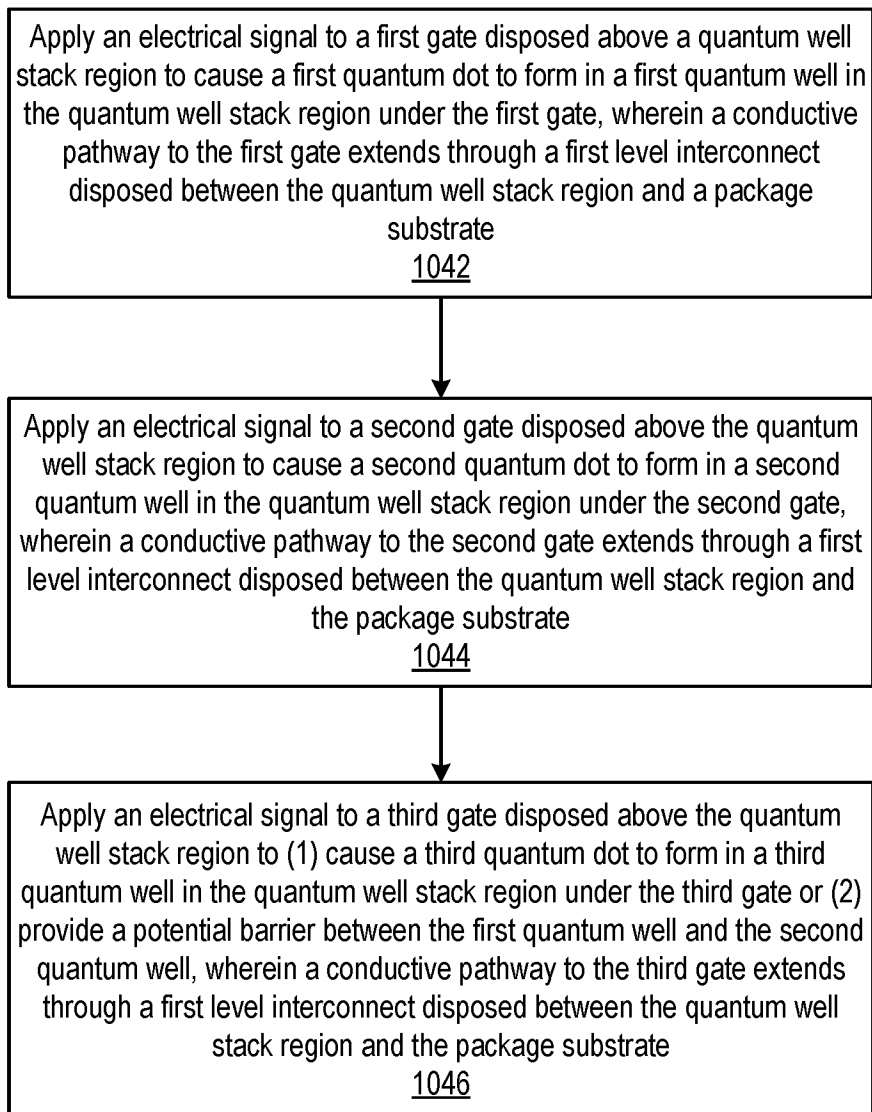
1040 

FIG. 72

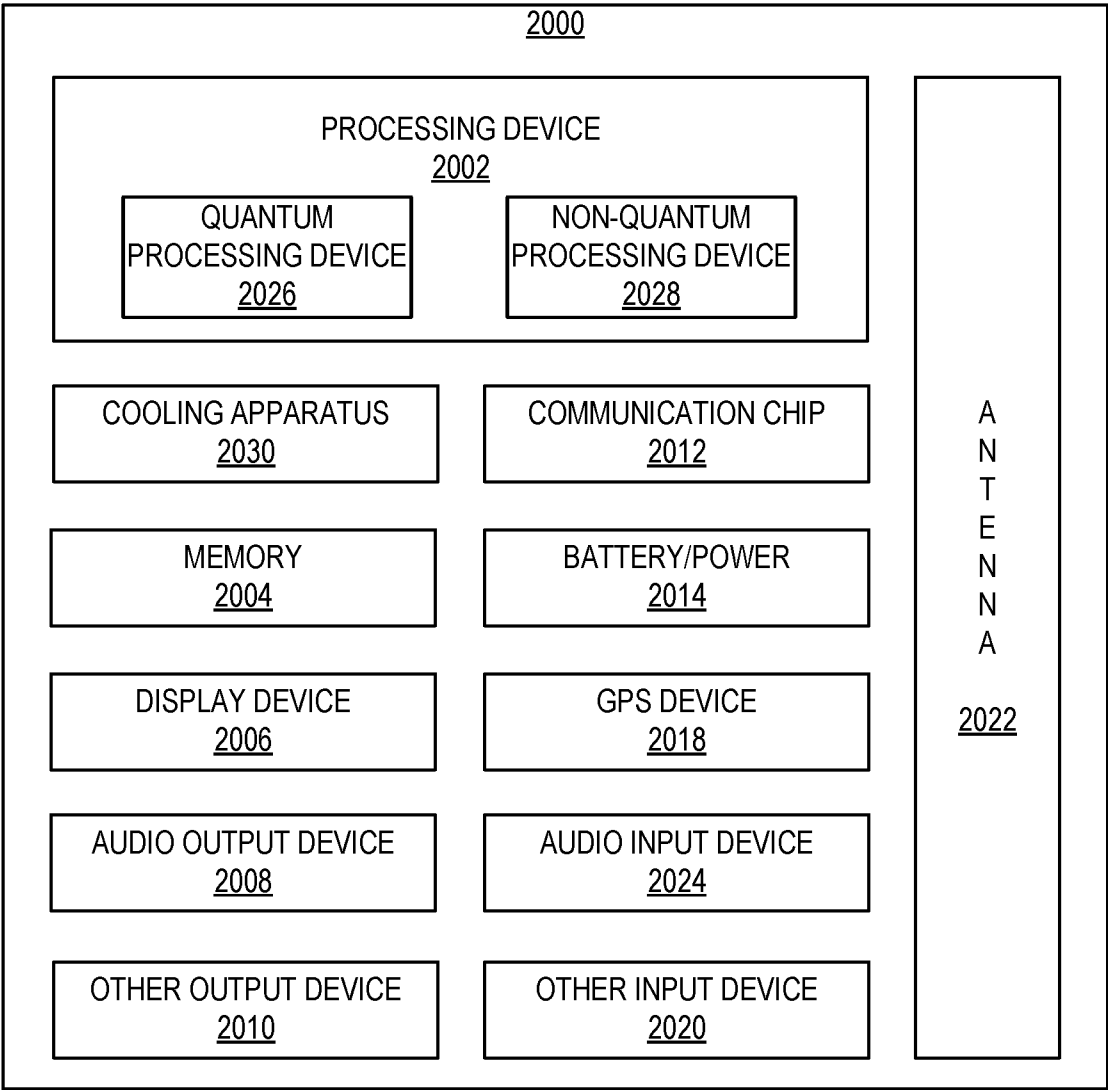


FIG. 73

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/036327**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/778(2006.01)i, H01L 29/12(2006.01)i, H01L 29/66(2006.01)i, H01L 29/80(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/778; H01L 39/02; H01L 21/336; H01L 29/78; H01L 29/94; H01L 21/338; H01L 31/119; H01L 23/498; H01L 21/02; H05K 3/00; H01L 29/06; H01L 29/12; H01L 29/66; H01L 29/80

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: quantum well stack, package, fin, gate, voltage

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012-0280210 A1 (RAVI PILLARISETTY) 08 November 2012 See paragraphs [0029]-[0036] and figures 14-15.	1-10
A		11-25
Y	US 2004-0175881 A1 (LEONARD FORBES et al.) 09 September 2004 See paragraphs [0037]-[0041], claim 16 and figures 1A-1D.	1-10
Y	US 2014-0001644 A1 (CHEN-HUA YU et al.) 02 January 2014 See paragraphs [0009]-[0014] and figures 1-3A.	2-9
Y	US 2009-0099025 A1 (SERGEY V. UCHAYKIN) 16 April 2009 See paragraph [0026] and claim 1.	4-6
Y	US 2011-0147711 A1 (RAVI PILLARISETTY et al.) 23 June 2011 See paragraphs [0019]-[0032], claim 1 and figures 1-7.	10



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

06 March 2017 (06.03.2017)

Date of mailing of the international search report

06 March 2017 (06.03.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



Facsimile No. +82-42-481-8578

Authorized officer

Lee, Eun Kyu

Telephone No. +82-42-481-3580



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/036327

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0280210 A1	08/11/2012	CN 103563085 A	05/02/2014
		EP 2705537 A1	12/03/2014
		EP 2705537 A4	19/11/2014
		JP 2014-517511 A	17/07/2014
		JP 5801474 B2	28/10/2015
		KR 10-1515746 B1	28/04/2015
		KR 10-2014-0003642 A	09/01/2014
		SG 194740 A1	30/12/2013
		TW 201246535 A	16/11/2012
		TW 201448206 A	16/12/2014
		TW 201631642 A	01/09/2016
		TW I455305 B	01/10/2014
		TW I528553 B	01/04/2016
		US 2014-0014903 A1	16/01/2014
		US 2015-0097158 A1	09/04/2015
		US 8541773 B2	24/09/2013
		US 8946679 B2	03/02/2015
		US 9293546 B2	22/03/2016
		WO 2012-150965 A1	08/11/2012
US 2004-0175881 A1	09/09/2004	US 6744082 B1	01/06/2004
		US 6991988 B2	31/01/2006
US 2014-0001644 A1	02/01/2014	CN 103515342 A	15/01/2014
		KR 10-1452056 B1	22/10/2014
		KR 10-2014-0002457 A	08/01/2014
		US 8803323 B2	12/08/2014
US 2009-0099025 A1	16/04/2009	US 8315678 B2	20/11/2012
		WO 2009-046546 A1	16/04/2009
US 2011-0147711 A1	23/06/2011	CN 102656699 A	05/09/2012
		CN 102656699 B	04/05/2016
		CN 104900693 A	09/09/2015
		CN 105870168 A	17/08/2016
		EP 2517256 A1	31/10/2012
		EP 2517256 A4	11/03/2015
		EP 2996154 A2	16/03/2016
		EP 2996154 A3	20/04/2016
		JP 2013-513250 A	18/04/2013
		JP 2016-028447 A	25/02/2016
		KR 10-1378661 B1	26/03/2014
		KR 10-2012-0085929 A	01/08/2012
		US 2013-0032783 A1	07/02/2013
		US 2014-0054548 A1	27/02/2014
		US 2014-0103397 A1	17/04/2014
		US 2016-0172472 A1	16/06/2016
		US 8283653 B2	09/10/2012
		US 8575596 B2	05/11/2013

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/036327Patent document
cited in search reportPublication
datePatent family
member(s)Publication
date

US 9153671 B2

06/10/2015

US 9263557 B2

16/02/2016

WO 2011-087570 A1

21/07/2011