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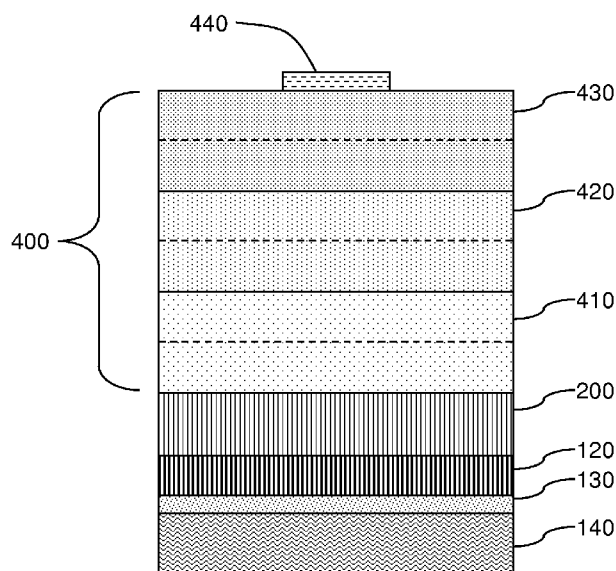


Fig. 4

(57) Abstract: Methods for forming semiconductor devices include providing a crystalline template having an initial grain size, annealing the crystalline template, the annealed template having a final grain size larger than the initial grain size, forming a buffer layer over the annealed template, and forming a semiconductor layer over the buffer layer.

LARGE-GRAIN CRYSTALLINE THIN-FILM STRUCTURES AND DEVICES
AND METHODS FOR FORMING THE SAME

Cross-Reference to Related Application

[0001] This application claims priority to and the benefit of, and incorporates herein by reference in its entirety, U.S. Provisional Patent Application No. 61/147,879, which was filed on
5 January 28, 2009.

Technical Field

[0002] In various embodiments, the present invention relates to thin-film structures and devices.

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Background

[0003] Both the alternative-energy and flat-panel display markets have a need for high-quality, flexible substrates on which to produce highly crystalline semiconductor thin films.

[0004] The current solar cell (i.e., photovoltaic) market relies on technology that has been
15 essentially unchanged for decades. Over 90% of the market is served by crystalline silicon (Si), either single-crystal or polycrystalline, with average conversion efficiencies of 12 – 20%. The costs of crystalline Si devices are high due to high-cost production methods and high demand for the raw materials in competition with the semiconductor electronics industry. Si devices must also be quite thick to achieve these efficiencies, consuming significant quantities of material.

20 The remaining 10% of the market is served largely by thin-film structures based on amorphous Si, CdTe, or copper-indium-gallium-selenide (“CIGS”) that are cheaper to produce but have energy conversion efficiencies below 10%. Amorphous Si efficiencies also degrade with time.

[0005] Higher conversion efficiencies, over 30%, have been demonstrated for thin film multi-junction devices based on III-V semiconductors such as GaAs. However, their production
25 costs are very high since these devices are most advantageously grown on single-crystal germanium (Ge) or GaAs wafers costing over \$10,000 per square meter.

[0006] Emerging low-cost photovoltaic technologies include ribbon-grown Si, polymeric/organic films, and nanotechnology-based approaches. None of these new solutions

fully addresses the market needs for increased production volume, increased efficiency, and lower cost per watt generated.

[0007] A useful substrate for the growth of high efficiency semiconductor films (e.g., III-V semiconductor films) preferably enables the growth of low-defect films (similar to those formed on single-crystal wafers) but at much lower cost and with higher area. Flexibility is a useful attribute. The substrate is also preferably chemically compatible with both the semiconductor material and with the semiconductor process environment. These demanding attributes restrict the number of materials that may effectively be used for this application.

[0008] The ability to produce polycrystalline metals with crystallographic orientation (e.g., “biaxial texture”) approaching single-crystal quality in pure metals has been known since the 1940's. Practical applications of such texture control have included the production of aluminum sheet with textures that enhance the production of cans. Most commercial uses of sheet materials avoid texture, however, because the properties of sheet materials are more isotropic in its absence.

[0009] Face-centered cubic (fcc) metals, some body-centered cubic (bcc) metals, and some alloys based on fcc metals may be useful as substrate materials, as they may be biaxially textured using well-known rolling-deformation and annealing processes. A well-known texture in fcc metals and alloys is the “cube texture,” in which the c-axis of each of the substrate grains is substantially perpendicular to the substrate surface, and the a-axes align primarily along a length direction. Under controlled rolling and annealing processes, these deformation-textured metals may possess biaxial texture approaching that of single crystals.

[00010] Nickel (Ni) is one fcc metal that may be made into thin foils with a well-defined cube texture using a rolling and annealing process. Prior work has shown that oxide intermediate layers may be deposited on a biaxially textured Ni surface using conditions under which nickel oxide is not stable, but where the intermediate layer (for example, CeO_2 or Y_2O_3) is stable, allowing the oxide to inherit the texture of the underlying Ni foil, i.e., form epitaxially thereon. The high-purity Ni required to achieve good biaxial texture is expensive and Ni is mechanically weak following the typical annealing heat treatment used to form the cube texture.

[00011] For these reasons, Ni alloys and other alloys have been developed to make stronger, non-magnetic biaxially textured foils. These alloys often contain alloying elements such as tungsten (W), molybdenum (Mo), vanadium (V), or chromium (Cr) in small controlled amounts. Relatively pure copper (Cu) may also be processed to produce a high-quality cube texture. Commercial grades of Cu with relatively low oxygen content and relatively low content of

substitutional and interstitial elements have been of particular utility. In addition, prior work has shown that a wide range of Ni-Cu alloys may also be processed to produce high-quality cube textures.

[00012] Epitaxial films of other materials such as metals, oxides and nitrides can be grown on the biaxially textured foil. As used herein, “epitaxial” means that the crystallographic orientation of the deposited film is derived from and directly related to the crystallographic orientation of the underlying template.

[00013] Unfortunately, the existing deformation-textured foil approach is frequently not commercially viable for the deposition of semiconducting films necessary for high-performance optical and photovoltaic devices, e.g., Si, Ge, GaAs, InP, and related alloys and compounds. One promising approach utilizing Cu or Cu-Ni alloy textured foils is described in U.S. Patent Application Publication No. 2007/0044832A1, the entire disclosure of which is incorporated by reference herein. However, such foils may be incompatible with conventional semiconductor processes. Both Cu and Ni form arsenide and silicide phases when exposed to As- or Si-containing gases at typical processing temperatures above approximately 350 °C. The formation of these phases causes a significant increase in volume, embrittles the foils, and renders the foils largely unusable for subsequent processing and for most applications.

[00014] One potential solution to the above-described problem appears in U.S. Patent Application Publication Nos. 2009/0117679 and 2009/0114274. Therein, a buffer layer inert to semiconductor precursors “inherits” the texture of the metal foil after formation thereon. The metal foil is then removed before formation of one or more semiconductor layers upon the buffer layer. While this approach addresses the semiconductor process incompatibility issue, the grain size and crystalline orientation of the buffer layer and semiconductor layer(s) are constrained to match those of the original textured metal foil. For many devices and applications, different (e.g., larger) grain size and/or texture are preferred. For example, compound semiconductor films such as GaAs are preferably formed on non-polar substrates (e.g., Ge) having a crystalline orientation tilted away (“off-axis”) from a low-index crystallographic plane. When formed on such substrates, the compound semiconductor films advantageously contain no (or a few closely confined to the growth interface) anti-phase boundaries that may compromise the quality and efficiency of subsequently formed devices. In contrast, compound semiconductor films formed on non-polar substrates having a low-index crystallographic orientation (“on-axis”), e.g., (001) orientation, contain many deleterious anti-phase boundaries. Conventional methods utilizing cube-textured metal films are generally incapable of producing semiconductor films thereon

having tilted crystallographic orientations; the cube texture represents a low-energy state for the growing films, and there is no driving force to form tilted orientations in such layers.

[00015] Thus, while considerable progress has been made in the use of biaxially textured foils in the production of inexpensive and/or flexible semiconductor thin films and devices, there is a need for processes and structures incorporating larger grain size and crystalline orientations different from the conventional cube texture.

Summary

[00016] The foregoing limitations of conventional semiconductor thin-film platforms and fabrication processes are herein addressed by annealing, preferably in a single step, a polycrystalline template layer at a temperature sufficient to cause abnormal grain growth therein (i.e., at a temperature higher than the layer's secondary recrystallization temperature). The abnormal grain growth results in a textured layer with very large grains, although the texture is generally not cube-textured. Rather, the grains of the annealed layer tend to have a crystallographic orientation that is tilted away from a low-index plane. Buffer layers and/or semiconductor layers formed thereon have grain sizes larger than those achievable with conventional methods. Furthermore, the formation process, thickness, and/or post-formation processing of such subsequently formed layers may be optimized to achieve particular crystalline orientations not obtainable with conventional methods.

[00017] In an aspect, embodiments of the invention feature a method for forming a semiconductor device. A crystalline template having an initial grain size is provided. The crystalline template is annealed, the annealed template having a final grain size larger than the initial grain size. A buffer layer is formed over the annealed template, and a substrate layer is formed over the buffer layer. The annealed template is removed to expose a surface of the buffer layer, and a semiconductor layer is formed over the exposed surface of the buffer layer.

[00018] Before annealing the crystalline template may have an initial crystallographic orientation, and after annealing the annealed template may have a final crystallographic orientation different from the initial crystallographic orientation. The annealed template may have a final crystallographic orientation tilted away from (001) by a tilt angle, e.g., a tilt angle ranging from approximately 15° to approximately 20°. The semiconductor layer may have a crystallographic orientation approximately equal to the final crystallographic orientation of the annealed template, and/or a crystallographic orientation tilted away from (001) by an angle ranging from approximately 2° to approximately 8°, e.g., approximately 6°. The grain size of the

annealed template may be greater than approximately 1 cm, and even greater than approximately 10 cm. The grain size of the annealed template may be greater than approximately ten times the thickness of the annealed template.

[00019] A semiconductor device, which may include or consist essentially of at least one polar compound semiconductor material, may be formed on the semiconductor layer. The semiconductor layer may include or consist essentially of a non-polar semiconductor material, and the semiconductor device may be substantially free of anti-phase boundaries. The buffer layer may include or consist essentially of Cr, Pd, Ir, an oxide, and/or a nitride. The crystalline template may include or consist essentially of Cu, Ni, and/or a Cu-Ni alloy.

[00020] In another aspect, embodiments of the invention feature a method for forming a semiconductor device. A crystalline template having an initial grain size is provided. The crystalline template is annealed, the annealed template having a final grain size larger than the initial grain size. A buffer layer is formed over the annealed template, and a semiconductor layer is formed over the buffer layer. The crystalline template includes or consists essentially of a material substantially impervious to reaction with As-containing gases and/or Si-containing gases at a temperature greater than approximately 350°C.

[00021] The crystalline template may include or consist essentially of steel. Before annealing the crystalline template may have an initial crystallographic orientation, and after annealing the annealed template may have a final crystallographic orientation different from the initial crystallographic orientation. The annealed template may have a final crystallographic orientation tilted away from (001) by a tilt angle, e.g., a tilt angle ranging from approximately 15° to approximately 20°. The semiconductor layer may have a crystallographic orientation approximately equal to the final crystallographic orientation of the annealed template, and/or a crystallographic orientation tilted away from (001) by an angle ranging from approximately 2° to approximately 8°, e.g., approximately 6°. The grain size of the annealed template may be greater than approximately 1 cm, and even greater than approximately 10 cm. The grain size of the annealed template may be greater than approximately ten times the thickness of the annealed template.

[00022] A semiconductor device, which may include or consist essentially of at least one polar compound semiconductor material, may be formed on the semiconductor layer. The semiconductor layer may include or consist essentially of a non-polar semiconductor material, and the semiconductor device may be substantially free of anti-phase boundaries. The buffer layer may include or consist essentially of Cr, Pd, Ir, an oxide, and/or a nitride. The crystalline

template may include or consist essentially of Cu, Ni, and/or a Cu-Ni alloy.

[00023] In yet another aspect, embodiments of the invention feature a semiconductor structure including or consisting essentially of a substantially amorphous substrate layer, a tilted buffer layer disposed over the substrate layer, and a semiconductor layer disposed over the tilted buffer layer. The tilted buffer layer and/or the semiconductor layer has a grain size greater than approximately 1 cm.

[00024] The crystallographic orientation of the tilted buffer layer and/or the semiconductor layer may be tilted away from (001) by a tilt angle, e.g., a tilt angle ranging from approximately 15° to approximately 20°, ranging from approximately 2° to approximately 8°, or of approximately 6°. A semiconductor device, which may include or consist essentially of at least one polar compound semiconductor material, may be formed on the semiconductor layer. The semiconductor layer may include or consist essentially of a non-polar semiconductor material, and the semiconductor device may be substantially free of anti-phase boundaries. The magnitude of the tilt away from a low-index crystallographic direction of the semiconductor layer may be less than the magnitude of tilt away from the low-index crystallographic direction of the tilted buffer layer.

[00025] In a further aspect, embodiments of the invention feature a semiconductor structure including or consisting essentially of a template layer, a tilted buffer layer disposed over the template layer, and a semiconductor layer disposed over the tilted buffer layer. The template layer includes or consists essentially of a material substantially impervious to reaction with As-containing gases and/or Si-containing gases at a temperature greater than approximately 350°C.

[00026] The template layer, the tilted buffer layer, and/or the semiconductor layer may have a grain size greater than approximately 1 cm. The template layer may include or consist essentially of steel. The crystallographic orientation of the template layer, the tilted buffer layer, and/or the semiconductor layer may be tilted away from (001) by a tilt angle, e.g., a tilt angle ranging from approximately 15° to approximately 20°, ranging from approximately 2° to approximately 8°, or of approximately 6°. A semiconductor device, which may include or consist essentially of at least one polar compound semiconductor material, may be formed on the semiconductor layer. The semiconductor layer may include or consist essentially of a non-polar semiconductor material, and the semiconductor device may be substantially free of anti-phase boundaries. The template layer may be substantially tilted. The grain size of the template layer may be greater than approximately ten times the thickness of the template layer. The magnitude of the tilt away from a low-index crystallographic direction of the semiconductor layer may be

less than the magnitude of tilt away from the low-index crystallographic direction of the tilted buffer layer.

[00027] These and other objects, along with advantages and features of the present invention herein disclosed, will become more apparent through reference to the following description, the accompanying drawings, and the claims. Furthermore, it is to be understood that the features of the various embodiments described herein are not mutually exclusive and may exist in various combinations and permutations.

Brief Description of the Drawings

[00028] In the drawings, like reference characters generally refer to the same parts throughout the different views. Also, the drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the present invention are described with reference to the following drawings, in which:

[00029] Fig. 1A is a schematic cross-sectional diagram of an exemplary structure formed on a crystalline template in accordance with various embodiments of the invention;

[00030] Fig. 1B is a schematic diagram of the structure of Fig. 1A after removal of the crystalline template;

[00031] Figs. 2-4 are schematic diagrams of the structure of Fig. 1B after further deposition and processing in accordance with various embodiments of the invention; and

[00032] Fig. 5 is a schematic cross-sectional diagram of an exemplary structure formed on a crystalline template in accordance with additional embodiments of the invention.

Detailed Description

[00033] Templates suitable for use in embodiments of the present invention include crystallographically oriented material layers that are chemically compatible and are lattice-matched with known and anticipated semiconductor materials, in particular with compound semiconductors (e.g., III-V or II-VI semiconductor materials). "Lattice-matched," as used herein, refers to layers or materials having relative lattice spacings that allow the epitaxial growth of one layer (e.g., a buffer) on the other (e.g., a template) with a controlled crystallographic orientation and an acceptable level of defects to enable the subsequent integration of high-quality semiconductor materials and/or high-efficiency semiconductor devices. For metallic films, lattice-matching may be within an approximately 10% relative

difference in lattice spacing, preferably within approximately 5%, and more preferably within approximately 2%. The lattice spacing may refer to the material's unit-cell lattice constant as it is commonly defined in the art, or to another interatomic spacing that can be defined in reference to the lattice constant. For instance, the lattice constant of a material may be lattice-matched to the lattice spacing defined by the diagonal of a face of a cubic crystal (which is approximately equal to 1.414 times the lattice constant). Furthermore, a material having a lattice constant (or other lattice spacing) that is approximately an integral multiple (again, within approximately 10%, approximately 5%, or approximately 2%) of that of another material may also be considered to be "lattice matched." For example, a material having a lattice spacing approximately twice that of a second material will achieve approximate lattice registry with every other atom of the second material. The necessary degree of matching may depend on the type of material under consideration. For example, a high-quality semiconductor layer may require closer lattice-matching to an underlying layer than a metal layer deposited on another metal layer. Non-limiting examples of lattice-matching include Cr and palladium (Pd), which are matched to within approximately 8%, as well as the cube-face diagonal of Cr and one-half the cube-face diagonal of Ge, which are matched to within approximately 3%.

[00034] Many of the materials described herein are preferably inexpensive, flexible, mechanically strong and/or compatible with a semiconductor processing environment. Generally, compatibility with a semiconductor processing environment includes resistance to degradation resulting from exposure to elevated temperatures and/or chemicals within the processing environment, including, e.g., resistance to hydrogen, arsenic, or silicon absorption.

[00035] "Chemically compatible", as used herein, refers to materials that do not react with or contaminate semiconductor layers to the extent that performance thereof is substantially affected. "Chemically compatible," as used herein, means that a material is not reactive with a semiconductor process environment and preferably is not reactive with and does not react with (at least at the processing temperatures contemplated herein) or contaminate a semiconductor material integrated thereon. Further, even if a reaction does occur, a chemically compatible material should not react with a semiconductor to the extent that it degrades the quality or performance of the semiconductor. As one non-limiting example of chemical compatibility, Ge and Cr may react to form a GeCr compound, but this compound is stable and does not affect the performance of either the Ge or other semiconductors formed atop the Ge.

[00036] As used herein, "tilted" refers to a layer having multiple grains that are textured but not crystallographically aligned along a low-index crystallographic direction, e.g., (111) or

(100). (Thus, the above-described cube-textured layers are not tilted, as the grains thereof are substantially aligned with a (100) direction.) Rather, the grains are aligned at a non-zero angle (i.e., “tilted”) with respect to a low-index crystallographic direction. Generally, grains in a tilted layer are tilted at approximately the same angle; however, the tilt may be toward one of several, e.g., two or even four, crystallographically equivalent directions. Thus, while the magnitude of a tilted layer is typically approximately equal in the grains of a tilted layer, the direction of the tilt may be different grain-to-grain. The magnitude of the tilt may be approximately constant throughout the thickness of the layer. In certain embodiments (further described below), the magnitude of the tilt may decrease as a function of thickness of the layer due to certain conditions, e.g., total layer thickness, growth rate of the layer, and/or the temperature of deposition. Herein, references to tilt and crystallographic orientation of polycrystalline layers are to at least one of the grains therein.

[00037] Referring to Fig. 1A, a polycrystalline template 100 is provided by, e.g., deformation rolling processes known in the art. Template 100 may be in the form of a thin foil, and may have a thickness between approximately 10 micrometers (μm) and approximately 100 μm , e.g., approximately 25 μm . A surface of template 100 may be polished, e.g., to mirror smoothness. Template 100 may include or consist essentially of a metal or a metal alloy, e.g., Cu, Ni, a Cu alloy, and/or a Ni alloy. Template 100 may include or consist essentially of a steel, e.g., an austenitic stainless steel. In its cold-rolled form, template 100 may have a grain size between approximately 100 nm and approximately 10 μm , e.g., approximately 1 μm . Template 100 may not be chemically compatible with semiconductor materials such as Ge, Si, and III-V semiconductors (e.g., template 100 may react with gases containing Ge, Si, and/or III-V semiconductor precursors such as As) at typical processing temperatures above approximately 350 °C. In certain embodiments, template 100 includes or consists essentially of a material that reacts with As-containing gases and/or Si-containing gases at temperatures greater than approximately 350 °C.

[00038] Template 100 is annealed at a temperature and/or time sufficient to cause abnormal grain growth therein. For example, template 100 may be annealed at a temperature between approximately 900 °C and approximately 950 °C in vacuum for a time between approximately 15 minutes and approximately 60 minutes. After annealing, template 100 exhibits large grain size, i.e., has one or more crystalline grains at least an order of magnitude (or even two orders of magnitude or more) larger than the pre-anneal grain size. For example, annealed template 100 may have one or more elongated grains approximately 1 – 10 μm wide and approximately 5 – 30 μm long.

cm long (or even longer). Generally, the average size of grains of annealed template 100 is larger than approximately five times the thickness of template 100, or even larger than approximately ten times the thickness of template 100. Thus, the grain size of annealed template 100 is larger than that of a “cube-textured” metal film, as such films have average grain sizes generally limited to only one to five times their thickness. The large grain(s) of template 100 are typically tilted. For example, the large grains of annealed template 100 may each have a crystallographic orientation tilted approximately 15° – 20° from a (001) orientation. In some embodiments, annealed template 100 includes only a single grain, i.e., is substantially single-crystalline. Preferably, the anneal is performed at a single step, without deliberate heating at an intermediate temperature. The anneal is also preferably performed without a seed (sometimes utilized to “select” a particular grain) proximate template 100. After annealing, template 100 is generally still polycrystalline and may still have large-angle grain boundaries separating its large grains. In some embodiments, annealed template 100 includes both tilted grains and cube-textured grains; generally, any cube-textured grains are smaller in size than the tilted grains.

[00039] The quality of annealed template 100 measured by x-ray diffraction is superior to that of conventional cube-textured metal layers. For example, the out-of-plane (002) rocking curve full-width half-maximum (FWHM) of a cube-textured metal film may typically be approximately $4 - 5^{\circ}$. Layers subsequently formed on such cube-textured layers also tend to have FWHM values of no less than approximately $4 - 5^{\circ}$. In contrast, the FWHM of annealed template 100 formed as described above may be less than approximately 1° , e.g., may range from approximately 0.1° to approximately 0.2° .

[00040] Optionally, a sacrificial layer 110 is formed over annealed template 100. Sacrificial layer 110 may include or consist essentially of a metal or a metal alloy, e.g., Pd, platinum (Pt), aluminum (Al), or silver (Ag), or may include or consist essentially of an element or compound enabling improved lattice matching between template 100 and buffer layer 120 (described below), e.g., a material having a lattice spacing therebetween. Sacrificial layer 110 may be formed by deposition, e.g., evaporation, sputtering, chemical vapor deposition, atomic layer deposition, molecular beam epitaxy, metallorganic deposition, or by electrochemical means such as electroplating (with or without electrodes). During formation, sacrificial layer 110 preferably inherits the crystallographic orientation (herein, the “crystallographic orientation” of a polycrystalline layer refers to the collective crystallographic orientations of the grains of the layer, each of which may be different from the others) and thus the tilt of annealed template 100. In some embodiments, the crystallographic orientation of sacrificial layer 110 initially replicates

that of annealed template 100 but tilts back toward a low-index crystallographic orientation during formation; hence, the crystallographic orientation of sacrificial layer 110 may change in a tilt direction through at least a portion of its thickness. In such embodiments, the magnitude of the tilt at a top surface of sacrificial layer 110 may be less than the magnitude of the tilt at a top surface of annealed template 100. Further, the grain size of sacrificial layer 110 may be approximately equal to that of annealed template 100, e.g., greater than approximately 1 μm . Preferably, the grain size of sacrificial layer 110 is larger than that of unannealed template 100. In some embodiments, multiple sacrificial layers 110 may be formed over annealed template 100. Formation of sacrificial layer 110 may be performed without ion-beam assistance. During subsequent processing of annealed template 100, sacrificial layer 110 may substantially react with or diffuse into annealed template 100. Sacrificial layer 110 may have a thickness of, e.g., less than approximately 200 nm, e.g., less than approximately 100 nm, or even less than approximately 50 nm. In some embodiments, sacrificial layer(s) 110 have a thickness less than approximately 10 μm .

[00041] A buffer layer 120 is formed over annealed template 100 and optional sacrificial layer 110. Buffer layer 120 may include or consist essentially of a metal or a metal alloy, e.g., Cr and/or Ir, or may include or consist essentially of a nitride or an oxide. Such an oxide may be a compound consisting essentially of oxygen and at least one non-metallic element, e.g., Si. Buffer layer 120 may have a thickness of, e.g., between approximately 100 nm and approximately 500 nm, e.g., approximately 200 nm. In some embodiments, buffer layer 120 have a thickness less than approximately 10 μm . Buffer layer 120 may be formed by deposition, e.g., evaporation, sputtering, chemical vapor deposition, atomic layer deposition, molecular beam epitaxy, metallorganic deposition, or by electrochemical means such as electroplating (with or without electrodes). During formation, buffer layer 120 may inherit the crystallographic orientation (and thus the tilt) of annealed template 100 and/or sacrificial layer 110. In some embodiments, the crystallographic orientation of buffer layer 120 initially replicates that of annealed template 100 and/or sacrificial layer 110 but tilts back toward a low-index crystallographic orientation during formation; hence, the crystallographic orientation of buffer layer 120 may change in a tilt direction through at least a portion of its thickness. In embodiments in which the crystallographic orientation of sacrificial layer 110 tilts back toward a low-index crystallographic orientation, the crystallographic orientation of buffer layer 120 may further tilt toward the same low-index crystallographic orientation, i.e., the magnitude of the tilt at a top surface of buffer layer 120 may be less than the magnitude of the tilt at a top surface of

annealed template 100 and/or sacrificial layer 110. Further, the grain size of buffer layer 120 may be approximately equal to that of annealed template 100, e.g., greater than approximately 1 cm. Preferably, the grain size of buffer layer 120 is larger than that of unannealed template 100. Buffer layer 120 may be provided without ion-beam assistance. In some embodiments, multiple
5 buffer layers 120 may be formed over textured template 100.

[00042] Buffer layer 120 and/or sacrificial layer 110 may have an out-of-plane (002) rocking curve FWHM (as described above in relation to template 100) of less than approximately 1°, e.g., it may range from approximately 0.1° to approximately 0.2°. In preferred embodiments, the FWHM of buffer layer 120 and/or sacrificial layer 110 is approximately equal to that of annealed
10 template 100.

[00043] An optional diffusion barrier 130 is formed over buffer layer 120. Diffusion barrier 130 may be formed substantially non-epitaxially and thus be substantially lacking the crystallographic orientation of buffer layer 120 and annealed template 100; diffusion barrier 130 may even be amorphous in some embodiments. Diffusion barrier 130 may include or consist
15 essentially of a metal or a metal alloy, e.g., W or rhenium (Re), or may include or consist essentially of a nitride or an oxide, e.g., a compound consisting essentially of oxygen and at least one non-metallic element such as Si. Diffusion barrier 130 prevents substantially all interdiffusion or reaction between substrate layer 140 and semiconductor materials and devices formed over buffer layer 120 (as further described below).

[00044] In addition to or instead of diffusion barrier 130, an insulator layer (not shown), e.g., a dielectric or other electrical insulator, may be formed over buffer layer 120. The insulator layer may be amorphous, and may include or consist essentially of an oxide, e.g., a compound consisting essentially of oxygen and at least one non-metallic element such as Si. In an
25 embodiment, the insulator layer may include or consist essentially of a nitride or aluminum oxide. The insulator layer may be formed by deposition, e.g., evaporation, sputtering, chemical vapor deposition, atomic layer deposition, or molecular beam epitaxy, and may be formed without ion-beam assistance. The insulator layer may provide electrical insulation between substrate layer 140 and subsequently formed semiconductor materials and devices (as further described below).

[00045] A substrate layer 140 is formed over buffer layer 120 and optional diffusion barrier 130 (and/or the insulator layer, if present). Substrate layer 140 provides structural support to semiconductor materials and devices formed over buffer layer 120 after removal of annealed
30 template 100 (as further described below), and is preferably chemically compatible with

semiconductor materials such as Ge, Si, and III-V semiconductors at typical processing temperatures above approximately 350 °C. In a preferred embodiment, substrate layer 140 includes or consists essentially of a material substantially impervious to reaction with As-containing gases and/or Si-containing gases at temperatures greater than approximately 350 °C.

5 Substrate layer 140 may be formed substantially non-epitaxially and thus be substantially lacking the crystallographic orientation of buffer layer 120 and annealed template 100; substrate layer 140 may even be amorphous in some embodiments. Therefore, substrate layer 140 may be formed by any method known in the art, e.g., vacuum deposition, chemical vapor deposition, heat lamination, electrodeposition, slurry coating, metallorganic deposition, or lamination. In the
10 case of lamination, the laminating agent such as, for example, a braze alloy or adhesive, should also be chemically compatible and thermally stable with any subsequent semiconductor processes. In an embodiment, substrate layer 140 is formed by electron-beam evaporation at a temperature greater than approximately 900 °C. Substrate layer 140 may include or consist essentially of a composite, a ceramic (e.g., alumina and/or zirconia), a glass, a metal alloy, or a
15 metal, e.g., a Fe-Ni-Co alloy (e.g., KOVAR™), W, Mo, and/or Al. In an embodiment, substrate layer 140 includes or consists essentially of a metal coated with a thicker ceramic material for additional structural support. In various embodiments, substrate layer 140 is flexible and thus capable of being manipulated into non-planar configurations. Substrate layer 140 may be substantially electrically conductive, enabling it to function as a contact, e.g., a back contact, for
20 a subsequently formed semiconductor device. Substrate layer 140 may have a thickness of, e.g., between approximately 1 µm and approximately 0.5 mm.

[00046] Referring to Fig. 1B, annealed template 100 (and optional sacrificial layer 110, if present) is removed, exposing surface 150 of buffer layer 120. Annealed template 100 may be removed by a selective process and/or with end-point monitoring. As utilized herein, a selective
25 process will remove substantially all of annealed template 100 without adversely affecting surface 150, thereby rendering surface 150 suitable for the subsequent formation of semiconductor materials and/or devices thereon. Suitable selective processes may include, e.g., chemical etching (with, e.g., an acid such as nitric acid), electrochemical etching, plasma etching, ion-beam bombardment, laser ablation, melting, and reverse-bias sputtering. Suitable
30 end-point monitoring methods may include, e.g., surface reflectance, residual-gas analysis, optical-absorption spectroscopy, and other methods known in the art to be capable of detecting the substantially complete removal of annealed template 100. Optionally, the exposed surfaces of substrate layer 140 may be protected from damage or removal by a protective layer (not

shown) during removal of annealed template 100. The crystallographic orientation and grain size of buffer layer 120 (derived from annealed template 100), and thus, surface 150, remains substantially unchanged after removal of annealed template 100.

[00047] Referring to Fig. 2, at least one semiconductor layer 200 is formed over surface 150 of buffer layer 120. Buffer layer 120 and semiconductor layer 200 are preferably lattice-matched and chemically compatible. Semiconductor layer 200 may include or consist essentially of at least one group IV element or compound (e.g., Si, Ge, or SiGe), a III-V compound (e.g., a compound including a combination of Al, Ga, In, As, P, and/or N), or a compound such as PbTe, ZnTe, and/or an alloy or bilayer thereof, and may be doped (i.e., include n-type and/or p-type dopants). In a preferred embodiment, semiconductor layer 200 includes or consists essentially of at least one of Si, Ge, or InGaAs. Semiconductor layer 200 may initially inherit the crystallographic orientation (e.g., the tilt) of buffer layer 120 and may thus be substantially oriented away from a low-index crystallographic orientation, e.g., tilted between approximately 15° and 20° away from (001). The crystallographic orientation of semiconductor layer 200 may change as a function of thickness. For example, the orientation may tilt back toward a low-index crystallographic orientation, i.e., the magnitude of the tilt at a top surface of semiconductor layer 200 may be less than the magnitude of the tilt of buffer layer 120 (e.g., at surface 150). Thus, a top surface 210 of semiconductor layer 200 may be tilted away from (001) by between (and including) approximately 2° and approximately 8°, e.g., 6°. Preferably, all portions of semiconductor layer 200 (including top surface 210) have a non-zero tilt away from a low-index crystallographic orientation (e.g., the orientation of template 100 before annealing and abnormal grain growth. Semiconductor layer 200 may be formed by deposition, e.g., chemical vapor deposition, atomic layer deposition, molecular beam epitaxy, liquid phase epitaxy, or physical vapor deposition, at a deposition temperature between approximately 25 °C and approximately 700 °C. The thickness of semiconductor layer 200 may be between approximately 100 nm and approximately 5 μm, e.g., approximately 2 μm. In an embodiment, semiconductor layer 200 is doped to form a p-n junction and/or a p-i-n junction therein. Such a junction may function as part of a subsequently fabricated semiconductor device (as described further below).

Semiconductor layer 200 may include or consist essentially of at least one homojunction or of at least one heterojunction (incorporating multiple semiconductor materials, e.g., forming a quantum well of one material “sandwiched” between layers of another material).

[00048] Semiconductor layer 200 preferably has a grain size larger than that achievable with conventional methods (and larger than that of unannealed template 100), e.g., greater than

approximately 1 cm. In an embodiment, the grain size of semiconductor layer 200 is approximately equal to the grain size of annealed template 100 and/or buffer layer 120. Semiconductor layer 200 preferably is free of anti-phase boundaries.

[00049] In a preferred embodiment, coefficients of thermal expansion of semiconductor layer 200 (and/or subsequently formed semiconductor materials and devices) and substrate layer 140 are substantially matched, thus enabling the fabrication of semiconductor materials and devices substantially free of deleterious residual stresses and/or cracks. According to various embodiments of the invention, substantially matched coefficients of thermal expansion have a relative difference of less than approximately 20%, preferably less than approximately 10-15%, and even more preferably less than approximately 5%. For example, a coefficient of thermal expansion of Mo is approximately $4.8 \times 10^{-6} / ^\circ\text{C}$, matched to within approximately 15% of that of Ge or GaAs (approximately $5.7 \times 10^{-6} / ^\circ\text{C}$).

[00050] Referring to Fig. 3, in various embodiments of the invention, a semiconductor device 300 is formed over semiconductor layer 200. Semiconductor device 300 may include or consist essentially of a photovoltaic cell (see also, e.g., Fig. 4), a light-emitting diode, a laser, or backplane electronics to drive, e.g., a thin-film display. Semiconductor device 300 may include or consist essentially of a III-V compound (e.g., a compound including a combination of Al, Ga, In, As, P, and/or N), or a compound such as CdTe, CdS, ZnTe, MgTe and/or an alloy thereof, and may be doped (i.e., include n-type and/or p-type dopants). In an embodiment, semiconductor device 300 includes or consists essentially of at least one of GaAs, AlGaAs, InGaP, InGaAsN, InGaAsP, InP, AlInAs, InGaAs, CdTe, CdS, CdZnTe, or CdMgTe. Semiconductor device 300 may be doped to form at least one p-n junction and/or p-i-n junction. In Fig. 3, boundary 310 represents the approximate boundary between p- and n-type doped regions in a p-n junction or the intrinsic region in a p-i-n junction. Semiconductor device 300 may be lattice-matched to semiconductor layer 200, and may have a tilt substantially equal to that of semiconductor layer 200. Semiconductor device 300 may include or consist essentially of at least one homojunction or of at least one heterojunction.

[00051] In an embodiment, semiconductor device 300 includes or consists essentially of one or more polar compound-semiconductor materials, and semiconductor layer 200 includes or consists essentially of a non-polar semiconductor material such as Si, SiGe, or Ge. The non-zero crystallographic tilt of semiconductor layer 200 enables the formation of semiconductor device 300 containing substantially no anti-phase boundaries.

[00052] Fig. 4 illustrates a multijunction photovoltaic cell 400 formed over semiconductor

layer 200. Cell 400 includes a plurality of p-n or p-i-n junctions; three such junctions 410, 420, 430 are depicted in Fig. 4. Each of the junctions may have a different bandgap; thus, each junction may absorb light of a different wavelength, increasing the overall efficiency of cell 400. The intrinsic layer in a p-i-n junction may decrease dark current of cell 400 (or a junction therein) by substantially preventing the formation of current leakage paths from the p-type doped layer to the n-type doped layer (or vice versa) along grain boundaries in one or more of the layers. The intrinsic layer may also substantially increase collection efficiency (i.e., the internal quantum efficiency) of photogenerated carriers by enabling transport by the faster drift process rather than by slower diffusion transport). One or more of the semiconductor materials in cell 400 may be substantially lattice-matched to semiconductor layer 200, and semiconductor layer 200 may include a p-n or p-i-n junction (and thus form an active portion of the device, as mentioned above). A top contact 440, which may include or consist essentially of, e.g., a metal or a transparent conductor (such as indium tin oxide), may be formed to enable electrical contact to cell 400. Substrate layer 140 may function as a back contact to cell 400. In structures containing an optional insulator layer over substrate layer 140, the insulator layer may provide isolation between multiple semiconductor devices 300 and/or cells 400 formed over a common substrate layer 140. Cell 400 (and/or other semiconductor devices 300) may exhibit energy conversion efficiencies greater than approximately 15%, greater than approximately 20%, or even greater than approximately 30% under one-sun terrestrial illumination conditions. The devices may exhibit greater than 80% of the energy conversion efficiencies of substantially similar devices fabricated over single-crystal semiconductor substrates.

[00053] Referring to Fig. 5, embodiments of the invention may be practiced utilizing a template 500 that is chemically compatible and thermally stable with subsequent semiconductor formation and processing. For example, template 500 may be chemically compatible with semiconductor materials such as Ge, Si, and III-V semiconductors at typical processing temperatures above approximately 350 °C. In certain embodiments, template 500 includes or consists essentially of a material substantially impervious to reaction with As-containing gases and/or Si-containing gases at temperatures greater than approximately 350 °C, such as steel (e.g., an austenitic stainless steel). Such templates 500 may be annealed and may have grain sizes and tilts as described above with respect to template 100. The utilization of such templates 500 enables the formation of semiconductor layer 200, semiconductor device 300, and/or cell 400 without the formation of substrate layer 140 and the removal of template 500. In such embodiments, semiconductor layer 200 is formed on buffer layer 120 while template 500 is

present. Semiconductor device 300 and/or cell 400 (not shown in Fig. 5) may be formed on semiconductor layer 200 as described above.

[00054] The layer and/or device fabrication processes described herein may be practiced in a conventional batch or single-wafer process or by a roll-to-roll continuous or stepwise

5 manufacturing method. The resulting devices may have surface areas greater than approximately 115 cm^2 . Roll-to-roll processes may take place in a continuous system in which each step of the process is performed, or in a series of systems, each of which performing one or more of the steps in the process. A roll-to-roll process (or processes) may include or consist essentially of deposition of sacrificial layer 110, buffer layer 120, diffusion layer 130, and one or more
10 semiconductor layers 200. A roll-to-roll process may also include the removal of template 100. Moreover, devices and materials utilized in accordance with embodiments of the present invention may be substantially non-superconducting.

[00055] The terms and expressions employed herein are used as terms and expressions of description and not of limitation, and there is no intention, in the use of such terms and

15 expressions, of excluding any equivalents of the features shown and described or portions thereof. In addition, having described certain embodiments of the invention, it will be apparent to those of ordinary skill in the art that other embodiments incorporating the concepts disclosed herein may be used without departing from the spirit and scope of the invention. Accordingly, the described embodiments are to be considered in all respects as only illustrative and not
20 restrictive.

What is claimed is:

- 1 1. A method for forming a semiconductor device, the method comprising:
2 providing a crystalline template having an initial grain size;
3 annealing the crystalline template, the annealed template having a final grain size larger
4 than the initial grain size;
5 forming a buffer layer over the annealed template;
6 forming a substrate layer over the buffer layer;
7 removing the annealed template to expose a surface of the buffer layer; and
8 forming a semiconductor layer over the exposed surface of the buffer layer.
- 1 2. The method of claim 1, wherein, before annealing, the crystalline template has an initial
2 crystallographic orientation, and after annealing the annealed template has a final
3 crystallographic orientation different from the initial crystallographic orientation.
- 1 3. The method of claim 1, wherein the annealed template has a final crystallographic
2 orientation tilted away from (001) by a tilt angle.
- 1 4. The method of claim 3, wherein the tilt angle ranges from approximately 15° to
2 approximately 20°.
- 1 5. The method of claim 3, wherein the semiconductor layer has a crystallographic
2 orientation approximately equal to the final crystallographic orientation of the annealed template.
- 1 6. The method of claim 3, wherein the semiconductor layer has a crystallographic
2 orientation tilted away from (001) by an angle ranging from approximately 2° to approximately
3 8°.
- 1 7. The method of claim 6, wherein the semiconductor layer has a crystallographic
2 orientation tilted away from (001) by approximately 6°.
- 1 8. The method of claim 1, wherein a grain size of the annealed template is greater than
2 approximately 1 cm.
- 1 9. The method of claim 8, wherein a grain size of the annealed template is greater than
2 approximately 10 cm.

- 1 10. The method of claim 1, wherein a grain size of the annealed template is greater than
2 approximately ten times a thickness of the annealed template.
- 1 11. The method of claim 1, further comprising forming a semiconductor device on the
2 semiconductor layer.
- 1 12. The method of claim 11, wherein the semiconductor device comprises at least one polar
2 compound semiconductor material.
- 1 13. The method of claim 12, wherein the semiconductor layer comprises at least one non-
2 polar semiconductor material, and the semiconductor device is substantially free of anti-phase
3 boundaries.
- 1 14. The method of claim 1, wherein the buffer layer comprises at least one of Cr, Pd, Ir, an
2 oxide, or a nitride.
- 1 15. The method of claim 1, wherein the crystalline template comprises at least one of Cu, Ni,
2 or a Cu-Ni alloy.
- 1 16. A method for forming a semiconductor device, the method comprising:
2 providing a crystalline template having an initial grain size;
3 annealing the crystalline template, the annealed template having a final grain size larger
4 than the initial grain size;
5 forming a buffer layer over the annealed template; and
6 forming a semiconductor layer over the buffer layer,
7 wherein the crystalline template comprises a material substantially impervious to reaction
8 with at least one of As-containing gases or Si-containing gases at a temperature greater than
9 approximately 350 °C.
- 1 17. The method of claim 16, wherein the crystalline template comprises steel.
- 1 18. The method of claim 16, wherein, before annealing, the crystalline template has an initial
2 crystallographic orientation, and after annealing the annealed template has a final
3 crystallographic orientation different from the initial crystallographic orientation.

- 1 19. The method of claim 16, wherein the annealed template has a final crystallographic
2 orientation tilted away from (001) by a tilt angle.
- 1 20. The method of claim 19, wherein the tilt angle ranges from approximately 15° to
2 approximately 20°.
- 1 21. The method of claim 19, wherein the semiconductor layer has a crystallographic
2 orientation approximately equal to the final crystallographic orientation of the annealed template.
- 1 22. The method of claim 19, wherein the semiconductor layer has a crystallographic
2 orientation tilted away from (001) by an angle ranging from approximately 2° to approximately
3 8°.
- 1 23. The method of claim 22, wherein the semiconductor layer has a crystallographic
2 orientation tilted away from (001) by approximately 6°.
- 1 24. The method of claim 16, wherein a grain size of the annealed template is greater than
2 approximately 1 cm.
- 1 25. The method of claim 24, wherein a grain size of the annealed template is greater than
2 approximately 10 cm.
- 1 26. The method of claim 16, wherein a grain size of the annealed template is greater than
2 approximately ten times a thickness of the annealed template.
- 1 27. The method of claim 16, further comprising forming a semiconductor device on the
2 semiconductor layer.
- 1 28. The method of claim 27, wherein the semiconductor device comprises at least one polar
2 compound semiconductor material.
- 1 29. The method of claim 28, wherein the semiconductor layer comprises at least one non-
2 polar semiconductor material, and the semiconductor device is substantially free of anti-phase
3 boundaries.
- 1 30. A semiconductor structure comprising:
2 a substantially amorphous substrate layer;

3 a tilted buffer layer disposed over the substrate layer; and
4 a semiconductor layer disposed over the tilted buffer layer,
5 wherein at least one of the tilted buffer layer or the semiconductor layer has a grain size greater
6 than approximately 1 cm.

1 31. The semiconductor structure of claim 30, wherein a crystallographic orientation of at
2 least one of the tilted buffer layer or the semiconductor layer is tilted away from (001) by a tilt
3 angle.

1 32. The semiconductor structure of claim 31, wherein the tilt angle ranges from
2 approximately 15° to approximately 20°.

1 33. The semiconductor structure of claim 31, wherein the tilt angle ranges from
2 approximately 2° to approximately 8°.

1 34. The semiconductor structure of claim 33, wherein the tilt angle is approximately 6°.

1 35. The semiconductor structure of claim 31, further comprising a semiconductor device
2 disposed over the semiconductor layer.

1 36. The semiconductor structure of claim 35, wherein the semiconductor layer comprises a
2 non-polar semiconductor material, the semiconductor device comprises a polar semiconductor
3 material, and the semiconductor device is substantially free of anti-phase boundaries.

1 37. The semiconductor structure of claim 31, wherein a magnitude of a tilt away from a low-
2 index crystallographic direction of the semiconductor layer is less than a magnitude of a tilt away
3 from the low-index crystallographic direction of the tilted buffer layer.

1 38. A semiconductor structure comprising:
2 a template layer comprising a material substantially impervious to reaction with at least
3 one of As-containing gases or Si-containing gases at a temperature greater than approximately
4 350 °C;
5 an tilted buffer layer disposed over the template layer; and
6 a semiconductor layer disposed over the tilted buffer layer.

1 39. The semiconductor structure of claim 38, wherein at least one of the template layer, the
2 tilted buffer layer, or the semiconductor layer has a grain size greater than approximately 1 cm.

- 1 40. The semiconductor structure of claim 38, wherein the template layer comprises steel.
- 1 41. The semiconductor structure of claim 38, wherein a crystallographic orientation of at
2 least one of the template layer, the tilted buffer layer, or the semiconductor layer is tilted away
3 from (001) by a tilt angle.
- 1 42. The semiconductor structure of claim 41, wherein the tilt angle ranges from
2 approximately 15° to approximately 20°.
- 1 43. The semiconductor structure of claim 41, wherein the tilt angle ranges from
2 approximately 2° to approximately 8°.
- 1 44. The semiconductor structure of claim 43, wherein the tilt angle is approximately 6°.
- 1 45. The semiconductor structure of claim 38, further comprising a semiconductor device
2 disposed over the semiconductor layer.
- 1 46. The semiconductor structure of claim 45, wherein the semiconductor layer comprises a
2 non-polar semiconductor material, the semiconductor device comprises a polar semiconductor
3 material, and the semiconductor device is substantially free of anti-phase boundaries.
- 1 47. The semiconductor structure of claim 38, wherein the template layer is substantially
2 tilted.
- 1 48. The semiconductor structure of claim 38, wherein a grain size of the template layer is
2 greater than approximately ten times a thickness of the template layer.
- 1 49. The semiconductor structure of claim 38, wherein a magnitude of a tilt away from a low-
2 index crystallographic direction of the semiconductor layer is less than a magnitude of a tilt away
3 from the low-index crystallographic direction of the tilted buffer layer.

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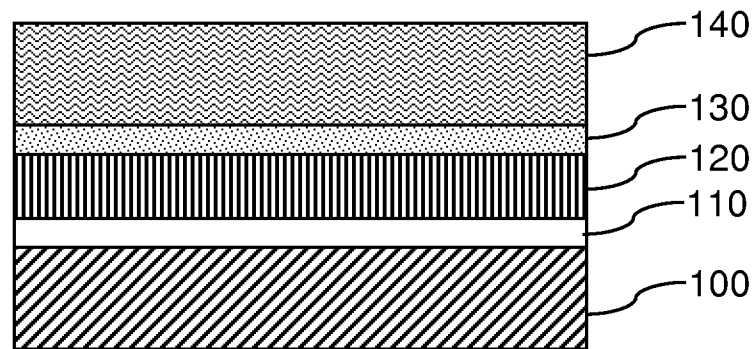


Fig. 1A

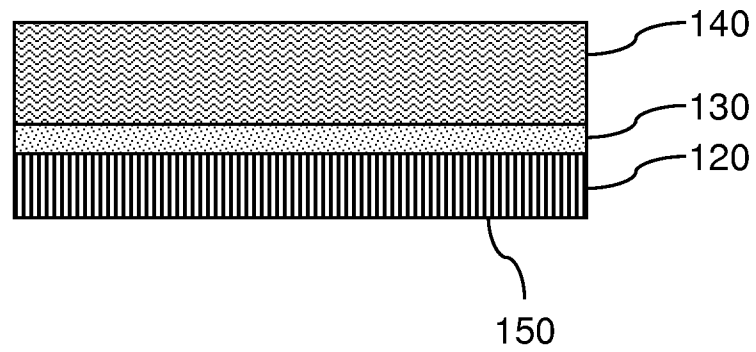


Fig. 1B

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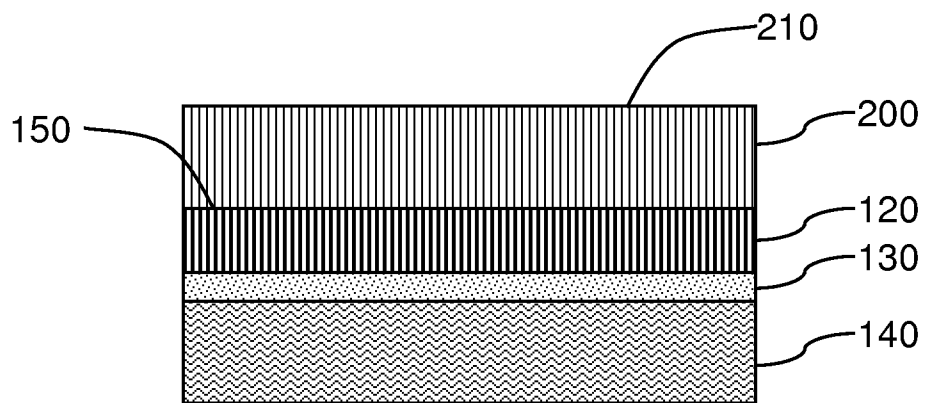


Fig. 2

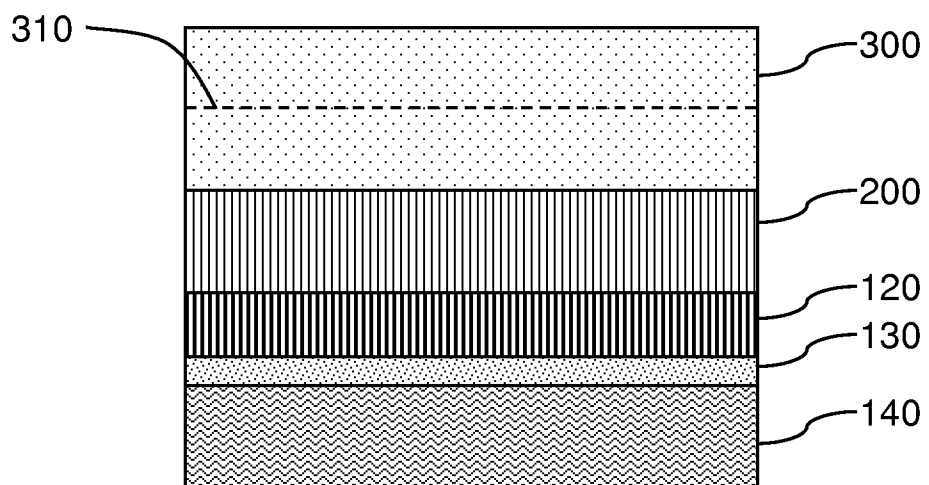


Fig. 3

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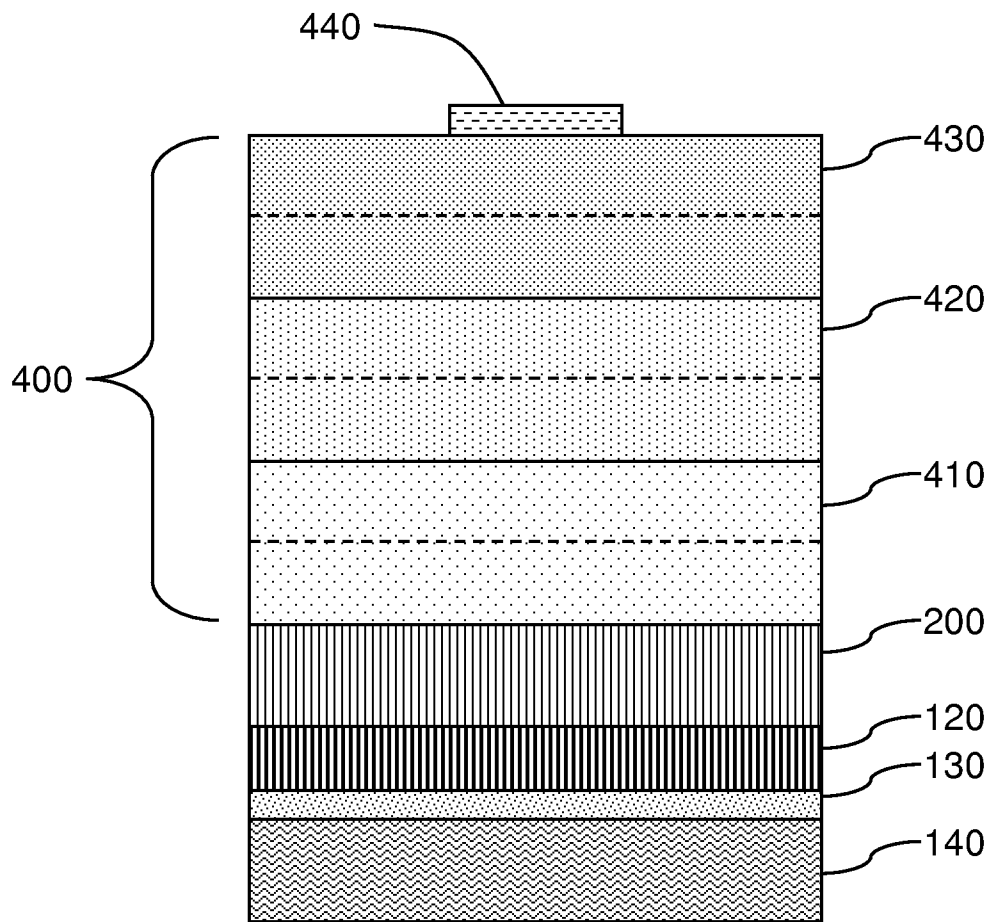


Fig. 4

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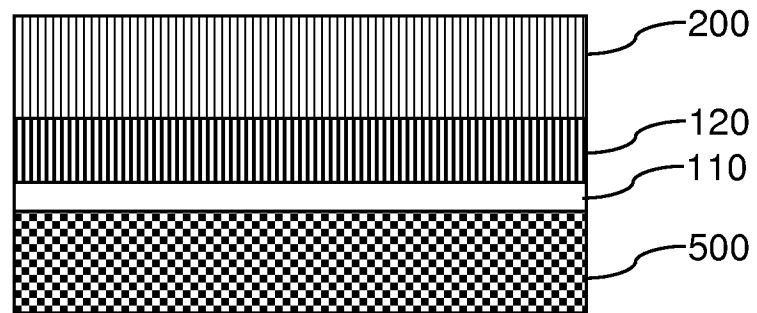


Fig. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/022381

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L21/20 H01L21/02
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/217622 A1 (GOYAL AMIT [US]) 11 September 2008 (2008-09-11) paragraphs [0080] - [0109], [0134] - [0136], [0147], [0158] - [0162], [0188]; figures 1,2,6-17, 23-29	1-49
X	US 2007/044832 A1 (FRITZEMEIER LESLIE G [US]) 1 March 2007 (2007-03-01) paragraphs [0014] - [0021], [0032] - [0080]; figures 1-7 ----- -/--	1,2, 8-12, 14-16, 18, 24-28, 38,39,48

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

28 May 2010

Date of mailing of the international search report

17/06/2010

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
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Fax: (+31-70) 340-3016

Authorized officer

Norga, Gerd

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/022381

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	R. W. Cahn and P. Haasen: "Physical Metallurgy" 1 January 1996 (1996-01-01), Elsevier Science, Amsterdam, XP002584210 ISBN: 0444898751 page 2482	1-15, 30-37
A	----- HUANG S H ET AL: "Simultaneous interfacial misfit array formation and antiphase domain suppression on miscut silicon substrate". APPLIED PHYSICS LETTERS AMERICAN INSTITUTE OF PHYSICS USA LNKD- DOI:10.1063/1.2970997, vol. 93, no. 7, 18 August 2008 (2008-08-18), pages 071102-1, XP002584211 ISSN: 0003-6951 the whole document	12,13
A	----- US 6 730 410 B1 (FRITZEMEIER LESLIE G [US] ET AL) 4 May 2004 (2004-05-04) the whole document -----	1-15, 30-37

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/022381

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-15, 30-37

A method for forming a semiconductor device and the corresponding semiconductor device, the method comprising: providing a crystalline template having an initial grain size; annealing the crystalline template, the annealed template having a final grain size larger than the initial grain size; forming a buffer layer over the annealed template; forming a substrate layer over the buffer layer; removing the annealed template to expose a surface of the buffer layer; and forming a semiconductor layer over the exposed surface of the buffer layer.

2. claims: 16-29, 38-49

A method for forming a semiconductor device and the corresponding semiconductor device, the method comprising: providing a crystalline template having an initial grain size; annealing the crystalline template, the annealed template having a final grain size larger than the initial grain size; forming a buffer layer over the annealed template; and forming a semiconductor layer over the buffer layer, wherein the crystalline template comprises a material substantially impervious to reaction with at least one of As-containing gases or Si-containing gases at a temperature greater than approximately 350 °C.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2010/022381

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 2008217622	A1	11-09-2008	WO	2008112115 A1	18-09-2008
US 2007044832	A1	01-03-2007	NONE		
US 6730410	B1	04-05-2004	NONE		