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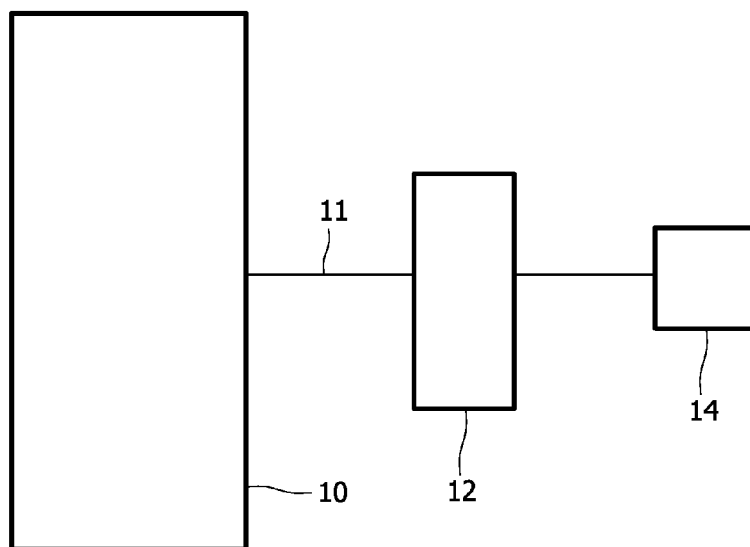
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(54) Title: ELECTRONIC CIRCUIT WHEREIN AN ASYNCHRONOUS DELAY IS REALIZED



(57) Abstract: The electronic circuit contains a basic delay circuit (14). A delay is realized by activating the same basic delay circuit (14) a plurality of times in response to a single start signal before generating a response to that start signal. A control circuit (12) receives a start signal and an outputs a response. The control circuit (12) causes a series of signals to be passed through the delay circuit (14), the series starting at a time that is time-continuously triggered by the start signal. Each successive signal in the series starts after a preceding signal has emerged from the delay circuit (12) and the series being terminated after a controlled number of more than one signal has been passed. The control circuit (12) supplies the response upon termination of the series. In one embodiment the series is realized by means of a handshake sequencing circuit (120) that generates a series of successive handshake transactions.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER

INV. H03K5/13

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	paragraph [0015] - paragraph [0048]; figures 2-4	2,10
A		3,7,8
Y	US 2004/140832 A1 (SHIAH CHUN [TW]) 22 July 2004 (2004-07-22)	2,10
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A	the whole document	2,3,6,10
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☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	TEMPLE S ET AL: "On-chip timing reference for self-timed microprocessor" ELECTRONICS LETTERS, IEE STEVENAGE, GB, vol. 36, no. 11, 25 May 2000 (2000-05-25), pages 942-943, XP006015282 ISSN: 0013-5194 the whole document -----	1-5,7,8, 11
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