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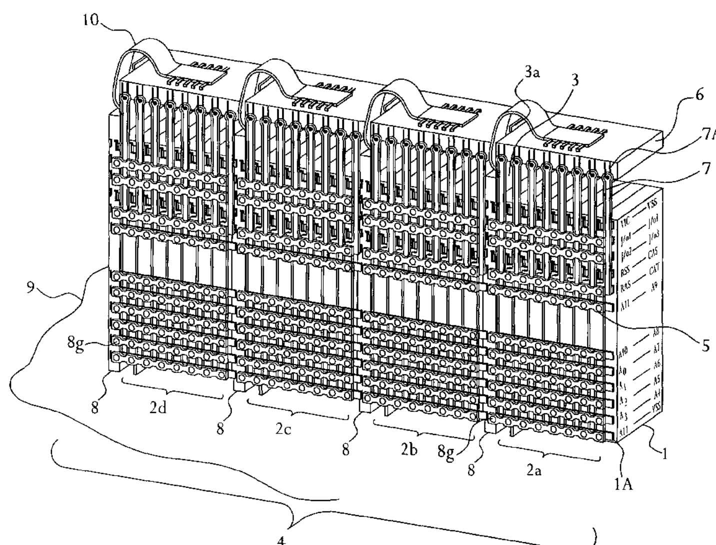
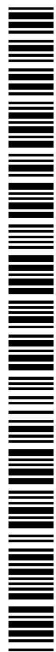
(54) Title: HIGH DENSITY PACKAGING OF ELECTRONIC COMPONENTS



(57) **Abstract:** Disclosed is an electronics packaging systems, which provides for a high density assembly of groups (2a, 2b, 2c, 2d) of similar solid state part packages. The system provides a novel method which includes the use of interconnect members (5) and crossover members (8) for interconnecting the signal paths, structurally assembling and supporting the parts (2a, 2b, 2c, 2d), and removing heat generated within the components (1). The system approach disclosed typically starts at the level of assembling pre-packaged parts (2a, 2b, 2c, 2d) into modules, and permeates through to the printed circuit board (6, 9) and box levels of assembly. The system is applicable, but not limited to, solid state memory device packaging, which typically consists of many similar parts interconnected in a matrix bus type configuration. The assembly of a building block of numerous memory components allows for the modular construction of large amounts of solid state memory.



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HIGH DENSITY PACKAGING OF ELECTRONIC COMPONENTS

Field of the Invention

The present invention relates generally to packaging of electronic
5 components and, more particularly, to apparatus and methods that achieve compact packaging of a plurality of similar electronic components by combining the components to form an interconnected module.

Background of the Invention

10 Large systems of many interconnected solid state devices, such as those found in solid state data recorders, require significant numbers of similar parts to be assembled and interconnected in a high density fashion. Typically, a designer attempts to assemble as many memory components, for example, on a single printed circuit board (PCB) as possible within architectural and other constraints, thus achieving increased
15 packing density, and increased utilization of the support or overhead electronics associated with each PCB. Increasing the number of memory devices on a single PCB also affects other overhead costs, such as structural and weight overhead associated with the PCB structure and its share of the box structure.

On one extreme, populating a PCB with a single layer of devices
20 represents a strictly two-dimensional approach, and the highest structural and support electronics overhead cost. By contrast, stacking multiple layers of devices on the same footprint improves the structural and support electronics overhead by supporting more components in basically the same space. Although the stacking approach is a departure from a strictly two-dimensional, or area, approach, it is not a true three-dimensional, or
25 volumetric, approach, since all interconnects between components must come down to the plane of the PCB.

Many approaches are known which stack bare die or modified packaged die to increase packing density. These approaches typically require special forms of the basic device, different from what is available as a mass-produced part. From an
30 economic and yield perspective, it is usually best to use a mass produced component as it is available from the supplier, in a standard package and in a pre-tested state. Changing packages, or handling bare die increases cost, and increases the risk of yield reduction for

the components. In a rapidly changing technological environment, the newest components are typically available only in the commercially mass produced form since the market usually consumes all that the factory can initially produce, and the manufacturer is unwilling to supply the device in any other form than that which is commercially available.

Therefore, it would be advantageous to designers of systems that require high density packaging of electronic components if a true three-dimensional approach were available to package commercially available electronic components in a high density fashion.

Summary of the Invention

The present invention satisfies these needs in the art by providing apparatus and methods for high density packaging of electronic components that make use of commercially packaged and pre-tested devices in a novel grouping and three dimensional interconnection method, creating a module or block of several components, aimed at maximizing usage of structural and electronics overhead. Achieving a compact block of components allows for mounting a large number of components on a given size PCB surface, thus minimizing the number of PCB's for a given piece of equipment, the overall size and weight of the equipment, and maximizing the usage of overhead functions on the PCB.

This approach also provides methods that can be used to assemble the components into modules such as those just described, and methods to assemble such modules onto PCB assemblies. The disclosed approach has the additional advantage that once an architecture is developed for a standard part, multiple suppliers can be used to supply the standard part, and future updates of the part can be substituted into the assembly.

Brief Description of the Drawings

The foregoing summary, as well as the following detailed description of the preferred embodiments, is better understood when read in conjunction with the appended drawings. For the purpose of illustrating the invention, there is shown in the drawings an embodiment that is presently preferred, it being understood, however, that

the invention is not limited to the specific apparatus and methods disclosed. In the drawings:

Figure 1A depicts a preferred embodiment of the present invention as applied to a 24-pin TSOP for DRAM;

5 Figure 1B depicts a typical electronic component that can be used in an interconnect system according to the present invention;

Figure 1C depicts an interconnect ribbon that can be used in an interconnect system according to the present invention;

Figure 1D depicts a cross-over device that can be used in an interconnect

10 system according to the present invention;

Figure 2 depicts a preferred embodiment of the present invention in which the packaging methods have been replicated many times to package an increased number of components into a group;

Figure 3A depicts a preferred embodiment of the present invention in

15 which a thin insulative material with specific conductive paths is assembled to a solid state component and electrically interconnected with the component;

Figure 3B depicts an interconnect ribbon that can be used in an interconnect system according to the present invention; and

Figure 4 depicts another preferred embodiment of the present invention

20 which includes a thin insulative layer of material having specific conductive paths.

Detailed Description of Preferred Embodiments

Figure 1A depicts a preferred embodiment of the present invention

25 wherein the inventive grouping and interconnect method is applied to a 24-pin, thin small outline package (TSOP) for dynamic random access memory (DRAM). Although DRAM chips are shown by way of example, it should be understood that the invention can be applied to many other types of electronic components, such as, for example, VRAMS, FLASH ROMs, EPROMS, SRAMS, programmable logic arrays (PLAs),

30 microprocessors (CPUs), coprocessors, and other related integrated circuit elements.

As shown in Figure 1A, a plurality of subgroups 2a-d are bonded together to form a group or module 4. Each subgroup 2a-d includes a plurality of commercially

packaged electronic components 1, such as DRAM chips, for example.

Figure 1B depicts a typical electronic component 1 that can be used in accordance with the present invention. As shown, component 1 has a first face 1a, a second face 1b opposite first face 1a, a first end 1c extending between first face 1a and second face 1b, a second end 1d opposite first end 1c, a first side 1e extending between first face 1a and second face 1b, and a second side 1f opposite first side 1e. A set of one or more leads 1g extends from first side 1e of component 1, and a second set of one or more leads 1g extends from second side 1f of component 1.

Preferably, leads 1g are arranged as linear arrays on each side 1e, 1f of component 1, and are formed as so-called "gull wing" leads, which are typically used in surface-mount applications. Alternatively, 1g could be formed as L-shaped leads, for example, which are typically used in through-mount applications. In general, however, leads 1g can have any shape, or be formed with any desired custom feature. Gull wing leads are preferred for reasons that will be discussed in detail below. For purposes of clarity, it should be understood that, in typical prior art applications, components 1 would be mounted to a substrate, such as a printed circuit board, with second face 1b adjacent the substrate, regardless of whether the components were mounted individually, or in a stacked configuration. Thus, second face 1b is typically considered to be the "bottom" of the chip.

With reference once again to Figure 1A, a plurality of components 1 are arranged in a stacked configuration such that the second face of each component 1 is adjacent the first face of the adjacent component. With the plurality of components 1 arranged as such, the leads on each side of the subgroup form respective lead arrays that define respective lead planes on each side of module 4. Note that the lead planes are generally parallel to the planes defined by the respective sides of the components. Significantly, and in contradistinction to known prior art devices, the interconnect system of the present invention can be mounted to one or more PCBs such that the ends of the electronic components are proximate the substrates, rather than the bottoms.

It is well known that electronic components generate heat, and that, unless excess heat is drawn away from the components, the components can overheat, and possibly malfunction as a result. In many applications, the environment in the immediate vicinity of the components is nearly as hot as the components themselves, and, therefore,

the heat will not dissipate naturally from the components. In many such applications, cooling devices such as fans are used to circulate the air, but in some cases such cooling devices are undesirable due to space limitations or other design considerations.

To address the problem of component overheating, the interconnect system of the present invention preferably includes one or more thermally conductive members 3 that serve to conduct heat generated in the components 1 out of module 4 to a heat sink (not shown), which is located away from the stack. Preferably, thermal member 3 is stamped from a sheet of thermally conductive material, such as aluminum or copper, for example, and is bonded to one or more electronic components via thermally conductive epoxy. Thermal member 3 can be bonded either between two components 1 or at the end of a subgroup 2, and there can be any ratio of components 1 to thermal members 3, depending on the needs of the particular application.

Preferably, thermal member 3 is about 50 mils thick, and is about as wide as the component(s) to which it is bonded. Preferably, thermal member 3 is somewhat longer than the component(s) to which it is bonded so that heat generated by the component(s) is carried away from the stack. For example, thermal member 3 can include one or more tabs 3a that extend away from the components to the heat sink.

The heat sink can be merely a location away from the stack where the ambient temperature is lower, or it can be a physical element, such as a metalization area on a PCB, for example. Such a metalization layer can be formed, for example, by depositing layers of a metal, such as copper, for example, on the side of the PCB. Alternatively or additionally, the system can also include thermally conductive bars, made from a material such as aluminum, for example, that connect across a plurality of tabs 3a to carry excess heat away from module 4. This approach is particularly useful in an application where several modules 4 are aligned side by side on the same PCB, with the thermally conductive bars extending across two or more modules. Thus, thermal members 3 permit heat generated by electronic components 1 to be drawn away from module 4. It should be understood that thermally conductive members 3 can also provide structural support to the stack.

Preferably, the plurality of electronic components 1 are bonded together using a thermally conductive epoxy. The use of a thermally conductive epoxy to bond the components to one another is preferred because it will tend to draw heat generated by

the individual components 1 through the stack to thermally conductive member 3, which, as just described, carries the heat away from the stack.

Each sub-group 4 also includes one or more electrically conductive interconnection members or ribbons 5. Each ribbon 5 is coupled to each of a plurality of
5 selected component leads 1g to form a bus type interconnect between the components 1 that form the subgroup. Interconnection member 5 serves to interconnect the selected leads 1g, that is, to make all the selected leads 1g electrically the same. Preferably, the plurality of components 1 are all of the same type (*e.g.*, all DRAMs) and, consequently, all have the same lead configuration (*e.g.*, the leads are aligned in linear arrays on both
10 sides of the components). Preferably, each ribbon is connected to the same respective lead for each of the components. For example, as shown in Figure 1A, each DRAM chip has an A11 lead, and the ribbon designated by reference numeral 5 interconnects all of the A11 leads for subgroup 2a.

In general, the number of components 1 that form a subgroup 2 is
15 variable, and interconnect member 5 can extend across as many leads 1g as desired. In practice, however, because interconnect member 5 serves as a signal bus between the components, the number of components 1g that can be interconnected by one ribbon 5 is typically limited by signal losses that increase as the length of ribbon 5 increases. Thus, the number of components that form a subgroup 2 can be based on certain design
20 considerations such as signal losses that can be tolerated in the bus line so that the component at end of bus line gets enough voltage or does not suffer too much timing loss.

Other design considerations, such as the desired system architecture, can also influence the number of components 1 that form a subgroup 2. For example, an
25 architecture that is favorable for fault tolerances can be chosen wherein the collection of devices can operate at a reduced level in the event of a single device failure. The ability to draw sufficient excess heat away from module 4 can also affect the number of components.

Preferably, interconnect member 5 is both physically and electrically
30 connected to each of the selected leads. To accomplish this, the present invention provides a unique interconnect ribbon design that enables the manufacturer of the interconnect system to more easily build the device. As shown in Figure 1C, an

interconnect ribbon 5 according to the present invention is generally elongated, and includes a plurality of spring clips or other such ribbon connection members 5a, which are spaced along the length of ribbon 5.

Each ribbon connection member 5a is sized and shaped to clip onto one of
5 the selected leads 1g to which ribbon 5a is to be connected. Preferably, spring clips 5a include solder application holes 5b as shown. Thus, ribbon 5 can be clipped onto the selected leads and thereby held in place temporarily until a solder drop can be deposited through each solder application hole 5b to secure ribbon 5 to leads 1g. Thus, stable physical and electrical connections can be established between ribbon 5 and each of the
10 selected leads 1g. This design also lends itself to automated soldering techniques, such as wave soldering, for example.

According to the present invention, each sub-group 2a-2d also includes a crossover member 8, which is attached to the respective sub-group 2. Each crossover member 8 provides interconnectivity between an interconnect member 5, and one or both
15 of a main PCB or "motherboard" 9 and a support PCB or "daughterboard" 6. In general, the PCBs 6, 9 can include multiple layers of interconnect and active electronic components. Preferably, one or both of the PCBs 6, 9 is attached to thermal members 3 for structural support of the system, and for thermal sinking.

Basically, from an interconnection perspective, crossover member 8
20 mimics the electronic components that form the subgroup 2. Preferably, as shown in Figure 1D, crossover member 8 includes a housing having an interior region formed by a first face 8a, a second face 8b opposite first face 8a, a first end 8c extending between first face 8a and second face 8b, a second end 8d opposite first end 8c, a first side 8e extending between first face 8a and second face 8b, and a second side 8f opposite first
25 side 8e. Each side 8e, 8f of crossover member 8 includes a linear array of leads 8g, which mimics the linear array of leads 1g on each side 1e, 1f of the electronic components 1. Thus, as shown in Figure 1A, interconnect member 5 can be electrically and physically connected to crossover member 8 in the same manner as it is connected to the selected leads 1g of the electrical components 1 that form subgroup 2.

30 Preferably, as shown in Figure 1A, crossover member 8 is coupled to one or more PCBs, such as support PCB 6 or main PCB 9, for example, via a flexible interconnect ribbon 10. Within the interior region of crossover member 8, circuit paths

can be arranged in any desired fashion to route signals between the interconnect members 5 and the PCB(s) (or between multiple interconnect members). Signals present on PCB 6, for example, can then drive, via crossover member 8, the bus type interconnect formed by the connections between ribbon 5 and leads 1g. Thus,
5 components on the PCB(s) can communicate with electrical components 1. Thus, a device on support PCB 6, for example, can send a signal through interconnect member 10, through crossover member 8, through interconnect ribbon 5, to the leads designated A11 on all of the components 1 that form a particular subgroup 2.

It should be understood that, in certain applications, it is desirable to
10 convey certain signals between one or more devices on one of the PCBs and a specified, individual lead on one of the components 1, without the signals being conveyed to all of the corresponding leads on all of the other components 1 that form the subgroup. That is, the designer will not always want signals traveling between the substrate and the subgroup to be transported via ribbon interconnect 5. Therefore, as shown in Figure 1,
15 support PCB 6, for example, can also interconnect with individual component leads via a conductive member 7, which attaches from support PCB 6 to a selected lead 1g of a selected component 1. The interconnect system of the present invention can include any number of conductive members 7, or none at all, depending on the requirements of the particular application.

20 Conductive members 7 are preferably thin and elongated, as shown, although they may be of a flex circuit design. Conductive members 7 can be stamped out of a sheet of conductive material, such as aluminum or copper, and may be covered with insulation. Each conductive member 7 is electrically connected to a device on the PCB to which the conductive member 7 is physically connected. Traces 7a interconnect
25 conductive member 7 to devices (not shown) on PCB 6. Thus, conductive member 7 can be electrically and physically connected to only one lead, with no connections to other leads of the same component or of other components in the subgroup 2. Consequently, the interconnect system of the present invention allows for some leads to be connected bus style, while others can be addressed individually.

30 The addition of conductive members 7 is particularly desirable for purposes of controlling individual components. For example, a device on PCB 6 can control a specified component by conveying a control signal via conductive member 7 to

the specified component, which causes the specified component to read a data signal traveling on the bus formed by ribbon interconnect 5. It should be understood that, alternatively or additionally, one or more conductive members 7 can interconnect with individual leads with main PCB 9.

5 Thus, in contradistinction to known prior art devices, an interconnect system according to the present invention is a true 2D to 3D converter. That is, the inventive interconnect system does not restrict signal flow to a particular plane, but rather, allows the signals to change direction. For example, the interconnect system permits a signal traveling in the plane defined by interconnect ribbon 5 to be diverted 10 between the plane formed by support PCB 6 and the plane defined by interconnect ribbon 5. As these planes are not necessary parallel, and can even be orthogonal, the interconnect system of the present invention is a true three-dimensional system.

A shown in Figure 2, the above-described approach can be replicated as many times as necessary to package any desired number of components 1 into a group 4. 15 Any number of groups 4 can be assembled on the surface of a base PCB 9 to achieve high-density packaging and maximum overhead utilization of base PCB 9, and thereby, to maximize the use of overhead electronics resident on base PCB 9. Interconnection between base PCB 9 and support PCB 6 can be accomplished by the use of flexible circuitry, as well as across multiple support PCBs.

20 Techniques by which the modules described above can be made include well known automated solder reflow and solder wave techniques, which can be modified as necessary to satisfy the requirements of a specific application. Also, automated techniques by which a plurality of chips can be stacked and bonded are also known.

Figure 3A depicts another preferred embodiment of the present invention, 25 which is particularly suitable for applications wherein the electronic components 1 have small lead pitches (*i.e.*, the distance between leads). In some cases, the lead pitches can be small enough to cause practical difficulties in attaching a ribbon interconnect, such as ribbon interconnect 5 described in detail above. In such circumstances, as shown in Figure 3, a substrate or pad 11, which can be made of a thin insulative material, for 30 example, can be assembled to an electronic component 12, as by bonding with epoxy, for example. Pad 11 includes a conductive trace 13 that corresponds to each lead 12g, and to which the leads 12g are soldered or otherwise electrically connected.

A plurality of pads 11 can then be electrically interconnected to form an interconnect system as described above via one or more thin, bus-type interconnects 15, such as wires, for example. A particularly preferred interconnect 15 is shown in Figure 3B. Interconnect 15 includes a first elongated portion 15a, which can be a wire, for
5 example, and a plurality of notched connection members 15b, having notches 15c that are sized, shaped, and positioned to correspond to notches 11a at interface locations 11b on pad 11. Interconnect 15 can then be placed against pad 11 such that notches 15c line up with notches 11a, and soldered to form an electrical and physical connection. Thus, interface locations 11b contain features which allow interconnection with conductors
10 acting perpendicular to the insulator plane, and serve to interconnect multiple stacked components in a similar fashion as that shown in Figure 2. Electrical support components (not shown) can also be mounted to pad 11.

The interface features can also serve to connect individual conductor paths to specific locations on adjacent PCBs. For example, traces 17 can serve the same
15 purpose as conductive members 7 described above for controlling individual leads of specified components.

Figure 4 depicts still another preferred embodiment of the present invention which includes a thin insulating layer of material 24 having specific conductive paths 26 (electrical and thermal). Layer 24 is elongated in one or more directions to
20 allow multiple devices 25 to be attached and interconnected, and to allow positioning of the multiple devices into an effective stack. Electrical support components (not shown) can also be mounted to the insulating layer and connected to the conductor circuit. Conductive paths 26 can also route to selected interface locations 26a on the periphery of insulating material 24.

25 Thus there have been described apparatus and methods for high density packaging of electronic components. Those skilled in the art will appreciate that numerous changes and modifications may be made to the preferred embodiments of the invention and that such changes and modifications may be made without departing from the spirit of the invention. It is therefore intended that the appended claims cover all such
30 equivalent variations as fall within the true spirit and scope of the invention.

I claim:

1. A high density electronic interconnect system, comprising:
a plurality of electronic components, each having a plurality of leads, the
5 plurality of electronic components positioned adjacent to one another such that the leads define a lead plane;
an electrically conductive interconnect member that is electrically coupled to a respective lead from each of the electronic components; and
a cross-over device that is electrically coupled to the interconnect member
10 and adapted to carry electrical signals between the interconnect member and a signaling source.

2. The interconnect system of claim 1, wherein the interconnect member defines a first plane, and the cross-over device is adapted to be coupled to a substrate that
15 defines a second plane that is at a nonzero angle to the first plane.

3. The interconnect system of claim 1, wherein the cross-over device is adapted to be coupled to the signaling source via a flexible ribbon extending from an end of the cross-over device.
20

4. The interconnect system of claim 1, wherein the cross-over device has at least one lead, and the interconnect member is electrically coupled to the at least one lead.

25 5. The interconnect system of claim 1, wherein the cross-over device has a plurality of leads, and is disposed relative to the plurality of electronic components such that the leads of the cross-over device are in the lead plane.

6. The interconnect system of claim 1, further comprising:
30 a second electrically conductive interconnect member that is electrically coupled to a second respective lead from each of the electronic components,
wherein the cross-over device is adapted to carry electrical signals

between the interconnect ribbons.

7. The interconnect system of claim 1, wherein at least one the electronic components has a control lead, the interconnect system further comprising:

5 an electrically conductive control member that is electrically coupled to the control lead and adapted to electrically couple the at least one electronic component to a control signal source.

8. The interconnect system of claim 1, further comprising:

10 a thermally conductive member coupled to the plurality of electronic components and extending beyond an end of at least one of the electronic components.

9. The interconnect system of claim 8, wherein the thermally conductive member is stamped from a sheet of thermally conductive material, and includes a tab that

15 extends beyond the end of the at least one electronic component.

10. The interconnect system of claim 1, wherein the electronic components are affixed to one another via a thermally conductive epoxy.

20 11. A high density electronic interconnect system, comprising:

a plurality of electronic components, each having a plurality of leads;

an electrically conductive interconnect member that is electrically coupled to a respective lead from each of the electronic components and defines a first plane; and

a cross-over device that is electrically coupled to the interconnect member

25 and adapted to be coupled to a substrate that defines a second plane.

12. An interconnect ribbon for a high density electronic interconnect system, comprising:

an electrically conductive elongated member, and

30 a plurality of electrically conductive lead connection members disposed along a length of the elongated member, each said spring clip being adapted to couple the interconnect member to a respective lead of an electronic component.

13. The interconnect ribbon of claim 12, wherein the lead connection members are spring clips.

5 14. The interconnect ribbon of claim 12, further comprising a plurality of solder holes disposed along the length of the elongated member and extending therethrough via which the interconnect ribbon can be soldered to the respective lead.

15. A high density electronic interconnect system, comprising:

10 a plurality of electronic components, each said electronic components having a plurality of leads and being mounted to a respective substrate, each said substrate having a respective trace corresponding to each said lead and extending from the corresponding lead to an edge of the substrate; and

an electrically conductive interconnect member that is electrically coupled

15 to a respective lead from each of the electronic components via the traces corresponding to the respective leads.

16. The interconnect system of claim 15, wherein the traces extend to notches at the edge of the substrate.

20

17. The interconnect system of claim 15, wherein the interconnect member includes an elongated portion and a plurality of connection members disposed along a length of the elongated portion, each said connection member adapted to engage the edge of the substrate and establish electrical contact with a corresponding trace.

25 18. The interconnect system of claim 17, wherein the traces extend to notches at the edge of the substrate, and each said connection member includes a notch that is adapted to engage a corresponding notch at the edge of the substrate.

19. The interconnect system of claim 15, wherein the substrates are portions

30 of a flexible ribbon and the interconnect member is an electrically conductive trace disposed on the flexible ribbon.

20. A method for manufacturing a high density electronic interconnect system, the method comprising:

bonding together a plurality of electronic components, each said electronic component having a plurality of leads, such that the plurality of electronic
5 components are positioned adjacent to one another and the leads define a lead plane;

electrically coupling an electrically conductive interconnect member to a respective lead from each of the electronic components; and

electrically coupling to the interconnect member a cross-over device that is adapted to carry electrical signals between the interconnect member and a signaling
10 source.

21. The method of claim 20, further comprising:

coupling the interconnect member to the electronic components and the cross-over device such that the interconnect member defines a first plane, and the cross-
15 over device can be coupled to a substrate that defines a second plane that is at a nonzero angle to the first plane.

22. The method of claim 20, further comprising:

coupling to the interconnect member to a cross-over device that is adapted
20 to carry electrical signals between the interconnect member and a signaling source via a flexible ribbon extending from an end of the cross-over device.

23. The method of claim 20, wherein coupling the interconnect member to the cross-over device comprises electrically coupling the interconnect member to a lead of
25 the cross-over device.

24. The method of claim 20, further comprising:

electrically coupling a second electrically conductive interconnect member to the cross-over device and to a second respective lead from each of the
30 electronic components, such that the cross-over device can carry electrical signals between the interconnect ribbons.

25. The method of claim 20, further comprising:

electrically coupling an electrically conductive control member to a control lead of at least one of the electronic components, the control member being adapted to electrically couple the at least one electronic component to a control signal
5 source.

26. The method of claim 20, further comprising:

coupling a thermally conductive member to a least one of the electronic components such that the thermally conductive member extends beyond an end of the at
10 least one electronic component.

27. The method of claim 20, wherein bonding together the plurality of electronic components comprises affixing the electronic components to one another via a thermally conductive epoxy.

15

28. The method of claim 20, wherein coupling the electrically conductive interconnect member to the respective leads comprises soldering the interconnect member to the respective leads.

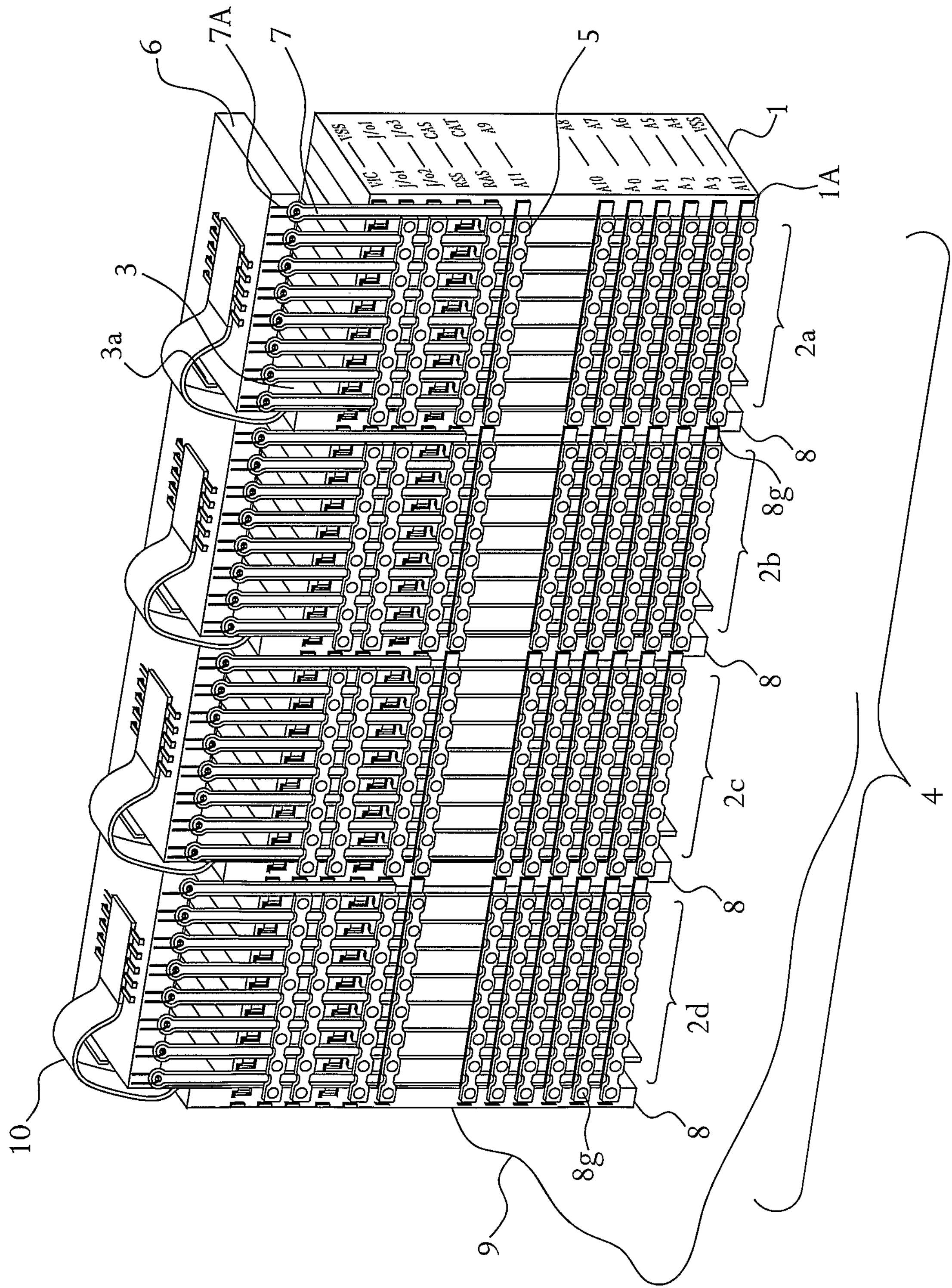


FIG. 1A

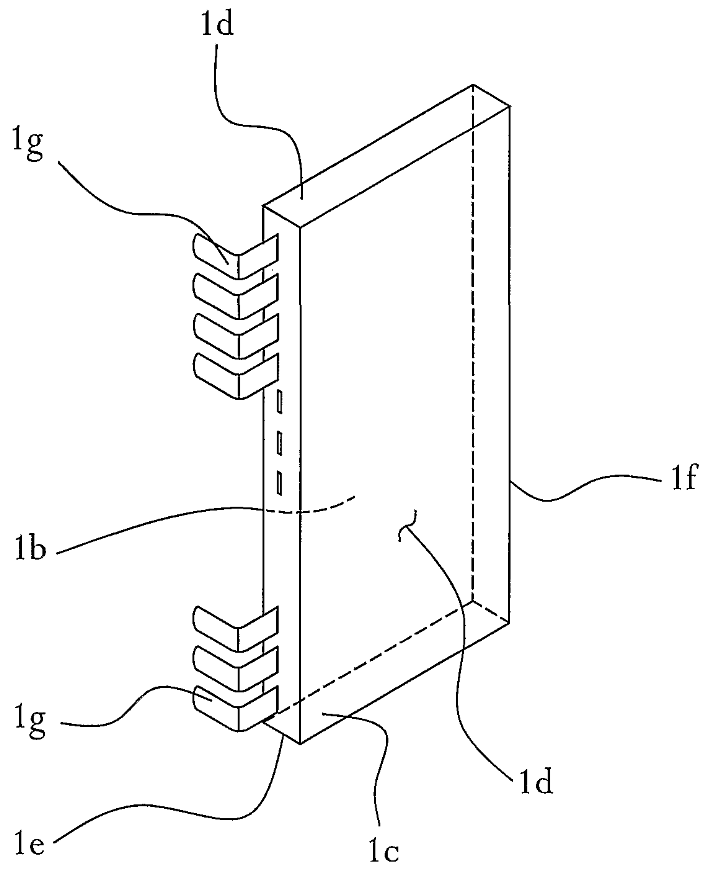


FIG. 1B

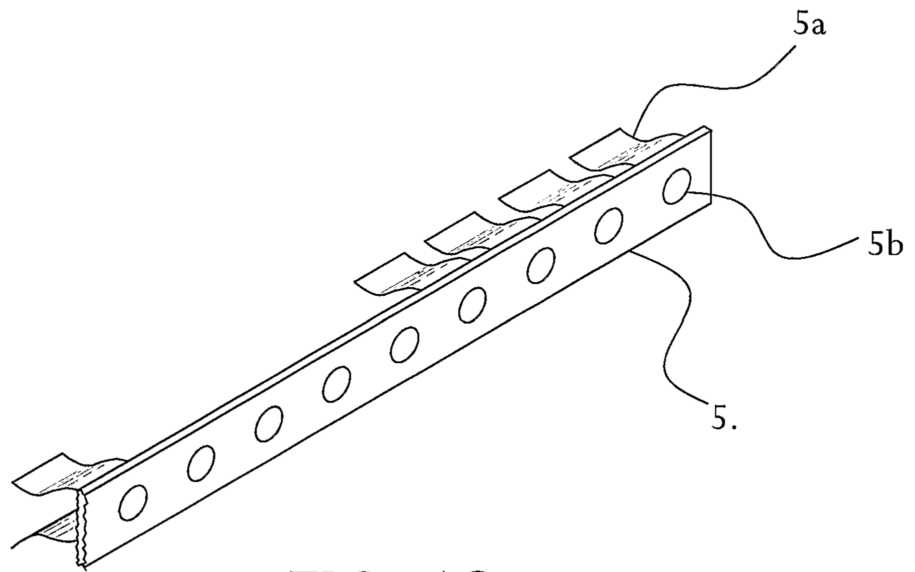


FIG. 1C

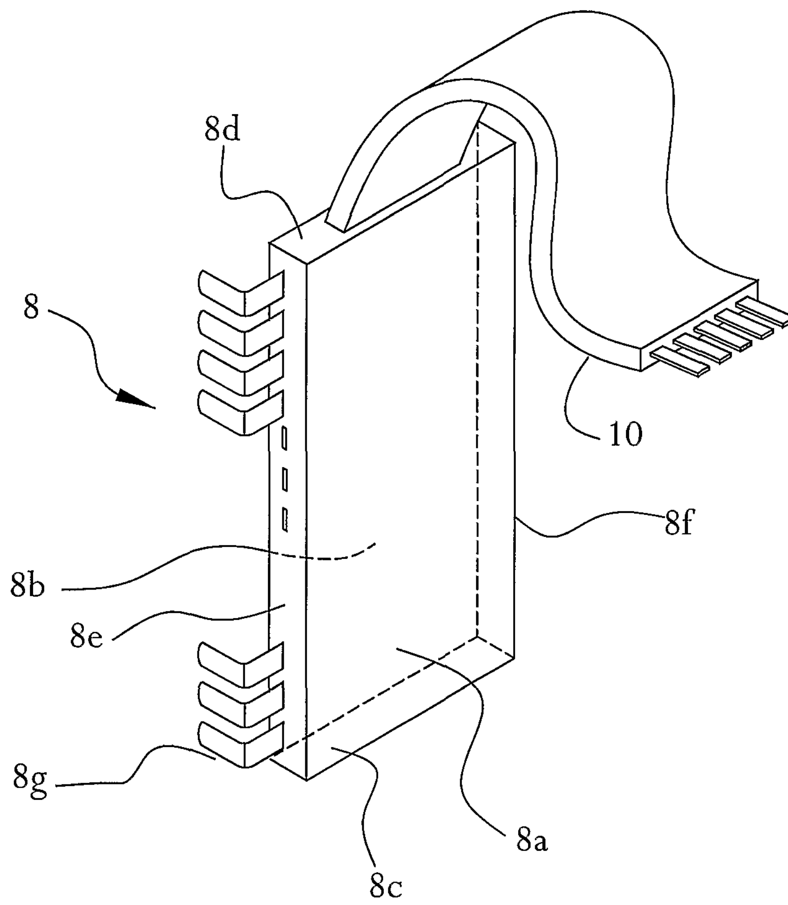


FIG. 1D

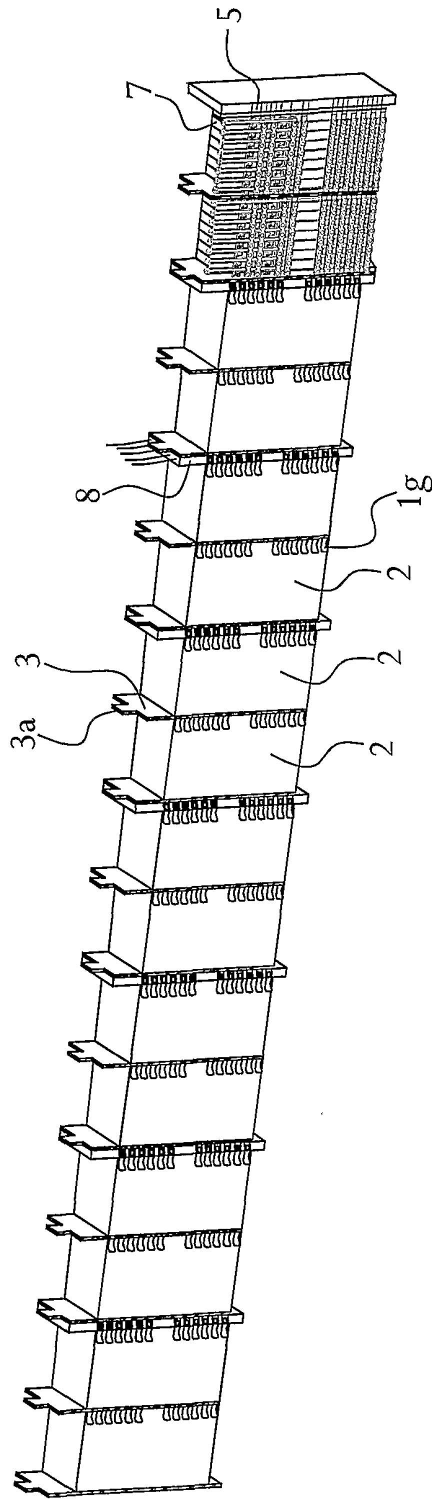


FIG. 2

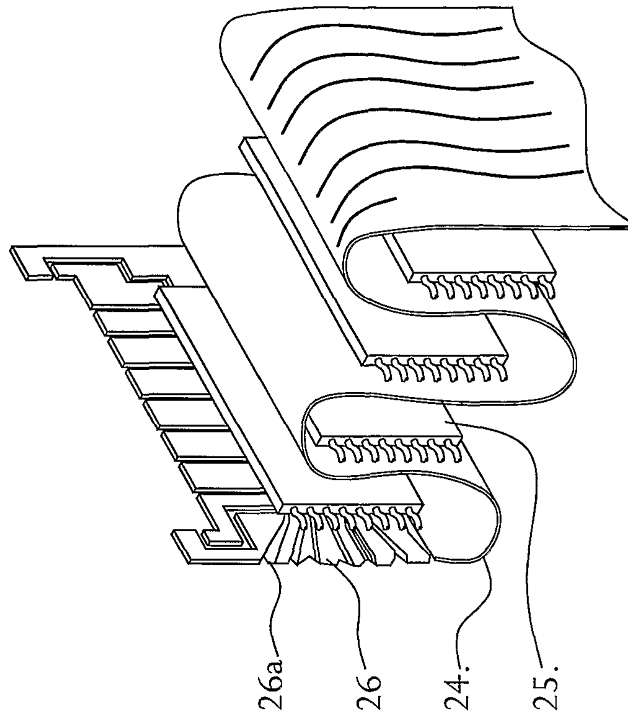


FIG. 4

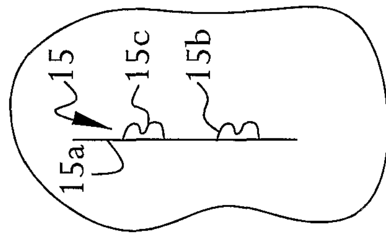


FIG. 3B

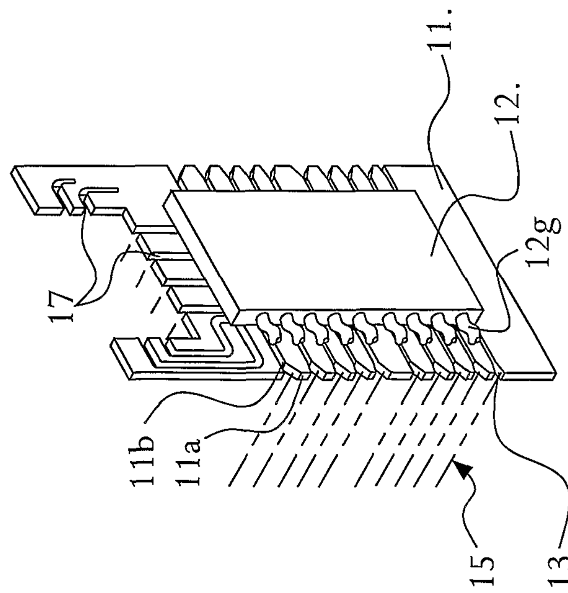
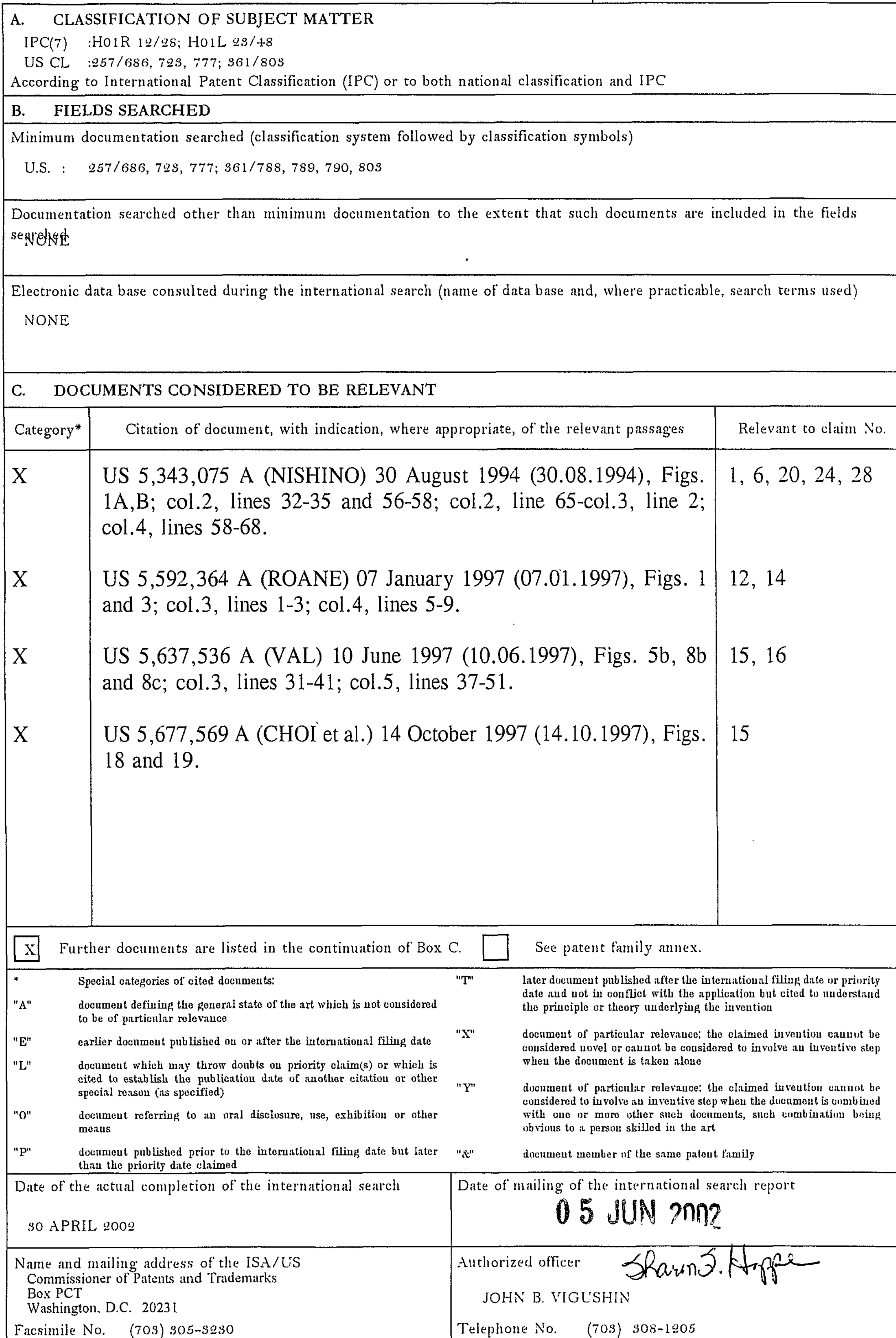


FIG. 3A



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/05594

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01R 12/28; H01L 23/48
US CL :257/686, 723, 777; 361/803
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/686, 723, 777; 361/788, 789, 790, 803

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,343,075 A (NISHINO) 30 August 1994 (30.08.1994), Figs. 1A,B; col.2, lines 32-35 and 56-58; col.2, line 65-col.3, line 2; col.4, lines 58-68.	1, 6, 20, 24, 28
X	US 5,592,364 A (ROANE) 07 January 1997 (07.01.1997), Figs. 1 and 3; col.3, lines 1-3; col.4, lines 5-9.	12, 14
X	US 5,637,536 A (VAL) 10 June 1997 (10.06.1997), Figs. 5b, 8b and 8c; col.3, lines 31-41; col.5, lines 37-51.	15, 16
X	US 5,677,569 A (CHOI et al.) 14 October 1997 (14.10.1997), Figs. 18 and 19.	15

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
30 APRIL 2002	05 JUN 2002

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/05594

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 6,153,929 A (MODEN et al.) 28 November 2000 (28.11.2000), Figs. 1-6; col.3, lines 22-25; col.5, lines 26-34 and 59-67; col.6, lines 41-46. ------- Fig. 12; col.7, lines 58-62; col.8, lines 1-7.	1, 6, 7, 20, 24, 25 -------- 3, 4, 11
Y	US 5,764,497 A (MIZUMO) 09 June 1998 (09.06.1998), Figs. 1-3; col.2, lines 40-44.	3, 4, 11