

[54] **FUNCTION GENERATOR**
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[22] Filed: **Dec. 7, 1970**
[21] Appl. No.: **95,550**

3,435,196 3/1969 Schmid.....235/150.53
3,513,301 5/1970 Howe235/150.53
3,529,138 9/1970 Andre et al.....235/150.53
3,557,347 1/1971 Robertson235/150.53

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[52] U.S. Cl.....235/197, 235/150.53
[51] Int. Cl.....G06g 7/36
[58] Field of Search.....235/197, 150.53, 150.3, 183,
235/152; 340/347 D-347 A; 307/229;
328/142

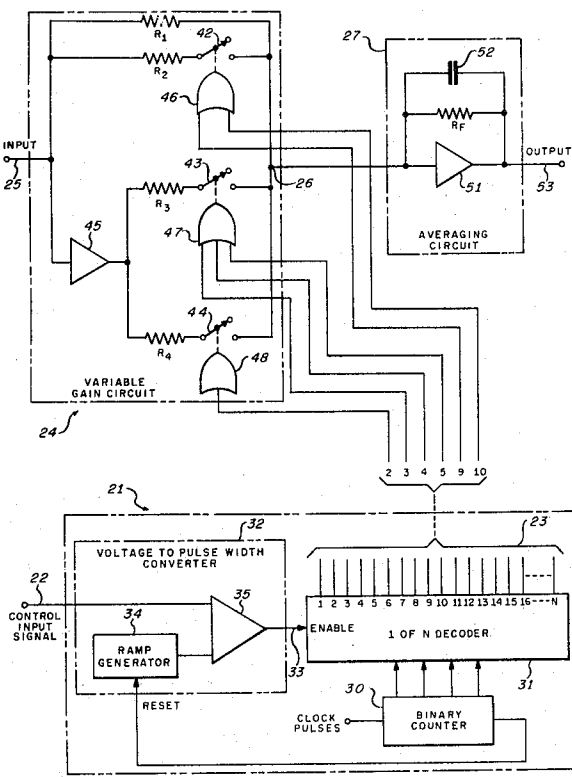
[56] **References Cited**

UNITED STATES PATENTS

3,226,641 12/1965 Miller235/197 UX
3,345,505 10/1967 Schmid.....235/197
3,506,810 4/1970 Katell235/150.53

[57] **ABSTRACT**
The invention comprises a means for providing a non-linear function. A first independent variable signal may be applied to a multiple switch variable gain circuit. A second independent variable signal, after being weighted by pulse width techniques in a sequencing circuit, controls the switching function of the variable gain circuit. The resultant signal is averaged and the output signal represents the first independent variable signal as a function of the second independent variable signal.

11 Claims, 2 Drawing Figures



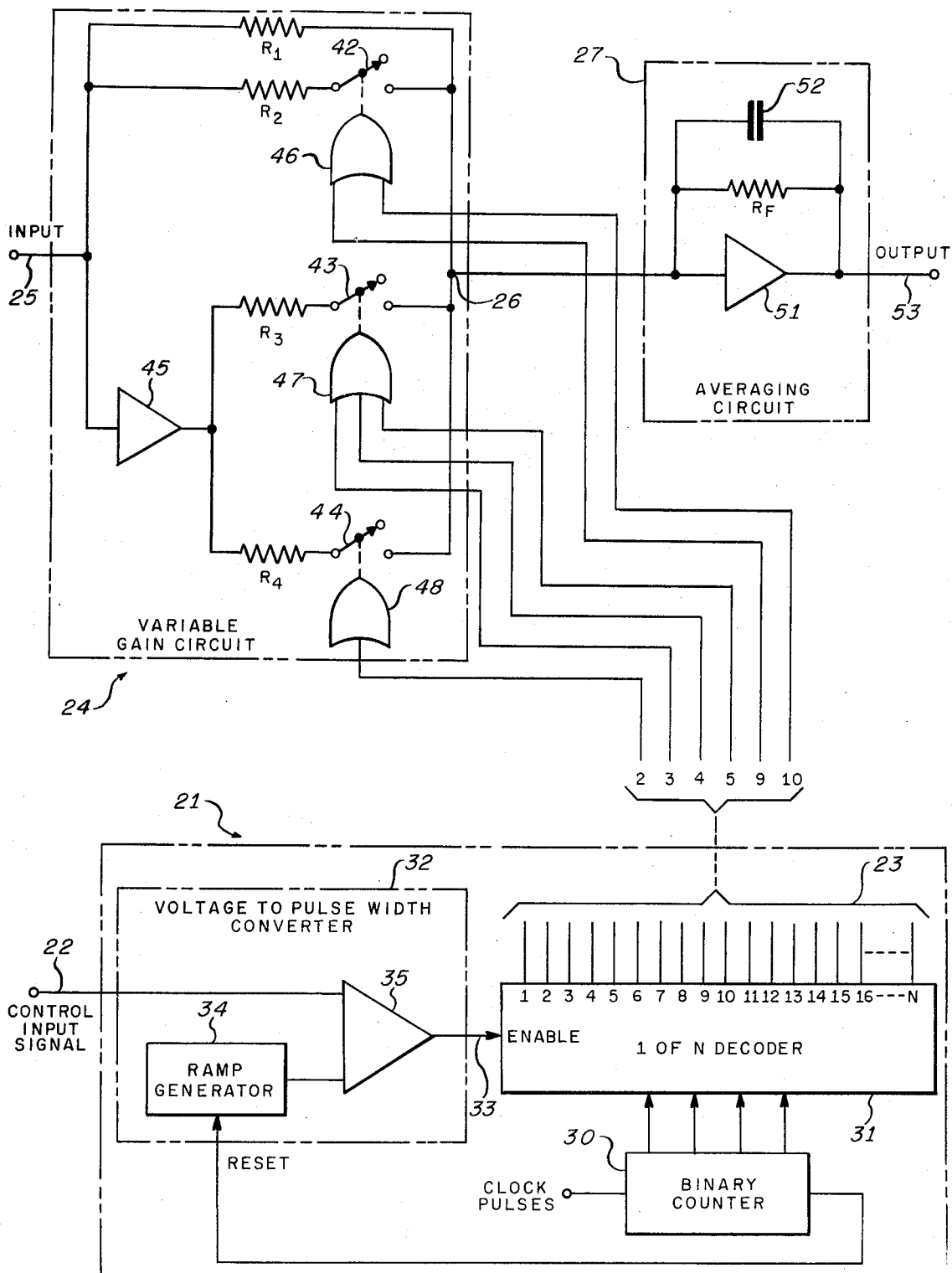


FIG.1.

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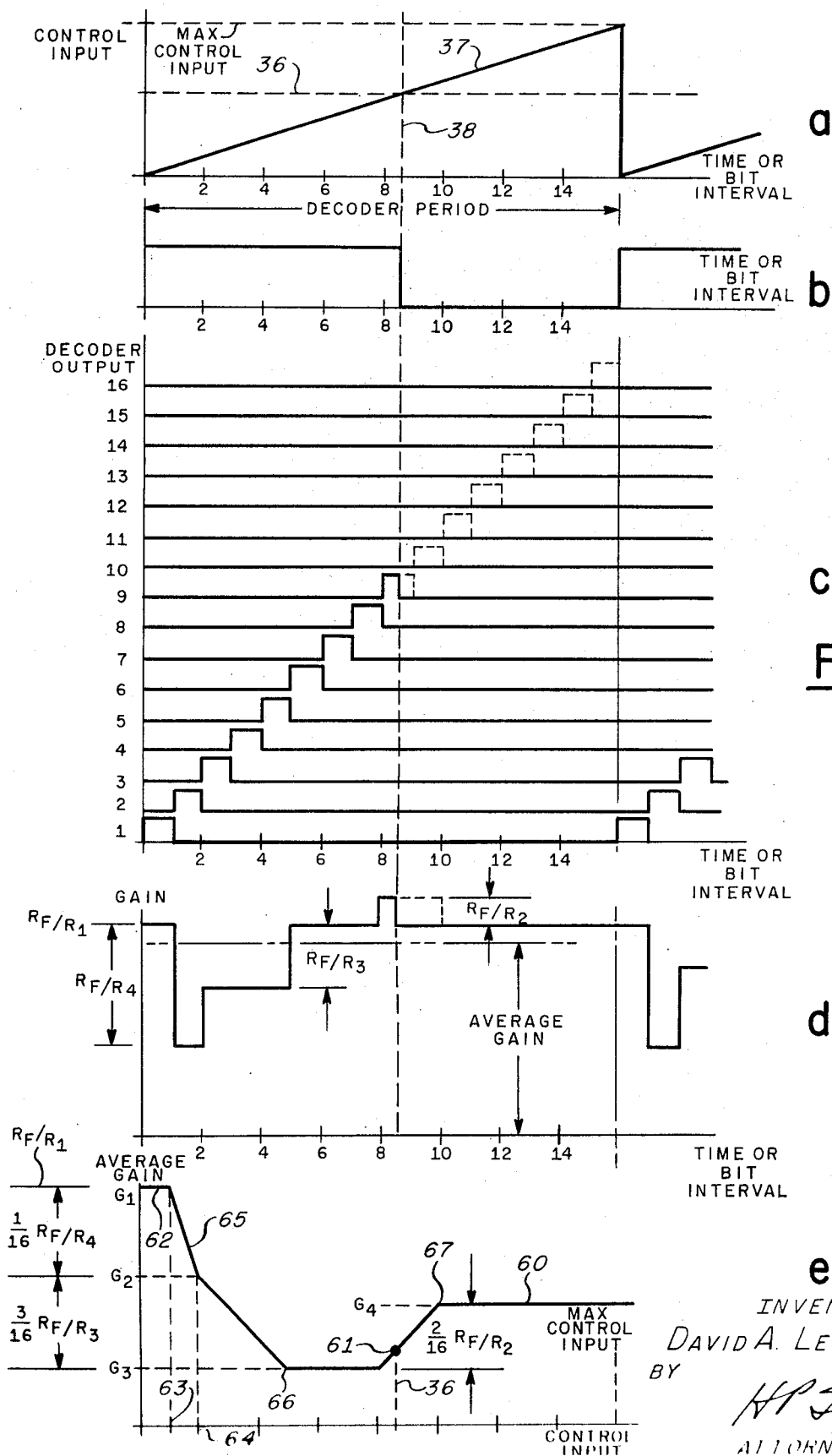


FIG. 2.

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FUNCTION GENERATOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention pertains to function generators particularly of the type suitable for the generation of non-linear functions comprised of connected linear segments.

2. Description of the Prior Art

Prior art function generators are known that generate non-linear functions comprised of connected linear segments. One such function generator type in wide spread usage utilizes diodes to determine the break points of the linear segments and respectively associated resistors for determining the slopes thereof. These generators have numerous disadvantages. The variability of diode characteristics with changes in temperature causes inaccuracies, thus requiring expensive and inconvenient environmental temperature control or additional temperature compensation circuits. Additionally, the variability of characteristics among commercially available diodes of the same type requires the inclusion of break point and slope adjustment potentiometers or selected resistors. In the design of a prior art generator, the component parameters are first calculated in accordance with the function to be generated and thereafter complex empirical adjustments to the numerous break point and slope potentiometers are required to correct for the variability of the diode characteristics providing an excessively time consuming and hence costly procedure.

An additional problem arising in the use of diode function generators is that as the input voltage increases, the diodes are sequentially turned on to provide the required break points of the generated function. Once a diode has been turned on, it normally remains on as the input voltage continues to increase. Thus, the errors and inaccuracies due to the variability of the diode characteristics tend to accumulate additively as the input voltage to the circuit increases resulting in inordinately large errors at the high range of operating input voltages. The variability due to temperature changes further aggravates the problem. Additionally, since the break point and slope characteristics associated with a particular diode of a function generator are dependent upon the characteristics of the previously turned diodes, the calculations required in the design of such diode function generators becomes cumbersome.

Diode function generators are not particularly suited to bipolar input voltages, hence limiting the applicability of such devices. Additionally, they inherently provide monotonic functions and in order to obtain non-monotonic functions, the outputs of two such generators are subtractively combined resulting in an excessive amount of equipment.

Several of the disadvantages associated with diode function generators can be obviated by utilizing an operational amplifier in combination with each required diode, the diode being connected in the feedback loop of the amplifier. In this manner, the effects of the variability of the diode characteristics are minimized. This approach has the disadvantage of requiring a large number of expensive operational amplifiers. Since the operating principles of such function generators are similar to the diode function generators,

the operational amplifier diode function generators also suffer from many of the disadvantages previously discussed.

It is often desirable to provide in synchronism a variety of functions of the same input variable. With prior devices a substantially complete generator is required for each function to be provided, and the designs are not particularly suited to equipment saving, time sharing techniques.

SUMMARY OF THE INVENTION

The present invention provides a function generator that overcomes the disadvantages discussed above utilizing a minimum of equipment compared to the prior art devices. The generator of the present invention provides one or more gain functions of respective independent variable input signals under control of another independent variable input signal.

The desirable features of the present invention are achieved by a function generator comprising a sequencing circuit that provides a sequence of signals, the number of which is proportional to the control input signal. Variable gain means responsive to the sequence of signals selectively provides predetermined gains corresponding to the sequence of signals. An averaging circuit coupled to the variable gain means provides an output signal representative of the average of the selectively provided gains thus generating the required functions of the control input signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block schematic diagram of a preferred embodiment of the invention; and

FIG. 2 is a waveform diagram illustrating waveforms useful in explaining the operation of the preferred embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiment of the function generator of the present invention is particularly suited to the generation of a gain function of an input signal under control of another input signal. For example, it is often desirable to vary the gain of a servo of an aircraft autopilot as a function of the flight regimes of the aircraft in order to effect proper control in accordance with the aircraft dynamics. This is particularly desirable in modern jet transports. This gain scheduling may be achieved by the present invention by connecting an aircraft attitude or rate sensor as an input to the function generator of the invention, the output thereof being applied as the input signal to the associated servo. The control input to the function generator may be derived from the airspeed output of the air data system of the aircraft. Thus, the gain of the autopilot servo is controlled as a function of airspeed.

Referring to FIG. 1, a preferred embodiment of the invention is illustrated as a function generator. A basic overall scheme of operating will first be discussed and followed by a detailed analysis. The function generator is comprised of a sequencing circuit 21 responsive to an independent variable control input signal applied to a lead 22. The sequencing circuit 21 provides a sequence of signals on control leads 23 from decoder 31, the

total number turned on per period in the sequence being proportional to the control input signal. The function generator further includes a variable gain circuit 24 responsive to particular individual outputs of the decoder 31. The variable gain circuit 24 provides predetermined gains at terminal 26 of an independent variable input signal applied to terminal 25. The predetermined gains correspond respectively to the outputs of decoder 31. The predetermined gains provided at the terminal 26 are applied to an averaging circuit 27 which in turn provides the average per period. Thus, a gain function of the signal at the terminal 25 is generated in accordance with the control input signal applied to the lead 22.

In more detail, the sequencing circuit 21 comprises a conventional binary counter 30 adapted to count clock pulses of any convenient frequency. The outputs of the counter 30 are applied to a conventional one of N decoder 31 that sequentially energizes its output control leads 23 as the count from the counter 30 increases in response to the applied clock pulses. FIG. 2c illustrates the sequence of signals provided on the leads 23 (where N=16). It is understood that the counter 30 and the decoder 31 comprise digital counting circuits of a type familiar to practitioners in the art.

The sequencing circuit 21 further includes a voltage to pulse width converter 32. The control input signal on the lead 22 is applied to the voltage to pulse width converter 32 which in turn provides enabling pulses on a lead 33. The enabling pulses on the lead 33 have pulse widths linearly proportional to the amplitude of the control input signal on the lead 22. The enabling pulses on the lead 33 are applied to an enable input of the decoder 31. Only during application of a pulse to the enable input will the decoder 31 provide energization to the leads 23.

The voltage to pulse width converter 32 comprises a conventional ramp voltage generator 34 and a conventional voltage comparator 35. The ramp generator 34 provides a ramp voltage signal to one of the inputs of the comparator 35. The control input signal on the lead 22 is applied to the second input of comparator 35. The ramp generator 34 is reset in response to a predetermined count of the counter 30, which may for convenience be the most significant bit count. In this manner, the output of the ramp generator 34 is synchronized to the counting period of the counter 30. The comparator 35 provides the enabling pulses on the lead 33 where each enabling pulse is initiated coincident with the initiation of the ramp signal and is terminated by the comparator 35 when the ramp voltage equals the signal on the lead 22.

Referring now to FIGS. 1 and 2, the ramp voltage from the generator 34, the enabling pulses on the lead 33 and the sequence of signals on the leads 23 are illustrated in FIGS. 2a, b, and c, respectively. For a given level 36 of control input signal, the ramp voltage 37 equals the level 36 at a time 38 of the counter/decoder period. The time 38 corresponding to the level 36 occurs half way between the initiation of the count of 9 and the count of 10 of the counter 30. The enabling pulses corresponding to this condition are illustrated in FIG. 2b. It is appreciated that the width of the enabling pulses illustrated is proportional to the control input signal level 36 of FIG. 2a as previously explained. Thus,

for the illustrated level 36, the decoder outputs 1 through 9 are sequentially energized providing a sequence of signals on the leads 23 as illustrated in FIG. 2c. In the example illustrated, the decoder outputs 1-8 are energized for complete bit intervals while the decoder output 9 is energized for one-half of a bit interval. It is therefore appreciated that the number of sequence signals provided by the decoder 31 is linearly proportional to the enabling pulse width which in turn is linearly proportional to the control input signal on the lead 22. In the example illustrated in FIG. 2, the number of sequence signals is 8.5. It is therefore further appreciated that the sequencing circuit 21 provides a linear time quantization of the amplitude of the control input signal applied to the lead 22.

Referring again to FIG. 1, the variable gain circuit 24 will be described in more detail. A gain controlling resistor R1 is connected between terminals 25 and 26. Switches 42, 43 and 44 are also connected between terminals 25 and 26 and selectively couple gain controlling resistors R2, R3 and R4, respectively. The resistors R3 and R4 are coupled between the terminals 25 and 26 in a series circuit with inverter 45 for providing inverse polarity gains. The switches 42-44 are controlled by logic gates 46, 47 and 48, respectively. An output on lead 2 of the decoder 31 controls the logic gate 48 and the latter actuates the switch 44. Outputs on leads 3, 4 and 5 of the decoder 31 controls logic gate 47 and the latter actuates the switch 43. In a similar manner, outputs on control leads 9 and 10 control logic gate 46 and the latter actuates the switch 42. It is understood that the switches 42-44 and gates 46-48 are schematically illustrated and would normally be instrumented by electronic switching circuits.

The terminal 26 of the variable gain circuit 24 provides an input to the averaging circuit 27 as previously explained. The averaging circuit 27 which may, for example, comprise a lag circuit, includes an inverting operational amplifier 51 with a capacitor 52 and a feedback resistor R_f connected in shunt therewith. The time constant of the averaging circuit 27 is chosen to be sufficiently long so that the operational amplifier 51 provides a signal representative of the average of the signals applied thereto over the period of the counter/decoder 30-31. The output of the averaging circuit 27 appears on output lead 53 and thus provides gain functions of the control input signal on the lead 22 with respect to input signals applied to the terminal 25.

Networks of the type comprising the terminal 25, the resistors R1-R4, the terminal 26, the operational amplifier 51 and the feedback resistor R_f, generally have a gain relationship of the form —

$$\text{Gain} = \frac{\text{output}}{\text{input}} = -R_f \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4} \right)$$

where the negative sign associated with R_f is caused by the inversion provided by the amplifier 51. Thus specifically in the circuits 24 and 27, with none of the switches 42-44 actuated, the gain from the input 25 to the output is -R_f/R₁, disregarding the averaging effect of the capacitor 52. Similarly, with the switch 44 actuated, the gain is -R_f/R₁ + R_f/R₄. When the switch 43 is actuated, the gain is -R_f/R₁ + R_f/R₃ and when the switch 42 is actuated, the gain is -R_f/R₁ - R_f/R₂. It is appreciated that the sign appearing in the gain expres-

sions associated with the resistors R_3 and R_4 are provided by the inverter 45.

The gains provided by the circuits 24 and 27, disregarding the averaging effect of the capacitor 52, are illustrated in FIG. 2d. The low frequency roll off of the averaging circuit 27 prevents the circuits 24 and 27 from providing the rapidly changing gain as illustrated. Instead, the averaging circuit 27 provides the average of the gains on the lead 53 over the period of the counter/decoder 30-31 as previously explained.

It is now appreciated from the foregoing that during each period of the counter/decoder 30-31, the leads 23 are sequentially energized beginning at least 1 and ending with the energization of one of the decoder outputs from a complete or fractional bit interval in accordance with the width of the enable pulses on the lead 33. Thus, the number of the leads 23 energized, including the fractional bit energization, is linearly proportional to the amplitude of the control input signal on the lead 22. Since the gain controlling resistors R_2 , R_3 and R_4 are rendered effective by the switches 42, 43 and 44, respectively, which in turn are controlled by the leads 23, the variable gain circuit 24 provides the predetermined gains corresponding to the bit intervals of the decoder 31 as illustrated in FIG. 2d.

When the control input signal on the lead 22 is, for example, at the level 36 (FIG. 2a), the variable gain circuit 24 provides the predetermined gains illustrated in solid line in FIG. 2d. During bit interval 1 none of the switches 42-44 are actuated, and the gain is $-R_f/R_1$. During bit interval 2, the switch 44 is actuated and the instantaneous gain drops to $-R_f/R_1 + R_f/R_4$. During bit intervals 3, 4 and 5 the switch 43 is actuated and the instantaneous gain becomes $-R_f/R_1 + R_f/R_3$. During bit intervals 6, 7 and 8 none of the switches 42-44 are actuated and the instantaneous gain again becomes $-R_f/R_1$. During the first half of bit interval 9, the switch 42 is actuated resulting in an instantaneous gain of $-R_f/R_1 - R_f/R_2$. During the second half of bit interval 9 and during the bit intervals 10-16, none of the switches 42-44 are actuated and the gain again becomes $-R_f/R_1$. These predetermined gains provided during a period of the decoder 31 are averaged by the circuit 27 and the output appears on the lead 53 as indicated by the legend of FIG. 2d. Generally, the average gain during a period of the decoder 31 is the sum of the gains provided during each bit interval thereof divided by the number of bit intervals in the period.

Should the control input signal be at maximum level, as indicated by the legend in FIG. 2, the predetermined gains provided by the circuit 24 will be as shown in dotted line in FIG. 2d. Thus, for different levels of control input voltage on the lead 22, different predetermined gains will be selected during the period of the counter/decoder 30, 31 providing different average gains on the lead 53.

It should be appreciated that in the bit interval during which the enabling pulse terminates, the active switch associated with that bit interval is on for a time linearly proportional to the control input signal on the lead 22. Thus during that bit interval, the gain provided by the variable gain circuit 24 varies as a linear function of the control input signal.

Analytically, the networks of the type comprising the circuits 24 and 27 have a gain relationship in accordance with the expression

$$\text{GAIN} = \frac{\text{output}}{\text{input}} = \frac{R_f}{R_1} + \frac{R_f}{N} \sum_{i=1}^n \left(-\frac{2n_2}{R_2} + \frac{3n_3}{R_3} + \frac{n_4}{R_4} \right)$$

where n_2 is defined as

$$9 < n < 11 \text{ and } (n-9)/2 = n_2$$

n_3 is defined as

$$3 < n < 6 \text{ and } n - 3/3 = n_3$$

n_4 is defined as

$$2 < n < 3 \text{ and } n - 2 = n_4$$

where n is defined as

$0 < n < N$. Thus, with none of the switches 42-44 actuated, the gain from terminal 25 to the output 53 is $-R_f/R_1$. Similarly, with switch 44 actuated during the entire interval 2, the average gain is

$$-\frac{R_f}{R_1} + \frac{R_f}{R_4} \frac{1}{N}$$

When switch 43 is actuated during the entire intervals of 3 through 5 the average gain is

$$-\frac{R_f}{R_1} + \frac{R_f}{R_4} \frac{1}{N} + \frac{R_f}{R_3} \frac{3}{N}$$

and when switch 42 is actuated for the entire intervals of 9 through 10 the average gain is

$$-\frac{R_f}{R_1} + \frac{R_f}{R_4} \frac{1}{N} + \frac{R_f}{R_3} \frac{3}{N} - \frac{R_f}{R_2} \frac{2}{N}$$

During the operation of the function generator, illustrated in FIG. 1, the gain of the output 53 with respect to the input 25 varies as a function of the control input signal on the lead 22. This function is illustrated by curve 60 of FIG. 2e, the gain point 61 thereof corresponding to the average gain provided at the lead 53 in response to a control input signal at the level 36 as previously discussed.

The manner in which the gain curve 60 is derived will now be explained. For any control input signal of magnitude sufficiently small so that only decoder output 1 energizes during the decoder periods, none of the switches 42-44 are actuated. Hence, the average gain G_1 provided is $-R_f/R_1$ and the linear segment 62, over which the gain does not change, of the curve 60 is generated. For control input voltages in the range between levels 63 and 64, the length of time that the switch 44 is actuated is linearly proportional to the control input. When the control input is at the level 64, the average gain G_2 provided is $-R_f/R_1 + 1/N R_f/R_4$. Because of the linearity relationship discussed, the average gain decreases from $-R_f/R_1$ to $-R_f/R_1 + 1/N R_f/R_4$ as the control input voltage increases from level 63 to level 64, hence generating the linear segment 65 of the curve 60. In a similar manner, the break points 66 and 67 have average gain values of $G_3 = -R_f/R_1 + 1/N R_f/R_4 + 3/N R_f/R_3$ and $G_4 = -R_f/R_1 + 1/N R_f/R_4 + 3/N R_f/R_4 + 3/N R_f/R_3 - 2/N R_f/R_2$, respectively, thus generating the remainder of the connected linear segments of the gain function 60. Parameters found suitable for the generation of the function 60 are $R_f = 100 \text{ K}$, $R_1 = 100 \text{ K}$, $R_2 = 59 \text{ K}$, $R_3 = 47 \text{ K}$ and $R_4 = 19 \text{ K}$.

It is now appreciated that the design of the variable gain circuit 24 to provide the gain schedule 60 is a relatively simple additive process compared to the design and adjustment of the prior art function generators. The gain function break points are calculated as

described above, where the values of the resistors determine the magnitudes of the slopes of the linear segments. The polarities of the slopes are determined by whether or not the signal applied to the terminal 25 is inverted by the inverter 45. When no switch is associated with a given bit interval, the average gain remains the same over the range of control input signals associated therewith, resulting in a segment of zero slope. Generally, a segment is generated by selecting the end points thereof and calculating the gain required in the bit intervals associated therewith to change the average gain over the entire decoder period from that at the beginning of the segment to that at the end of the segment. From the foregoing it will be appreciated that the break points of a generated function are accurately determined because of the clocked precision of the sequencing circuit 21. This accuracy is substantially temperature insensitive compared to the prior art function generators previously discussed.

Although the function generator provides a single gain function 60, it is appreciated that the sequencing circuit 21 may synchronously control the generation of a plurality of functions of the control input signal applied to the lead 22. By appropriate gating, a plurality of variable gain circuits with associated averaging circuits may synchronously provide the plurality of functions. Alternatively, logic circuits interposed between the decoder 31 and the gates 46-48 may program the variable gain circuit 24 to provide a plurality of functions in accordance with digital inputs to the logic circuits.

Although the sequencing circuit 21 is explained in terms of a counter and a decoder, other sequencing means such as shift registers or stepping circuits may be utilized to the same effect. Furthermore, the function generator may be used to control an output voltage as a function of an input voltage similar in result to prior art function generators. This may be accomplished by connecting the input voltage to both the lead 22 and the terminal 25.

It will be appreciated that the averaging effect of circuit 27 tends to prevent saturation of the amplifier 51 from occurring under adversely high transient signal conditions. Hence, a significantly large dynamic range is provided without scaling the voltages into the circuit. Additionally, the present invention can readily generate functions comprising large numbers of linear segments because of the inherent simplicity of the invention relative to the prior devices and because the present invention does not suffer from a reduction in dynamic range with large numbers of segments as do the prior devices.

The present invention may conveniently be tested for circuit failures by measuring the gain of the last break point of the generated function when the control input voltage exceeds that required to provide this break point. Simultaneous failures of equal magnitude, positive and negative gain contributions may not be detectable by this method. However, this type of failure may be precluded by the appropriate selection of unequal positive and negative gains. A very high assurance of failure detection may be achieved by gain measurements at the maximum and minimum inflection points of the gain function curve.

It will now be understood with respect to the aircraft servo application of the present invention, as previously discussed, that the aircraft attitude or rate sensor signal is applied to the input 25, the output 53 being applied as the input to the servo and the airspeed signal being applied to the control input 22.

While the invention has been described in its preferred embodiment, it is to be understood that the words which have been used are words of description rather than limitation and that changes may be made within the purview of the appended claims without departing from the true scope and spirit of the invention in its broader aspects.

I claim:

1. Apparatus for generating functions of an input signal comprising

sequencing means responsive to said input signal for sequentially providing a plurality of pulse signals, the total of the pulse durations thereof being proportional to said input signal,

variable gain means responsive to said plurality of pulse signals for selectively providing a plurality of predetermined gains corresponding thereto, respectively,

means included in said variable gain means for rendering said predetermined gains effective during the durations of the corresponding pulse signals, and

averaging means coupled to said variable gain means for providing an output signal representative of the average of said selectively provided gains thereby providing said functions of said input signal.

2. The apparatus of claim 1 in which said sequencing means comprises

a plurality of control leads, and

means for sequentially energizing a number of said control leads, all but the last thereof being energized for equal time durations, the last thereof being energized for a time duration linearly proportional to said input signal, thereby generating said plurality of pulse signals.

3. Apparatus for generating functions of an input signal comprising

sequencing means responsive to said input signal for providing a sequence of signals the number thereof being proportional to said input signal,

variable gain means responsive to said sequence of signals for selectively providing predetermined gains corresponding to said sequence of signals, respectively, and

averaging means coupled to said variable gain means for providing an output signal representative of the average of said selectively provided gains thereby providing said functions of said input signal,

said sequencing means comprising pulse width converter means for providing enabling pulses of widths proportional to said input signal and digital counting means adapted to count clock pulses and having a plurality of control leads for sequential energization in response to said clock pulses, said digital counting means being responsive to said enabling pulses for enabling energization of said control leads only during the presence thereof thereby providing said sequence of signals.

4. The apparatus of claim 1 in which said variable gain means comprises,

a plurality of gain controlling elements, and switching means responsive to said plurality of pulse signals,

said gain controlling elements and said switching means being so arranged with respect to each other to provide said predetermined gains. 5

5. The apparatus of claim 1 in which said variable gain means comprises

a first terminal,

a second terminal,

a plurality of resistor means, and

switching means responsive to said plurality of pulse signals for selectively coupling said resistor means between said first and second terminals thereby providing said predetermined gains. 15

6. The apparatus of claim 5 in which said variable gain means further includes inverting means coupled in series circuit with respect to certain of said resistor means between said first and second terminals for providing inverse polarity predetermined gains. 20

7. The apparatus of claim 1 in which said averaging means comprises lag circuit means.

8. Apparatus for generating functions of an input signal comprising

pulse width converter means for providing enabling pulses of widths proportional to said input signal, 25

digital counting means adapted to count clock pulses and having a plurality of control leads for sequential energization in response to said clock pulses, 30

said digital counting means being responsive to said enabling pulses for enabling energization of said control leads only during the presence thereof,

a first terminal,

a second terminal, 35

a plurality of resistor means,

a plurality of switching means coupled to said plurality of control leads for selectively coupling said resistor means between said first and second terminals thereby selectively providing predetermined gains with respect to signals applied to said first terminal, and 40

averaging means coupled to said second terminal for providing an output signal representative of the average of said selectively provided gains thereby providing said functions of said input signal. 45

9. The apparatus of claim 8 in which said pulse width converter means comprises

ramp generator means coupled to said digital counting means for providing a ramp signal 50

synchronized to a predetermined count thereof, and

comparator means responsive to said ramp signal and said input signal for providing said enabling pulses to said digital counting means in accordance with said ramp signal equalling said input signal.

10. The apparatus of claim 1 in which said sequencing means comprises

pulse width converter means for providing enabling pulses of widths proportional to said input signal, and 10

digital counting means adapted to count clock pulses and having a plurality of control leads for sequential energization in response to said clock pulses, 15

said digital counting means being responsive to said enabling pulses for enabling energization of said control leads only during the presence thereof thereby providing said plurality of pulse signals.

11. Apparatus for generating a function of an input signal, a point of said function being generated during a predetermined time period, the combination comprising 20

sequencing means responsive to said input signal adapted for sequentially providing a predetermined number of equal duration pulse signals, the total of the pulse durations thereof being equal to said predetermined time period, 25

means included in said sequencing means for sequentially enabling said pulse signals until the total pulse durations thereof are proportional to said input signal, the duration of the last enabled pulse signal being linearly proportional to said input signal, 30

variable gain means coupled to said sequencing means adapted for providing a predetermined number of predetermined gains corresponding to said predetermined number of pulse signals, respectively, 35

means included in said variable gain means for rendering effective those predetermined gains corresponding to said enabled pulse signals during the durations thereof, and 40

averaging means coupled to said variable gain means for providing an output signal representative of the average over said predetermined time period of said predetermined gains rendered effective during said time period, thereby providing said point of said function of said input signal. 45

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