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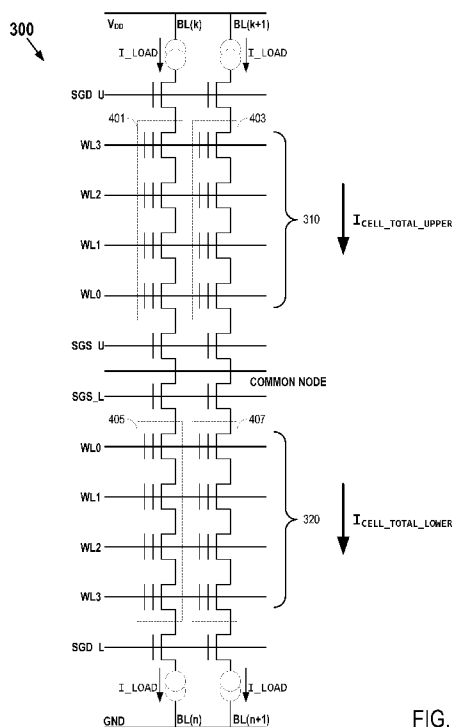


FIG. 4

(57) Abstract: Various embodiments comprise apparatuses and methods in-
cluding a three-dimensional memory apparatus having upper strings and
lower strings. The upper strings can include a first string of memory cells
and a second string of memory cells arranged substantially parallel and adja-
cent to one another. The lower strings can include a third string of memory
cells and a fourth string of memory cells arranged substantially parallel and
adjacent to one another. The strings can each have a separate sense amplifier
coupled thereto. The first and third strings and the second and fourth strings
can be configured to be respectively coupled in series with each other during
a read operation. Additional apparatuses and methods are described.

MEMORY ARRAY WITH POWER-EFFICIENT READ ARCHITECTURE

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PRIORITY APPLICATION

[0001] This application claims the benefit of priority to U.S. Application
Serial No. 13/599,962, filed 30 August 2012, which is incorporated herein by
10 reference in its entirety.

BACKGROUND

[0002] Computers and other electronic systems, for example, digital
televisions, digital cameras, and cellular phones, often have one or more memory
and other devices to store information. Increasingly, memory and other devices
15 are being reduced in size to achieve a higher density of storage capacity and/or a
higher density of functionality. Also, memory devices are being redesigned to
achieve higher operational (e.g., read or write) speeds.

BRIEF DESCRIPTION OF THE DRAWINGS

20 [0003] FIG. 1 shows a block diagram of a memory device having a memory
array with memory cells, according to an embodiment;

[0004] FIG. 2 shows a partial block diagram of a memory device having a
memory array including memory cells with access components and memory
elements, according to an embodiment;

25 [0005] FIG. 3 shows a schematic circuit diagram and an associated block
diagram of a portion of a memory array, according to an embodiment;

[0006] FIG. 4 indicates current flow for the schematic circuit diagram of
FIG. 3, during a read operation of the memory array;

[0007] FIG. 5A and FIG. 5B show current source and sense amplifier arrangements that may be used with the schematic circuit of FIG. 3, according to an embodiment; and

[0008] FIG. 6 shows a block diagram of a system embodiment, including a
5 memory device according to various embodiments described herein.

DETAILED DESCRIPTION

[0009] A number of techniques have been proposed to increase the read speed of various types of memory devices. For example, in a conventional flash
10 memory cell, a read operation is performed with a bit line pre-charged to a pre-determined voltage. The pre-charged bit line is then floated so only a pre-charge current is needed. However, only alternative bit lines (e.g., even and odd bit lines alternately connected to every other cell along a word line) are read at a time, since two alternate bitlines are multiplexed into a single sense amplifier.

15 [0010] In some cases, an All-Bit-Line (ABL) read operation has been proposed to increase the parallelism of read operations within NAND flash memory by doubling the number of bit lines, and consequently the number of bits, that can be read simultaneously. Thus, the ABL technique can sometimes double the bandwidth during read, program, and verify operations of a memory
20 device. However, even though the number of accessible bit lines is doubled, the ABL technique requires more power during operation of the memory device. For example, in the ABL technique, direct current (DC) is forced to flow constantly through all memory cells in a string during a read operation, with commensurately higher power requirements than conventional techniques.

25 [0011] The disclosed subject matter proposes various memory device structures that increases the number of data lines (e.g., bit lines) that can be read concurrently by providing a data line and an associated sense amplifier for each string of memory cells. However, the current used by the memory structure may be reduced by a factor of two over standard ABL techniques.

[0012] The description that follows includes illustrative apparatuses (circuitry, devices, structures, systems, and the like) and methods (e.g., processes, protocols, sequences, techniques, and technologies) that embody the subject matter. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide an understanding of various embodiments of the subject matter. After reading this disclosure however, it will be evident to person of ordinary skill in the art that various embodiments of the subject matter may be practiced without these specific details. Further, well-known apparatuses and methods have not been shown in detail so as not to obscure the description of various embodiments. Additionally, although the various embodiments focus on implementation within a NAND flash memory device, the techniques and methods presented herein are readily applicable to a number of other memory device types.

[0013] Referring now to FIG. 1, a block diagram of an apparatus in the form of a memory device 101 is shown. The memory device 101 includes one or more memory arrays 102 having a number (e.g., one or more) of memory cells 100. The memory cells 100 can be arranged in rows and columns along with access lines 104 (e.g., wordlines to conduct signals WL0 through WLn) and first data lines 106 (e.g., bit lines to conduct signals BL0 through BLn). The memory device 101 can use the access lines 104 and the first data lines 106 to transfer information to and from the memory cells 100. A row decoder 107 and a column decoder 108 can operate to decode address signals A0 through AX on address lines 109 to determine which ones of the memory cells 100 are to be accessed.

[0014] Sense circuitry, such as a sense amplifier circuit 110, operates to determine the values of information read from the memory cells 100 in the form of signals on the first data lines 106. The sense amplifier circuit 110 can also use the signals on the first data lines 106 to determine the values of information to be written to the memory cells 100.

[0015] The memory device 101 is further shown to include circuitry 112 to transfer values of information between the memory array 102 and input/output

(I/O) lines 105. Signals DQ0 through DQN on the I/O lines 105 can represent values of information read from or to be written into the memory cells 100. The I/O lines 105 can include nodes of the memory device 101 (e.g., pins, solder balls, or other interconnect technologies such as controlled collapse chip connection (C4), or flip chip attach (FCA)) on a package where the memory device 101 resides. Other devices external to the memory device 101 (e.g., a memory controller or a processor, not shown in FIG. 1) can communicate with the memory device 101 through the I/O lines 105, the address lines 109, or the control lines 120.

10 [0016] The memory device 101 can perform memory operations, such as a read operation, to read values of information from selected ones of the memory cells 100 and a programming operation (also referred to as a write operation) to program (e.g., to write) information into selected ones of the memory cells 100. The memory device 101 can also perform a memory erase operation to clear
15 information from some or all of the memory cells 100.

[0017] A memory control unit 118 controls memory operations using signals from the control lines 120. Examples of the signals on the control lines 120 can include one or more clock signals and other signals to indicate which operation (e.g., a programming operation or read operation) the memory device 101 can or
20 should perform. Other devices external to the memory device 101 (e.g., a processor or a memory controller) can control the values of the control signals on the control lines 120. Specific combinations of values of the signals on the control lines 120 can produce a command (e.g., a programming, read, or erase command) that can cause the memory device 101 to perform a corresponding
25 memory operation (e.g., a program, read, or erase operation).

[0018] Although various embodiments discussed herein use examples relating to a single-bit memory storage concept for ease in understanding, the inventive subject matter can be applied to numerous multiple-bit schemes as well. In some embodiments, each of the memory cells 100 can be programmed
30 to a different one of at least two data states to represent, for example, a value of a

fractional bit, the value of a single bit or the value of multiple bits such as two, three, four, or a higher number of bits.

[0019] For example, each of the memory cells 100 can be programmed to one of two data states to represent a binary value of “0” or “1” in a single bit.

5 Such a cell is sometimes called a single-level cell (SLC).

[0020] In some embodiments, each of the memory cells 100 can be programmed to one of more than two data states to represent a value of, for example, multiple bits, such as one of four possible values “00,” “01,” “10,” and “11” for two bits, one of eight possible values “000,” “001,” “010,” “011,” “100,” “101,” “110,” and “111” for three bits, or one of another set of values for larger numbers of multiple bits. A cell that can be programmed to one of more than two data states is sometimes referred to as a multi-level cell (MLC). Various operations on these types of cells are discussed in more detail, below.

[0021] The memory device 101 can receive a supply voltage, including supply voltage signals V_{cc} and V_{ss} , on a first supply line 130 and a second supply line 132, respectively. Supply voltage signal V_{ss} can, for example, be at a ground potential (e.g., having a value of approximately zero volts). Supply voltage signal V_{cc} can include an external voltage supplied to the memory device 101 from an external power source such as a battery or alternating-current to direct-current (AC-DC) converter circuitry (not shown in FIG. 1).

[0022] The circuitry 112 of the memory device 101 is further shown to include a select circuit 115 and an input/output (I/O) circuit 116. The select circuit 115 can respond to signals SEL1 through SELn to select signals on the first data lines 106 and the second data lines 113 that can represent the values of information to be read from or to be programmed into the memory cells 100. The column decoder 108 can selectively activate the SEL1 through SELn signals based on the A0 through AX address signals present on the address lines 109. The select circuit 115 can select the signals on the first data lines 106 and the second data lines 113 to provide communication between the memory array 102 and the I/O circuit 116 during read and programming operations.

[0023] The memory device 101 may comprise a non-volatile memory device, and the memory cells 100 can include non-volatile memory cells, such that the memory cells 100 can retain information stored therein when power (e.g., V_{cc} , or V_{ss} , or both) is disconnected from the memory device 101.

5 [0024] Each of the memory cells 100 can include a memory element having material, at least a portion of which can be programmed to a desired data state (e.g., by being programmed to a corresponding charge storage state). Different data states can thus represent different values of information programmed into each of the memory cells 100.

10 [0025] The memory device 101 can perform a programming operation when it receives (e.g., from an external processor or a memory controller) a programming command and a value of information to be programmed into one or more selected ones of the memory cells 100. Based on the value of the information, the memory device 101 can program the selected memory cells to
15 appropriate data states to represent the values of the information to be stored therein.

[0026] One of ordinary skill in the art may recognize that the memory device 101 may include other components, at least some of which are discussed herein. However, several of these components are not shown in the figure, so as not to
20 obscure details of the various embodiments described. The memory device 101 may include devices and memory cells, and operate using memory operations (e.g., programming and erase operations) similar to or identical to those described below with reference to various other figures and embodiments discussed herein.

25 [0027] With reference now to FIG. 2, a partial block diagram of an apparatus in the form of a memory device 201 is shown to include a memory array 202, including memory cells 200 with access components 211 and memory elements 222, according to an example embodiment. The memory array 202 may be similar to or identical to the memory array 102 of FIG. 1. As further shown in
30 FIG. 2, the memory cells 200 are shown to be arranged in a number of rows 230,

231, 232, along with access lines, for example word lines, to conduct signals to the memory cells 200, such as signals WL0, WL1, and WL2. The memory cells are also shown to be arranged in a number of columns 240, 241, 242 along with data lines, for example bit lines, to conduct signals to the cells 200, such as
5 signals BL0, BL1, and BL2. The access components 211 can turn on (e.g., by using appropriate values of signals WL0, WL1, and WL2) to allow access to the memory elements 222, such as to operate the memory elements 222 as pass elements, or to read information from or program (e.g., write) information into the memory elements 222.

10 **[0028]** Programming information into the memory elements 222 can include causing the memory elements 222 to have specific resistance states. Thus, reading information from a memory cell 200 can include, for example, determining a resistance state of the memory element 222 in response to a specific voltage being applied to its access component 211. The act of
15 determining resistance may involve sensing a current (or the absence of current) flowing through the memory cell 200 (e.g., by sensing a current of a data line electrically coupled to the memory cell). Based on a measured value of the current (including, in some examples, whether a current is detected at all), a corresponding value of the information stored in the memory can be determined.
20 The value of information stored in a memory cell 200 can be determined in still other ways, such as by sensing the voltage on a data line electrically coupled to the memory cell.

[0029] Various ones or all of the memory cells 100, 200 of FIG. 1 and FIG. 2 can include a memory cell having a structure similar or identical to one or
25 more of the memory cells and devices described below.

[0030] With reference now to FIG. 3, a schematic circuit diagram 330 and an associated block diagram 350 of a portion of a memory array 300 are shown. In comparison with contemporaneous memory devices that use a conventional voltage sensing technique to read the memory cells, the memory array 300 can
30 use a current sensing technique during a read operation. Further, most contemporaneous memory devices have sense amplifiers coupled alternately to

odd-strings and even strings to reduce cross-talk and capacitive coupling effects between adjacent memory strings due to their use of voltage sensing techniques. The current sensing techniques described herein allow each of the strings of memory to be coupled to a separate sense circuit. Thus, the current sensing
5 technique enables concurrent parallel reading of all memory strings, thereby increasing read bandwidth.

[0031] The memory array 300 may correspond to a portion of the memory device 101 of FIG. 1. For example, the memory array 300 can form a part of the memory array 102 of FIG. 1. The memory array 300 can also include a control
10 unit similar to or identical to the memory control unit 118 of FIG. 1 to control memory operations (e.g., read, write, and erase operations) of the memory array 300.

[0032] As shown in FIG. 3, the memory array 300 can include a conductive voltage line 301 coupled to a first supply node (e.g., V_{DD}) to supply power to
15 upper current-sources 307. A left-side data line 303 (to carry a signal $BL(k)$) and a right-side data line 305 (to carry a signal $BL(k+1)$) can each be coupled to the respective upper current-sources 307 to provide current to upper strings 310 of memory cells 311. Although only two NAND strings are shown in FIG. 3, three or more NAND strings may be used. Further, the subject matter disclosed
20 herein is not limited to NAND memory but may include, instead of or in addition to, memories such as phase change memory (PCM), resistive RAM (RRAM), conductive-bridging RAM (CBRAM), and other memory types.

[0033] SGD select transistors 309 may have their respective gates coupled to each other and may be controlled (e.g., turned on or turned off) by a signal
25 SGD_U (e.g., a drain select-gate signal) on an upper SGD select-line 335 (e.g., a drain select line) of the memory array 300. During a memory operation (e.g., a read or write operation) of the memory array 300, the signal SGD_U can control whether current is provided to the upper strings 310 from the upper current-sources 307 (through a respective one of the data lines 303, 305).

[0034] The upper strings 310 include a number of memory cells 311 couplable to a respective one of the left-side data line 303 and the right-side data line 305 (through a respective one of the select transistors 309). Further, each of the memory cells 311 is coupled to a respective one of a number of access lines 337. The access lines 337 can each carry one of a signal WL0, WL1, WL2, and WL3 as indicated in FIG. 3. Only four memory cells 311 are depicted as being in each of the upper strings 310; however, a larger or a smaller number of the memory cells 311 may be used in each of the upper strings 310.

[0035] As shown, a common (e.g., source) node 319 may be coupled to the upper strings 310 by the operation of an upper SGS select-line 317 coupled to upper SGS select-transistors 313. The upper SGS select-transistors 313 can have their respective gates coupled to each other and may be controlled (e.g., turned on or turned off) by a signal SGS_U (e.g., a source select-gate signal) on the upper SGS select-line 317 (e.g., source select line) of the memory array 300.

[0036] With continuing reference to FIG. 3, a left-side data line 327 and a right-side data line 329 are each shown as being couplable to lower strings 320 of memory cells 323. The lower strings 320 include a number of the memory cells 323 couplable to a respective one of the left-side data line 327 and the right-side data line 329. Further, each of the memory cells 323 is coupled to a respective one of a number of access lines 339. The access lines 339 can each carry one of a signal WL0, WL1, WL2, and WL3 as further indicated in FIG. 3. The left-side data line 327 (to carry a signal BL(n)) and the right-side data line 329 (to carry a signal BL(n+1)) can each be coupled to a respective separate lower current-source 331 to provide current to the lower strings 320 of the memory cells 323.

[0037] The lower current-sources 331 can be coupled to a conductive line 333, which in turn may be coupled to a second supply node (e.g., V_{SS}). SGD select transistors 325 may have their respective gates coupled to each other and may be controlled (e.g., turned on or turned off) by a second signal SGD_L (e.g., a drain select-gate signal) on a lower SGD select line 341 (e.g., drain select line) of the memory array 300. During a memory operation (e.g., a read or write

operation) of the memory array 300, the signal SGD_L can control whether current is provided from the lower current-sources 331 to the strings 320 (e.g., through a respective one of the data lines 327, 329). Memory operations, including read operations, are described in more detail with reference to FIG. 4,
5 below.

[0038] As with the upper strings 310, the lower strings 320 are also depicted with only four memory cells 323 coupleable to a respective one of the data lines 327, 329; however, a larger or a smaller number of the memory cells 323 may be used in the lower strings 320. Also, the number of memory cells 323 in the
10 lower strings 320 may be different from the number of memory cells 311 in the upper strings 310.

[0039] As shown in FIG. 3, the common (e.g., source) node 319 may be coupled to the lower strings 320 by the operation of a lower SGS select-line 321 coupled to lower SGS select-transistors 315. The lower SGS select-transistors
15 315 may have their respective gates coupled to each other and may be controlled (e.g., turned on or turned off) by a signal SGS_L (e.g., a source select-gate signal) on the lower SGS select-line 321 (e.g., source select line) of the memory array 300.

[0040] Either or both of the upper SGS select-transistors 313 and the lower
20 SGS select-transistor 315 may be activated on the memory array 300. Thus, as indicated by FIG. 3, when activated, the upper strings 310 and the lower strings 320 may be coupled in series to each other through the common node 319 (e.g., a conductive line or other conductive structure). The common node 319 may comprise, for example, a common source (e.g., a source line, source slot, or
25 source diffusion region). As discussed in more detail below with reference to FIG. 5A and FIG. 5B, each of the data lines 303, 305, 327, 329 are coupled to a separate sense circuit. Thus the memory cells 311, 323 on both the left side strings and the right side strings may be operated on (e.g., read from) concurrently.

[0041] In an embodiment, the separate strings may be stacked in a three-dimensional memory device. Further, interconnect wiring within a physical memory array may be used to couple similar portions of the array together. For example, each of the access lines 337 coupled to the upper strings 310 may be coupled to respective ones of the access lines 339 coupled to the lower strings 320 through interconnect wiring. By electrically coupling the corresponding access lines 337, 339, a bias signal, for example, WL3, may be placed on each of the appropriate ones of the access lines substantially simultaneously.

[0042] As used herein, for example, with reference to FIG. 3, the terms “upper” and “lower,” “right” and “left,” “first,” “second,” “third,” and “fourth” are simply to aid a person of ordinary skill in the art in understanding the subject matter with respect to the Figures. Thus, the terms “upper” and “lower” do not necessarily relate to any particular physical placement in an actual circuit. For example, in some embodiments, the memory cells 311, 323 in each memory element 310, 320 can be physically located in multiple levels of the memory array 300, such that the memory cells 311, 323 can be stacked over each other in multiple levels of the memory array 300. In some embodiments, the memory cells 311 of the upper strings 310 can be physically located in the a first number of levels (e.g., levels 4-7) and the memory cells 323 of the lower strings 320 can be physically located in a second number of levels (e.g., levels 0-3).

[0043] With reference now to FIG. 4, the schematic circuit diagram 330 of FIG. 3 is shown, with current flow indicated during a read operation of the memory array 300. Various ones of the element numbers of FIG. 3 have been omitted so as not to obscure the conceptualization of current flow during the read operation.

[0044] FIG. 4 shows a first memory-cell string 401 and a second memory-cell string 403 as upper strings 310, and a third memory-cell string 405 and a fourth memory-cell string 407 as lower strings 320. With concurrent reference to FIG. 3 and FIG. 4, the first memory-cell string 401 comprises memory cells 311 couplable to the left-side data line 303 and the second memory-cell string 403 comprises memory cells 311 couplable to the right-side data line 305; with

both strings 401, 403 being located substantially parallel and adjacent to one another. The third memory-cell string 405 comprises memory cells 323 couplable to the left-side data line 327 and the fourth memory-cell string 407 comprises memory cells 323 couplable to the right-side data line 329, both
5 strings 405, 407 being located substantially parallel and adjacent to one another.

[0045] During a read operation, both of the strings 401, 405 couplable to the left-side data lines 303, 327 can be conductive at the same time, and/or both of the strings 403, 407 couplable to the right-side data lines 307, 329 can be conductive at the same time. For ease of understanding the description of read
10 operations that follow, one may assume that one or more of the memory cells 311, 323 in the first memory-cell string 401 and the third memory-cell string 405, both couplable to a respective one of the left-side data lines 303, 327, are to be read. It is noted that similar or identical operations can also be applied to one or more of the memory cells 311, 323 in the second memory-cell string 403 and the
15 fourth memory-cell string 407, both couplable to a respective one of the right-side data lines 305, 329.

[0046] Thus, to begin a read operation for memory cells in the strings 401, 405, the select transistors 309, 313, 315, 325 are activated (e.g., turned on) and a read current I_{LOAD} is provided through the first and third memory-cell strings
20 401 and 405. For each memory cell 311, 323 to be read in strings 401, 405, one or more of the signals WL0, WL1, WL2, and WL3 are asserted on corresponding ones of the access lines 337, 339.

[0047] With continuing reference to FIG. 4, during a read operation, a current $I_{CELL_TOTAL_UPPER}$ flows through the first memory-cell string 401 and a
25 current $I_{CELL_TOTAL_LOWER}$ flows through the third memory-cell string 405. As described in more detail below, during the read operation, the third memory-cell string 405 will receive at least a portion of the current flowing in the first memory-cell string 401.

[0048] As a first example, in a rare case (e.g., a degenerate case) where all
30 memory cells 311, 323 are conductive (e.g., they all store a value of "1"), then

substantially all of the current provided by I_LOAD flows through the first memory-cell string 401 and the third memory-cell string 405. For example, the total current, I_{DD_TOTAL}, flowing through the memory-cell strings 401, 405 in this example may be described using the following equation:

$$5 \quad I_{DD_TOTAL} = I_{CELL_TOTAL_UPPER} + I_{CELL_TOTAL_UPPER}.$$

[0049] This somewhat degenerate case of having all memory cells 311, 323 being conductive (e.g., all storing a value of “1”) presents the maximum total current flow, and consequently the highest energy usage, of the memory array 300. Thus, in this case, I_{DD_TOTAL} may be equal to or less than I_LOAD (e.g.,
 10 the maximum current that can be sourced). This maximum current flow, in this degenerate case, is approximately the same current flow used by the previously discussed ABL technique for any read operation, regardless of a stored value of the individual memory cells.

[0050] However, in cases where the memory cells of the memory array 300
 15 have stored a mixture of “0” values and “1” values, the total current, I_{DD_TOTAL}, may be much less than the cumulative value of current flowing through each of the memory-cell strings 401, 405 separately. For example, if the values stored within the cells being read causes more current to flow through the first memory-cell string 401 than through the third memory-cell string 405, such that:

$$20 \quad I_{CELL_TOTAL_UPPER} > I_{CELL_TOTAL_LOWER}; \text{ then}$$

$$I_{DD_TOTAL} = I_{CELL_TOTAL_UPPER}.$$

In this case, the total current flow, I_{DD_TOTAL}, is based on the current flow, I_{CELL_TOTAL_UPPER}, in the first memory-cell string 401 alone.

[0051] In another case however, where the values being read cause less
 25 current to flow through the first memory-cell string 401 than through the third memory-cell string 405:

$$I_{CELL_TOTAL_UPPER} < I_{CELL_TOTAL_LOWER}; \text{ and}$$

$$I_{DD_TOTAL} = I_{CELL_TOTAL_LOWER}.$$

Consequently, the total current flow, I_{DD_TOTAL} , is based on the current flow, $I_{CELL_TOTAL_LOWER}$, in the third memory-cell string 405 alone.

- [0052]** However, for reading stored data that are generally random in value,
 5 the total current flowing through each of the memory-cell strings 401, 405 may be approximately equal. That is:

$$I_{CELL_TOTAL_UPPER} \sim I_{CELL_TOTAL_LOWER}.$$

- Thus, in the case of random data, where the total current flowing through each of the memory-cell strings 401, 405 is approximately equal, the total current flow,
 10 I_{DD_TOTAL} is approximately half the maximum total current flow where the stored data are all at a value of “1” as discussed above.

- [0053]** In a specific example, to further aid in understanding the energy savings possible with the disclosed subject matter, assume 75% of the memory cells 311 in the first memory-cell string 401 have a stored value of “1.” Further
 15 assume that only 25% of the memory cells 323 in the third memory-cell string 405 have a stored value of “1.” Therefore, the first memory-cell string 401 has three times as many memory cells with a “1” value as the third memory-cell string 405. If 750 μ A flows through the first memory-cell string 401, then about one-third of that value (based on the ratio of “1” values stored in the first versus
 20 the third memory strings), or 250 μ A flows through the third memory-cell string 405. The remaining 500 μ A (e.g., the difference in current flow between the strings 401, 405) flows into the common node 319 (FIG. 3). In this example, since $I_{CELL_TOTAL_UPPER}$ is greater than $I_{CELL_TOTAL_LOWER}$; then I_{DD_TOTAL} equals $I_{CELL_TOTAL_UPPER}$. Consequently, I_{DD_TOTAL} equals 750 μ A.

- [0054]** As discussed above, the ABL technique sources the total amount of
 25 current for every read operation. Using the examples from the scenario described above, the ABL technique would source the total current flowing through both strings (750 μ A + 250 μ A) or 1 mA total, regardless of the data values stored in the memory cells. Thus, the ABL technique consumes 25%

more energy in this example than does the disclosed subject matter. Similar savings may be achieved in other scenarios.

[0055] FIG. 5A and FIG. 5B show exemplary current source and sense amplifier arrangements that may be used with the memory array 300 of FIG. 3.

5 An upper-circuit 500 may be used to source current to and sense the value of information stored in memory cells 311 of one of the upper strings 310 (e.g., one of the memory-cell strings 401 or 403). A lower circuit 550 may be used to source current to and sense the value of information stored in memory cells 323 in one of the lower strings 320 (e.g., one of memory-cell strings 405 or 407).

10 **[0056]** As shown, the upper circuit 500 includes a data enable element 501 coupled to, for example, the left-side data line 303, a power enable element 503, a sense amplifier 505, a data latch 507, and an input/output (I/O) enable element 509. The data enable element 501 clamps a data line (e.g., bit line) on which an operation is to be performed. The power enable element 503 may use a device
15 activated (e.g., turned on) by a negative bias, V_{REF_P} , being applied to the gate of the device. In a specific example, the power enable element 503 comprises a P-type metal-oxide semiconductor (PMOS) transistor.

[0057] A SENSE_EN signal activates the sense amplifier 505 for read operations. The sensed value is then temporarily stored in the data latch 507. As
20 shown, the data latch 507 may comprise a pair of cross-coupled inverters and may be used to temporarily store write data and read data until written in from or read out to an I/O buffer (not shown) through the I/O enable element 509. In some embodiments, other types of data latches may be employed.

[0058] The lower circuit 550 is similar in some respects to the upper circuit
25 500 described above and includes a data enable element 551 coupled to, for example, the left-side data line 327, a power enable element 553, a sense amplifier 555, a data latch 557, and an I/O enable element 559. Except for the power enable element 503 in circuit 500 and the power enable element 553 in circuit 550, each of the elements in the lower circuit 550 may be similar or
30 identical to the upper circuit 500.

[0059] The power enable element 553 may use a device activated (e.g., turned on) by a positive bias, V_{REF_N} , being applied to the gate of the device. Therefore, the operation of the power enable element 553 may be considered to be complementary (e.g., activated by a bias voltage of the opposite polarity) to the operation of the power enable element 503. In a specific example, the power enable element 553 comprises an N-type metal-oxide semiconductor (NMOS) transistor. Additional embodiments may be realized.

[0060] For example, FIG. 6 is a block diagram of an apparatus in the form of a system 600 with a memory device 609 that may include one or more of the various embodiments described herein. The system 600 is shown to include a controller 603, an input/output (I/O) device 611 (e.g., a keypad, a touchscreen, or a display), a memory device 609, a wireless interface 607, a static random access memory (SRAM) device 601, and a shift register 615, each coupled to each other via a bus 613. A battery 605 may supply power to the system 600 in one embodiment. The memory device 609 may include a NAND memory, a flash memory, a NOR memory, a combination of these, or the like.

[0061] The controller 603 may include, for example, one or more microprocessors, digital signal processors, micro-controllers, or the like. The memory device 609 may be used to store information transmitted to or by the system 600. The memory device 609 may optionally also be used to store information in the form of instructions that are executed by the controller 603 during operation of the system 600 and may be used to store information in the form of user data either generated, collected, or received by the system 600 (such as image data). The instructions may be stored as digital information and the user data, as disclosed herein, may be stored in one section of the memory as digital information and in another section as analog information. As another example, a given section at one time may be labeled to store digital information and then later may be reallocated and reconfigured to store analog information. The controller 603 may include one or more of the novel devices and structures described herein.

[0062] The I/O device 611 may be used to generate information. The system 600 may use the wireless interface 607 to transmit and receive information to and from a wireless communication network with a radio frequency (RF) signal. Examples of the wireless interface 607 may include an antenna, or a wireless
5 transceiver, such as a dipole antenna. However, the scope of the inventive subject matter is not limited in this respect. Also, the I/O device 611 may deliver a signal reflecting what is stored as either a digital output (if digital information was stored), or as an analog output (if analog information was stored). While an example in a wireless application is provided above, embodiments of the
10 inventive subject matter disclosed herein may also be used in non-wireless applications as well. The I/O device 611 may include one or more of the novel devices and structures described herein.

[0063] The various illustrations of the procedures and apparatuses are intended to provide a general understanding of the structure of various
15 embodiments and are not intended to provide a complete description of all the elements and features of the apparatuses and methods that might make use of the structures, features, and materials described herein. Based upon a reading and understanding of the disclosed subject matter provided herein, a person of ordinary skill in the art can readily envision other combinations and
20 permutations of the various embodiments. The additional combinations and permutations are all within a scope of the present invention.

[0064] The Abstract of the Disclosure is provided to comply with 37 C.F.R. §1.72(b), requiring an abstract allowing the reader to quickly ascertain the nature of the technical disclosure. The abstract is submitted with the understanding that
25 it will not be used to interpret or limit the claims. In addition, in the foregoing Detailed Description, it may be seen that various features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as limiting the claims. Thus, the following claims are hereby incorporated into the Detailed Description, with
30 each claim standing on its own as a separate embodiment.

CLAIMS

What is claimed is:

1. An apparatus, comprising:
 - 5 a first string of memory cells; and
 - a second string of memory cells, the second string of memory cells being configured to receive at least a portion of a current flowing in the first string of memory cells during a read operation.
- 10 2. The apparatus of claim 1, further comprising a common node coupled between the first string and the second string.
3. The apparatus of claim 2, wherein the common node comprises a common source.
- 15 4. The apparatus of claim 2, wherein the apparatus is configured to electrically couple the second string to the first string through the common node during a read operation.
- 20 5. The apparatus of claim 2, further comprising:
 - a first select transistor coupled to the first string; and
 - a second select transistor coupled to the second string.
6. The apparatus of claim 5, further comprising:
 - 25 a third select transistor coupled between the first string and the common node;
 - and
 - a fourth select transistor coupled between the second string and the common node.

7. The apparatus of claim 5, further comprising:
a first current source;
a first data line coupled to the first select transistor and the first current source,
wherein the first select transistor is configured to selectively couple
5 current provided by the first current source to the first string of memory
cells;
a second current source; and
a second data line coupled to the second select transistor and the second current
source, wherein the second select transistor is configured to selectively
10 couple current provided by the second current source to the second string
of memory cells.
8. The apparatus of claim 7, wherein the first current source comprises a first
power enable element coupled to the first data line and wherein the
15 second current source comprises a second power enable element coupled
to the second data line.
9. The apparatus of claim 8, wherein the first power enable element and the
second power enable element are configured to be activated by bias
20 voltages of opposite polarities.
10. The apparatus of claim 7, further comprising a first data enable element and
a second data enable element, wherein a first power element is coupled to
the first data line through the first data enable element and wherein a
25 second power element is coupled to the second data line through the
second data enable element.

11. The apparatus of claim 7, further comprising:
a first sense circuit coupled to the first data line; and
a second sense circuit coupled to the second data line.
- 5 12. The apparatus of claim 11, further comprising a first data enable element
and a second data enable element, wherein the first sense circuit is
coupled to the first data line through the first data enable element and
wherein the second sense circuit is coupled to the second data line
through the second data enable element.
- 10 13. The apparatus of claim 1, wherein the first string of memory cells and the
second string of memory cells are each configured to receive separate
currents.
- 15 14. The apparatus of claim 1, wherein each of the memory cells of the first
string are on a respective one of a first number of levels and wherein
each of the memory cells of the second string are on a respective one of a
second number of levels.
- 20 15. The apparatus of claim 14, further comprising:
a third string of memory cells; and
a fourth string of memory cells, a common node being coupled between the third
string of memory cells and the fourth string of memory cells, the fourth
string of memory cells being configured to receive at least a portion of a
25 current flowing in the third string of memory cells during a read
operation.

16. The apparatus of claim 15, wherein the apparatus is configured to couple the first string and the second string to each other in series during a concurrent read operation of the first string and the second string, and wherein the apparatus is configured to couple the third string and the fourth string to each other in series during a concurrent read operation of the third string and the fourth string.
17. The apparatus of claim 15, wherein the first string and the third string are adjacent to one another, and the second string and the fourth string are adjacent to one another.
18. The apparatus of claim 17, wherein each of the memory cells of the third string are on a respective one of the first number of levels and wherein each of the memory cells of the fourth string are on a respective one of the second number of levels.

19. The apparatus of claim 15, further comprising:
a first select transistor coupled to the first string;
a second select transistor coupled to the second string;
a third select transistor coupled to the third string;
5 a fourth select transistor coupled to the fourth string;
a first current source;
a second current source;
a third current source;
a fourth current source;
10 a first data line coupled to the first select transistor and the first current source,
wherein the first select transistor is configured to selectively couple
current provided by the first current source to the first string of memory
cells;
a second data line coupled to the second select transistor and the second current
15 source, wherein the second select transistor is configured to selectively
couple current provided by the second current source to the second string
of memory cells;
a third data line coupled to the third select transistor and the third current source,
wherein the third select transistor is configured to selectively couple
20 current provided by the third current source to the third string of memory
cells; and
a fourth data line coupled to the fourth select transistor and the fourth current
source, wherein the fourth select transistor is configured to selectively
couple current provided by the fourth current source to the fourth string
25 of memory cells.

20. The apparatus of claim 14, further comprising:
a third string of memory cells; and
a fourth string of memory cells, wherein each of the memory cells of the third
30 string are on a respective one of a third number of levels and wherein
each of the memory cells of the fourth string are on a respective one of a
fourth number of levels.

21. The apparatus of claim 1, wherein each of the memory cells within a string are located in different levels of the apparatus.
22. An apparatus comprising:
- 5 a number of first strings of memory cells each having a first end and a second end;
- a number of second strings of memory cells each having a first end and a second end, the second ends of the second strings being coupled to the second ends of the first strings at a common source; and
- 10 a separate data line coupled to each of the number of first strings and the number of second strings, each of the separate data lines being coupled to a separate sense circuit.
23. The apparatus of claim 22, further comprising a separate select transistor
- 15 coupled to each end of each of the strings of memory cells.
24. An apparatus comprising:
- upper strings of memory cells in a first number of levels and including at least a first memory string and a second memory string arranged substantially
- 20 parallel and adjacent to one another;
- lower strings of memory cells in a second number of levels located below the first number of levels and including at least a third memory string and a fourth memory string arranged substantially parallel and adjacent to one another, the upper strings and the lower strings being coupleable to each
- 25 other through a common node; and
- a separate sense circuit coupled to each of the memory strings.
25. The apparatus of claim 24, further comprising a separate current source coupled to each of the memory strings.
- 30
26. The apparatus of claim 24, wherein the upper strings and the lower strings are configured to be coupled to the common node by select transistors coupled to the memory strings.

27. The apparatus of claim 26, wherein the select transistors are configured to couple the first memory string to the third memory string and to separately couple the second memory string to the fourth memory string.

5

28. An apparatus comprising:
upper strings including:

a first string of memory cells and a second string of memory cells
arranged substantially parallel and adjacent to one another; and
10 a first sense circuit configured to be coupled to the first string of memory cells and a second sense circuit configured to be coupled to the second string of memory cells; and

lower strings including:

a third string of memory cells and a fourth string of memory cells
15 arranged substantially parallel and adjacent to one another; and
a third sense circuit configured to be coupled to the third string of memory cells and a fourth sense circuit configured to be coupled to the fourth string of memory cells, the first string of memory cells and the third string of memory cells being configured to be
20 coupled in series during a read operation and the second string of memory cells and the fourth string of memory cells being configured to be coupled in series during a read operation.

29. The apparatus of claim 28, wherein:
25 the first string of memory cells and the second string of memory cells are configured to be coupled to a first supply node by power enable elements activated by a bias voltage with a first polarity; and
the third string of memory cells and the fourth string of memory cells are configured to be coupled to a second supply node by power enable
30 elements activated by a bias voltage with a second polarity, the second polarity being opposite the first polarity.

30. The apparatus of claim 28, further comprising select transistors to separately couple the first string of memory cells and the third string of memory cells in series and the second string of memory cells and the fourth string of memory cells in series.
- 5
31. The apparatus of claim 30, wherein, during a read operation, the apparatus is configured to perform operations including:
- activating the select transistors to couple the first string of memory cells and the third string of memory cells in series;
- 10 coupling the first sense circuit and the third sense circuit to the first string of memory cells and the third first string of memory cells, respectively; and
- providing a read current through the first string of memory cells and through the third string of memory cells.
- 15 32. An apparatus comprising:
- a common node;
- a first string of memory cells and a second string of memory cells arranged substantially parallel and adjacent to one another;
- a third string of memory cells and a fourth string of memory cells arranged
- 20 substantially parallel and adjacent to one another;
- a first sense amplifier configured to be coupled to the first string of memory cells and a second sense amplifier configured to be coupled to the second string of memory cells;
- a third sense amplifier configured to be coupled to the third string of memory
- 25 cells and a fourth sense amplifier configured to be coupled to the fourth string of memory cells;
- first select transistors to couple the first string of memory cells and the second string of memory cells to the common node;
- second select transistors to couple the third string of memory cells and the fourth
- 30 string of memory cells to the common node; and
- a separate current source coupled to each of the memory strings.
33. The apparatus of claim 32, wherein:

the first string of memory cells and the second string of memory cells are
configured to be read from concurrently; and
the third string of memory cells and the fourth string of memory cells are
configured to be read from concurrently.

5

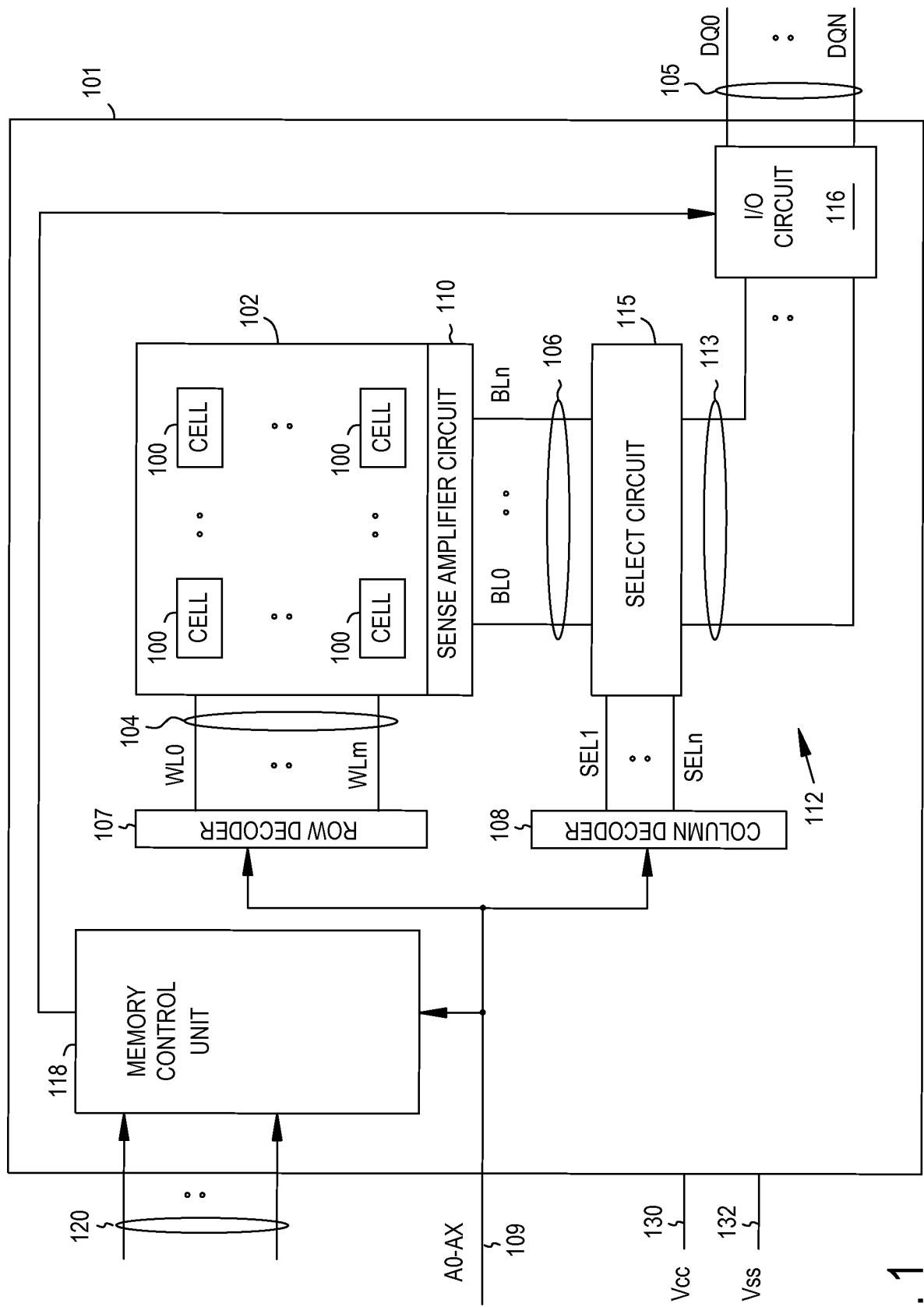


FIG. 1

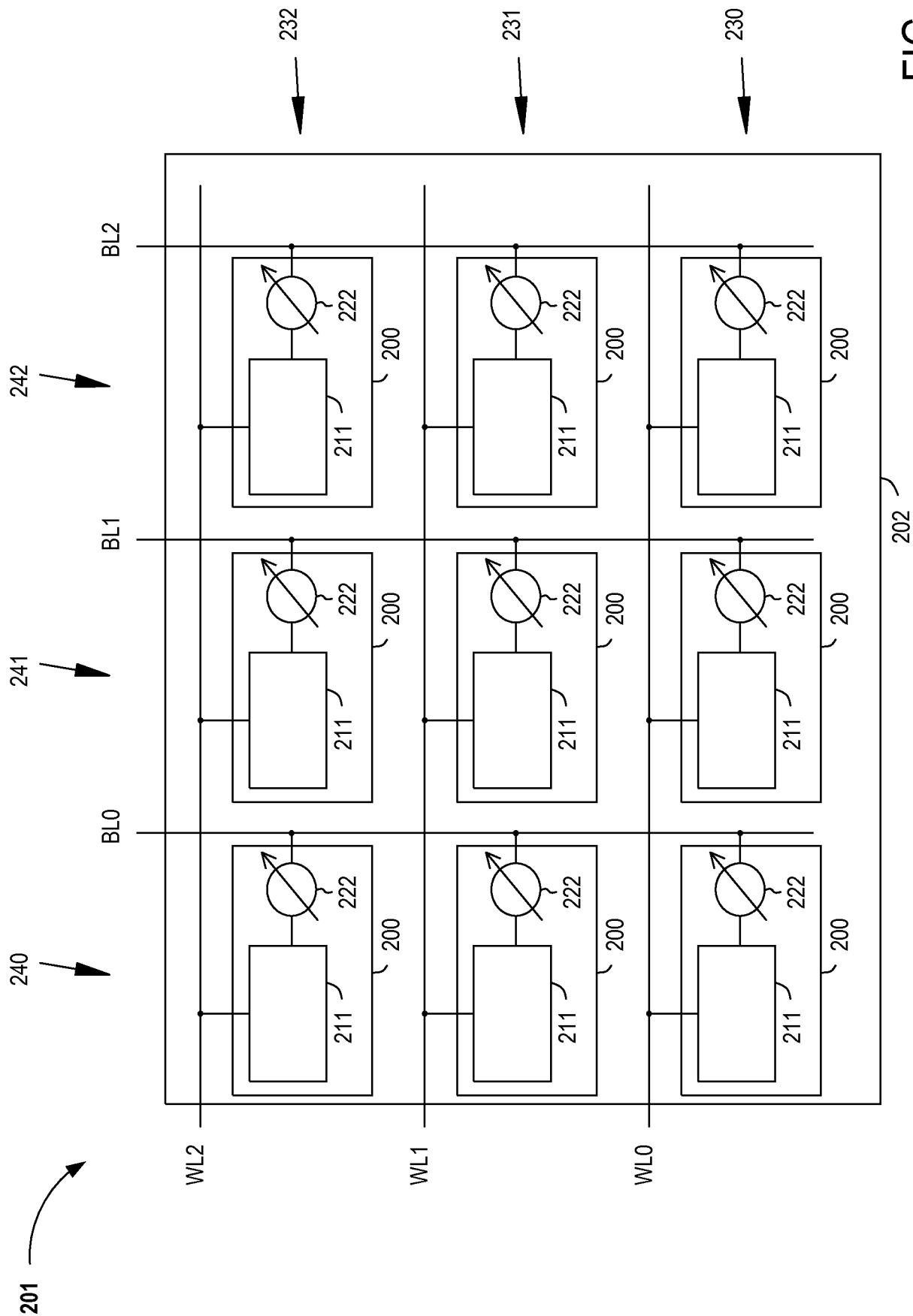


FIG. 2

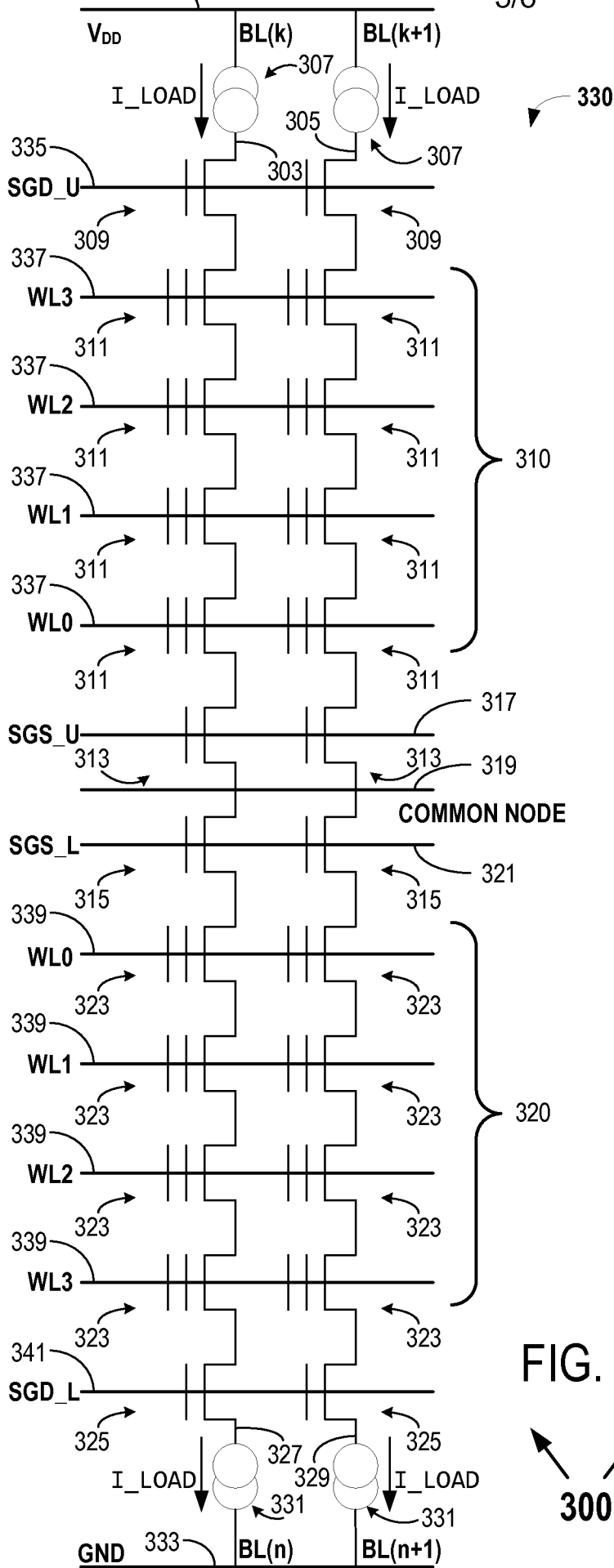
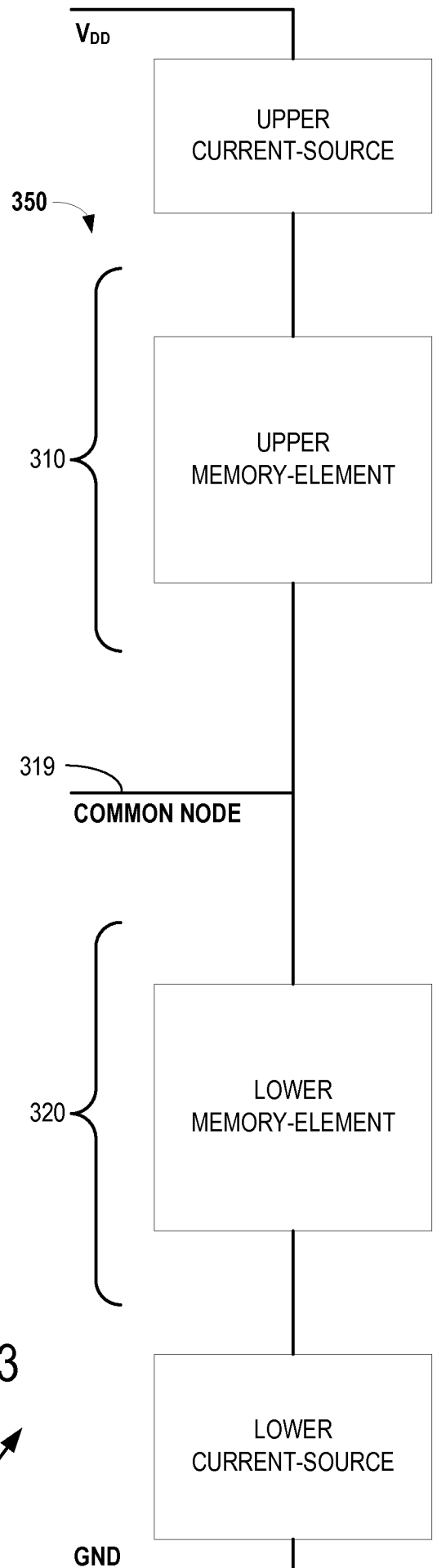


FIG. 3

300



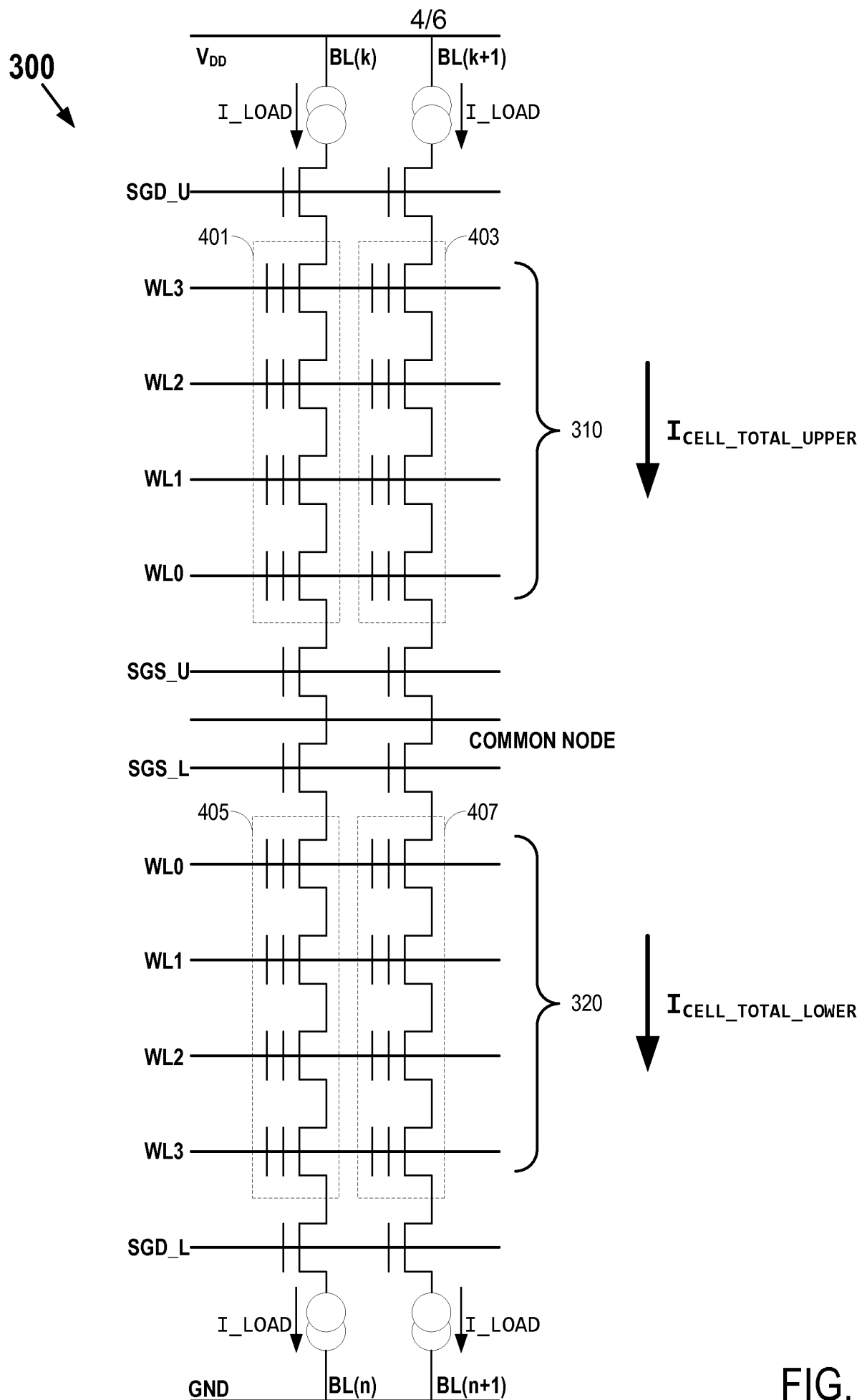


FIG. 4

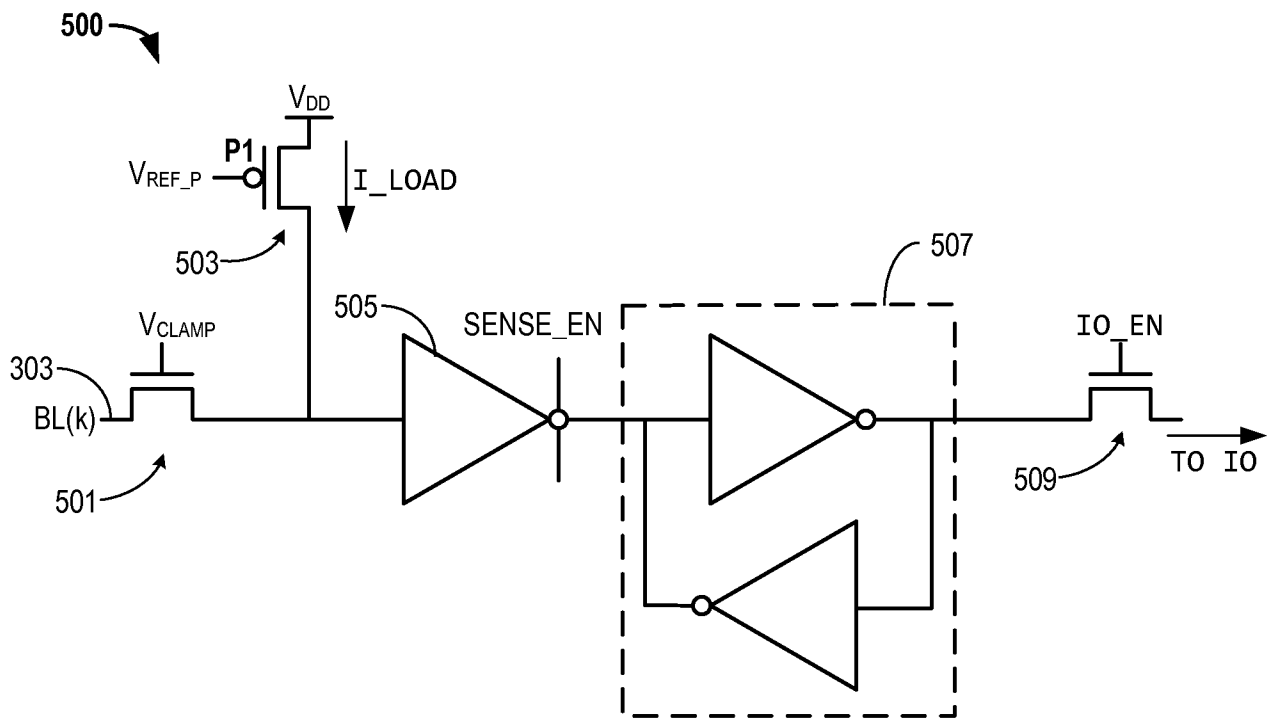


FIG. 5A

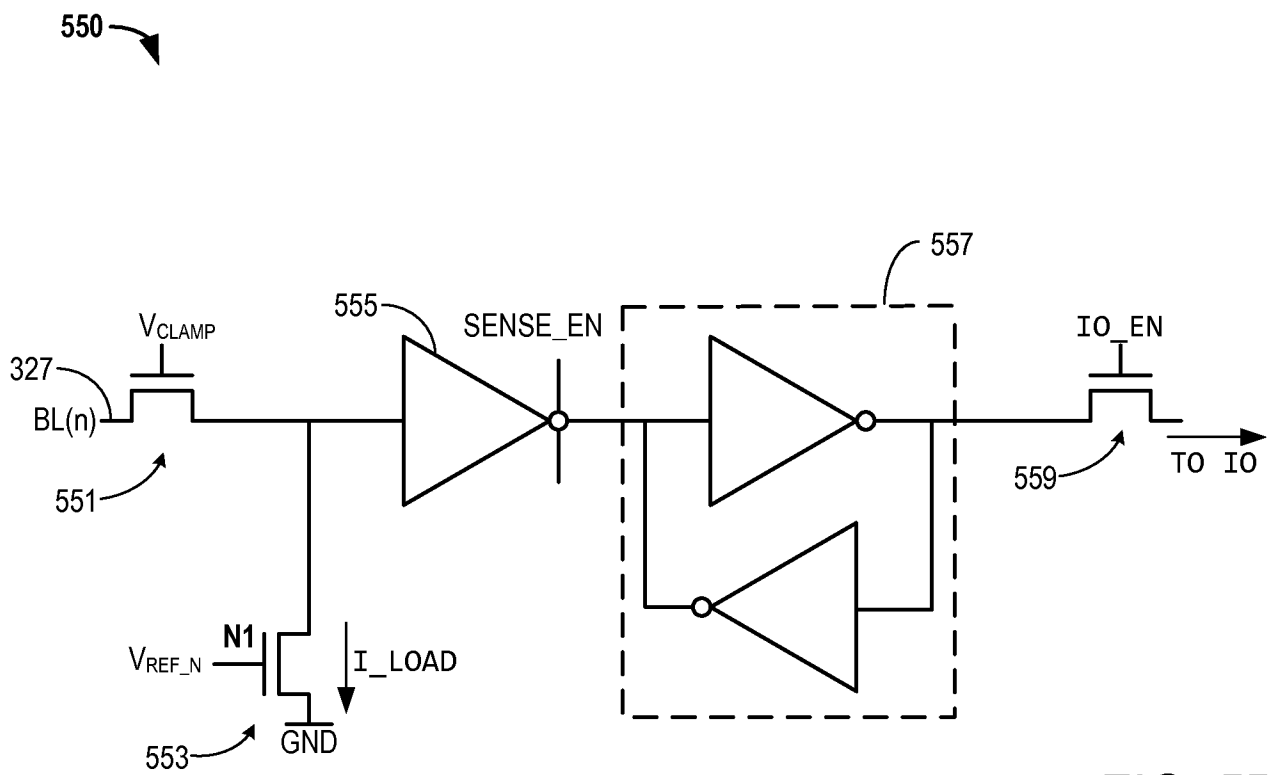
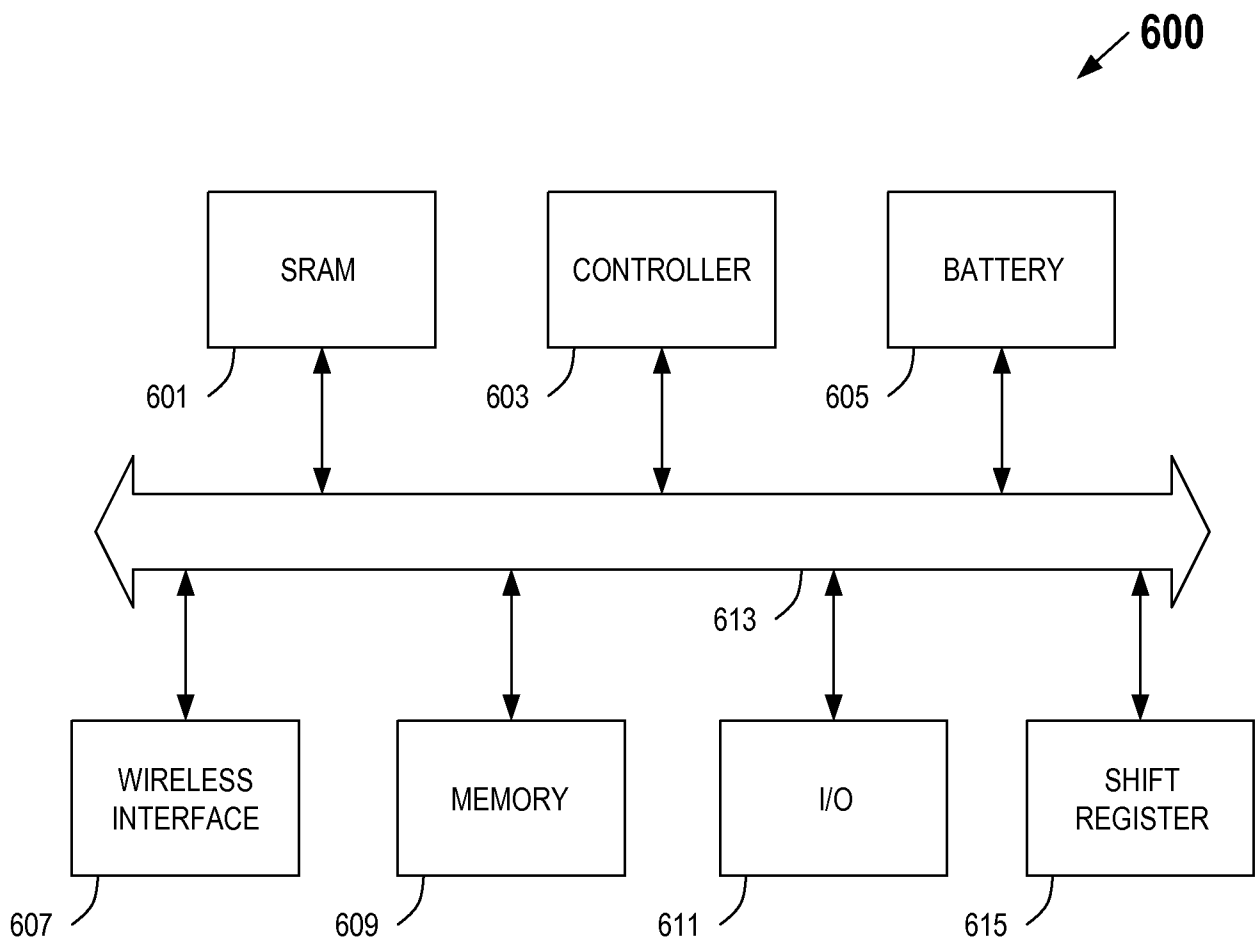


FIG. 5B

6/6

**FIG. 6**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/057362**A. CLASSIFICATION OF SUBJECT MATTER****G11C 16/02(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
G11C 16/02; G06F 11/07; G11C 16/04; G11C 17/16; G11C 7/00; H01L 29/792; G11C 16/06Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: 3D, memory string, upper, lower, separated sense amplifier, common node, and similar terms.**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0008400 A1 (YOSHIKI FUKUZUMI et al.) 12 January 2012 See paragraphs 37-51, 103-106; figures 1-3, 9; and claim 1.	1, 14, 20-21
A		2-13, 15-19, 22-33
A	US 2008-0205148 A1 (KAZUSHIGE KANDA) 28 August 2008 See paragraphs 34-48; figures 3-4; and claim 1.	1-33
A	US 2012-0198297 A1 (TAKESHI KAMIGAICHI et al.) 02 August 2012 See paragraphs 24-33; and figure 1.	1-33
A	US 2008-0181009 A1 (FUMITAKA ARAI et al.) 31 July 2008 See paragraphs 39-58; figures 1-2; and claim 1.	1-33
A	US 2002-0036936 A1 (JUNG HOON PARK et al.) 28 March 2002 See paragraphs 35-40; and figure 3.	1-33



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

06 December 2013 (06.12.2013)

Date of mailing of the international search report

09 December 2013 (09.12.2013)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/057362

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US 2002-0036936 A1	28/03/2002	DE 60136321 D1 EP 1191542 A2 EP 1191542 A3 EP 1191542 B1 JP 04435455 B2 JP 2002-117687 A KR 10-0407580 B1 KR 10-0428807 B1 TW 525167 A TW 525167 B US 6549461 B2	11/12/2008 27/03/2002 07/01/2004 29/10/2008 17/03/2010 19/04/2002 01/12/2003 29/04/2004 21/03/2003 21/03/2003 15/04/2003