635112

FORM 1
REGULATION 9

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952-1973

APPLICATION FOR A PATENT

We GEC PLESSEY TELECOMMUNICATIONS LIMITED

of New Century Park, P.O. Box 53, COVENTRY CV3 1HJ, GREAT BRITAIN

hereby apply for the grant of a Patent for an invention entitled:

METHOD AND APPARATUS FOR DETECTING A FRAME ALIGNMENT WORD IN A DATA STREAM

which is described in the accompanying complete specification. This Application is a Convention Application and is based on the Application numbered: 9004188.0 for a Patent or similar protection made in United Kingdom on 23 February 1990.

Our address for service is:

GRIFFITH HACK & CO
71 YORK STREET
SYDNEY NSW 2000

DATED this 20th day of February 1991

GEC PLESSEY TELECOMMUNICATIONS LIMITED
By their Patent Attorney

GRIFFITH HACK & CO

S020072 20/02/91

TO: THE COMMISSIONER OF PATENTS
COMMONWEALTH OF AUSTRALIA

2106A:rk

GPT/4114 AU

AUSTRALIA

PATENTS ACT 1952

B

APPLICATION BY ASSIGNEE OF INVENTOR

DECLARATION IN SUPPORT OF AN APPLICATION FOR A PATENT

NAME OF APPLICANT

In support of an application made by:
GEC PLESSEY TELECOMMUNICATIONS LIMITED,a British Company of New Century Park,P.O.Box 53, Coventry CV3 1HJ, England.

TITLE

for a patent for an invention entitled:
METHOD AND APPARATUS FOR DETECTING A FRAME ALIGNMENT WORD IN A DATA STREAM

FULL NAME AND ADDRESS OF SIGNATORY

I, COLIN FRANCIS HOSTE
of THE GENERAL ELECTRIC COMPANY PLC., PATENT DEPARTMENT, (WEMBLEY OFFICE) HIRST RESEARCH CENTRE, EAST LANE, WEMBLEY, MIDDX. HA9 7PP.

do solemnly and sincerely declare as follows:

1. I am authorised by the above mentioned applicant for the patent to make this declaration on its behalf.

FULL NAME AND ADDRESS OF INVENTOR(S)

2. The name and address of each actual inventor of the invention is as follows:
MARTIN REINHOLD ALEXANDER PAESLER,a British Subject of Plum Tree Cottage,Barton in Fabis,Nottingham NG11 OAA. (GB)
SOVER WING SAU WONG,a British Subject of 17 Elswick Drive, Beeston Rylands,Nottingham NG9 1NQ. (GB) respectively.

SEE NOTES OVER

3. The facts upon which the applicant is entitled to make this application are as follows: of the invention
By virtue of an Assignment/dated 5th February 1990.
From the Inventors to the above named applicant.

DELETE PARAGRAPHS 3 AND 4 FOR NON-CONVENTION APPLICATION

4. The basic application(s) as defined by Section 141 of the Act was (were) made as follows:
Country United Kingdom on 23rd February 1990
in the name(s) GEC PLESSEY TELECOMMUNICATIONS LIMITED
and in on
in the name(s)

PLACE AND DATE OF SIGNING

5. The basic application(s) referred to in the preceding paragraph was (were) the first application(s) made in a Convention country in respect of the invention the subject of this application.

For and on behalf of:
GEC PLESSEY TELECOMMUNICATIONS LTD.

Declared at Wembley, Middx. GB.
this 6th day of February 1991
Signed C. F. Hoste COLIN FRANCIS HOSTE
Position THEIR ATTORNEY.

GRIFFITH HACK & CO
PATENT AND TRADE MARK ATTORNEYS
MELBOURNE · SYDNEY · PERTH

AU9171240

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(54) Title
METHOD AND APPARATUS FOR DETECTING A FRAME ALIGNMENT WORD IN A DATA STREAM

International Patent Classification(s)
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(56) Prior Art Documents
GB 1069538
US 4943985
US 4835768

(57) Claim

1. Apparatus for detecting a frame alignment word in a time division multiplex data stream comprising storage means having a plurality of serial locations arranged to receive an ATDM data stream and pass each bit of the data stream serially through each location, and template pattern means connected to said storage means and arranged to provide a template pattern corresponding to a frame alignment word, and wherein said template pattern means is arranged in a plurality of bit groups, each bit group generating an output signal when it identifies a group of bits corresponding to its portion of the whole template pattern, a decoder circuit being connected to the bit groups to receive the output signals from the bit groups and generate a decoder output signal indicating frame alignment when a specified number of bit groups, which is less than or equal to the total number of bit groups, give output signals indicating that they have identified the groups of bits associated with them, wherein once a frame alignment word has been detected and frame alignment has been confirmed, the number of template pattern groups used to monitor said storage means is reduced in number whereby a defined lesser part of the total storage means is monitored by the template pattern means.

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6. A method of detecting a frame alignment word in a time division multiplex data stream, the method comprising the steps of passing the data stream through each bit location of a serial storage means, and checking the bits against a template pattern, the method being further characterised in that the template pattern is split into a predetermined number of bit groups and the detection of the frame alignment word is confirmed when a predetermined number of the bit groups indicate that they have detected a match in the data stream, and in that when detection of a frame alignment word has been confirmed, reaffirmation of frame alignment is provided by confirmatory outputs of a reduced number of the bit groups.

635112

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PATENTS ACT 1952 Form 10

SUBSTITUTE COMPLETE SPECIFICATION

(ORIGINAL)

FOR OFFICE USE

Short Title:

Int Cl:

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Lodged:

Complete Specification-Lodged:
Accepted:
Lapsed:
Published:

Priority:

Related Art:

TO BE COMPLETED BY APPLICANT

Name of Applicant: GEC PLESSEY TELECOMMUNICATIONS LIMITED

Address of Applicant: New Century Park, P.O. Box 53, COVENTRY CV3 1HJ, GREAT BRITAIN

Actual Inventor: Martin Reinhold Alexander Paesler and Sover Wing Sau Wong

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71 YORK STREET
SYDNEY NSW 2000

Complete Specification for the invention entitled:

METHOD AND APPARATUS FOR DETECTING A FRAME ALIGNMENT WORD IN A DATA STREAM

The following statement is a full description of this invention, including the best method of performing it known to us:-

GH&CO REF: 20319-R:COS:RK

2106A:rk

GPT/4114 ALL

METHOD AND APPARATUS FOR DETECTING A FRAME ALIGNMENT WORD IN A DATA STREAM

The present invention relates to a method and apparatus for detecting a frame alignment word in a data stream.

The invention finds utility in digital multiplex systems, and is generally applicable to digital communication systems where the detection of specific, recurring binary sequences is required under condition of medium to high binary error ratios.

In digital multiplex systems several independent tributary data streams are combined to a higher rate aggregate bit sequence. A specific set of characters, known as the Frame Alignment Word (FAW), is then inserted at regular intervals into the bit sequence of the aggregate signal prior to transmission. The FAW together with the subsequent bit sequence up to the start of the next FAW constitutes a digital frame.

At the demultiplexer, the received binary data is initially examined on a bit-by-bit basis until a FAW has been correctly detected. This process is known as Frame Search. When the frame search is complete a new digital frame is constructed which is a replica of the originally transmitted digital frame, the transmitted and received digital frames are then said to be in alignment. When the demultiplexer frame is in alignment the inverse of the multiplex procedures can be applied to reconstitute the original data streams.

In order to maintain correct operation of the demultiplexer it is necessary to continuously check the occurrence of a FAW in the expected position in the digital sequence to confirm that frame

alignment is being maintained. When the check procedure indicates loss of alignment a new frame search is initiated.

In practical digital transmission systems binary errors cause the corruption of the FAWs resulting in failure to recognise the FAW during frame alignment procedures and spurious detection of misalignment when the digital frame is already aligned. The probability of a corrupted FAW is dependent on the binary error ratio and the number of bits which constitute the FAW. The larger the error ratio and the number of bits in the FAW the greater the probability of corruption.

In many applications the FAW is constructed to give a sufficiently long binary sequence so that the probability of its pattern being simulated by a combination of data bits within the digital frame is negligibly small. Therefore a demultiplexer can readily identify a FAW within the received signal, using a template matching technique. By this technique the incoming data stream is compared, on a bit-by-bit basis, against a template pattern of the FAW; if there is a match between the incoming stream and the template pattern, then a FAW is declared as recognised.

If the detection of the FAW is based on an exact match between the incoming data stream and the FAW template pattern, it cannot recognise valid FAWs if they have been corrupted by digital errors. Under such conditions, the demultiplexer cannot achieve rapid frame alignment or, in the case of higher error rates, may be subject to frequent spurious realignment thus greatly increasing the impairment of the received digital signal.

It is an object of the invention to significantly enhance the frame alignment performance of demultiplexers in conditions of high error rates by applying specific error tolerant FAW detection procedures.

According to the present invention there is provided apparatus for detecting a frame alignment word in a data stream, comprising storage means having a plurality of serial locations arranged to receive an ATDM data stream and pass each bit of the data stream serially through each location, and template pattern means connected to said storage means and arranged to provide a template pattern corresponding to a frame alignment word, and wherein said template pattern means is arranged in a plurality of bit groups, each bit group generating an output signal when it identifies a group of bits corresponding to its portion of the whole template pattern, a decoder circuit being connected to the bit groups to receive the output signals from the bit groups and generate a decoder output signal indicating frame alignment when a specified number of bit groups, which is less than or equal to the total number of bit groups, give output signals indicating that they have identified the groups of bits associated with them, wherein once a frame alignment word has been detected and frame alignment has been confirmed, the number of template pattern groups used to monitor said storage means is reduced in number whereby a defined lesser part of the total storage means is monitored by the template pattern means.

Preferably first and second decoder circuits are provided, said first decoder circuit being connected to those template bit groups connected to the defined lesser part of said storage means and said second decoder circuit being connected to all of said template bit groups. Optionally the outputs of said first and second decoder circuits are connected to a selector circuit which indicates that a frame alignment word has been detected. Optionally the selector circuit comprises first and second AND-gates connected to an OR-gate, the output of said first decoder circuit being connected to first said AND-gate and the output of said second decoder circuit being connected to said second AND-gate circuit. Optionally an enabling signal is connected to an additional input of each of said first and second AND-gates, the input of said first AND-gates to which said enabling signal is applied being an inverting input.

According to a further aspect of the present invention there is provided a method of detecting a frame alignment word in a time division multiplex data stream, the method comprising the steps of passing the data stream through each bit location of a serial storage means, and checking the bits against a template pattern, the method being further characterised in that the template pattern is split into a predetermined number of bit groups and the detection of the frame alignment word is confirmed when a predetermined number of the bit groups indicate that they have detected a match in the data stream, and in that when detection of a frame alignment word has been confirmed, reaffirmation of frame alignment is provided by confirmatory outputs of a reduced number of the bit groups.

An embodiment of the present invention will now be described with reference to the accompanying drawing wherein:

Figure 1 shows a FAW detection template pattern,

Figure 2 shows a reduced FAW detection template pattern,

Figure 3 shows a block diagram of the circuits which implement the invention, and,

Figure 4 shows a block circuit diagram of a decoder.

Referring to Figure 1, a FAW detection template pattern is shown divided into groups 1 to 8.

A FAW is considered as correctly recognised and valid if any seven out of the eight groups are unambiguously detected and free of error. This FAW detection algorithm can be represented in the form of a truth table as shown in Table 1.

Table 1:

Groups								FAW detected
1	2	3	4	5	6	7	8	
M	M	M	M	M	M	M	M	YES
D	M	M	M	M	M	M	M	YES
M	D	M	M	M	M	M	M	YES
M	M	D	M	M	M	M	M	YES
M	M	M	D	M	M	M	M	YES
M	M	M	M	D	M	M	M	YES
M	M	M	M	M	D	M	M	YES
M	M	M	M	M	M	D	M	YES
M	M	M	M	M	M	M	D	YES
All other combinations								NO

M = all bits matched:- group matched

D = one or more bits do not match:- group not matched

When the demultiplexer has previously achieved frame alignment the FAW detection template pattern is reduced to only the middle four groups, 3, 4, 5 and 6 as shown in Figure 2.

During the check procedure in the alignment mode the FAW is considered to be valid if any three out of four groups are unambiguously recognised and free of error. The states of groups 1, 2, 7 and 8 are not taken into account. This FAW checking algorithm can be represented in a truth table as shown in Table 2.

Table 2:

Groups								FAW detected
1	2	3	4	5	6	7	8	
X	X	M	M	M	M	X	X	YES
X	X	D	M	M	M	X	X	YES
X	X	M	D	M	M	X	X	YES
X	X	M	M	D	M	X	X	YES
X	X	M	M	M	D	X	X	YES
All other combinations								NO

M = all bits matched:- group matched

D = one or more bits do not match:- group not matched

X = irrelevant

A block schematic for a specific implementation of the present invention is shown in Figure 3, and its operation is described as follows:

The incoming data is shifted on a bit-by-bit basis through a serial shift register 9. The contents of the shift register 9 is continuously

compared with the template pattern, a preset data pattern, by eight 'AND' functions 10, where each of the 'AND' functions relates to a particular group of digits in the template pattern. When the incoming data and the corresponding group in the template pattern match the 'AND' function indicates 'TRUE'. In the Search Mode outputs of the 'AND' functions are evaluated according to the truth table as given in Table 1 by using the DECODER B 12. When a FAW has been detected 12 generates a 'TRUE' signal which is output to the FRAME SEARCH selector 13.

In the Aligned Mode the outputs of the appropriate 'AND' functions are evaluated according to the truth table as given in Table 2 by using the DECODER A 11. When a FAW has been detected 11 generates a 'TRUE' signal which is output to 13.

The output of 13 is selected according to the current state of the demultiplexer i.e. alignment or search mode.

Referring to Figure 4, a block circuit diagram is shown of the decoder A, depicted in Figure 3. It will be appreciated that the decoder B is composed of similar elements except it will comprise eight inputs in all. The decoder A comprises four inputs A, B, C and D, each of which is directly applied to a respective AND-gate. Each input is also inverted by a respective inverter 14 to 17. Input A is applied directly to AND-gates 18 to 21, and the inverse input is applied to AND-gate 22. Input B is applied directly to AND-gates 18 to 20 and 22 and the inverse input applied to AND-gate 21. Input C is applied directly to AND-gate 18, 19, 21 and 22 and the inverse input is applied to AND-gate 20. Input D is applied to AND-gate 18, 20 to 22 and the inverse input is applied to AND-gate 19. The outputs from the AND-gates 18 to 22 are

applied to an OR-gate 23 which provides the output signal Q. The truth table for decoder A is shown below:

A	B	C	D	Q
1	1	1	1	1
0	1	1	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	1
other combinations				0

The truth table for decoder B is shown below:

A	B	C	D	E	F	G	H	Q
1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1
1	1	1	1	0	1	1	1	1
1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	0	1
other combinations								0

The above description has been of one embodiment of the present invention and is not intended to be limited thereto. It will

readily be appreciated by those skilled in the art that alternative applications are possible, such as in the recognition of specific binary bit sequences required when the digital signal is subject to binary errors.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. Apparatus for detecting a frame alignment word in a time division multiplex data stream comprising storage means having a plurality of serial locations arranged to receive an ATDM data stream and pass each bit of the data stream serially through each location, and template pattern means connected to said storage means and arranged to provide a template pattern corresponding to a frame alignment word, and wherein said template pattern means is arranged in a plurality of bit groups, each bit group generating an output signal when it identifies a group of bits corresponding to its portion of the whole template pattern, a decoder circuit being connected to the bit groups to receive the output signals from the bit groups and generate a decoder output signal indicating frame alignment when a specified number of bit groups, which is less than or equal to the total number of bit groups, give output signals indicating that they have identified the groups of bits associated with them, wherein once a frame alignment word has been detected and frame alignment has been confirmed, the number of template pattern groups used to monitor said storage means is reduced in number whereby a defined lesser part of the total storage means is monitored by the template pattern means.

2. Apparatus as claimed in Claim 1 wherein first and second decoder circuits are provided, said first decoder circuit being connected to those template bit groups connected to the defined lesser part of said storage means and said second decoder circuit being connected to all of said template bit groups.

3. Apparatus as claimed in Claim 2 wherein the outputs of said first and second decoder circuits are connected to a selector circuit which indicates that a frame alignment word has been detected.

4. Apparatus as claimed in Claim 3 wherein the selector circuit comprises first and second AND-gates connected to an OR-gate, the output of said first decoder circuit being connected to first said AND-gate and the output of said second decoder circuit being connected to said second AND-gate circuit.

5. Apparatus as claimed in Claim 4 wherein an enabling signal is connected to an additional input of each of said first and second AND-gates, the input of said first AND-gate to which said enabling signal is applied being an inverting input.

6. A method of detecting a frame alignment word in a time division multiplex data stream, the method comprising the steps of passing the data stream through each bit location of a serial storage means, and checking the bits against a template pattern, the method being further characterised in that the template pattern is split into a predetermined number of bit groups and the detection of the frame alignment word is confirmed when a predetermined number of the bit groups indicate that they have detected a match in the data stream, and in that when detection of a frame alignment word has been confirmed, reaffirmation of frame alignment is provided by confirmatory outputs of a reduced number of the bit groups.

7. Apparatus for detecting a frame alignment word in a time division multiplex data stream substantially as hereinbefore described with reference to the accompanying drawings.

8. A method of detecting a frame alignment word in a time division multiplex data stream substantially as hereinbefore described with reference to the accompanying drawings.

DATED this 14th day of January 1993

GEC PLESSEY TELECOMMUNICATIONS LIMITED

By their Patent Attorneys

GRIFFITH HACK & CO.

Fig.1.

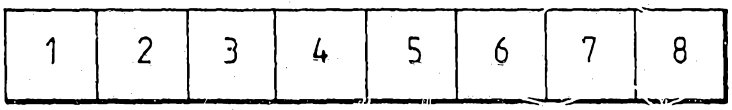

Fig.2.

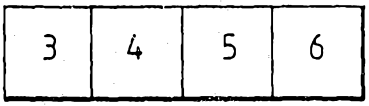

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Fig. 3.

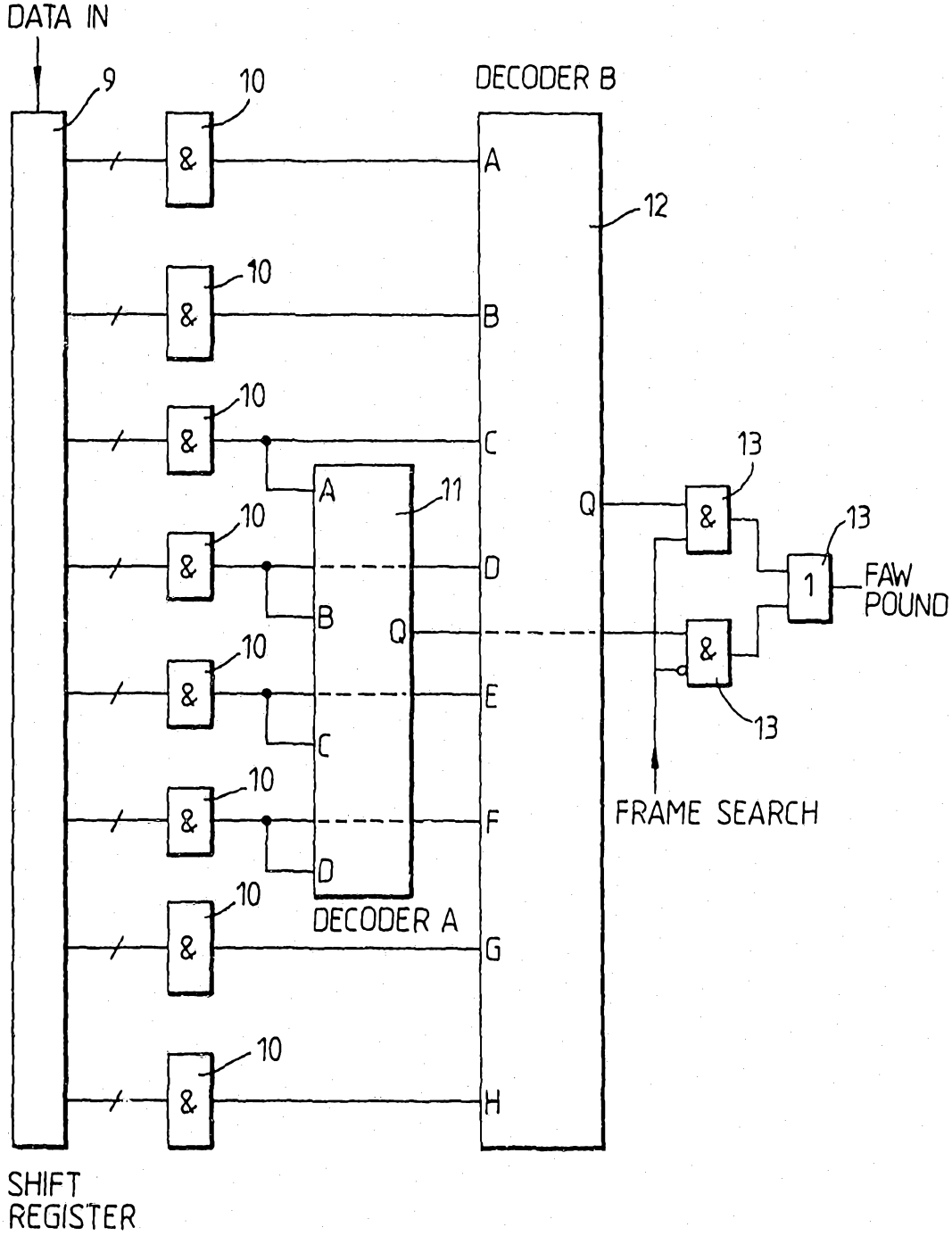

Fig.4.