(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 January 2008 (17.01.2008)

PCT

(10) International Publication Number
WO 2008/008630 A2

(51) International Patent Classification: Not classified

(21) International Application Number:
PCT/US2007/072301

(22) International Filing Date: 28 June 2007 (28.06.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/479,697 30 June 2006 (30.06.2006) US

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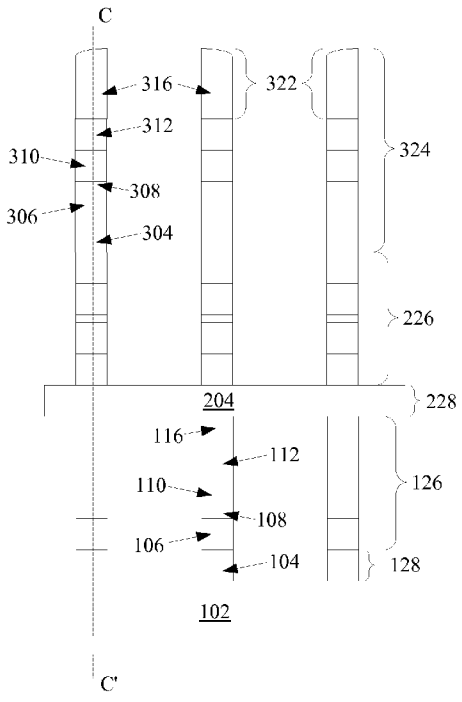
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: HIGHLY DENSE MONOLITHIC THREE DIMENSIONAL MEMORY ARRAY AND METHOD FOR FORMING



(57) Abstract: A method to form a highly dense monolithic three dimensional memory array is provided. In preferred embodiments, conductive or semiconductor spacers can be formed, then used as hard masks to pattern underlying layers, forming features at sublithographic pitch. Methods of the invention minimize photomasking steps and thus simplify fabrication.

WO 2008/008630 A2

Published:

— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

HIGHLY DENSE MONOLITHIC THREE DIMENSIONAL MEMORY ARRAY AND METHOD FOR FORMING

BACKGROUND OF THE INVENTION

[0001] The invention relates to a method to form a highly dense monolithic three dimensional memory array, the array comprising multiple memory levels formed in layers deposited above a substrate.

[0002] Monolithic three dimensional memory arrays are known, as in Johnson et al., US Patent No. 6,034,882, "Vertically stacked field programmable nonvolatile memory and method of fabrication"; Knall et al., US Patent No. 6,420,215, "Three Dimensional Memory Array and Method of Fabrication"; Vyvoda et al. (MA-075); and Herner et al., US Patent No. 6,952,030, "High-Density Three-Dimensional Memory Cell," *inter alia*.

[0003] In these memory arrays, memory cell size is limited by the size of features that can be defined using conventional photolithographic techniques. Fabrication of these memory arrays can be complex.

[0004] It would thus be advantageous to increase the density of such arrays and to reduce their cost and complexity.

SUMMARY OF THE PREFERRED EMBODIMENTS

[0005] The present invention is defined by the following claims, and nothing in this section should be taken as a limitation on those claims. In

general, the invention is directed to a highly dense monolithic three dimensional memory array and methods to form such an array.

[0006] A first aspect of the invention provides for a method for forming a first memory level, the method comprising: forming a plurality of substantially parallel, substantially coplanar first rails of a first layer or layerstack, the first rails above underlying layers; conformally depositing a second layer or layerstack on the first rails; etching the second layer or layerstack to form first spacers of the second layer or layerstack; removing the first rails; and etching the underlying layers self-aligned with the first spacers, wherein the first spacers serve as hard masks during the etching step. A hard mask is a material other than photoresist that serves to pattern underlying materials during an etch step. In various embodiments, the underlying layers are semiconductor layers and conductor layers, and are etched into substantially parallel rails or pillars.

[0007] Another aspect of the invention provides for a method for forming a monolithic three dimensional memory array above a substrate, the method comprising: depositing a first conductor layer or layerstack; depositing a first semiconductor layerstack comprising a first state-change layer, the first semiconductor layerstack above the first conductor layer or layerstack; depositing a first sacrificial material above the first semiconductor layer or layerstack; patterning and etching the first sacrificial material to form first sacrificial rails; conformally depositing a second layer or layerstack on the first sacrificial rails; etching the second layer or layerstack to form first spacers; removing the first sacrificial rails; and etching the first semiconductor layerstack and the first conductor layer or layerstack to form first memory material rails wherein the first spacers serve as hard masks during the step of etching first memory material rails.

[0008] Yet another aspect of the invention provides for a monolithic three dimensional memory array above a substrate comprising: a first plurality of substantially parallel, substantially coplanar conductors extending in a first direction; a second plurality of substantially parallel, substantially coplanar conductors extending in a second direction different from the first direction, the second conductors above the first conductors; a first plurality of pillars, each first pillar disposed between one of the first conductors and one of the second conductors, each first pillar having two substantially vertical sides aligned with sidewalls of one of the first conductors, and each first pillar having two substantially vertical sides aligned with sidewalls of one of the second conductors, wherein the first conductors have a pitch of about 300 nm or less.

[0009] Each of the aspects and embodiments of the invention described herein can be used alone or in combination with one another.

[0010] The preferred aspects and embodiments will now be described with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Fig. 1 is a perspective view illustrating feature size, gap size, and pitch in repeated features.

[0012] Figs. 2a-2e are cross-sectional views illustrating stages in formation of features formed at sizes smaller than photolithographic limits according to the present invention.

[0013] Figs. 3a-3j are cross-sectional views illustrating stages in formation of a monolithic three dimensional memory array formed according to a preferred embodiment of the present invention. Figs. 3e and 3f show the

structure at the same stage from perpendicular views, as do Figs. 3g and 3h, and Fig. 3i and 3j.

[0014] Figs. 4a-4d are cross-sectional views illustrating stages in formation of the final memory level according to a preferred embodiment of the present invention.

[0015] Figs. 5a and 5b are cross-sectional views illustrating stages in formation of a first memory level according to an alternative embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0016] A monolithic three dimensional memory array is one in which multiple memory levels are formed above a single substrate, such as a wafer, with no intervening substrates. The layers forming one memory level are deposited or grown directly over the layers of an existing level or levels. In contrast, stacked memories have been constructed by forming memory levels on separate substrates and adhering the memory levels atop each other, as in Leedy, US Patent No. 5,915,167, "Three dimensional structure memory." The substrates may be thinned or removed from the memory levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three dimensional memory arrays.

[0017] A monolithic three dimensional memory array formed above a substrate comprises at least a first memory level formed at a first height above the substrate and a second memory level formed at a second height different from the first height. Three, four, eight, or indeed any number of memory levels can be formed above the substrate in such a multilevel array.

[0018] A nonvolatile memory cell can be formed by disposing a non-linear electronic device like a diode, a MOS transistor, or a bipolar transistor, and a state-change element between conductors. The data state of the memory cell (data "0" or "1", for example) can be stored in the state of the state-change element. A state-change element is an element that can be changed between two or more readily detectable states. The difference in state may be detected as a difference in electrical resistance or current flow. A state-change element may be, for example, a fuse, an antifuse (such as a dielectric rupture antifuse), or may be formed of a material having variable or switchable resistivity, such as a chalcogenide, perovskites, or a binary metal oxide or nitride. The change in state can be permanent (as in a fuse or antifuse), forming a one-time-programmable memory cell; or reversible, forming a rewriteable memory cell.

[0019] By including a diode, or some other device exhibiting non-ohmic conduction characteristics, such memory cells can be formed in a large memory array. A diode provides electrical isolation, allowing a memory cell to be read or programmed without inadvertently programming adjacent cells sharing the same bitline or wordline.

[0020] Using methods according to the present invention, a highly dense monolithic three dimensional memory can be formed with a minimized number of photomasking steps and simplified construction.

[0021] The *feature size* is the smallest feature or gap in an integrated circuit that is patterned by photolithographic means. In a repeated pattern, the *pitch* is the distance between adjacent recurrences of the same feature. For example, as shown in Fig. 1, in an array of substantially parallel rails separated by gaps, the width F of a rail, or the width G of a gap, is the feature size, while the distance P from the center of one rail to the next is the pitch. It will be seen that when

patterned features and gaps between them have the same width, pitch will be twice the feature size.

[0022] Using methods of the present invention, a memory array can be formed having a pitch substantially less than twice the feature size, and features can be formed having dimensions below photolithographic limits.

[0023] Fig. 2a shows deposited layerstack 10 including layers which will be patterned to form semiconductor devices. Layerstack 10 may comprise layers of metal, silicon or other semiconductor material, grown or deposited dielectrics, etc. Sacrificial material 12 is deposited on layerstack 10.

[0024] As shown in Fig. 2b, sacrificial material 12 is patterned and etched, using conventional photolithographic and etch techniques, to form parallel rails 14, shown here in cross-section. Rails 14 extend out of the page. Suppose the width F of each rail is 55 nm, and the width G of gaps between them is 105 nm, for a pitch P1 of 160 nm. These drawings are not to scale.

[0025] In Fig. 2c, a conductive material 16 is conformally deposited over rails 14. In this example the thickness of conductive material 16 is 25 nm. In Fig. 2d, an anisotropic etch is performed, etching conductive material 16 vertically but with little or no lateral etch component. This etch thus removes conductive material 16 from horizontal surfaces on and between rails 14, leaving spacers 18.

[0026] Finally, as in Fig. 2e, sacrificial rails 14 are removed, and spacers 18 serve as hard masks during a subsequent etch of underlying layerstack 10 into parallel rails 20. Rails 20 have a width of 25 nm and are formed at a pitch P2 of 80 nm. The pitch P1 of rails 14 of Fig. 2b is 80 nm, which is one-half the pitch P2 (160 nm) of original rails 14 in Fig. 2b, and is substantially less than double the feature size of patterned rails 14, which was 55 nm. Pitch P1 of rails 14 is

shown in Fig. 2e for reference, though these rails were removed in an earlier step.

[0027] In this example, the gap width G and feature size F of rails were selected so that spacers 18 are evenly spaced at pitch P2. This arrangement is frequently advantageous, but not necessary; the relationship of gap width and feature size can be adjusted as desired. In this example, material 16 was described as conductive, and can act as an electrical interconnect to a patterned device. Depending on the structure to be formed, however, material 16, which will form the spacers 18, need not be conductive; it may be semiconductor material or a dielectric instead.

[0028] As will be described, in embodiments of the present invention, the methods illustrated in Figs. 2a-2e can be used iteratively to pattern and etch rails and pillars in a monolithic three dimensional memory array.

DETAILED EXAMPLE

[0029] A detailed example of fabrication of a monolithic three dimensional memory array formed according to a preferred embodiment of the present invention will be provided. For completeness, many materials, conditions, and steps will be described. It will be understood, however, that many of these details can be modified, augmented, or omitted while the results fall within the scope of the invention.

[0030] Turning to Fig. 3a, formation of the memory begins with a substrate 100. This substrate 100 can be any semiconducting substrate as known in the art, such as monocrystalline silicon, IV-IV compounds like silicon-germanium or silicon-germanium-carbon, III-V compounds, II-VII compounds, epitaxial layers over such substrates, or any other semiconducting material. The substrate may include integrated circuits fabricated therein.

[0031] An insulating layer 102 is formed over substrate 100. The insulating layer 102 can be silicon oxide, silicon nitride, high-K dielectric film, Si-C-O-H film, or any other suitable insulating material.

[0032] Conductive layer 104 is deposited on insulating layer 102. Conductive layer 104 is any appropriate conductive material or materials, including metals, metal alloys, conductive nitrides, conductive metal silicides, or heavily doped semiconductor material. For example, conductive layer 104 may be titanium nitride, and may have any appropriate thickness, for example between about 20 and about 100 nm, preferably about 50 nm. In some embodiments, conductive layer 104 may be a layerstack of two or more conductive materials.

[0033] Next a first heavily doped semiconductor layer 106 is deposited on conductive layer 104. Semiconductor layer 106 is preferably silicon, germanium, or an alloy of silicon and/or germanium. For simplicity, this example will describe the semiconductor material used in this and later semiconductor layers as silicon, but it will be understood that other semiconductor materials may be used for any or all semiconductor layers. Layer 106 is doped with either p-type or n-type dopants. For example, layer 106 may be doped with a p-type dopant such as boron or BF_2. Layer 106 may be any thickness, for example between about 10 and about 50 nm, preferably about 20 nm.

[0034] Heavily doped p-type silicon layer 106 and subsequent silicon layers can be deposited by any known method, including chemical vapor deposition, atomic layer deposition, or sputtering. Doping can be by any known method, including in situ doping, diffusion of doping impurities, or ion implantation. When silicon is deposited by sputtering, an n-type or p-type sputtering target can supply the dopant. Alternatively, dopant atoms may be implanted or

otherwise provided in a layer adjacent to a silicon layer which is to be doped; for example dopant may be implanted in a conductive layer immediately beneath the silicon layer to be doped. During subsequent thermal cycles, dopant will diffuse from the adjacent doped layer into the target silicon layer.

[0035] Depending on deposition temperature, semiconductor material such as silicon will be deposited in an amorphous or crystalline state. Amorphous semiconductor material can be crystallized into polycrystalline semiconductor material by annealing. This anneal may be performed as a separate step, or may take place as a result of subsequent thermal steps, and a separate anneal may not be required. Polycrystalline silicon will be referred to herein as *polysilicon*.

[0036] State-change layer 108 can be an antifuse. In a preferred embodiment, state-change layer 108 is a dielectric layer or layerstack which will behave as a dielectric rupture antifuse. For example, state-change layer 108 can be a layer of silicon dioxide grown by oxidizing a portion of silicon layer 106 in a rapid thermal anneal. Alternatively, a dielectric material, for example a high-K dielectric such as Al_2O_3, can be deposited instead. In this example, state-change layer 108 will be described as a dielectric rupture antifuse, but it will be understood that an of the other state change materials named herein could be used instead. Antifuse 108 is preferably very thin, for example less than about 5 nm.

[0037] Undoped or lightly doped silicon layer 110 is deposited on antifuse 108. Undoped or lightly doped silicon layer 110 may be any thickness, for example between about 10 and about 50 nm, preferably about 20 nm. If layer 110 is lightly doped, it is preferably doped with an n-type dopant such as phosphorus or arsenic.

[0038] Heavily doped n-type silicon layer 112 is deposited on undoped or lightly doped silicon layer 110. Heavily doped n-type silicon layer 112 may be

any thickness, for example between about 10 and about 50 nm, preferably about 20 nm.

[0039] If state-change layer 108 is a dielectric rupture antifuse layer, it will be insulating in its initial state. When subjected to sufficient voltage, it will suffer dielectric breakdown, and a permanent conductive path will be formed through it. Upon rupture of antifuse 108, heavily doped n-type layer 112, undoped or lightly doped layer 110, and heavily doped p-type layer 106 will form a vertically oriented junction diode. This diode is a p-i-n diode.

[0040] In alternative embodiments, state-change layer 108 is a fusible element or a resistance-switching element such as a chalcogenide layer. In this case, state-change layer 108 should not be located such that it prevents formation of a p-n junction. For example, if undoped or lightly doped layer 110 is in fact lightly n-doped, the diode is formed by the p-n junction between heavily doped p-type layer 106 and layer 110, and state-change layer 108 should be located above or below this junction. For example, state-change layer 108 can be located below heavily doped p-type layer 106, above undoped or lightly doped layer 110, or above heavily doped n-type layer 112. This placement applies to every state-change layer formed in subsequent memory levels.

[0041] In another alternative one-time-programmable embodiment, the diode itself can behave as a fuse. If the dimension of the pillar is sufficiently small and the power during programming is sufficiently high, the diode can be destroyed during programming, leaving a memory cell with very high resistance. In this case the diode serves as the state change element.

[0042] A *junction diode* is a semiconductor device with the property of conducting current more easily in one direction than the other, having two terminal electrodes, and made of semiconducting material which is p-type at

one electrode and n-type at the other. Examples are p-n diodes, p-i-n diodes, and Zener diodes. In alternative embodiments, the diode can be a Schottky barrier diode.

[0043] Next a layer of sacrificial material 114 is deposited on heavily doped n-type region 112. This layer will not be present in the final device, and thus can be any material that is compatible with process integration requirements. For example, the material should readily adhere to and should have good etch selectivity with both silicon and the spacer material to be deposited in an upcoming step. In the present embodiment, sacrificial material 114 is silicon dioxide, though other materials can be used. Preferably sacrificial layer 114 is between about 50 and about 200 nm thick, most preferably about 100 nm thick.

[0044] Layer 114 is patterned and etched by conventional means to form substantially parallel sacrificial rails 120. Sacrificial rails 120 are shown in cross-section, extending out of the page. In this example, sacrificial rails 120 are about 55 nm wide, and gaps between them are about 105 nm wide, so that the pitch of sacrificial rails 120 is about 160 nm. These feature and gap widths have been selected such that eventual spacers to be formed will be evenly spaced, but other dimensions may be selected; for example the pitch of sacrificial rails may be about 320 nm or less, for example 200 nm or less, for example about 160 nm or less. Feature and gap sizes may be adjusted accordingly. These drawings are not to scale.

[0045] A layer 116 of a conductive material is conformally deposited over sacrificial rails 120. Conductive layer 116 can be either a single material or a conductive layerstack, comprising any appropriate conductive material such as a metal, metal alloy, conductive nitride, or conductive metal silicide. In the present embodiment, layer 116 is preferably titanium nitride, though tantalum nitride, tungsten nitride, and many other appropriate conductive materials can

be used instead. The thickness of conductive layer 116 can be as desired, for example about 25 nm. The structure at this point is shown in Fig. 3a.

[0046] Turning to Fig. 3b, an anisotropic etch is performed, removing layer 116 from the top of sacrificial rails 120 and between them, forming spacers 122. Sacrificial rails 120 are then removed by a dry or wet etch. (To save space, substrate 100 is omitted in these and subsequent figures. Its presence should be assumed.)

[0047] Next spacers 122 serve as hard masks while heavily doped n-type silicon layer 112, undoped or lightly doped silicon layer 110, antifuse layer 108, heavily doped p-type silicon layer 106, and conductive layer 104 are etched into substantially parallel first memory material rails 124. First memory rails 124 comprise semiconductor rails (of layers 106, 110, and 112) formed above conductor rails (of layer 104). Dielectric material 118, which is deposited to fill gaps between first memory material rails 124, can be any appropriate dielectric, for example a high-density plasma (HDP) oxide.

[0048] Summarizing, memory rails 124 were formed by forming a plurality of substantially parallel, substantially coplanar first sacrificial rails 120 of a first layer or layerstack, the first rails above underlying layers; conformally depositing a second layer or layerstack 116 on the first rails; etching the second layer or layerstack to form first spacers 122 of the second layer or layerstack; removing the first rails 120; and etching the underlying layers self-aligned with the first spacers 122, wherein the first spacers serve as hard masks during the etching step. The underlying layers here comprise semiconductor layers and conductor layers.

[0049] As shown in Fig. 3c, a planarization step, for example by chemical mechanical polishing (CMP) or etchback, removes overfill of dielectric 118 exposing tops of first memory rails 124 and dielectric 118 at a substantially

planar surface 109. This planarization step removes some thickness of conductive material 116, leaving, for example, 10-20 nm of thickness.

[0050] Turning to Fig. 3d, layers are deposited on planar surface 109. Conductive layer 204 can be of a material and thickness comparable to conductive layer 104 of first memory rails 124. A silicon diode layerstack including a state-change layer is deposited. This stack may be the same as the layers in first memory rails 124; in this example, the polarity of the diode is reversed. Heavily doped n-type silicon layer 212 is deposited first, on conductive layer 204, followed by undoped or lightly doped silicon layer 210, antifuse layer 208, and heavily doped p-type silicon layer 206. These layers are preferably formed in the same manner and having the same thicknesses as the corresponding layers in first memory rails 124. As in the earlier stack, if antifuse layer 208 is replaced with a resistance-switching element or a fuse element, it should be located such that it does not prevent formation of a p-n junction.

[0051] The view of Fig. 3e is the same as that of Fig. 3d, while the view of Fig. 3f is a 90° rotation view. Fig. 3e is viewed along line A-A' of Fig. 3f. Referring to both Figs. 3e and 3f, sacrificial material 214 is deposited on heavily doped p-type silicon layer 206, and is patterned and etched into substantially parallel rails 220. Rails 220 preferably have the same width and pitch as rails 120 of Fig. 3a, but their width and pitch may be different if this is preferred. Note that rails 220 of sacrificial material 214 extend in a different direction than first memory material rails 124, preferably substantially perpendicular to them. Conductive material 216, which may be any appropriate conductive material, such as titanium nitride, is conformally deposited over rails 220. An anisotropic etch removes conductive material 216 from the top of and between rails 220, leaving spacers 222. Figs. 3e and 3f illustrate the structure at this point.

[0052] Fig. 3g shows the structure from the same view as Fig. 3e, while Fig. 3h shows the same view as Fig. 3f, the view of Fig. 3g along line B-B' of Fig. 3h. Referring to Figs. 3g and 3h, after removal of sacrificial rails 220 by a wet or dry etch, spacers 222 serve as hard masks while heavily doped p-type silicon layer 206, undoped or lightly doped silicon layer 210, antifuse layer 208, heavily doped p-type silicon layer 212, and conductive layer 204 are etched into substantially parallel second memory material rails 224.

[0053] Etching does not stop at this point, however. The etch continues, etching conductive material 116, heavily doped n-type layer 112, undoped or lightly doped layer 110, antifuse layer 108, and heavily doped p-type layer 106 of first memory rails 124. Etching stops on conductive layer 104. This etch is perpendicular to the etch that formed first memory rails 124; thus these doubly-etched layers, 116, 112, 110, 108, and 106 form first pillars 126. Conductive layer 104, however, is not etched; thus this material remains in first conductor rails 128. First conductor rails 128 will serve as bitlines in the completed memory array. Figs. 3g and 3h shows the structure after this etch is complete. Recall that in the structure formed in Figs 2a-2d, final rails 20 are spaced at one-half the pitch of sacrificial rails 14. Similarly, first conductor rails 128 are at one-half the pitch of sacrificial rails 120 of Fig. 3b; thus they are preferably formed at a pitch of 80 nm or less, though in other embodiments the pitch of first conductor rails 128 (and subsequent conductor rails) may be about 160 nm or less, for example 100 nm or less. In less preferred embodiments, the pitch of first conductor rails 128 may be larger, for example 300 nm or less, 200 nm or less, or 180 nm or less.

[0054] The process is repeated. After deposition of dielectric material to fills gaps between second memory material rails 224 and a CMP step to remove dielectric overfill expose tops of second memory rails 224 at a planar surface, turning to Figs. 3i and 3j, the next conductor and diode stack is deposited on

this planar surface. (Fig. 3i shows the structure viewed from the same angle as 3g, while Fig. 3j is viewed from the same angle as Fig. 3h. Fig. 3j is viewed along line C-C' of Fig. 3i.) In a preferred embodiment these layers include titanium nitride layer 304, heavily doped p-type silicon layer 306, antifuse layer 308 (this antifuse is again preferably thermally grown), undoped or lightly doped silicon layer 310, and heavily doped n-type silicon layer 312. Spacers 322 are of conductive layer 316 formed as before by conformally depositing layer 316 over sacrificial material which has been patterned and etched into substantially parallel rails (not shown), which are removed after the spacer etch. Spacers 322 preferably have the same width and pitch as spacers 122 in Fig. 3a.

[0055] As before, spacers 322 serve as hard masks while heavily doped n-type silicon layer 312, undoped or lightly doped silicon layer 310, antifuse layer 308, heavily doped p-type silicon layer 306, and conductive layer 304 are etched into substantially parallel third memory material rails 324. Third memory rails 324 are preferably substantially perpendicular to second memory rails 224 in Figs. 3g and 3h, and preferably substantially parallel to first conductor rails 128.

[0056] Also as before, the etch continues, etching conductive material 216, heavily doped p-type layer 206, antifuse layer 208, undoped or lightly doped layer 210, and heavily doped n-type layer 212, the layers forming second memory rails 224 of Figs. 3g and 3h. Etching stops before conductive layer 204 is etched. This etch is perpendicular to the etch that formed second memory rails 224; thus these doubly-etched layers, 216, 206, 208, 210 and 212, form second pillars 226. Conductive layer 204, however, is not etched; thus this material remains in second conductor rails 228.

[0057] First conductor rails 128, first pillars 126, and second conductor rails 228 form a first memory level. First conductor rails 128 serve as bitlines, while

second conductor rails 228 serve as wordlines. Each of first pillars 126 has a substantially square cross section, having four sides. Two opposing sides were formed in the same etch that formed first conductor rails 128, and thus these side are aligned with the sidewalls of first conductor rails 128. The other two opposing sides were formed in the same etch step that formed second conductor rails 228, and thus these sides are aligned with the sidewalls of second conductor rails 228.

[0058] The process described can be repeated to form additional memory levels. For example, once layers 306, 308, 310, and 312 are etched into pillars in a subsequent iteration, conductor layer 304 will remain as third conductor rails. A second memory level will include second conductor rails 228, second pillars 226, and these third conductor rails.

[0059] Turning to Fig. 4a, a final memory level will be formed above final memory rails 424, which have been exposed at planar surface 409 after gap fill with dielectric material 418. This final memory level can be the third, fourth, fifth, or higher memory level formed above the substrate. Dashed lines indicate pillars of a lower memory level. Fig. 4b shows the same structure viewed perpendicularly along line D-D'.

[0060] A sacrificial material (not shown) is deposited directly on planar surface 409, then the sacrificial material patterned and etched into sacrificial rails (not shown) which extend perpendicular to final memory rails 424. Turning to Figs. 4c and 4d, conductive material 516 is conformally deposited over the sacrificial rails, a spacer etch performed to form spacers 522, and the sacrificial rails removed. Spacers 522, which also extend perpendicular to final memory rails 424, serve as hard masks to etch the layers of final memory rails 424, including conductive layer 416, heavily doped p-type silicon layer 406, antifuse layer 408, undoped or lightly doped silicon layer 410, and heavily

doped n-type silicon layer 412, forming final pillars 426. The etch stops before etching conductive layer 404, leaving conductor rails 428. Dielectric fill will be deposited between spacers 522, which will serve as top conductor rails for the final memory level just formed.

[0061] For clarity one detailed example of the present invention has been provided, but many variations can be envisioned and fall within the scope of the invention. In the memory array described, a conductive layer appeared at both the bottom and the top of each deposited stack, for example layers 104 and 116; eventually these layers became the bottom conductors 128 and the spacers 122 serving as hard masks. The use of a conductive material as the hard mask at the top of each rail is preferred: this layer provides good electrical contact between the diode of each pillar and the overlying conductor, and the fact that the hard masks are a material other than silicon allows them improved longevity during the etch that defines the pillars. If desired, however, the top conductive layer could be omitted, and the heavily doped layer of each diode could instead be used to form spacers which will serve as hard masks. For example, turning to Fig. 5a, in one embodiment, conductive layer 104, heavily doped p-type silicon layer 106, antifuse layer 108, and undoped or lightly doped layer 110 are deposited above insulating layer 102. Sacrificial rails 120 are formed on undoped or lightly doped layer 110. Heavily doped n-type layer 112 is conformally deposited over rails 120. As shown in Fig. 5b, an anisotropic etch forms spacers 122, which are formed of heavily doped n-type material rather than of conductive material 116 as in Fig. 3b. Fabrication continues as in prior embodiments; spacers 122 serve as hard masks to etch a first memory rail.

[0062] In the detailed example provided earlier, polarity of diodes alternated from one level to the next. Referring to Fig. 3j, for example, in the first memory level, the diodes had a heavily doped p-type layer (106) at the bottom and a heavily doped n-type (112) layer at the top, while on the second memory

level, the diodes had a heavily doped n-type layer (212) at the bottom and a heavily doped p-type layer (206) at the top. In other embodiments, other arrangements may be preferred; for example, it may be preferred for all diodes on all memory levels to have p-type layers at the bottom and n-type layers at the top, or vice versa.

[0063] When the state-change element is an antifuse, in preferred embodiments it is located at the diode junction, and is thus either between the bottom heavily doped layer and the undoped or lightly doped layer, or between the top heavily doped layer and the undoped or lightly doped layer. In other alternative embodiments, the state-change element may be elsewhere in the memory cell; above or below the polysilicon stack, for example. The state-change element can be a part of the pillars, as shown, or, alternatively, may be coextensive with the conductor rails.

[0064] Additional layers that have not been mentioned, such as barrier, adhesion, or etch stop layers, may be included in one or more memory levels of the memory array.

[0065] Detailed methods of fabrication have been described herein, but any other methods that form the same structures can be used while the results fall within the scope of the invention.

[0066] The foregoing detailed description has described only a few of the many forms that this invention can take. For this reason, this detailed description is intended by way of illustration, and not by way of limitation. It is only the following claims, including all equivalents, which are intended to define the scope of this invention.

WHAT IS CLAIMED IS:

1. A method for forming a first memory level, the method comprising:
   forming a plurality of substantially parallel, substantially coplanar first rails of a first layer or layerstack, the first rails above underlying layers;
   conformally depositing a second layer or layerstack on the first rails;
   etching the second layer or layerstack to form first spacers of the second layer or layerstack;
   removing the first rails; and
   etching the underlying layers self-aligned with the first spacers, wherein the first spacers serve as hard masks during the etching step.

2. The method of claim 1 wherein the step of etching the underlying layers comprises:
   etching first semiconductor layers; and
   etching first conductor layers.

3. The method of claim 2 wherein, during the step of etching the first semiconductor layers, the first semiconductor layers are etched into a first plurality of substantially parallel semiconductor rails.

4. The method of claim 3 wherein the first rails are spaced at a first pitch and the first semiconductor rails are spaced at a second pitch, the second pitch less than the first pitch.

5. The method of claim 4 wherein the second pitch is about one-half the first pitch.

6. The method of claim 2 wherein, during the step of etching the first conductor layers, the first semiconductor layers are etched into substantially parallel conductor rails.

7. The method of claim 6 wherein the first rails are spaced at a first pitch and the first conductor rails are spaced at a second pitch, the second pitch less than the first pitch.

8. The method of claim 7 wherein the second pitch is about one-half the first pitch.

9. The method of claim 2 wherein, during the step of etching the first semiconductor layers, the first semiconductor layers are etched into a plurality of first semiconductor pillars.

10. The method of claim 9 wherein the first rails are spaced at a first pitch and the first semiconductor pillars are spaced at a second pitch, the second pitch less than the first pitch.

11. The method of claim 10 wherein the second pitch is about one-half the first pitch.

12. The method of claim 9 wherein the first semiconductor layers comprise:

a first heavily doped semiconductor layer of a first conductivity type; and

a second heavily doped semiconductor layer of a second conductivity type, the second conductivity type opposite the first, the second heavily doped semiconductor layer above the first heavily doped semiconductor layer.

13. The method of claim 12 wherein the first semiconductor layers further comprise a third undoped or lightly doped semiconductor layer of the first or the second conductivity type, the undoped or lightly doped semiconductor layer disposed between the first heavily doped layer and the second heavily doped layer.

14. The method of claim 13 wherein each first pillar comprises a state-change element.

15. The method of claim 14 wherein the state-change element of each first pillar is a dielectric rupture antifuse.

16. The method of claim 14 wherein the dielectric rupture antifuse of each first pillar is disposed either:
    a) between the undoped or lightly doped semiconductor layer and the first heavily doped semiconductor layer, or
    b) between the undoped or lightly doped semiconductor layer and the second heavily doped semiconductor layer, or
    c) above and in contact with the second heavily doped semiconductor layer, or
    d) below and in contact with the first heavily doped semiconductor layer.

17. The method of claim 16 wherein, after rupture of the dielectric rupture antifuse, the first and second heavily doped semiconductor layers and the undoped or lightly doped semiconductor layer of each pillar form a vertically oriented p-i-n diode.

18. The method of claim 15 wherein the dielectric rupture antifuse comprises a silicon oxide layer.

19. The method of claim 14 wherein the state-change element of each first pillar comprises a chalcogenide material.

20. The method of claim 19 wherein the state-change element of each first pillar is disposed either:
    a) above and in contact with the second heavily doped semiconductor layer, or
    b) below and in contact with the first heavily doped semiconductor layer.

21. The method of claim 14 wherein the state-change element of each first pillar comprises a fuse element.

22. The method of claim 2 wherein the first semiconductor layers comprise polycrystalline semiconductor material.

23. The method of claim 22 wherein the polycrystalline semiconductor material comprises silicon.

24. The method of claim 22 wherein the polycrystalline semiconductor material comprises an alloy of silicon and/or germanium.

25. The method of claim 2 wherein the first semiconductor layers comprise:
    a first heavily doped semiconductor layer of a first conductivity type; and
    a second heavily doped semiconductor layer of a second conductivity type, the second conductivity type opposite the first, the second heavily doped semiconductor layer above the first heavily doped layer.

26. The method of claim 25 wherein the first semiconductor layers further comprise a third undoped or lightly doped layer of the first or the second conductivity type, the undoped or lightly doped layer disposed between the first heavily doped layer and the second heavily doped layer.

27. The method of claim 1 wherein the first memory level is formed above a substrate.

28. The method of claim 27 wherein the substrate is monocrystalline semiconductor material.

29. The method of claim 1 wherein the second layer or layerstack comprises a metal, metal alloy, conductive nitride, or conductive metal silicide.

30. A monolithic three dimensional memory array above a substrate comprising:

a first plurality of substantially parallel, substantially coplanar conductors extending in a first direction;

a second plurality of substantially parallel, substantially coplanar conductors extending in a second direction different from the first direction, the second conductors above the first conductors;

a first plurality of pillars, each first pillar disposed between one of the first conductors and one of the second conductors, each first pillar having two substantially vertical sides aligned with sidewalls of one of the first conductors, and each first pillar having two substantially vertical sides aligned with sidewalls of one of the second conductors,

wherein the first conductors have a pitch of about 300 nm or less.

31. The monolithic three dimensional memory array of claim 30 wherein each first pillar comprises:

a first heavily doped semiconductor layer of a first conductivity type;

a second heavily doped semiconductor layer of a second conductivity type opposite the first conductivity type; and

a state-change element.

32. The monolithic three dimensional memory array of claim 31 wherein the state-change element of each first pillar is a dielectric rupture antifuse.

33. The monolithic three dimensional memory array of claim 32 wherein the dielectric rupture antifuse of each first pillar comprises a silicon oxide layer.

34. The monolithic three dimensional memory array of claim 31 wherein the state-change element of each first pillar comprises a chalcogenide layer.

35. The monolithic three dimensional memory array of claim 31 wherein the state-change element of each first pillar comprises a fuse.

36. The monolithic three dimensional memory array of claim 30 wherein the first conductors, first pillars, and second conductors comprise a first memory level, the first memory level comprising first memory cells.

37. The monolithic three dimensional memory array of claim 30 wherein the first conductors comprise a metal, metal alloy, conductive nitride, or conductive metal silicide.

38. The monolithic three dimensional memory array of claim 30 wherein the first pillars comprise polycrystalline semiconductor material.

39. The monolithic three dimensional memory array of claim 30 further comprising:

a third plurality of substantially parallel, substantially coplanar conductors extending in the first direction;

a second plurality of pillars, each second pillar disposed between one of the second conductors and one of the third conductors, each second pillar having two substantially vertical sides aligned with sidewalls of one of the second conductors, and each second pillar having two substantially vertical sides aligned with sidewalls of one of the third conductors.

40. The monolithic three dimensional memory array of claim 30 wherein the first conductors have a pitch of about 200 nm or less.

41. The monolithic three dimensional memory array of claim 30 wherein the first conductors have a pitch of about 180 nm or less.

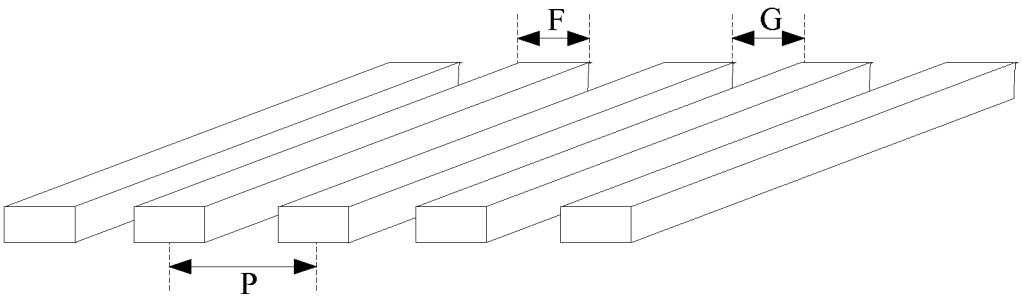


Fig. 1

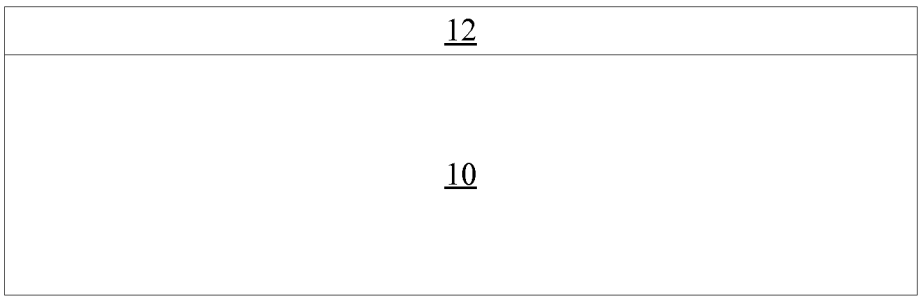


Fig. 2a

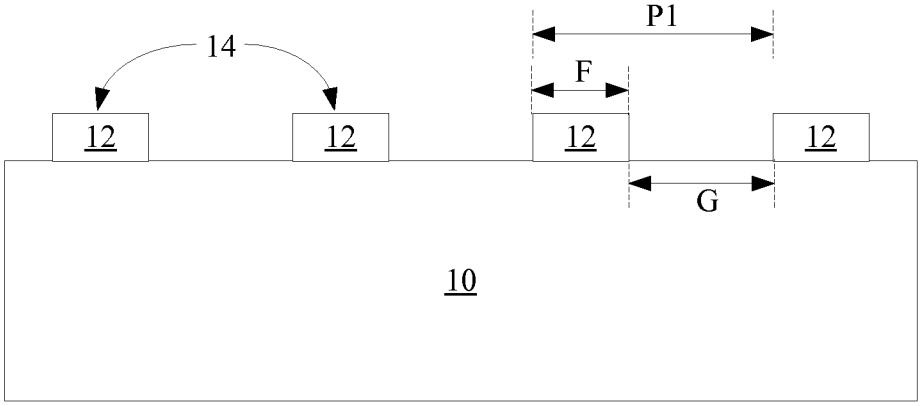


Fig. 2b

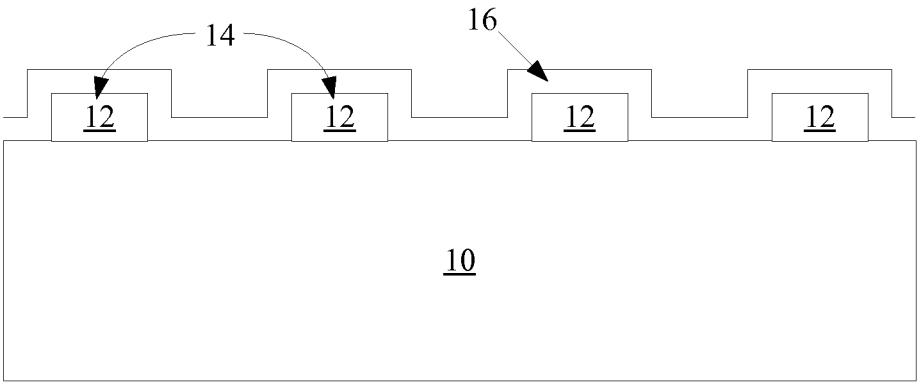


Fig. 2c

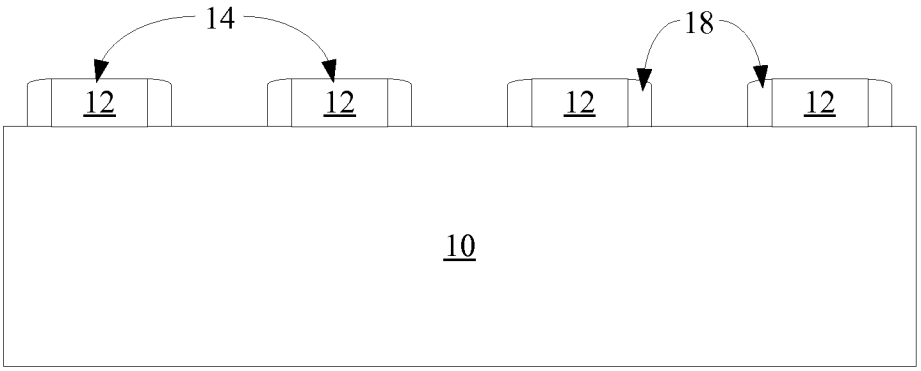


Fig. 2d

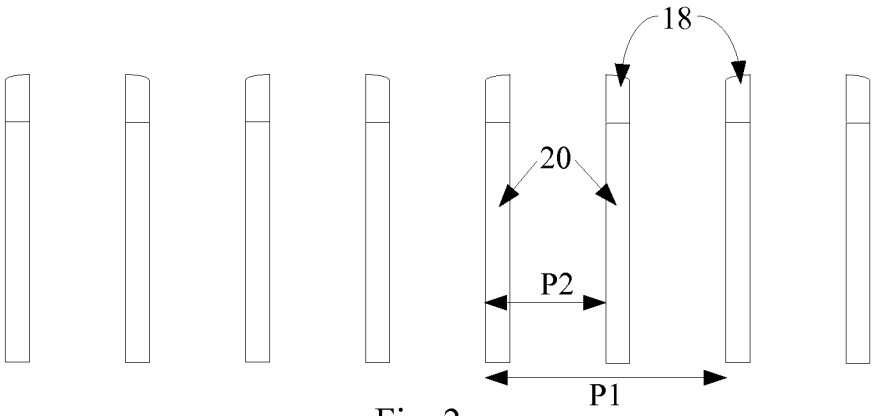


Fig. 2e

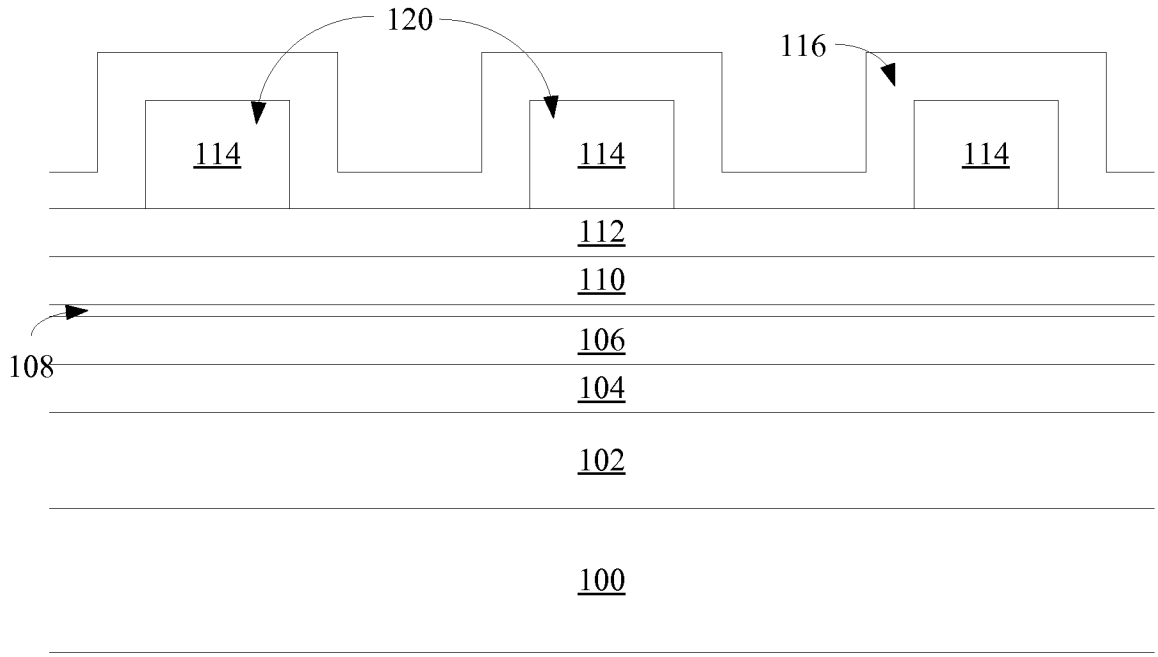

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Fig. 3a

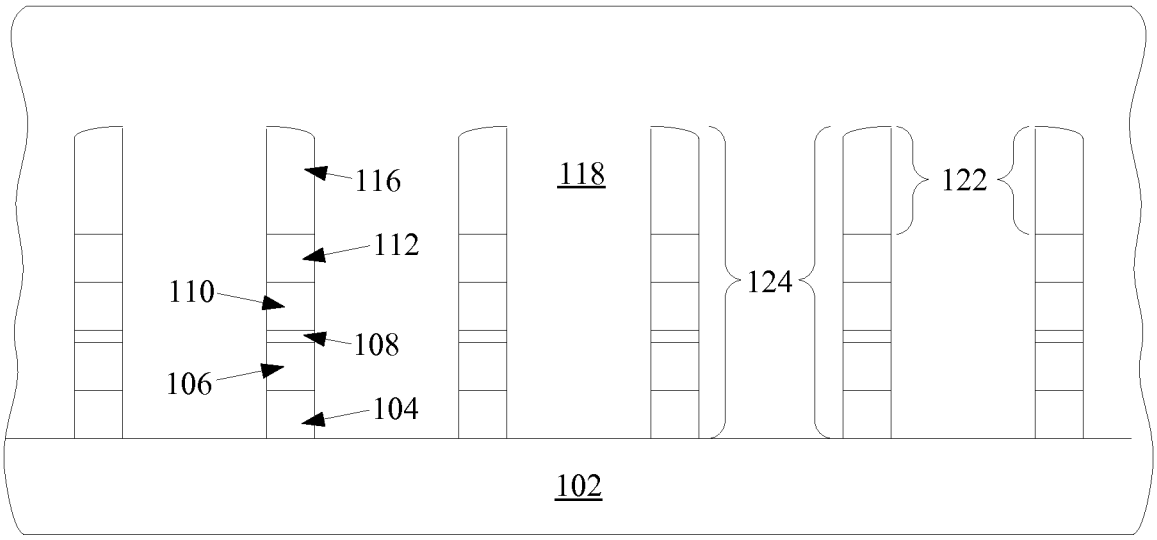
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Fig. 3b

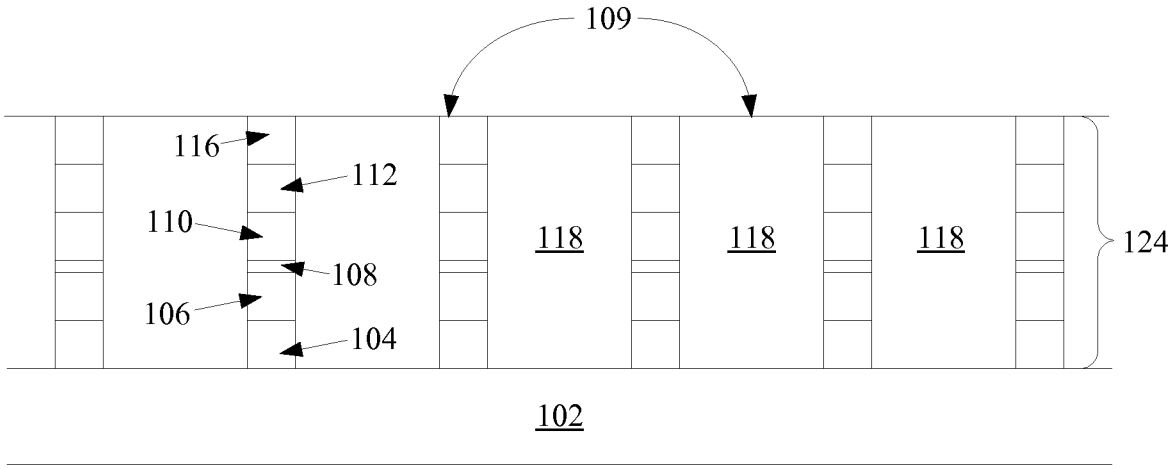
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Fig. 3c

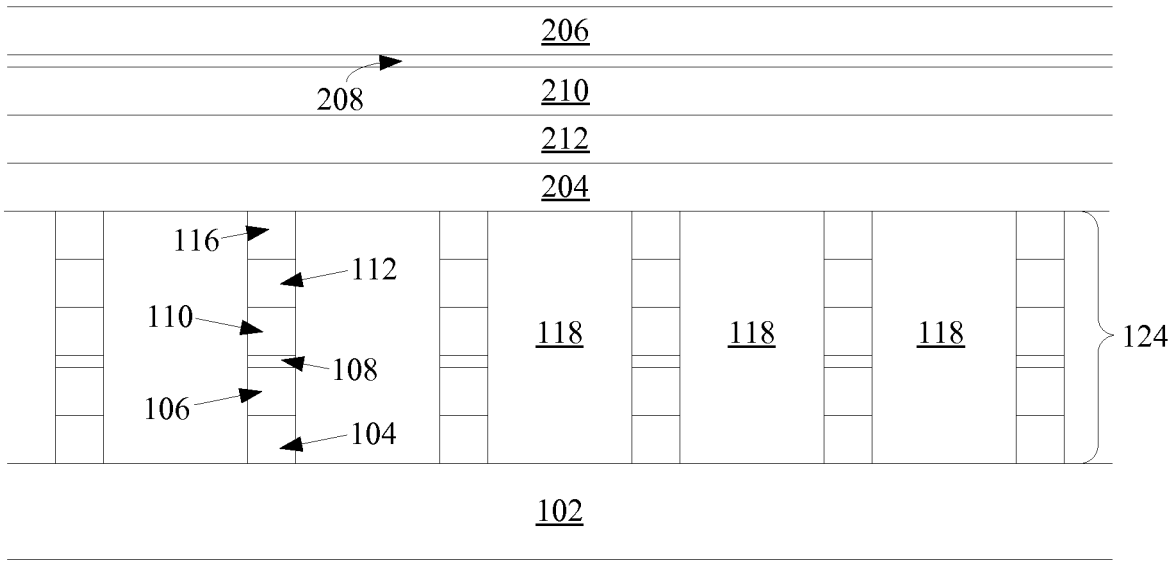
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Fig. 3d

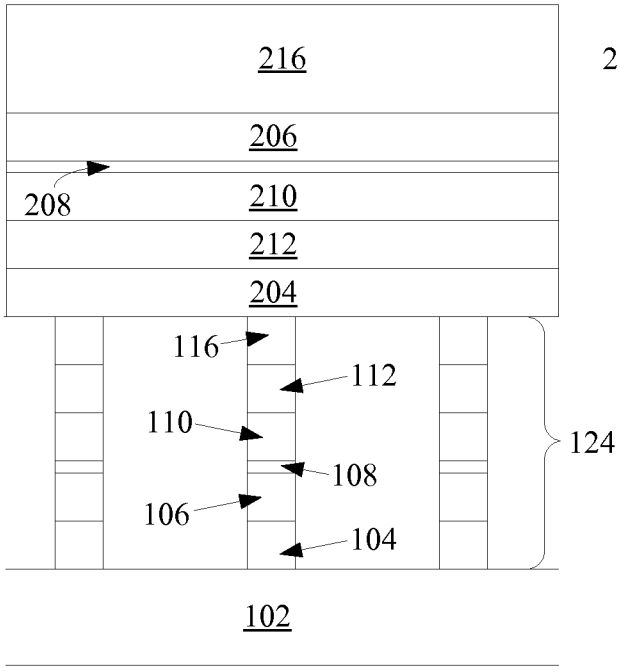
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Fig. 3e

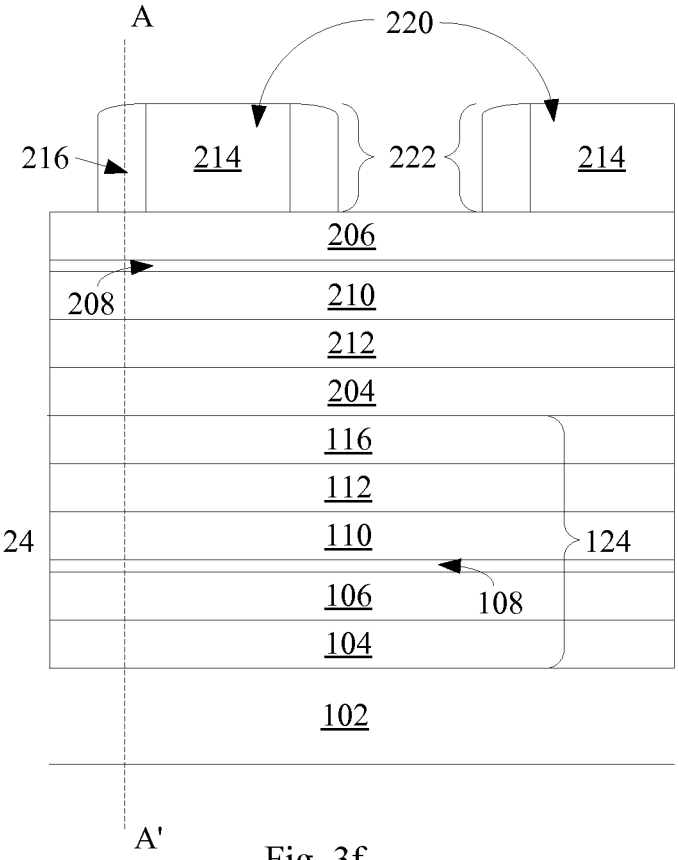
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Fig. 3f

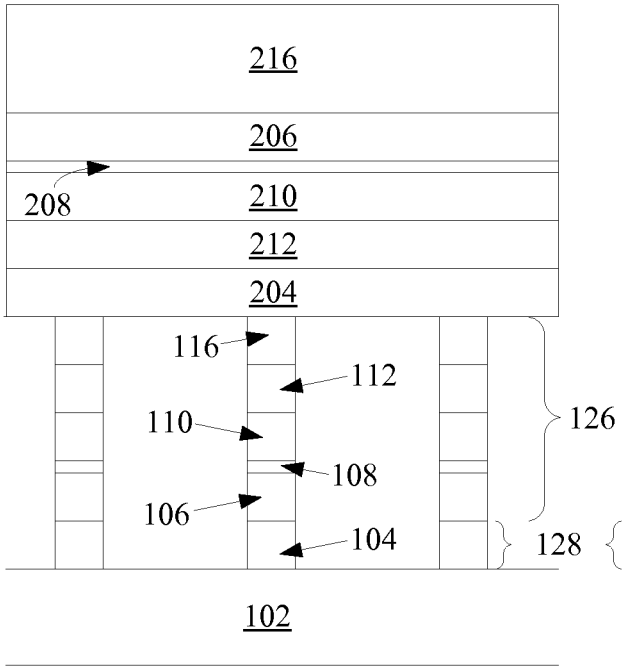
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Fig. 3g

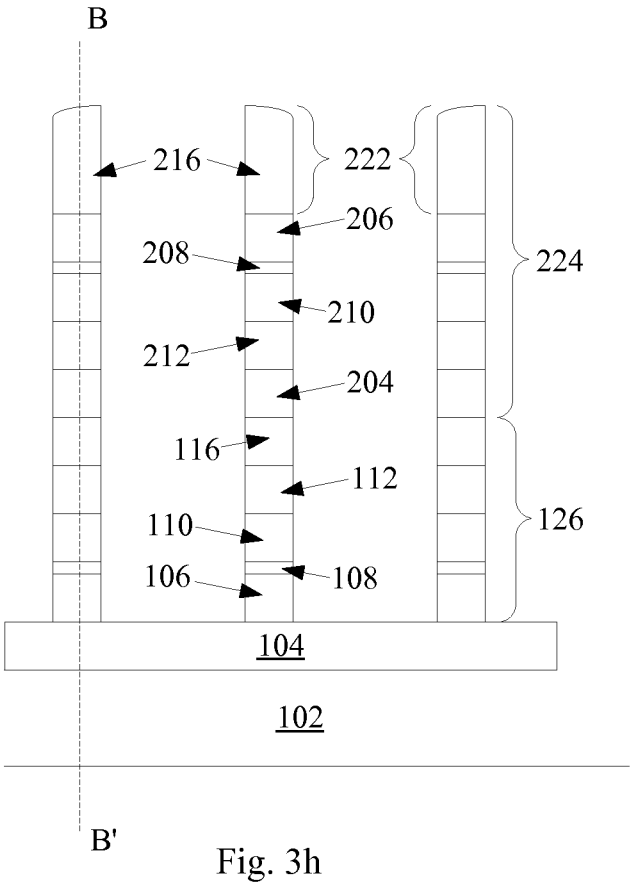
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Fig. 3h

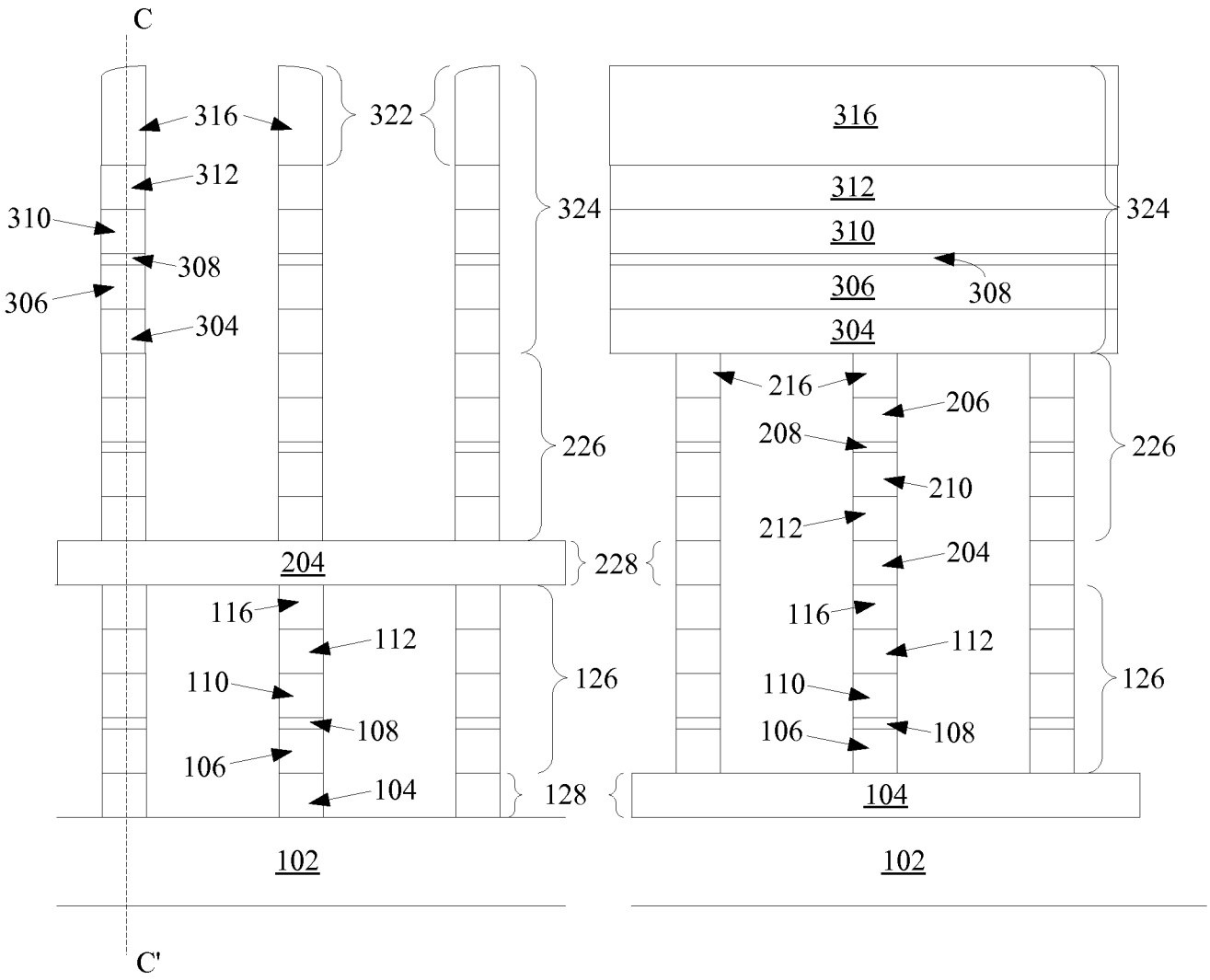
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Fig. 3i

Fig. 3j

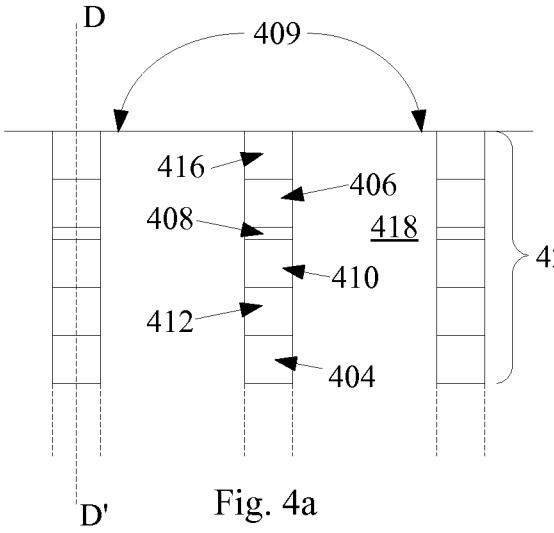

Fig. 4a

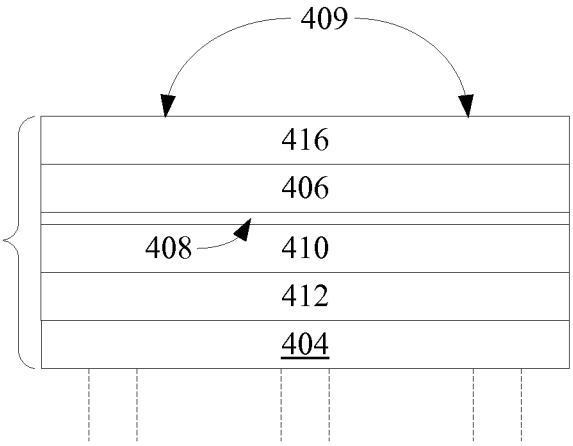

Fig. 4b

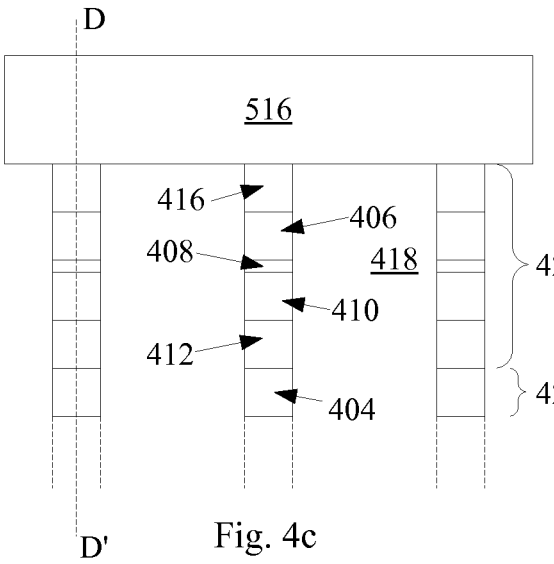

Fig. 4c

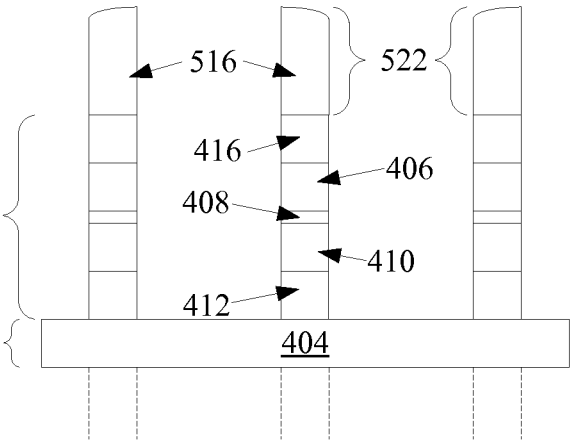

Fig. 4d

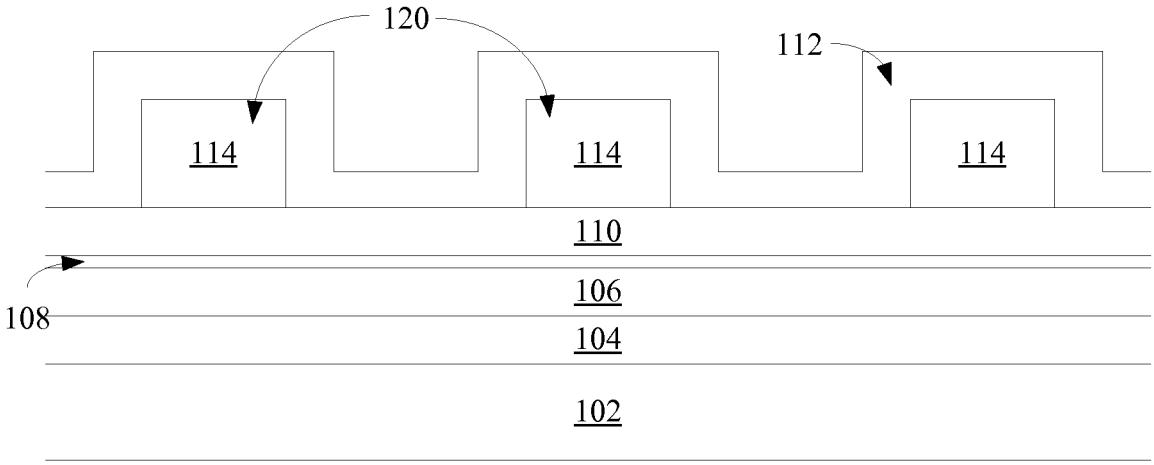
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Fig. 5a

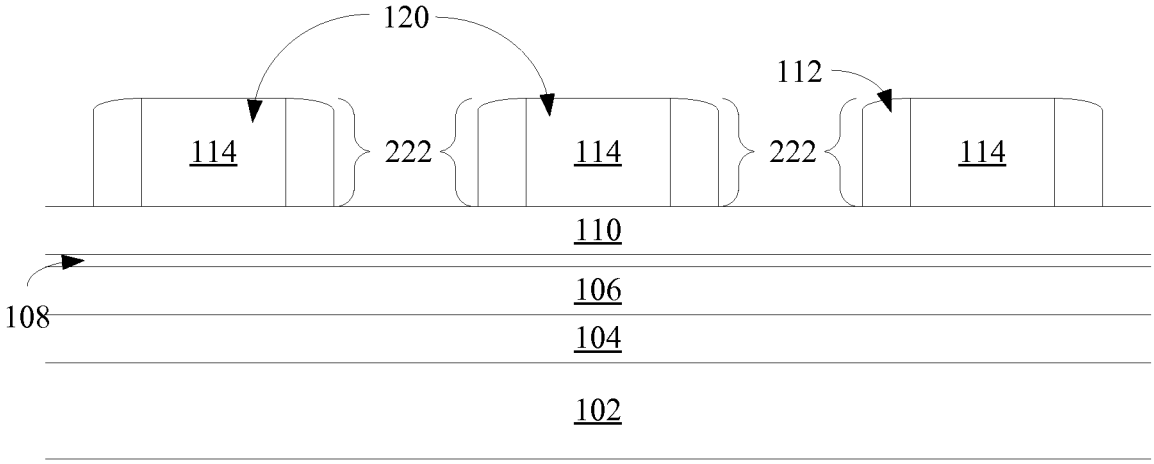
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Fig. 5b