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(54) **Title:** SEMICONDUCTOR SWITCH WITH RELIABLE BLACKOUT BEHAVIOR AND LOW CONTROL POWER

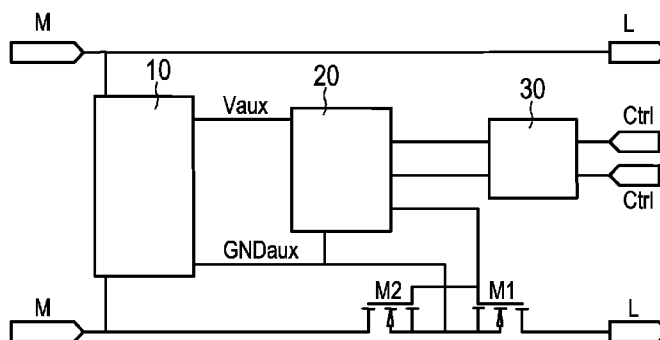


FIG. 1

(57) **Abstract:** The present invention relates to a bidirectional semiconductor switch (M1, M2) with extremely low control power consumption and a bootstrap circuit which allows reliable start of operation of the switch and the hosting device after unlimited duration of mains interruptions. Intelligent control options are provided by operating from a small energy storage and no extra means are required to recover from a depleted energy storage condition. The absence of audible noise and mechanical wear also enables more frequent recharging cycles and allows smaller and thus cheaper energy storage components.

SEMICONDUCTOR SWITCH WITH RELIABLE BLACKOUT BEHAVIOR AND LOW CONTROL POWER

FIELD OF THE INVENTION

The present invention relates to a switching apparatus for connecting and disconnecting appliances and devices to a power grid.

BACKGROUND OF THE INVENTION

5 Standby power consumption reduction is becoming a major issue for appliances and devices, supplied from the utility grid, such as consumer lifestyle appliances or networked lighting ballasts. In the past, solutions have been proposed, which solved the above problem by using a very-low-power controller circuit in combination with an energy storage element and a bi-stable or latching relay. Major disadvantages of the relay are the
10 audible switching noise, the limited lifetime, the large physical size, limited reliability under mechanical shocks, and eventually high cost. Audible noise and mechanical wear during switching mandates avoiding frequent recharging of the energy storage and thus demands for a substantial capacity of the storage element, leading to higher cost. Return of the mains voltage after a blackout leads to synchronous inrush current of all connected devices which
15 may trip circuit breakers and thus may lead to another blackout.

A simple replacement of the mechanical relay by a semiconductor switch has the disadvantages of risking dead-lock situations after mains blackout and depletion of the energy storage element in consequence. There is also a constant effort keeping it into a desired state, compared to the latching or bi-stable relay solution.

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SUMMARY OF THE INVENTION

It is an object of the present invention to provide a switching apparatus with extremely low control power consumption, which allows reliable start of operation of the switching apparatus and the hosting device after unlimited duration of mains interruptions.

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This object is achieved by an apparatus as claimed in claim 1.

Accordingly, a bidirectional semiconductor switch is proposed with extremely low control power consumption and an ultra low power bias supply circuit which allows reliable start of operation of the switch and the hosting device after unlimited duration of mains interruptions. This allows hosting applications to operate in standby conditions without

electrical connection to the mains at all, and offer intelligent control options just operating from a small energy storage and does not require extra means anymore to recover from a depleted energy storage condition. The absence of audible noise and mechanical wear also enables more frequent recharging cycles and allows smaller and thus cheaper energy storage components.

According to a first aspect, an additional randomizer can be provided which delays the operation of the switching apparatus after a mains interruption in a random way (e.g. between zero and an acceptable maximum time delay) and thus enforces an asynchronous behaviour of the connected devices, avoiding repeated tripping of the circuit breakers.

According to a second aspect which can be combined with said first aspect, the semiconductor switch may comprise at least two metal oxide semiconductor field effect transistors or at least two insulated gate bipolar transistors. Thus, it can be ensured that control power of the semiconductor switch is minimized.

According to a third aspect which can be combined with said first or second aspect, the bias supply circuit may comprise a serial connection of the at least one capacitor and a zener diode adapted to limit the supply voltage derived from the power grid, and a diode for rectifying the limited supply voltage to obtain the floating auxiliary voltage. Thereby, discharge resistor(s) across the at least one capacitor can be omitted, which helps to reduce power consumption.

According to a fourth aspect which can be combined with at least one of the first to third aspects, a buffer capacitor may be provided for buffering the floating auxiliary voltage. This measure ensures that supply voltage of the switching control circuit is buffered for a certain duration.

According to a fifth aspect which can be combined with at least one of the first to fourth aspects, the switching control circuit may comprise a latch circuit (such as for example a flip flop or other bistable realization) and wherein the isolation circuit comprises an isolating signal transformer or optical coupler for supplying the at least one control signal to a signal processing circuit for generating control commands to be supplied to the latch circuit.

According to a sixth aspect which can be combined with at least one of the first to fifth aspects, a watchdog circuit may be provided, which is adapted to sense the floating auxiliary voltage and to provide a control signal to the latch circuit if the floating auxiliary voltage is below a predetermined threshold, wherein the control signal triggers a

dominant reset of the semiconductor switch. Thereby, damage to the semiconductor switch due to excessive power dissipation can be prevented. As an additional option, another watchdog circuit may be provided, which is adapted to determine the status (e.g. energy level) of at least some energy storage elements in the apparatus, and of which the output signal may also provide a control signal to the latch circuit to initiate a turn-on cycle with subsequent recharging of fore-mentioned energy storing elements of the apparatus.

According to a seventh aspect which can be combined with at least one of the first to sixth aspects, wherein the watchdog circuit may comprise a transistor activated by the floating auxiliary voltage as soon as said auxiliary voltage has reached its nominal value, and wherein a collector voltage of the transistor is supplied to an input terminal of the latch circuit. Thereby, a simple supply voltage detection and watchdog functionality can be implemented.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter. In the following drawings:

Fig. 1 shows a schematic block diagram of a switching apparatus according to the embodiments;

Fig. 2 shows a more detailed block diagram of a switching apparatus according to a first embodiment;

Fig. 3 shows a more detailed block diagram of a switching apparatus according to a second embodiment;

Fig. 4 shows a more detailed block diagram of a switching apparatus according to a third embodiment; and

Fig. 5 shows a more detailed diagram of a switching apparatus according to a fourth embodiment.

DETAILED DESCRIPTION OF EMBODIMENTS

The following embodiments are based on a switching apparatus with bidirectional semiconductor switch with extremely low control power consumption and an ultra low power bias supply circuit which allows reliable start of operation of the switch and the hosting device after unlimited duration of mains interruptions.

Fig. 1 shows a schematic block diagram with the basic components of a switching apparatus according to the following embodiments of the present invention. Power transistors (e.g. N-MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) or

IGBTs (Insulated Gate Bipolar Transistor)) M1 and M2 form a bidirectional mains switch. A control voltage referenced to the common source GNDaux of the MOSFETs is generated by an On/Off controller 20. The On/Off control block or controller 20 is supplied by an ultra low power bias supply 10, which can be designed for very low power consumption, e.g., less than 1mW. Activation of the switch is done by the On/Off controller 20, which takes care about turning the switch on or off after mains failure and on request of control signals Ctrl supplied via a signal isolation block 30. The signal isolation block 30 serves to isolate the switching apparatus from a control circuit (not shown) which supplies the control signals Ctrl and may include one or more opto-couplers or an inductive link, such as an isolation transformer.

A MOSFET is a transistor where a voltage on an oxide-insulated gate electrode can induce a conducting channel between the two other contacts called source and drain. The channel can be of n-type or p-type, and the transistor is accordingly called an N-MOSFET or a P-MOSFET.

The MOSFETS of Fig. 1 may be replaced by insulated gate bipolar transistors (IGBTs), which are three-terminal power semiconductor devices for high efficiency and fast switching. The IGBT combines the simple gate-drive characteristics of the MOSFETs with the high-current and low-saturation-voltage capability of bipolar transistors by combining an isolated gate FET for the control input, and a bipolar power transistor as a switch, in a single device.

An N-MOSFET or an IGBT need a significantly positive charge applied to the gate in order to turn on. Using N-MOSFET/IGBT devices is a common cost reduction method due largely to die size reduction (there are other benefits as well).

A MOSFET/IGBT is a voltage controlled device which, in theory, will not have any direct gate current. This makes it possible to utilize the charge inside the capacitor for control purposes. However, eventually the capacitor will lose its charge (due to parasitic gate current and non ideal (i.e. infinite) internal resistance),

Fig. 2 shows a schematic block diagram of a first embodiment of the switching apparatus with a more detailed implementation of the ultra low power bias supply 10. A floating auxiliary voltage between nodes Vaux and GNDaux is generated from the mains voltage by use of two small capacitors C1 and C2, limited by zener diode DZ and rectified by diode D1. The floating auxiliary voltage is buffered by a capacitor C3. The values of the capacitors C1 and C2 can for instance be a few nano-farad (nF) at typical AC mains voltages of 115V at 60Hz or 230V at 50Hz. These capacitor values are so low that discharge resistors,

parallel to the capacitors C1 respectively C2, are not required, which helps to reduce power consumption.

The values of the capacitors C1 and C2 need not be equal. In the best optimized case the power consumption of the On/Off controller 20 becomes such low that the capacitors C1 and C2 can be chosen in a range below 100pF. In this case, the capacitor C2 could even be omitted.

It is noted that in the ultra low power bias supply used in the embodiments there are no requirements to the duty cycle of the bidirectional switch formed by the power transistors M1 and M2. The capacitive supply (with C1, C2 and DZ, D1) recharges storage capacitor C3 as long as the AC mains voltage is present between terminals M, independent of the state of the bidirectional switch.

Fig. 3 shows a schematic block diagram of a second embodiment of the switching apparatus with more detailed implementation of the bias supply 10, where the capacitor C2 has been removed in view of the fact that the MOSFETs M2 and M1 of the mains switch provide some amount of parasitic capacitance also (not shown).

Fig. 4 shows a schematic block diagram of a third embodiment of the switching apparatus with a more detailed implementation of the bias supply 10, and the signal isolation block 30. The signal isolation block 30 is provided with a signal processing circuit 24 that extracts set (S) and reset (R) commands from short signal pulses that are transmitted from a control unit (not shown), e.g., a DALI (digital addressable lighting interface), DMX (digital multiplexing) or other control system including an isolating signal transformer. The signal processing functionality in block 24 suppresses common-mode events e.g. due to capacitive coupling in the signal transformer and provides signal rejection to disturbances, transients, surges, etc. The signal transformer may resemble the ones used in ISDN (Integrated Services Digital Network) applications. The signalling chain may also be implemented by an optocoupler (a photo-transistor and a photodiode in active mode) (not shown) or more than one optocoupler.

The extracted pulses are used to set or reset a bi-stable latch circuit (e.g. 1-bit flip-flop with output drivers) which is incorporated in a signal processing block 26 which provides the gate control signal to the power transistors M1 and M2. As already mentioned above, this kind of transistors has (aside from leakage) negligible energy consumption in the gate-source input port to maintain a switching state. Energy is dissipated in the signal processing block 26 only during turn-on or turn off. As such, there is substantially no or negligible control energy consumption during steady state operation.

A further element is a watchdog circuit 22, which constantly senses the differential voltage between the Vaux and GNDaux nodes and outputs a signal to the signal processing block 26. The output signal of the watchdog circuit 22 changes state when the differential voltage crosses a predetermined level. The watchdog output signal is thus continuously present, indicating whether the differential floating voltage is above or below the threshold value. Whether a turn-on cycle with subsequent recharging of the energy storage elements of the hosting device is necessary is not dependent on the output signal of the described watchdog circuit 22, but may be initiated by a separate watchdog circuit in the hosting device, monitoring the energy level of at least some of the energy storage elements in the hosting device. Thus, the other watchdog circuit is adapted to determine a status of the at least some energy storage elements and to provide another control signal to the latch circuit 26 if an energy level of the energy storage elements is below a predetermined threshold. The control signal may then trigger a turn-on cycle of the power transistors M1, and M2 with subsequent recharging of the at least some energy storage elements.

The purpose of the watchdog circuit 22 is to guarantee that the power transistors M1 and M2 are never conductive (dominant reset) when the differential voltage between the Vaux and GNDaux nodes is not sufficiently high, to prevent brown-out of the power transistors M1 and M2, due to excessive power dissipation. A separate watchdog circuit (not shown) may be added in the hosting device, monitoring the energy of the energy storage elements in the hosting device. Its purpose is to have the system recover from a situation where the energy storage is completely exhausted. This allows the application to execute a provisional turn-on cycle automatically and a subsequent period of recharging the energy storage elements (including those in the control unit). The turn-on-cycle is provisional in that sense that normal operation of the appliance (i.e. load L in Fig. 4) is not entered unless an appropriate control signal is received and the appliance will be disconnected from mains again, if the energy storage elements are recharged again.

Fig. 5 shows a schematic block diagram of a fourth embodiment of the switching apparatus in which the ultra low power bias supply 10 comprises a simple ultra-low-power bias supply generation and auxiliary supply voltage detection (watchdog functionality) with resistors R1 and R2, and a transistor Q1 without adding a further voltage reference (which saves static energy consumption). R1 could be omitted, if the base of the transistor Q1 can stand the current through the zener diode DZ. As soon as the capacitor C3 is charged to the normal operation voltage, some current starts flowing through the zener diode DZ in the positive direction, which activates the transistor Q1. The collector voltage of

the transistor Q1 is the output signal of the watchdog circuit and forms an input signal to the On/Off controller 20. This circuit can be extended by adding a hysteresis function, e.g., through a feedback circuit or element (not shown). As shown in Fig. 5, the signal isolation block 30 comprises a signal transformer U1 for achieving the required isolation between switching and control circuits.

Another way to implement the watchdog functionality is to use a commercially-available integrated circuit (IC). Such a commercially-available IC might be a micro-power low-voltage comparator, such as Linear Technology LT6703, which can be connected as a watchdog circuit. Although its current consumption in normal operation (e.g. supply voltage above 1.4V) is reasonably low (e.g. below 10 μ A), during start-up (e.g. supply voltage below 1V) the IC draws a supply current with a value exceeding 30 μ A. To guarantee that the auxiliary voltage supply supplies sufficient current, in that case the values of the capacitors C1 and C2 need to be chosen higher, e.g. 3.3nF, each at a typical root mean square (RMS) mains voltage of 230V at 50Hz. Furthermore, a signal-processing electronics may be connected to the secondary side of the isolation transformer. More specifically, digital building blocks of CMOS IC's may be used.

In another modification of the above embodiments, an input circuit for inputting an on/off input signal, e.g. as generated by a DALI or DMX decoder interface, may be provided, which includes a circuit built with CMOS logic cells, so as to convert the on/off input signal into short on/off pulses that are fed to the primary-side terminals of the isolation transformer. The input circuit can be supplied e.g. with 10V DC, and may consume less than 1 μ A at an on/off switch frequency of less than once per second.

An additional feature can be a randomizing function or randomizer which delays the turn-on of the power transistors M1 and M2 after a mains interruption and depletion of the storage elements in order to prevent synchronous inrush currents in all devices in a circuit branch and in response tripping circuit breakers, which might lead to another blackout situation. This would be particularly useful in large lighting installations with many ballast circuits and large buffer capacity in the power supplies.

The invention can be applied for instance in appliances offering remote control of appliances and having extended standby periods while still being responsive to remote control commands. This includes remotely controlled lighting systems, e.g. by means of DALI, ZigBee, DMX or other lighting or building control solutions, as well as consumer lifestyle appliances, such as television (TV) sets, set-top-boxes, household appliances, or consumer lighting solutions.

In summary, a bidirectional semiconductor switch with extremely low control power consumption and an ultra low power bias supply circuit has been described, which allows reliable start of operation of the switch and the hosting device after unlimited duration of mains interruptions. Intelligent control options are provided by operating from a small energy storage and no extra means are required to recover from a depleted energy storage condition. The absence of audible noise and mechanical wear also enables more frequent recharging cycles of energy storage elements in the hosting device and allows smaller and thus cheaper energy storage components.

Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure, and the appended claims.

In the claims, the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. A single processor, sensing unit or other unit may fulfil the functions of several items recited in the claims. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

Any reference signs in the claims should not be construed as limiting the scope thereof.

CLAIMS:

1. A switching apparatus for connecting/disconnecting appliances or devices to a power grid, said apparatus comprising:

- a. a bidirectional semiconductor switch (M1, M2);
- b. a bias supply circuit (10) for generating a floating auxiliary voltage by use of at least one capacitor (C1, C2); and
- c. a switching control circuit (20) powered by said floating auxiliary voltage and adapted to turn on said bidirectional semiconductor switch (M1, M2) in response to an appearance of a supply voltage derived from said power grid or to at least one control signal supplied via an isolation circuit (30).

2. The apparatus according to claim 1, further comprising a randomizer which delays an operation of said semiconductor switch (M1, M2) in response to an interruption of said supply voltage.

3. The apparatus according to claim 1, wherein said semiconductor switch (M1, M2) comprises at least two metal oxide semiconductor field effect transistors or at least two insulated gate bipolar transistors.

4. The apparatus according to claim 1, wherein said bias supply circuit (10) comprises a serial connection of said at least one capacitor (C1, C2) and a zener diode (ZD) adapted to limit said supply voltage derived from said power grid, and a diode (D1) for rectifying the limited supply voltage to obtain said floating auxiliary voltage.

5. The apparatus according to claim 4, further comprising a buffer capacitor (C3) for buffering said floating auxiliary voltage.

6. The apparatus according to claim 1, wherein said switching control circuit (20) comprises a latch circuit (26) and wherein said isolation circuit (30) comprises a signal transformer or optical coupler for supplying said at least one control signal to a signal

processing circuit (24) for generating control commands to be supplied to said latch circuit (26).

7. The apparatus according to claim 6, wherein said latch circuit (26) comprises a
5 bi-stable flip-flop.

8. The apparatus according to claim 6, further comprising a watchdog circuit (22)
adapted to sense said floating auxiliary voltage and to provide a control signal to said latch
circuit (26) if said floating auxiliary voltage is below a predetermined threshold, wherein said
10 control signal triggers a dominant reset of said semiconductor switch (M1, M2).

9. The apparatus according to claim 8, further comprising another watchdog
circuit adapted to determine a status of energy storage elements in the apparatus and to
provide another control signal to said latch circuit (26) if an energy level of the energy
15 storage elements is below a predetermined threshold, where said control signal triggers a
turn-on cycle of said semiconductor switch (M1, M2) with subsequent recharging of energy
storage elements of said apparatus.

10. The apparatus according to claim 8, wherein said watchdog circuit (22)
20 comprises a transistor (Q1) activated by said auxiliary voltage as soon as said auxiliary
voltage has reached its nominal value, and wherein a collector voltage of said transistor (Q1)
is supplied to an input terminal of said latch circuit (26).

1/3

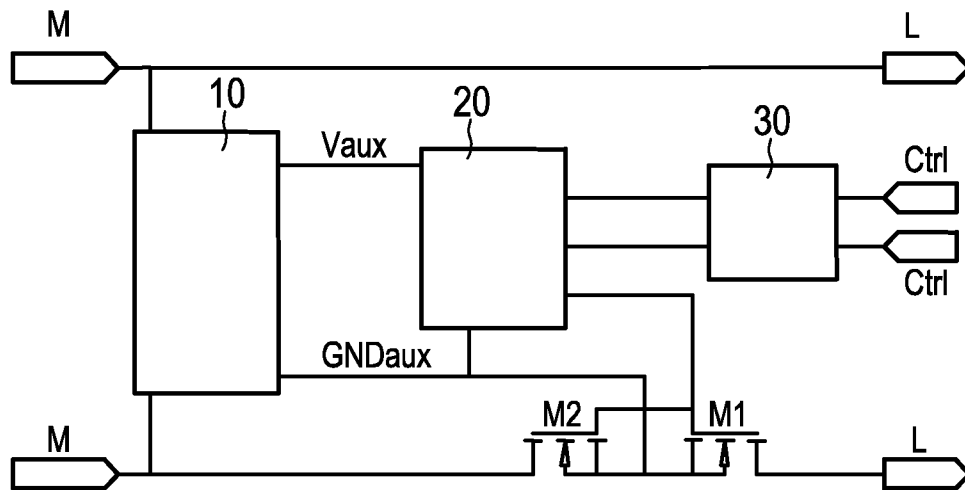


FIG. 1

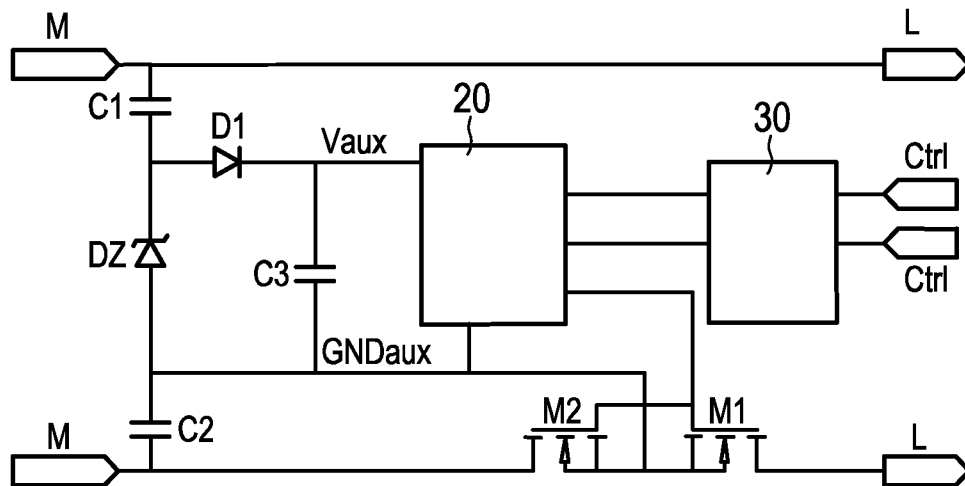


FIG. 2

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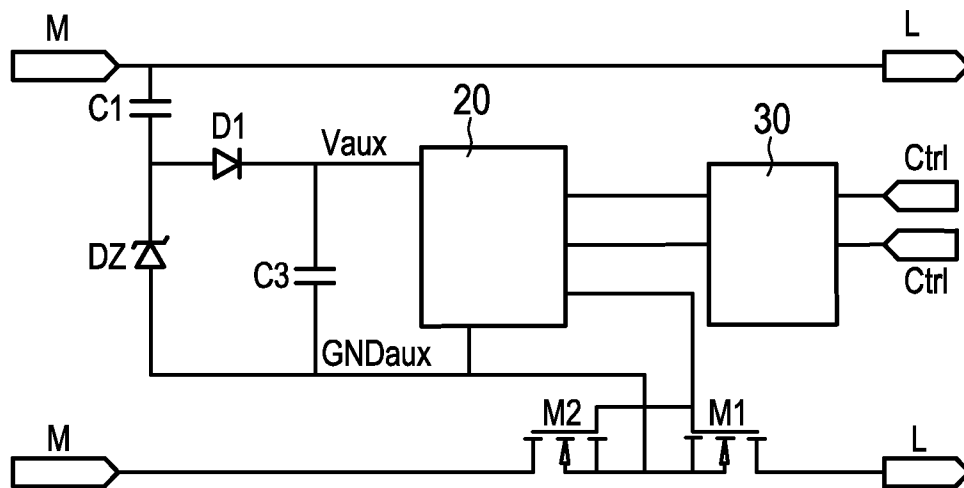


FIG. 3

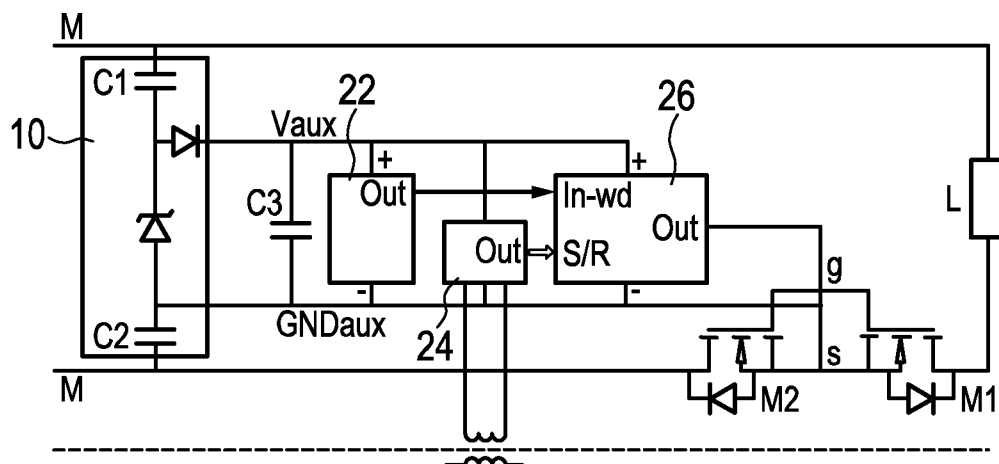


FIG. 4

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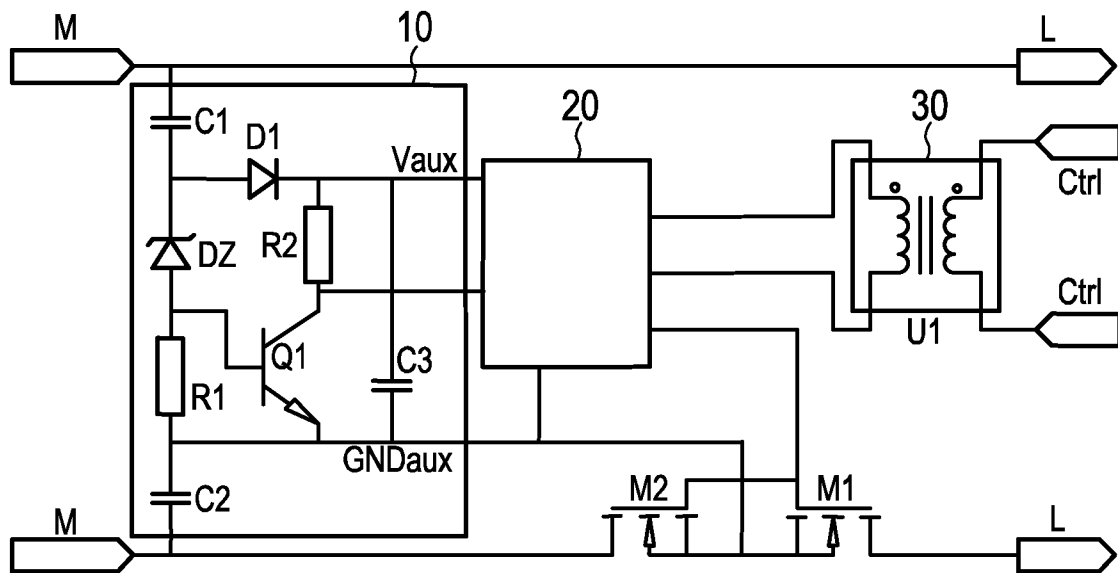


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No

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A. CLASSIFICATION OF SUBJECT MATTER

INV. H03K17/687 H03K17/691
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 5 349 242 A (TANAKA MINORU [JP] ET AL) 20 September 1994 (1994-09-20) abstract; figures 1,7 ----- -/--	1,3,6,7



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search

27 June 2012

Date of mailing of the international search report

03/07/2012

Name and mailing address of the ISA/

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Mesic, Maté

INTERNATIONAL SEARCH REPORT

International application No

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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