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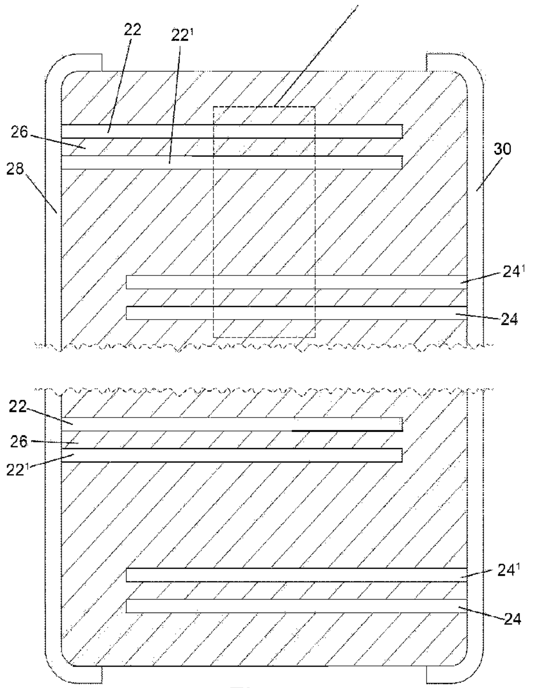

Fig. 4

(57) **Abstract:** Provided is an improved multilayered ceramic capacitor and an electronic device comprising the multilayered ceramic capacitor. The multilayer ceramic capacitor comprises first conductive plates electrically connected to first external terminations and second conductive plates electrically connected to second external terminations. The first conductive plates and second conductive plates form a capacitive couple. A ceramic portion is between the first conductive plates and said second conductive plates wherein the ceramic portion comprises paraelectric ceramic dielectric. The multilayer ceramic capacitor has a rated DC voltage and a rated AC VPP wherein the rated AC VPP is higher than the rated DC voltage.

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RESONANT MULTILAYER CERAMIC CAPACITORS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to pending U.S. Provisional Appl. No. 63/076,444 filed September 10, 2020 which is incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention is related to an improved capacitor which is particularly suitable for high voltage AC applications. More specifically, the present invention is related to a multilayered ceramic capacitor that can be reliably operated at a higher peak-to-peak AC voltage than the DC voltage rating.

BACKGROUND

[0003] There is a continuing trend towards high power electrical circuits. Though not limited thereto, the increasing demand for electric vehicles has placed a significant burden on developers of electrical circuits and components used therein. For the purposes of this invention, the focus is on the demand for the use of high voltage AC power and electronic capacitors for use therein. Multilayered ceramic capacitors (MLCC's) have been very successfully used in high voltage DC circuits and they are now often the technology of choice in such applications. The use of MLCC's in AC circuits has significant issues which has limited their wide spread use in high voltage AC applications.

[0004] A higher capacitance value MLCC draws more current so the capacitor heats-up more than an equivalent MLCC with a lower capacitance. Current $(\mathbf{I})$ is related to voltage $(\mathbf{V})$ and impedance of the capacitor $(\mathbf{Z_c})$ by the relationship shown in Equation 1.

$$\mathbf{I} = {}^{\mathbf{V}}\!/_{\mathbf{Z_c}} \quad \text{Equation 1}$$

The impedance of the capacitor ($\mathbf{Z_c}$) is a reasonable approximation to the reactance of the capacitor ($\mathbf{X_c}$) and therefore reactance can be approximated based on the measurement frequency ($\mathbf{f}$) and capacitance ($\mathbf{C}$) as shown in Equation 2.

$$\mathbf{Z_c} \cong \mathbf{X_c} = {}^{\mathbf{1}}\!/_{\mathbf{2 * \pi * f * C}} \qquad \text{Equation 2}$$

Transposing Equations 1 and 2 results in Equation 3.

$$\mathbf{I = V * 2 * \pi * f * C} \qquad \text{Equation 3}$$

Based on the relationships of Equation 3, for a given voltage and frequency, increasing capacitance will increase the current. Furthermore, Real Power dissipated is related to the current ($\mathbf{I}$) and ESR of the capacitor by Equation 4.

$$\mathbf{Real\ Power = I^2 * ESR} \qquad \text{Equation 4}$$

ESR at a given frequency is reactance of the capacitor ($\mathbf{X_c}$) multiplied by the dissipation factor of the capacitor at that frequency ($\mathbf{DF_f}$) as indicated in Equation 5.

$$\mathbf{ESR_f = X_c * DF_f} \qquad \text{Equation 5}$$

The Real Power dissipated is therefore directly proportional to the capacitance as indicated in Equation 6.

$$\mathbf{Real\ Power = V^2 * 2 * \pi * f * C * DF_f} \qquad \text{Equation 6}$$

Based on the foregoing relationships it is evident that as the current draw increases from increased capacitance, the power dissipated also increases.

[0005] In the case of MLCC’s using C0G ceramics the capacitance does not change with temperature so the current remains relatively constant. Therefore, as the part heats up the temperature generated through the real power heat dissipation must be removed, such as through external conduction, away from the MLCC. This is a critical design limitation which must be addressed.

[0006] In AC applications it is important to minimize the ripple current heating in order to achieve reliable performance. However, this is complicated by the fact that the frequency has a significant effect which must be accounted for in the design. At lower frequencies, typically at or below 100kHz, the performance of the MLCC is in a voltage-limited region whereas at higher frequencies the capability is in the current-limited region. In the current-limited region the current is limited by the subsequent heating of the part based on the relationship of Equation 4. This is illustrated the diagram in Fig. 1.

[0007] In the voltage limited region the peak-to-peak (V_{pp}) AC voltage should not exceed the DC voltage level to ensure reliable performance without excessive heating. MLCCs are typically rated by their DC voltage ($\mathbf{V_{dc}}$) that is equivalent to the AC (V_{pp}) rating. The RMS AC Voltage (V_{rms}) being related to V_{dc} by the relationship given in Equation 7.

$$\mathbf{V_{rms}} = \frac{\mathbf{V_{dc}}}{2\sqrt{2}} \quad \text{Equation 7}$$

[0008] Therefore, advances in MLCC's intended for use in DC circuitry and AC circuitry have been on a parallel course since the relationship of voltage rating has been considered correlated by the relationship of Equation 7. This has limited the use of MLCC's in high voltage AC applications to only those capacitors having a high rated DC voltage since the peak-to-peak voltage, $V_{PP} = 2\sqrt{2}\,V_{rms}$, the V_{PP} should not exceed the rated DC voltage in accordance with the prior art.

[0009] The present invention provides a MLCC with a peak to peak rated AC peak to peak voltage which far exceeds the expectation in the art based on the established relationship set forth in Equation 7. The present invention therefore provides an MLCC, and devices using an MLCC, which can withstand significantly higher AC voltage than previously considered suitable.

SUMMARY OF THE INVENTION

[0010] The present invention is related to an improved MLCC which is particularly suitable for use in high AC voltage application.

[0011] More specifically, the present invention is related to an improved MLCC which has a higher rated peak-to-peak AC voltage than DC rated voltage which is contrary to accepted theory and practice in the art.

[0012] A particular feature of the improved MLCC is the ability to withstand high AC voltage, such as 950 to 5700 V_{PP}, without significant degradation of ESR.

[0013] Yet another particular feature of the improved MLCC is the ability to withstand elevated temperature, at high AC V_{PP}, without degradation of ESR or lack of performance.

[0014] These and other embodiments, as will be realized, are provided in a multilayer ceramic capacitor comprising first conductive plates electrically connected to first external terminations and second conductive plates electrically connected to second external terminations. The first conductive plates and second conductive plates form a capacitive couple. A ceramic portion is between the first conductive plates and said second conductive plates wherein the ceramic portion comprises paraelectric ceramic dielectric. The multilayer ceramic capacitor has a rated DC voltage and a rated AC voltage wherein the rated AC V_{PP} is higher than the rated DC voltage.

[0015] Yet another embodiment is provided in an electronic device comprising a first multilayer ceramic capacitor. The multilayered ceramic capacitor comprises comprises first conductive plates electrically connected to first external terminations and second conductive plates electrically connected to second external terminations wherein the first conductive plates and second conductive plates form a capacitive couple. A ceramic portion is between the first conductive plates and second conductive plates wherein the ceramic portion comprises paraelectric ceramic dielectric. The multilayer ceramic capacitor has a rated DC voltage and a rated AC V_{PP} wherein the rated AC V_{PP} is higher than the rated DC voltage.

[0016] Yet another embodiment is provided in a method of forming a multilayered ceramic capacitor comprising:

forming a paraelectric dielectric ceramic comprising an oxide represented by General Formula A:

$$(Ca_eSr_g)_j(Zr_kTi_p)_qO_3$$

General Formula A

wherein:

$e = 0.60$ to 1.00; $g = 0.00$ to 0.40; $k = 0.50$ to 0.97; $p = 0.03$ to 0.50; and $j/q = 0.99$ to 1.01;

forming a ceramic slip comprising the dielectric ceramic;

forming a coating of the ceramic slip on a substrate;

printing a pattern of conductive ink on said coating to form a printed coating;

forming a stack comprising the printed coating wherein adjacent printed coatings are offset and alternated printed coatings are registration;

forming a laminate of the stack;

separating the laminate into green chips;

sintering the green chips wherein the conductive ink forms first conductive plates and second conductive plates and the ceramic slip forms a ceramic portion between the first conductive plates and second conductive plates; and terminating the sintered green chips.

[0017] Yet another embodiment is provided in a method of forming a multilayered ceramic capacitor comprising:

forming a paraelectric ceramic dielectric defined by General Formula B:

$$U_aX_bY_cZ_d((Ca_{1-x-y}Sr_xM_y)_m(Zr_{1-u-v}Ti_uHf_v)O_3)_{1-a-b-c-d}$$

General Formula B

wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$; $0.0001<b<0.15$; $0<c\leq0.06$; $0<d<0.06$; $0\leq x\leq1$; $0\leq y\leq1$; $0\leq u\leq1$; $0\leq v\leq0.2$; and $0.98\leq m\leq1.02$;

forming a ceramic slip comprising the paraelectric ceramic dielectric;

forming a coating of ceramic slip on a substrate;

printing a pattern of conductive ink on the coating to form a printed coating;

forming a stack comprising the printed coating wherein adjacent printed coatings are offset and alternated printed coatings are registration;

forming a laminate of the stack;

separating the laminate into green chips;

sintering the green chips wherein the conductive ink forms first conductive plates and second conductive plates and the ceramic slip forms a ceramic portion between the first conductive plates and second conductive plates; and

terminating the sintered green chips.

BRIEF DESCRIPTION OF DRAWINGS

[0018] Fig. 1 graphically illustrates MLCC capability limits as a function of frequency.

[0019] Fig. 2 graphically illustrates Temperature Coefficient of Capacitance.

[0020] Fig. 3 illustrates an MLCC in cross-sectional schematic view.

[0021] Fig. 4 illustrates an embodiment of the invention in cross-sectional schematic view.

[0022] Fig. 5 illustrates a portion of Fig. 4.

[0023] Fig. 6 illustrates an embodiment of the invention in schematic view.

[0024] Fig. 7 illustrates a schematically a ripple current testing circuit.

[0025] Fig. 8 graphically illustrates a prior art example.

[0026] Fig. 9 graphically illustrates and embodiment of the invention.

[0027] Fig. 10 graphically illustrates ripple current heating.

[0028] Fig. 11 graphically illustrates a comparison of a control and an embodiment of the invention.

[0029] Fig. 12 graphically illustrates a prior art example.

[0030] Fig. 13 graphically illustrates an embodiment of the invention.

[0031] Fig. 14 graphically illustrates a prior art example.

[0032] Fig. 15 graphically illustrates an embodiment of the invention.

[0033] Fig. 16 graphically illustrates a comparison of a prior art example and an embodiment of the invention.

[0034] Fig. 17 graphically illustrates a test condition.

[0035] Fig. 18 graphically illustrates a comparison of a prior art example and an embodiment of the invention.

[0036] Fig. 19 graphically illustrates a prior art example.

[0037] Fig. 20 graphically illustrates and embodiment of the invention.

[0038] Fig. 21 graphically illustrates and embodiment of the invention.

[0039] Fig. 22 graphically illustrates a prior art example.

[0040] Fig. 23 graphically illustrates and embodiment of the invention.

[0041] Fig. 24 is a flow-chart illustration of an embodiment of the invention.

DESCRIPTION

[0042] The present invention is related to an improved MLCC wherein the peak-to-peak rated AC (V_{PP}) exceeds the rated DC voltage by at least 10% and more preferably by at least 20%, which is contrary to expectations in the art and contradicts accepted theoretical models. More specifically, the present invention provides an MLCC with a Voltage Enhanced U2J (VEU2J) paraelectric ceramic dielectric.

[0043] A particular feature of the invention is the ability to provide an MLCC which is particularly suitable for use as a high AC V_{PP} resonant capacitor. These MLCCs are made with paraelectric VEU2J ceramic which can achieve reliable performance at higher AC V_{PP} than current MLCC's with comparable rated DC voltage as evidenced by comparative low surface temperature under the application of high AC V_{PP} for extended time. Their stability is enhanced, in part, due to a negative coefficient of capacitance above 25°C as well as a stable ESR with respect to high AC V_{PP} and temperature. These MLCCs, utilizing VEU2J dielectric, are very effective at distributing temperature evenly throughout multi-capacitor arrays under high AC V_{PP} operation. If the temperature of an individual capacitor increases the capacitance of the capacitor decreases thereby reducing the current in accordance with Equation 3. As the current decreases temperature also decreases thereby compensating for any manufacturing differences in the components themselves.

[0044] As discussed above, In the case of capacitors made with C0G ceramics the capacitance does not change significantly with temperature so the current remains relatively constant. By convention, for a C0G capacitor, capacitance changes +/-30 PPM/°C, relative to the value at 25 °C, over a temperature range of -55 °C to + 125 °C. As the capacitor heats up the temperature generated through the real power heat dissipation must be removed from the MLCC such as through external conduction. In contrast, with a capacitor comprising VEU2J ceramic the capacitance decreases with increasing temperature, as illustrated in Fig. 2, and therefore the capacitor draws less current as the part heats up.

[0045] More specifically, the present application provides a multilayer ceramic capacitor device formed by a plurality of laminated ceramic layers and a plurality of internal electrode layers wherein the ceramic layers and internal electrode layers are alternatively stacked. The ceramic layers are made by the disclosed dielectric compositions, and the internal electrodes layers are made by conductive paste mainly containing base metals such as Ni and the like. The obtained multilayer ceramic capacitor can have a temperature coefficient of capacitance within ±1000 ppm/°C over a temperature range from -55°C to 150°C after co-firing at low oxygen partial pressure.

[0046] The declining capacitance of VEU2J with increasing temperature leads to a slower increase in temperature with time even at increased AC voltages and currents. In order to assess the reliability of an MLCC under AC voltage conditions the extent of AC ripple current heating has been defined in terms of risk of failure as the surface temperature increases above ambient. For the purposes of this invention a temperature increase of ≤ 25°C above ambient is considered low risk, a temperature increase of ≥ 25°C to ≤ 50°C above ambient is considered medium risk and application specific dependent and a temperature increase ≥ 50°C above ambient is considered to have an increased risk of thermal runaway and overvoltage failures.

[0047] Rated DC voltage is the maximum DC voltage that a capacitor can store and reliably operate under this bias. Whereas rated DC voltage and rated AC V_{PP} are considered related by Equation 7, the rated AC V_{PP} and rated DC voltage are not related in the inventive capacitors. In the present invention the rated AC V_{PP} is higher than expected based rated DC voltage in accordance with Equation 7. Rated DC voltage is typically confirmed by taking a sacrificial capacitor, equivalent to a test capacitor, and exposing the sacrificial capacitor to increasing DC voltage until breakdown is achieved which is referred to as breakdown voltage. For the purpose of this invention rated DC voltage is defined as 60% of mean breakdown voltage to allow for manufacturing and test variation. Therefore, for the purposes of this invention the rated AC voltage is higher peak to peak than 60% of the DC breakdown voltage of an equivalent part.

[0048] The invention will be described with reference to the figures forming an integral, non-limiting, component of the disclosure. Throughout the various figures similar elements will be numbered accordingly.

[0049] An embodiment of the invention will be described with reference to Fig. 3 wherein a multilayered ceramic capacitor is illustrated in cross-sectional side view. First conductive plates, 3, serve as electrodes and are electrically connected to first external terminations, 9. Second conductive plates, 5, serve as electrodes and are electrically connected to second external terminations, 7. The first conductive plates and second conductive plates have opposing polarity and form a conductive couple. The electrodes are separated or isolated by VEU2J dielectric, 11. An optional but preferred resin, 12, encases a portion of the capacitor as known in the art.

[0050] An embodiment of the invention will be described with reference to Fig. 4. A portion of the capacitor of Fig. 4 is enlarged as Fig. 5. In Fig. 4, a double print capacitor, 20, is illustrated schematically in cross-sectional view. First conductive plates, 22 and 22', are double printed in close proximity and terminate at a first external termination, 28, and therefore have common polarity. The double print conductive plates are separated by VEU2J dielectric, 26. Second conductive plates, 24 and 24', are also double printed in close proximity and terminate at a second external termination, 30, and therefore have common polarity. VEU2J dielectric, 26, is between adjacent conductive plates of opposite polarity such as 22 and 24 or 22' and 24'. The separation between conductive plates of opposite polarity, D1 of Fig. 5, is at least five times the separation distance between conductive plates of common polarity, D2 of Fig. 5. More preferably the separation between conductive plates of opposite polarity is at least seven times the separation distance between conductive plates of common polarity.

[0051] The preparation of laminated ceramic capacitors is well documented and the present invention does not alter the manufacturing process to any significant degree relative to standard procedures known in the art.

[0052] A process for forming a MLCC will be described with reference to Fig. 24 wherein the process is illustrated by a flow chart representation. With reference to Fig. 24, a dielectric ceramic is formed at 60, from the dielectrics described herein preferably by solid state synthetic methods which are well known in the art. A ceramic slip is formed at 62 wherein the ceramic slip comprises the dielectric ceramic. The ceramic slip is a formable material. The ceramic slip typically comprises organic carriers and the like to allow for coating of the ceramic slip onto a substrate. A coating is formed, 64, of the ceramic slip onto a substrate. The substrate is not particularly limiting since it does not become part of the finished product. Polyethylene terephthalate (PET) is widely used in the art due to, among other things, cost and availability, and is suitable for demonstration of the invention. The method of forming the coating is not particularly limited with the exception of preference for those methods suitable for forming a coating of consistent thickness. Doctor blade methods are widely used and suitable for demonstration of the invention. The ceramic slip is dried at 66. The internal electrodes are formed by printing electrode patterns of conductive ink onto the dried ceramic slip at 68. The conductive ink preferably comprises a base metal with nickel or nickel alloy being preferred. A stack is formed at 70 wherein the stack comprises ceramic precursor layers, without printing, to form the dielectric ceramic layer which is external to the capacitive couple. Layers comprising the printed electrode pattern are then layered sequentially with adjacent layers are offset such that alternate printed electrode patterns are in registration. Additional layers which do not have printing are applied to form the opposite dielectric ceramic which is external to the capacitive couple. The layered structure is pressed and heated to form a laminate at 72. The laminate is diced to form green chips at 74. The green chips are sintered and terminated as known in the art to form a capacitor at 76.

[0053] The conductor which forms the internal electrode layers is preferably a base metal. Typical base metals are nickel and nickel alloys. Preferred nickel alloys are alloys of nickel with at least one member selected from Mn, Cr, Co, and Al, with such nickel alloys containing at least 95 wt % of nickel being more preferred. The nickel and nickel may alloys may contain up to about 0.1 wt % of phosphorous and other trace components. Other conductors which may be employed as internal electrodes such as copper, precious metal or alloys thereof with particularly preferred precious metals selected from palladium and silver. It would be understood that with copper or precious metal containing internal electrodes lower temperature firing is preferred.

[0054] The Voltage Enhanced U2J (VEU2J) ceramic is based on a calcium zirconate structure further comprising additives which enhance the ability of a capacitor comprising the VEU2J ceramic to withstand high AC V_{PP} sufficient to have a rated AC V_{PP} of at least 950 V_{PP}, up to 5700 V_{PP}, while having a rated DC voltage below the AC V_{PP}.

[0055] The VEU2J ceramic comprises a paraelectric ceramic dielectric with a negative coefficient of capacitance above 25°C. More preferably the VEU2J ceramic comprises at least 95 mole% of a paraelectric ceramic dielectric with a negative coefficient of capacitance above 25°C The paraelectric ceramic dielectric of the VEU2J dielectric is a calcium strontium zirconium titanate ceramic having General Formula A:

$$(Ca_eSr_g)_j(Zr_kTi_p)_qO_3$$

General Formula A

wherein:

e = 0.60 to 1.00;

g = 0.00 to 0.40;

k = 0.50 to 0.97;

$p = 0.03$ to 0.50; and

$j/q = 0.99$ to 1.01.

In General Formula A the VEU2J major component preferably comprises at least 90 mole % of the dielectric of General Formula A to which minor constituents are added. In General Formula A, the Ca or Zr can be substituted with Ba or Mg . In General Formula A the Zr or Ti can be substituted with Hf. The minor components may comprise a secondary component comprising Zn, Cu, Ni, Co, Fe, Mn, Cr, Al, Li, B, Si, W, Ta, Mo, Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Yu. A minimum of 0.5 mole% of these minor components is preferred.

[0056] More specifically, the VEU2J ceramic comprises an oxide represented General Formula B:

$$U_aX_bY_cZ_d((Ca_{1-x-y}Sr_xM_y)_m(Zr_{1-u-v}Ti_uHf_v)O_3)_{1-a-b-c-d}$$

General Formula B

wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$; $0.0001<b<0.15$; $0<c\leq0.06$; $0<d<0.06$; $0\leq x\leq1$; $0\leq y\leq1$; $0\leq u\leq1$; $0\leq v\leq0.2$; and $0.98\leq m\leq1.02$.

[0057] Even more specifically, the VEU2J ceramic comprises an oxide represented by General Formula B selected from the group consisting of Formula I wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo; $0<a<0.06$; $0.0001<b<0.15$; $0<c\leq 0.06$; $d=0$; $0\leq x\leq 1$; $0\leq y\leq 1$; $0\leq u<0.8$; $0\leq v\leq 0.2$; and $0.98\leq m\leq 1.02$;

Formula II wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$; $0.0001<b<0.15$; $c=0$; $0<d<0.06$; $0\leq x\leq 1$; $0\leq y\leq 1$; $0.03<u\leq 1$; $0\leq v\leq 0.2$; and $0.98\leq m\leq 1.02$;

Formula III wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$; $0.0001<b<0.15$; $c=0$; $0<d<0.02$; $0\leq x\leq 1$; $0\leq y\leq 1$; $0\leq u\leq 1$; $0\leq v\leq 0.2$; and $0.98\leq m\leq 1.02$;

Formula IV wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$; $0.0001<b<0.15$; $c=0$; $0<d<0.06$; $0\leq x\leq 1$; $0\leq y\leq 1$; $0\leq u\leq 1$; $0\leq v\leq 0.2$; and $0.98\leq m\leq 1.02$;

Formula V wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$; $0.0001<b<0.15$; $c=0$; $0<d<0.06$; $0\leq x\leq 1$; $0\leq y\leq 1$; $0.1<u<0.55$; $0\leq v\leq 0.2$; and $0.98\leq m\leq 1.02$;

Formula VI wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$; $0.0001<b<0.15$; $c=0$; $0.015<d<0.06$; $0\leq x\leq 1$; $0\leq y\leq 1$; $0.1<u<0.55$; $0\leq v\leq 0.2$; $0.98\leq m\leq 1.02$; and

Formula VII wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$; $0.0001<b<0.15$; $0<c\leq 0.06$; $0<d<0.06$; $0\leq x\leq 1$; $0\leq y\leq 1$; $0.1<u<0.8$; $0\leq v\leq 0.2$; and $0.98\leq m\leq 1.02$.

[0058] A particular advantage of the instant invention is the lack of degradation of ESR at high voltage or temperature when measured at a frequency such as 50 kHz or when measured at a frequency from 10 Hz to no more than 1 MHz and more preferably a frequency from 20 kHz to no more than 200 kHz . ESR degradation causes an increase in local heating which can further degrade the capacitor. By minimizing, or eliminating, ESR degradation the capacitor remains stable after many cycles of high AC V_{PP} or extended periods of time at high AC V_{PP}. ESR degradation due to the dielectric is best observed at lower frequencies where this is the dominant component of the ESR.

[0059] A particular advantage of the instant invention is the ability to improve thermal dissipation management in electronic devices. Inventive capacitors, with different capacitance, can be incorporated in electrical parallel. The capacitor with the higher capacitance will dissipate the most Real Power as shown by the relationship in Equation 6. Therefore, the capacitor with a higher capacitance can be physically positioned for improved heat dissipation.

[0060] In addition to the ESR stability, further advantages of the instant invention are illustrated in Fig. 6 wherein an electronic device, 40, is illustrated in partial cut-away schematic view. In Fig. 6, the electronic device comprises two capacitors, C1 and C2, in electrical parallel. If C1 increases in temperature the capacitance decreases as does the current, based on the relationship of Equation 3, which causes the temperature of C1 to decrease due to the negative thermal coefficient of capacitance of the VEU2J dielectric. Therefore, C1 is self correcting with regards to temperature increase. Unfortunately, the decrease in current in C1 causes the current to increases at C2. A thermal dissipation component, D1, positioned closer to C2 dissipates the heat from C2 which allows the combination of C1 and C2 to handle more current without heat buildup. As would be realized, thermal dissipation components can be strategically located in the vicinity of various capacitors, particularly capacitors in electrical parallel, to increase the ability of the combination of capacitors to handle more current. The thermal dissipation component is not particularly limited herein with passive devices, such as a heat sink, or active devices, such as devices which move a flowing medium or provide physical cooling, suitable for demonstration of the invention.

EXAMPLES

[0061] To assess the comparative ripple current heating the capacitors being tested were mounted on similar test coupons and the top surface temperatures were measured. This test apparatus is illustrated in schematically Fig. 7. In Fig. 7, the test apparatus, 50, comprises a sine wave generator, 52, a power amplifier, 54, a coil auto-transformer, 56, and an impedence matching unductance coil, 58, all in a circuit as illustrated schematically with the device under test (DUT).

[0062] The test apparatus design is based on the principle of inductor-capacitor resonance. A device under test (DUT) is selected, and inductance is matched to insure the assembly’s resonance frequency is appropriate for the testing conditions. While under excitation, the device temperature is taken on the top of the DUT which is the highest temperature spot. The ambient temperature is also measured continuously as a function of time. The difference between the device temperature and the ambient is reported.

[0063] The Effective Series Resistance (ESR) and Impedance (Z) measurements were acquired on a Keysight E4990A impedance analyzer with custom-made fixturing. Custom fixturing was used to provide mitigation of electromagnetic coupling between the voltage and current connections that are used to measure the

DUT. The electromagnetic coupling is mitigated by making the current and voltage traces to the DUT perpendicular to one another as they approach the DUT.

[0064] This decoupling is particularly necessary in measuring Class 1 parts made with paraelectric dielectrics to more accurately characterize their very low ESR values. The custom fixturing also allows the part to be soldered to the test fixture to reduce contact resistance and to simulate the way it would be used in practice. The traces are routed from the DUT pads on the top side to vias which connect to the back of the fixturing where they are terminated with MMCX connectors. Four short cables are used to connect the MMCX connectors on the back of the fixture to BNC connector on the front of the fixture. The measurement cables are made as short as possible to reduce any potential phase error and to increase the bandwidth of the setup.

[0065] Four separate fixtures are used in the measuring process, three for compensation and one for the DUT. Open, Short and Load fixtures are used to compensate for the parasitic residuals from the wires and fixturing used to measure the DUT. The open compensation uses the fixture as-is without a DUT or any other components soldered to the pads. The short compensation uses a copper shorting block approximately the same dimensions as a typical DUT which is soldered to the fixture pads. The load compensation uses a 50-Ω resistor soldered to the fixture pads to create a stable impedance across all measurement frequencies.

[0066] The fixture can be placed in an oven and used to measure ESR at elevated temperatures. The same fixturing and setup is used except for the measurement cables to connect the fixture and analyzer. High-temperature, 1-m cables were used so that the fixturing can be placed inside a Sun Systems chamber. The compensation is done at room temperature, typically 25°C. Then, the chamber is set to the desired test temperature and the DUT is left to soak for 10 minutes. Once the DUT temperature has reached steady state, the ESR of the DUT is measured and the temperature is adjusted to next temperature point. This process is repeated until the temperature rating of the DUT is reached. As needed, the compensation can be re-verified at each measurement temperature.

[0067] The pre and post ripple current ESR measurements are shown for the single print C0G (6 A_{rms} 750 V_{rms}) and double print VEU2J (10 A_{rms} 1250 V_{rms}) in Figs. 8 and 9 respectively.

[0068] The expected temperature rise at a distant time is projected with a power curve fit as in Equations 8 & 9 wherein A and B are summarized in the tables for all examples. If there is minimal increase in temperature rise as a function of time, the fit weakens.

$$\boldsymbol{Temperature} = \boldsymbol{A} * \boldsymbol{Time}^{\boldsymbol{B}} \qquad \text{Equation 8}$$

$$\boldsymbol{Time} = \sqrt[B]{\boldsymbol{Temperature}/\boldsymbol{A}} \qquad \text{Equation 9}$$

[0069] A series of MLCC’S were manufactured using C0G, as a control, and VEU2J dielectrics as described herein. Comparative ripple current tests were run under different conditions using the test fixtures describe above. A summary of the MLCC’s tested is provided in Table 1.

Table 1:

Comparison Example #	Dielectric	EIA Case Size	Nominal Cap. (nF)	DC Voltage rating (V_{dc})	Fired Dielectric Thick (μm)	Artwork	Single/Double Print	# Electrodes
1	COG	3640	15	2000	25	2- Serial	Single	73
	VEU2J	3640	15	2000	38	2- Serial	Single	49
	VEU2J	3640	15	2000	38	2- Serial	Double	90
2	C0G	1210	15	1000	13	Standard	Single	118
	VEU2J	1210	15	1000	23	Standard	Single	92
3	C0G	1206	10	630	10	Standard	Single	120
	VEU2J	1206	10	630	15	Standard	Single	73
4	C0G	1210	33	630	10	Standard	Single	202
	VEU2J	1210	33	630	15	Standard	Single	130

[0070] The ripple current testing comparison examples are described below.

Example 1

[0071] A series of EIA case size 3640 15nF MLCCs with a rated DC voltage of 2000 V_{dc} were manufactured using C0G and VEU2J dielectrics as described in Table 1. The ripple current heating of these MLCCs were measured at 85 kHz under various currents and temperatures as shown in Fig. 10. The electrical properties of these MLCC are show in Table 2.

Table 2:

Dielectric Type	Cap (nF)	DF (%)	IR @25°C(GOhms)	IR @125°C(GOhms)	Mean Voltage Breakdown (V_{dc})
C0G	14.87	0.018	5471	4.2	3888
VEU2J	15.79	0.013	1300	7.9	4061

[0072] These electrical properties are typical for MLCCs with a rated DC voltage of 2000 V_{dc}. In Table 2 the mean breakdown voltage of the VEU2J Capacitor slightly exceeded that of the C0G capacitor but the minimum voltage breakdowns are very similar with a mean 3 sigma for C0G of 3718V compared to 3751V for VEU2J.

[0073] In both cases the C0G and U2J can be rated as 2000 Vdc to achieve an AC rating of 707 V_{rms} based on the expected relationship of Equation 7. However, when AC Voltages are applied to each MLCC, contrary to the expectations based on theory, the VEU2J MLCC does not exhibit the self-heating expected at these and higher voltages, Fig. 10. It is important to note that in the case of the C0G the 6 A_{rms}, 750 V_{rms} applied results in the temperature reaching 25°C above ambient after about 24 hours. This AC voltage level is slightly above the 707 V_{rms} limit in accordance with Equation 7. The single print version of this VEU2J part does not heat up as much at 8.4 A_{rms}, 980 V_{rms} despite having fewer electrodes than the C0G. The fewer number of electrodes inhibits the conduction of heat from the center of the MLCC. In the case of this C0G MLCC if the AC voltage is increased to 8 A_{rms} 1000 V_{rms} the MLCCs heat up rapidly above the high-risk temperature range and at 10 A_{rms}, 1250 V_{rms} the MLCC breakdown point is reached and the capacitors breakdown.

[0074] This demonstrates that the VEU2J dielectric has unexpected benefits in terms of the ripple current handling. Increasing the number of electrodes in the VEU2J MLCCs by double printing, to match the C0G capacitors, would further improve the performance. The double printed VEU2J MLCC remains at 25°C after 24 hours at 10 A_{rms} 1250 V_{rms} which is 1.77 higher than the recommended AC voltage limit based on Equation 7. Furthermore, although the temperature of the VEU2J MLCCs increase rapidly at these high AC Voltages the temperature remains stable with time. This stability with temperature can only partially be explained by the difference in change of capacitance with temperature described earlier. Since the real power dissipated is directly proportional to ESR, as shown in Equation 4, the ESR and impedance were measured before and after exposure to ripple current.

With the post exposure parts the C0G sample had been exposed to 6 A_{rms} at 750 V_{rms} whereas the VEU2J sample had been exposed to 10 A_{rms} and 1250 V_{rms}.

[0075] Despite the VEU2J sample being tested at far higher ripple current the post test ESR shows only a small change whereas the post test ESR of the C0G sample is significantly higher. This increased ESR on exposure to high ripple current contributes to the increase in temperature observed.

Example 2

[0076] A series of EIA case size 1210 15nF MLCCs with a rated DC voltage of 1000V_{dc} were manufactured using C0G and VEU2J dielectrics. The ripple current heating of these MLCCs were measured at 100 kHz using the test method previously described and the results are shown in Fig. 11.

[0077] Under the same conditions, the VEU2J MLCCs remain in the safe range of ripple current heating whereas the C0G MLCCs rapidly heat-up to over 50°C above ambient. This AC voltage is far higher than the 353 V_{rms} expected according to Equation 7 but the VEU2J MLCC's do not exhibit significant ripple current heating.

[0078] To further understand these differences Impedance and ESR measurements were made over a broad frequency range on MLCCs before exposure to this high AC voltage and the results were compared to the MLCC post-exposure. Measurements were also made at elevated temperatures using the aforementioned test method.

[0079] The ESR results obtained at ambient temperatures for the 15nF C0G and VEU2J MLCC's are shown in Figs. 12 and 13, respectively.

[0080] The impedance values are not significantly affected by exposure to high AC Voltage whereas in the case of the C0G capacitors, at frequencies of less than 1MHz, the ESR post-exposure can be 10 times higher than the pre-exposure ESR or above an order of magnitude. In the case of the VEU2J capacitors the ESR remains very similar in the post-exposure MLCC at less than two times increase at any frequency. This is very critical for ripple current heating since the Real Power dissipated is directly proportional to ESR as indicate by Equation 4. Measurements were also made pre (virgin) and post-exposure up to 100°C. Examples of these measurements over a broad frequency range are shown in Figs. 14 and 15 respectively.

[0081] At higher temperatures there is little difference in the pre (virgin) and post-exposure ESR data for VEU2J capacitors. This can be seen more clearly by extracting the ESR data measured at different temperatures at 100kHz as shown in Fig. 16.

[0082] At 100kHz the ESR of the post-exposure VEU2J capacitor barely changes with increased temperature whereas the ESR of the post exposure C0G capacitor is increased by over 5 times at 100°C compared to the pre-test part.

Example 3

[0083] A series of EIA case size 1206 10nF MLCCs with a rated DC voltage of 630 V_{DC} were manufactured using C0G and VEU2J capacitors. The ripple current heating of these MLCCs were measured at 85 kHz using the test method previously described. In this case the heating of the parts is similar as shown in Fig. 17.

[0084] Although the ripple current heating appears similar the temperature of the VEU2J capacitors has a slower rate of increase with time so the parts do not reach 25°C as quickly as the C0G capacitors.

Example 4

[0085] A series of EIA case size 1210 33nF MLCCs with a rated DC voltage of 630 V_{DC} were manufactured using C0G and VEU2J dielectrics. The ripple current heating of these MLCCs were measured at 50 kHz at an ambient temperature of 85°C and the results are shown in Fig. 18.

[0086] At this elevated ambient temperature of 85°C the ripple current heating is far less for VEU2J than for the equivalent C0G MLCC. The pre (virgin) and post ripple ESR for these parts are shown in Figs. 19 and 20.

[0087] The results of ESR at various temperatures pre (virgin) and post ripple measured as 50 kHz is reported in Table 3.

Table 3:

Dielectric	**Treatment**	**ESR (mOhm)**		
		25°C	**85°C**	**125°C**
C0G	Pre(virgin)	4.2	6.5	14.0
C0G	Post Ripple	6.5	10.3	17.3
VEU2J	Pre(virgin)	8.1	9.7	13.1
VEU2J	Post Ripple	8.3	9.8	12.9

[0088] As indicated in Table 3, the ESR of the C0G sample increases over 23% at all temperature and over 50% at 25°C and 85°C. The VEU2J capacitor exhibited less than 2% increase in ESR.

[0089] To understand the rate of heating differences in the C0G vs VEU2J MLCC’s all the time to temperatures of 25°C and 50°C using the aforementioned power curve fitting Examples 1, 2, 3 and 4 are summarized with the test conditions in Table 4 and the results in Table 5. To achieve a better curve fitting in 2 cases the surface temperatures recorded from the first 5 hours were not considered as noted.

Table 4:

Example	**Dielectric**	**Print**	**Test AC Voltage V_{RMS}**	**Test AC V_{PP}**	**Test AC Current (A_{RMS})**	**Frequency (kHz)**	**Test voltage/Max AC voltage**
1	C0G	single	750	2114	6	85	1.06
1	VEU2J	single	980	2762	8.4	85	1.39
1	VEU2J	double	750	2114	6	85	1.06
1	VEU2J	double	1125	3170	9	85	1.59
1	VEU2J	double	1250	3523	10	85	1.77
2	C0G	single	575	1620	5.4	100	1.62
2	VE2UJ	single	575	1620	5.4	100	1.62
3	C0G	single	375	1057	2.0	85	1.68
3	VEU2J	single	375	1057	2.0	85	1.68
4	C0G	single	380	1071	3.5	50	1.70
4	VEU2J	Single	380	1071	3.5	50	1.70

Table 5:

Example	**Dielectric**	**Print**	**Time to 25°C (hours)**	**Time to 50°C (hours)**	**A**	**B**	**R2 Factor (%)**
1	C0G	single	24	470	11.8	0.235	98.6
1	VEU2J	single	1560	4,359,845,471	17.4	0.0467	95.4
1	VEU2J	double	4,420,000	5,150,000,000	5.57	0.09817	78.3[#]
1	VEU2J	double	43,912	42,976,359,107	14.6	0.0503	96.0
1	VEU2J	double	35	563,126	19.0	0.0715	96.3
2	C0G	single	0.0019	1.5	48.3	0.105	94.6
2	VEU2J	single	5.68×10^{8}	50.7×10^{12}	7.34	0.0608	81.0[#]
3	C0G	single	35,000	1,790,891	3.91	0.177	98.6
3	VEU2J	single	1,547,441	414,262,132	4.27	0.124	94.7

4	C0G	single	4	145	19.3	0.191	98.5
4	VEU2J	Single	23,000	1,230,000	4.35	0.174	98.6

Surface temperature data from initial 5 hours not fitted in these cases

[0090] In Example 1 the VEU2J double print MLCCs remain at 25°C after 24 hours at 10 A_{rms} 1250 V_{rms} which is 1.77 times higher than the AC voltage limit based on Equation 7. Furthermore, although the temperature of the VEU2J MLCCs increase rapidly at these high AC Voltages the temperature remains stable with time. This temperature stability under applied AC Voltage is critical with respect to long term reliability. The predicted times to reach critical temperatures of 25°C and 50°C remain far higher for VEU2J even when the test voltages are increased compared to the C0G.

[0091] The VEU2J MLCC of Example 2 experienced far less heating than a C0G MLCC with the same nominal capacitance so their reliability under AC voltage at this frequency is much better. In the case of Example 3, even when the surface heating of the C0G and VEU2J MLCCs appears similar, the curve fitting shows that the VEU2J surface temperature does not increase as quickly with time so it will take far longer to reach the critical temperature.

[0092] Furthermore, in arrays of 2 or more capacitors of VEU2J in electrical parallel in the same circuit the higher capacitance value MLCC would have a higher proportion of the current, indicated by Equation 3, but as this heated up capacitance would be lowered and so the current shared more evenly between the 2 MLCCs. This helps distribute the current more evenly between arrays of capacitors even when these are arranged serially in a matrix.

Example 5

[0093] A series of EIA case size 1210 33nF MLCCs with a rated DC voltage of 630V_{DC} manufactured using C0G and VEU2J dielectrics were mounted on a test board. The ripple current heating was measured for both types of dielectrics at 100kHz with and without a DC bias voltage of 472.5V applied at 25°C. The temperature rise as a function of time was measured and is shown in Figure 21.

[0094] The C0G MLCCs failed short as the test was continued. The same C0G MLCC was exposed for a shorter time of 1.5 hours under the same conditions with DC Bias voltage applied at an ambient temperature of 25°C to allow ESR changes to be assessed. The pre(virgin) and post ripple ESR for the C0G are compared after 1.5 hours exposure to this ripple current and bias is shown in Figure 22. As already shown in the other examples of exposure to pure AC voltages the ESR increased significantly even when DC bias was applied. Ripple current testing of the VEU2J MLCC with the biased voltage applied was continued for 66 hours but no further increase in temperature was detected. The pre(virgin) and post ripple ESR for these VEU2J MLCCs are shown in Figure 23. Despite this long exposure no increase in ESR was detected in the VEU2J MLCC.

[0095] These results show that the VEU2J heats up less than C0G even when a DC bias voltage is applied in addition to the AC ripple voltage.

[0096] The invention has been described with reference to the preferred embodiments without limit thereto. Additional embodiments and improvements may be realized which are not specifically set forth herein but which are within the scope of the invention as more specifically set forth in the claims appended hereto.

Claimed is:

1. A multilayer ceramic capacitor comprising:

first conductive plates electrically connected to first external terminations and second conductive plates electrically connected to second external terminations wherein said first conductive plates and said second conductive plates form a capacitive couple; and

a ceramic portion between said first conductive plates and said second conductive plates wherein said ceramic portion comprises paraelectric ceramic dielectric;

wherein said multilayer ceramic capacitor has a rated DC voltage and a rated AC V_{PP} wherein said rated AC V_{PP} is higher than said rated DC voltage.

2. The multilayer ceramic capacitor of claim 1 wherein said rated AC V_{PP} is 950 V_{PP} to 5700 V_{PP}.

3. The multilayer ceramic capacitor of claim 1 wherein said paraelectric ceramic dielectric comprises an oxide defined by General Formula A:

$$(Ca_eSr_g)_j(Zr_kTi_p)_qO_3$$

General Formula A

wherein:

e = 0.60 to 1.00;

g = 0.00 to 0.40;

k = 0.50 to 0.97;

p = 0.03 to 0.50; and

j/q = 0.99 to 1.01.

4. The multilayer ceramic capacitor of claim 3 wherein at least 90 mole % of said ceramic portion is said paraelectric ceramic dielectric defined by General Formula A.

5. The multilayer ceramic capacitor of claim 3 wherein said Ca or Zr are substituted with Ba or Mg.

6. The multilayer ceramic capacitor of claim 3 wherein said Zr or Ti are substituted with Hf.

7. The multilayer ceramic capacitor of claim 3 wherein said paraelectric ceramic dielectric further comprise a secondary component comprising at least one element selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, Al, Li, B, Si, W, Ta, Mo, Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Yu.

8. The multilayer ceramic capacitor of claim 7 wherein said paraelectric ceramic dielectric comprises at least 0.5 mole% of said secondary component.

9. The multilayer ceramic capacitor of claim 1 wherein said paraelectric ceramic dielectric is defined by General Formula B:

$$U_aX_bY_cZ_d((Ca_{1-x-y}Sr_xM_y)_m(Zr_{1-u-v}Ti_uHf_v)O_3)_{1-a-b-c-d}$$

General Formula B

wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$0<c\leq 0.06$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0\leq u\leq 1$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$.

10. The multilayer ceramic capacitor of claim 9 wherein said paraelectric ceramic dielectric is selected from the group consisting of Formula I wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

$0<a<0.06$;

$0.0001<b<0.15$;

$0<c\leq0.06$;

$d=0$;

$0\leq x\leq1$;

$0\leq y\leq1$;

$0\leq u<0.8$;

$0\leq v\leq0.2$; and

$0.98\leq m\leq1.02$;

Formula II wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.06$;

$0\leq x\leq1$;

$0 \le y \le 1$;

$0.03 < u \le 1$;

$0 \le v \le 0.2$; and

$0.98 \le m \le 1.02$;

Formula III wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0 < a < 0.06$;

$0.0001 < b < 0.15$;

$c = 0$;

$0 < d < 0.02$;

$0 \le x \le 1$;

$0 \le y \le 1$;

$0 \le u \le 1$;

$0 \le v \le 0.2$; and

$0.98 \le m \le 1.02$;

Formula IV wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0\leq u\leq 1$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$;

Formula V wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0.1<u<0.55$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$;

Formula VI wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0.015<d<0.06$;

$0 \leq x \leq 1$;

$0 \leq y \leq 1$;

$0.1<u<0.55$;

$0 \leq v \leq 0.2$; and

$0.98 \leq m \leq 1.02$; and

Formula VII wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$0<c \leq 0.06$;

$0<d<0.06$;

$0 \leq x \leq 1$;

$0 \leq y \leq 1$;

$0.1 < u < 0.8$;

$0 \leq v \leq 0.2$; and

$0.98 \leq m \leq 1.02$.

11. The multilayer ceramic capacitor of claim 9 wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

$0 < a < 0.06$;

$0.0001 < b < 0.15$;

$0 < c \leq 0.06$;

$d = 0$;

$0 \leq x \leq 1$;

$0 \leq y \leq 1$;

$0 \leq u < 0.8$;

$0 \leq v \leq 0.2$; and

$0.98 \leq m \leq 1.02$.

12. The multilayer ceramic capacitor of claim 11 wherein U is Mn.

13. The multilayer ceramic capacitor of claim 11 wherein X is Si.

14. The multilayer ceramic capacitor of claim 11 wherein Y is W.

15. The multilayer ceramic capacitor of claim 9 wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0.03<u\leq 1$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$.

16. The multilayer ceramic capacitor of claim 15 wherein M is Ba.

17. The multilayer ceramic capacitor of claim 15 wherein U is Mn.

18. The multilayer ceramic capacitor of claim 15 wherein X is Si.

19. The multilayer ceramic capacitor of claim 15 wherein Z is selected from the group consisting of Ce, Eu, Gd, Tb, and Dy.

20. The multilayer ceramic capacitor of claim 9 wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.02$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0\leq u\leq 1$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$.

21. The multilayer ceramic capacitor of claim 20 wherein M is Ba.

22. The multilayer ceramic capacitor of claim 20 wherein U is Mn.

23. The multilayer ceramic capacitor of claim 20 wherein X is Si.

24. The multilayer ceramic capacitor of claim 20 wherein Z is selected from the group consisting of Pr, Eu, Gd, Tb and Dy.

25. The multilayer ceramic capacitor of claim 9 wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0\leq u\leq 1$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$.

26. The multilayer ceramic capacitor of claim 25 wherein M is Ba.

27. The multilayer ceramic capacitor of claim 25 wherein U is Mn.

28. The multilayer ceramic capacitor of claim 25 wherein X is Si.

29. The multilayer ceramic capacitor of claim 25 wherein Z is selected from the group consisting of Nd, Eu, Gd and Tb.

30. The multilayer ceramic capacitor of claim 9 wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0.1<u<0.55$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$.

31. The multilayer ceramic capacitor of claim 30 wherein M is Ba.

32. The multilayer ceramic capacitor of claim 30 wherein U is Mn.

33. The multilayer ceramic capacitor of claim 30 wherein X is Si.

34. The multilayer ceramic capacitor of claim 30 wherein Z is selected from the group consisting of Eu, Gd, Tb and Dy.

35. The multilayer ceramic capacitor of claim 9 wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0.015<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0.1<u<0.55$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$.

36. The multilayer ceramic capacitor of claim 35 wherein M is Ba.

37. The multilayer ceramic capacitor of claim 35 wherein U is Mn.

38. The multilayer ceramic capacitor of claim 35 wherein X is Si.

39. The multilayer ceramic capacitor of claim 35 wherein Z is selected from the group consisting of Y, Eu, Gd, Tb and Dy.

40. The multilayer ceramic capacitor of claim 9 wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$0<c\leq0.06$;

$0<d<0.06$;

$0\leq x\leq1$;

$0\leq y\leq1$;

$0.1<u<0.8$;

$0\leq v\leq0.2$; and

$0.98\leq m\leq1.02$.

41. The multilayer ceramic capacitor of claim 40 wherein M is Ba.

42. The multilayer ceramic capacitor of claim 40 wherein U is Mn.

43. The multilayer ceramic capacitor of claim 40 wherein X is Si.

44. The multilayer ceramic capacitor of claim 40 wherein Y is W.

45. The multilayer ceramic capacitor of claim 40 wherein Z is Y.

46. The multilayer ceramic capacitor of claim 1 having a temperature characteristic of capacitance within ±1000 ppm/°C over a temperature range from -55 °C to 150 °C.

47. The multilayer ceramic capacitor of claim 1 wherein said paraelectric ceramic dielectric has a negative coefficient of capacitance above 25°C.

48. The multilayered ceramic capacitor of claim 1 wherein said capacitor has a first ESR measured at 50kHz prior to exposure to a AC V_{PP} above said rated DC voltage and a second ESR measured at 50kHz after exposure to said AC V_{PP} wherein said second ESR is no more than 20% higher than said first ESR.

49. The multilayered ceramic capacitor of claim 48 wherein said exposure to said AC V_{PP} is at a temperature above 25°C.

50. The multilayered ceramic capacitor of claim 49 wherein said exposure to said AC V_{PP} is at a temperature above 50°C.

51. The multilayered ceramic capacitor of claim 50 wherein said exposure to said AC V_{PP} is at a temperature of up to 100°C.

52. The multilayered ceramic capacitor of claim 48 wherein said second ESR is no more than 10% higher than said first ESR.

53. The multilayered ceramic capacitor of claim 1 wherein said capacitor has a first ESR measured at 10 Hz to no more than 1 MHz prior to exposure to a AC V_{PP} above said rated DC voltage and a second ESR measured at 10 Hz to no more than 1 MHz after exposure to said AC V_{PP} wherein said second ESR is no more than 20% higher than said first ESR.

54. The multilayered ceramic capacitor of claim 52 wherein said frequency is at least 20 kHz to no more than 200 kHz.

55. The multilayered ceramic capacitor of claim 1 wherein said capacitor has a surface temperature and said surface temperature does not exceed 25°C after exposure to a AC V_{PP} above said rated DC voltage for 24 hours.

56. The multilayered ceramic capacitor of claim 55 wherein said surface temperature does not exceed 25°C after exposure to a said AC V_{PP} for at least 35,000 hours.

57. The multilayered ceramic capacitor of claim 56 wherein said surface temperature does not exceed 25°C after exposure to a said AC V_{PP} for at least 500,000 hours.

58. The multilayered ceramic capacitor of claim 57 wherein said surface temperature does not exceed 25°C after exposure to an said AC V_{PP} for at least 2,000,000 hours.

59. The multilayered ceramic capacitor of claim 1 wherein said first conductive plates are first double printed conductive plates.

60. The multilayered ceramic capacitor of claim 59 further comprising paraelectric ceramic dielectric between said first double printed conductive plates.

61. The multilayered ceramic capacitor of claim 60 wherein said first conductive plates and said second conductive plates are separated by a first distance and said first double printed conductive plates are separated by a second distance wherein said first distance is larger than said second distance.

62. The multilayered ceramic capacitor of claim 61 wherein said first distance is at least twice said second distance.

63. The multilayered ceramic capacitor of claim 1 wherein at least one of said first conductive plates or said second conductive plates comprise a base metal.

64. The multilayered ceramic capacitor of claim 63 wherein said base metal is nickel.

65. The multilayered ceramic capacitor of claim 64 wherein said DC rated voltage is 60% of a mean breakdown voltage.

66. An electronic device comprising:

a first multilayer ceramic capacitor comprising:

first conductive plates electrically connected to first external terminations and second conductive plates electrically connected to second external terminations wherein said first conductive plates and said second conductive plates form a capacitive couple; and

a ceramic portion between said first conductive plates and said second conductive plates wherein said ceramic portion comprises paraelectric ceramic dielectric;

wherein said multilayer ceramic capacitor has a rated DC voltage and a rated AC V_{PP} wherein said rated AC V_{PP} is higher than said rated DC voltage.

67. The electronic device of claim 66 further comprising a second multilayer ceramic capacitor wherein said first multilayer ceramic capacitor and said second multilayer ceramic capacitor are in electrical parallel.

68. The electronic device of claim 67 wherein said first multilayer ceramic capacitor has a higher capacitance than said second multilayer ceramic capacitor.

69. The electronic device of claim 68 wherein said electronic device further comprises a thermal dissipation element.

70. The electronic device of claim 69 wherein said thermal dissipation element is closer to said first capacitor than said second capacitor.

71. The electronic device of claim 66 further comprising a second multilayer ceramic capacitor wherein said first multilayer ceramic capacitor and said second multilayer ceramic capacitor are in electrical series.

72. The electronic device of claim 71 wherein said first multilayer ceramic capacitor has a higher capacitance than said second multilayer ceramic capacitor.

73. The electronic device of claim 72 wherein said electronic device further comprises a thermal dissipation element.

74. The electronic device of claim 73 wherein said thermal dissipation element is closer to said first capacitor than said second capacitor.

75. The electronic device of claim 66 wherein said rated AC V_{PP} is 950 V_{PP} to 5700 V_{PP}.

76. The electronic device of claim 66 wherein said paraelectric ceramic dielectric is defined by General Formula A:

$$(Ca_eSr_g)_j(Zr_kTi_p)_qO_3$$

General Formula A

wherein:

e = 0.60 to 1.00;

g = 0.00 to 0.40;

k = 0.50 to 0.97;

p = 0.03 to 0.50; and

j/q = 0.99 to 1.01.

77. The electronic device of claim 76 wherein at least 90 mole % of said ceramic portion is said paraelectric ceramic dielectric defined by General Formula A.

78. The electronic device of claim 76 wherein said Ca or Zr are substituted with Ba or Mg.

79. The electronic device of claim 76 wherein said Zr or Ti are substituted with Hf.

80. The electronic device of claim 76 wherein said paraelectric ceramic dielectric further comprise a secondary component comprising at least one element selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, Al, Li, B, Si, W, Ta, Mo, Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Yu.

81. The electronic device of claim 80 wherein said paraelectric ceramic dielectric comprises at least 0.5 mole% of said secondary component.

82. The electronic device of claim 66 wherein said paraelectric ceramic dielectric is defined by General Formula B:

$$U_aX_bY_cZ_d((Ca_{1-x-y}Sr_xM_y)_m(Zr_{1-u-v}Ti_uHf_v)O_3)_{1-a-b-c-d}$$

General Formula B

wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$0<c\leq 0.06$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0\leq u\leq 1$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$.

83. The electronic device of claim 82 wherein said paraelectric ceramic dielectric is selected from the group consisting of Formula I wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

$0<a<0.06$;

$0.0001<b<0.15$;

$0<c\leq 0.06$;

$d=0$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0\leq u<0.8$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$;

Formula II wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0.03<u\leq 1$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$;

Formula III wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.02$;

$0 \leq x \leq 1$;

$0 \leq y \leq 1$;

$0 \leq u \leq 1$;

$0 \leq v \leq 0.2$; and

$0.98 \leq m \leq 1.02$;

Formula IV wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0\leq u\leq 1$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$;

Formula V wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.06$;

$0 \leq x \leq 1$;

$0 \leq y \leq 1$;

$0.1<u<0.55$;

$0 \leq v \leq 0.2$; and

$0.98 \leq m \leq 1.02$;

Formula VI wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0.015<d<0.06$;

$0 \leq x \leq 1$;

$0 \leq y \leq 1$;

$0.1<u<0.55$;

$0 \leq v \leq 0.2$; and

$0.98 \leq m \leq 1.02$; and

Formula VII wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0 < a < 0.06$;

$0.0001 < b < 0.15$;

$0 < c \leq 0.06$;

$0 < d < 0.06$;

$0 \leq x \leq 1$;

$0 \leq y \leq 1$;

$0.1 < u < 0.8$;

$0 \leq v \leq 0.2$; and

$0.98 \leq m \leq 1.02$.

84. The electronic device of claim 82 wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

$0<a<0.06$;

$0.0001<b<0.15$;

$0<c\leq 0.06$;

$d=0$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0\leq u<0.8$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$.

85. The electronic device of claim 84 wherein U is Mn.

86. The electronic device of claim 84 wherein X is Si.

87. The electronic device of claim 84 wherein Y is W.

88. The electronic device of claim 82 wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.02$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0\leq u\leq 1$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$.

89. The electronic device of claim 88 wherein M is Ba.

90. The electronic device of claim 88 wherein U is Mn.

91. The electronic device of claim 88 wherein X is Si.

92. The electronic device of claim 88 wherein Z is selected from the group consisting of Ce, Eu, Gd, Tb, and Dy.

93. The electronic device of claim 82 wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.02$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0\leq u\leq 1$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$.

94. The electronic device of claim 93 wherein M is Ba.

95. The electronic device of claim 93 wherein U is Mn.

96. The electronic device of claim 93 wherein X is Si.

97. The electronic device of claim 93 wherein Z is selected from the group consisting of Pr, Eu, Gd, Tb and Dy.

98. The electronic device of claim 82 wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0\leq u\leq 1$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$.

99. The electronic device of claim 98 wherein M is Ba.

100. The electronic device of claim 98 wherein U is Mn.

101. The electronic device of claim 98 wherein X is Si.

102. The electronic device of claim 98 wherein Z is selected from the group consisting of Nd, Eu, Gd and Tb.

103. The electronic device of claim 82 wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0.1<u<0.55$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$.

104. The electronic device of claim 103 wherein M is Ba.

105. The electronic device of claim 103 wherein U is Mn.

106. The electronic device of claim 103 wherein X is Si.

107. The electronic device of claim 103 wherein Z is selected from the group consisting of Eu, Gd, Tb and Dy.

108. The electronic device of claim 82 wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0.015<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0.1<u<0.55$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$.

109. The electronic device of claim 108 wherein M is Ba.

110. The electronic device of claim 108 wherein U is Mn.

111. The electronic device of claim 108 wherein X is Si.

112. The electronic device of claim 108 wherein Z is selected from the group consisting of Y, Eu, Gd, Tb and Dy.

113. The electronic device of claim 82 wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$0<c\leq0.06$;

$0<d<0.06$;

$0\leq x\leq1$;

$0\leq y\leq1$;

$0.1<u<0.8$;

$0\leq v\leq0.2$; and

$0.98\leq m\leq1.02$.

114. The electronic device of claim 66 having a temperature characteristic of capacitance within ±1000 ppm/°C over a temperature range from -55 °C to 150 °C.

115. The electronic device of claim 66 wherein said paraelectric ceramic dielectric has a negative coefficient of capacitance above 25°C.

116. The electronic device of claim 66 wherein said capacitor has a first ESR measured at 50kHz prior to exposure to a AC V_{PP} above said rated DC voltage and a second ESR measured at 50kHz after exposure to said AC V_{PP} wherein said second ESR is no more than 20% higher than said first ESR.

117. The electronic device of claim 116 wherein said exposure to said AC V_{PP} is at a temperature above 25°C.

118. The electronic device of claim 117 wherein said exposure to said AC V_{PP} is at a temperature above 50°C.

119. The electronic device of claim 118 wherein said exposure to said AC V_{PP} is at a temperature of up to 100°C.

120. The electronic device of claim 116 wherein said second ESR is no more than 10% higher than said first ESR.

121. The electronic device of claim 66 wherein said capacitor has a first ESR measured at 10 Hz to no more than 1 MHz prior to exposure to a AC V_{PP} above said rated DC voltage and a second ESR measured at 10 Hz to no more than 1 MHz after exposure to said AC V_{PP} wherein said second ESR is no more than 20% higher than said first ESR .

122. The electronic device of claim 121 wherein said frequency is at least 20 kHz to no more than 200 kHz.

123. The electronic device of claim 66 wherein said capacitor has a surface temperature and said surface temperature does not exceed 25°C after exposure to a AC V_{PP} above said rated DC voltage for 24 hours.

124. The electronic device of claim 123 wherein said surface temperature does not exceed 25°C after exposure to a said AC V_{PP} for at least 35,000 hours.

125. The electronic device of claim 124 wherein said surface temperature does not exceed 25°C after exposure to a said AC V_{PP} for at least 500,000 hours.

126. The electronic device of claim 125 wherein said surface temperature does not exceed 25°C after exposure to an said AC V_{PP} for at least 2,000,000 hours.

127. The electronic device of claim 66 wherein said first conductive plates are first double printed conductive plates.

128. The electronic device of claim 127 further comprising paraelectric ceramic dielectric between said first double printed conductive plates.

129. The electronic device of claim 128 wherein said first conductive plates and said second conductive plates are separated by a first distance and said first double printed conductive plates are separated by a second distance wherein said first distance is larger than said second distance.

130. The electronic device of claim 129 wherein said first distance is at least twice said second distance.

131. The electronic device of claim 66 wherein at least one of said first conductive plates or said second conductive plates comprise a base metal.

132. The electronic device of claim 131 wherein said base metal is nickel.

133. The electronic device of claim 66 wherein said DC rated voltage is 60% of a mean breakdown voltage.

134. The electronic device of claim 66 wherein at least a portion of said electronic device operates with AC current.

135. The electronic device of claim 66 wherein at least a portion of said electronic device operates with DC current.

136. The electronic device of claim 66 wherein at least a portion of said electronic device operates with AC current and at least a portion of said electronic device operates with DC current.

137. A method of forming a multilayered ceramic capacitor comprising:

forming a paraelectric dielectric ceramic comprising an oxide represented by General Formula A:

$$(Ca_eSr_g)_j(Zr_kTi_p)_qO_3$$

General Formula A

wherein:

e = 0.60 to 1.00;

g = 0.00 to 0.40;

k = 0.50 to 0.97;

p = 0.03 to 0.50; and

j/q = 0.99 to 1.01;

forming a ceramic slip comprising said dielectric ceramic;

forming a coating of said ceramic slip on a substrate;

printing a pattern of conductive ink on said coating to form a printed coating;

forming a stack comprising said printed coating wherein adjacent printed coatings are offset and alternated printed coatings are registration;

forming a laminate of said stack;

separating said laminate into green chips;

sintering said green chips wherein said conductive ink forms first conductive plates and second conductive plates and said ceramic slip forms a ceramic portion between said first conductive plates and said second conductive plates; and

terminating said sintered green chips.

138. The method of forming a multilayered ceramic capacitor of claim 137 wherein at least 90 mole % of said ceramic portion is said paraelectric ceramic dielectric defined by General Formula A.

139. The method of forming a multilayered ceramic capacitor of claim 137 wherein said Ca or Zr are substituted with Ba or Mg.

140. The method of forming a multilayered ceramic capacitor of claim 137 wherein said Zr or Ti are substituted with Hf.

141. The method of forming a multilayered ceramic capacitor of claim 137 wherein said paraelectric ceramic dielectric further comprise a secondary component comprising at least one element selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, Al, Li, B, Si, W, Ta, Mo, Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Yu.

142. The method of forming a multilayered ceramic capacitor of claim 141 wherein said paraelectric ceramic dielectric comprises at least 0.5 mole% of said secondary component.

143. The method of forming a multilayered ceramic capacitor of claim 137 wherein said first conductive plates and said second conductive plates are separated by a first distance and said first double printed conductive plates are separated by a second distance wherein said first distance is larger than said second distance.

144. The method of forming a multilayered ceramic capacitor of claim 143 wherein said first distance is at least twice said second distance.

145. The method of forming a multilayered ceramic capacitor of claim 137 wherein at least one of said first conductive plates or said second conductive plates comprise a base metal.

146. The method of forming a multilayered ceramic capacitor of claim 145 wherein said base metal is nickel.

147. A method of forming a multilayered ceramic capacitor comprising:

forming a paraelectric ceramic dielectric defined by General Formula B:

$$U_aX_bY_cZ_d((Ca_{1-x-y}Sr_xM_y)_m(Zr_{1-u-v}Ti_uHf_v)O_3)_{1-a-b-c-d}$$

General Formula B

wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$0<c\leq 0.06$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0\leq u\leq 1$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$;

forming a ceramic slip comprising said paraelectric ceramic dielectric;

forming a coating of said ceramic slip on a substrate;

printing a pattern of conductive ink on said coating to form a printed coating;

forming a stack comprising said printed coating wherein adjacent printed coatings are offset and alternated printed coatings are registration;

forming a laminate of said stack;

separating said laminate into green chips;

sintering said green chips wherein said conductive ink forms first conductive plates and second conductive plates and said ceramic slip forms a ceramic portion between said first conductive plates and said second conductive plates; and

terminating said sintered green chips.

148. The method of forming a multilayered ceramic capacitor of claim 147 wherein said paraelectric ceramic dielectric is selected from the group consisting of Formula I wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

$0<a<0.06$;

$0.0001<b<0.15$;

$0<c\leq 0.06$;

$d=0$;

$0 \leq x \leq 1$;

$0 \leq y \leq 1$;

$0 \leq u < 0.8$;

$0 \leq v \leq 0.2$; and

$0.98 \leq m \leq 1.02$;

Formula II wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0 < a < 0.06$;

$0.0001 < b < 0.15$;

$c = 0$;

$0 < d < 0.06$;

$0 \leq x \leq 1$;

$0 \leq y \leq 1$;

$0.03 < u \leq 1$;

$0 \leq v \leq 0.2$; and

$0.98 \leq m \leq 1.02$;

Formula III wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.02$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0\leq u\leq 1$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$;

Formula IV wherein:

M is Ba;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, and Cr;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0\leq u\leq 1$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.02$;

Formula V wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$c=0$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0 \leq y \leq 1$;

$0.1 < u < 0.55$;

$0 \leq v \leq 0.2$; and

$0.98 \leq m \leq 1.02$;

Formula VI wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0 < a < 0.06$;

$0.0001 < b < 0.15$;

$c = 0$;

$0.015 < d < 0.06$;

$0 \leq x \leq 1$;

$0 \leq y \leq 1$;

$0.1 < u < 0.55$;

$0 \leq v \leq 0.2$; and

$0.98 \leq m \leq 1.02$; and

Formula VII wherein:

M is at least one alkaline earth selected from the group consisting of Ba and Mg;

U comprising a carbonate or oxide of at least one first transition metal selected from the group consisting of Zn, Cu, Ni, Co, Fe, Mn, Cr, and Al;

X comprises at least one sintering aid comprising a compound comprising at least one element selected from the group consisting of Li, B, and Si;

Y comprises a carbonate or oxide of at least one second transition metal selected from the group consisting of W, Ta, and Mo;

Z comprises at least one rare-earth element selected from the group consisting of Y, Sc, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu;

$0<a<0.06$;

$0.0001<b<0.15$;

$0<c\leq 0.06$;

$0<d<0.06$;

$0\leq x\leq 1$;

$0\leq y\leq 1$;

$0.1<u<0.8$;

$0\leq v\leq 0.2$; and

$0.98\leq m\leq 1.027$

149. The method of forming a multilayered ceramic capacitor of claim 147 wherein said first conductive plates and said second conductive plates are separated by a first distance and said first double printed conductive plates are

separated by a second distance wherein said first distance is larger than said second distance.

150. The method of forming a multilayered ceramic capacitor of claim 149 wherein said first distance is at least twice said second distance.

151. The method of forming a multilayered ceramic capacitor of claim 147 wherein at least one of said first conductive plates or said second conductive plates comprise a base metal.

152. The method of forming a multilayered ceramic capacitor of claim 151 wherein said base metal is nickel.

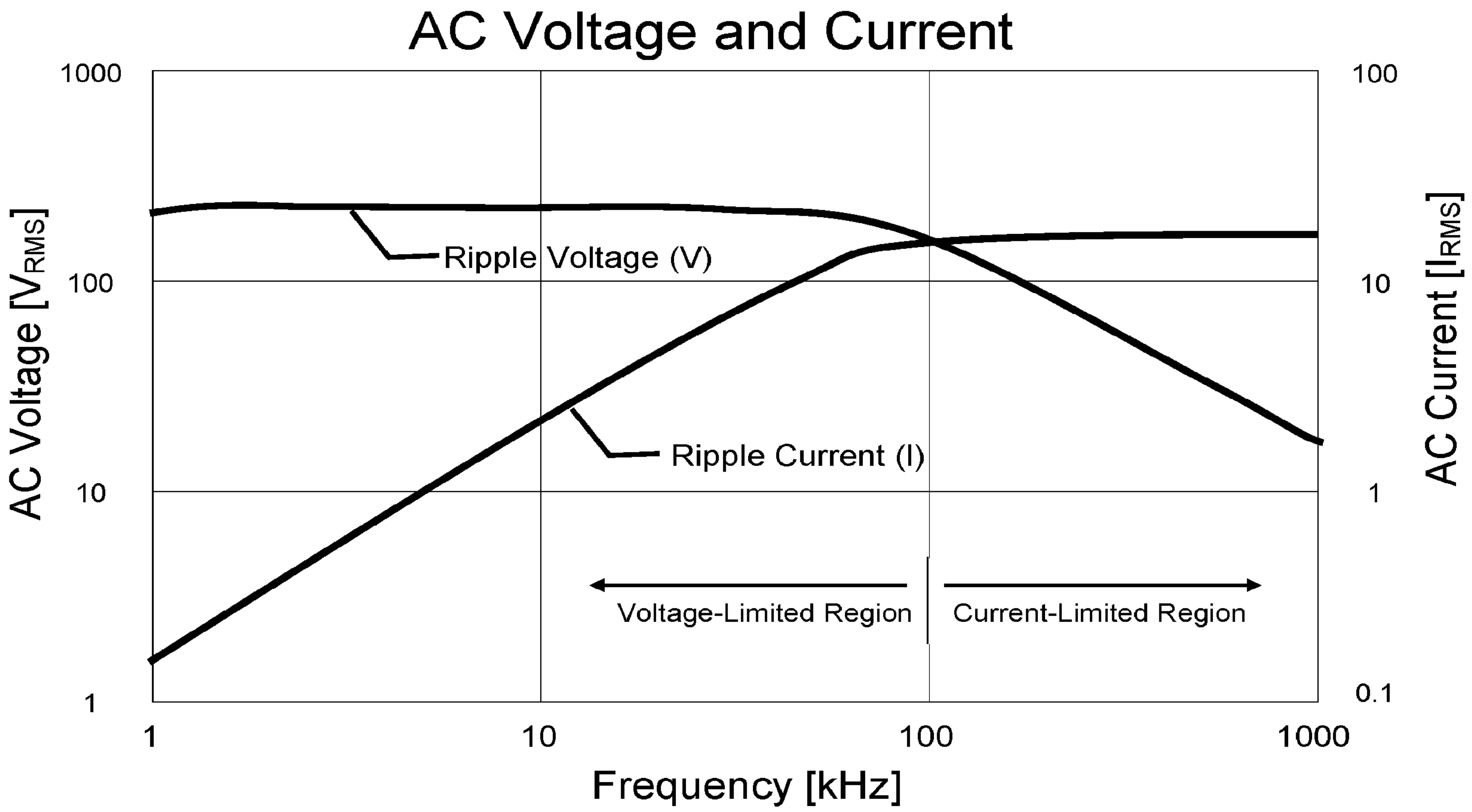
AC Voltage and Current
1000
100
10
1
AC Voltage [V$_{RMS}$]
100
10
1
0.1
AC Current [I$_{RMS}$]
Ripple Voltage (V)
Ripple Current (I)
Voltage-Limited Region
Current-Limited Region
1
10
100
1000
Frequency [kHz]

Fig. 1

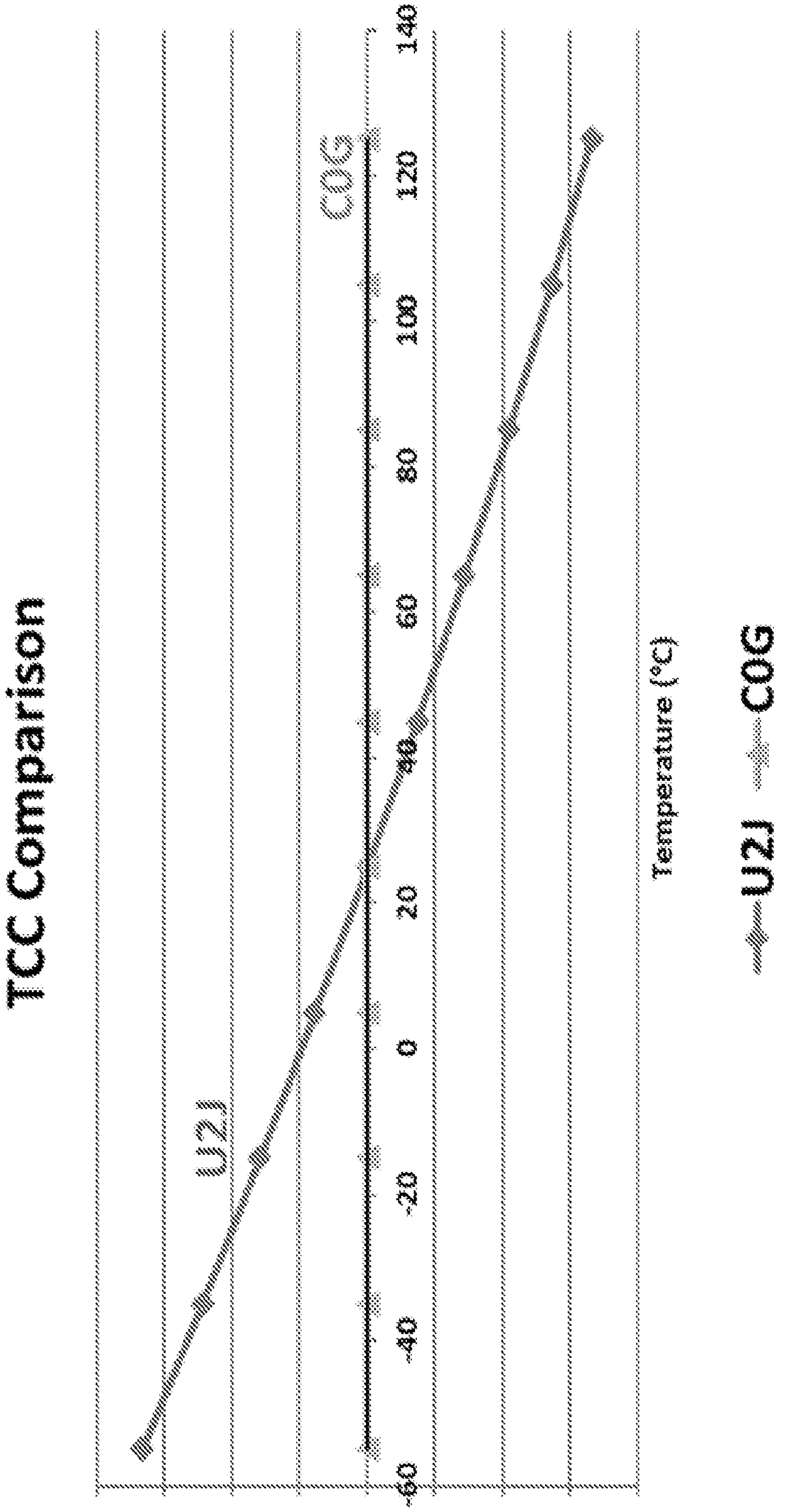
TCC Comparison
Cap Change (%)
8
6
4
2
0
-2
-4
-6
-8
-60
-40
-20
0
20
40
60
80
100
120
140
Temperature (°C)
U2J
C0G
U2J
C0G

Fig. 2

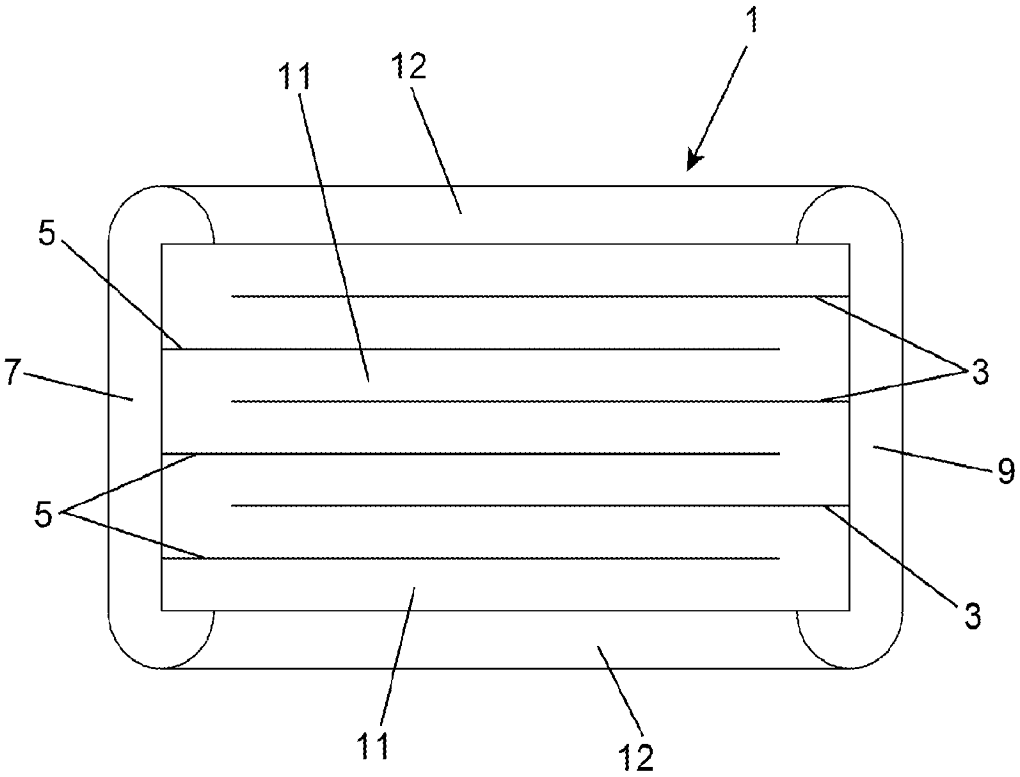

Fig. 3

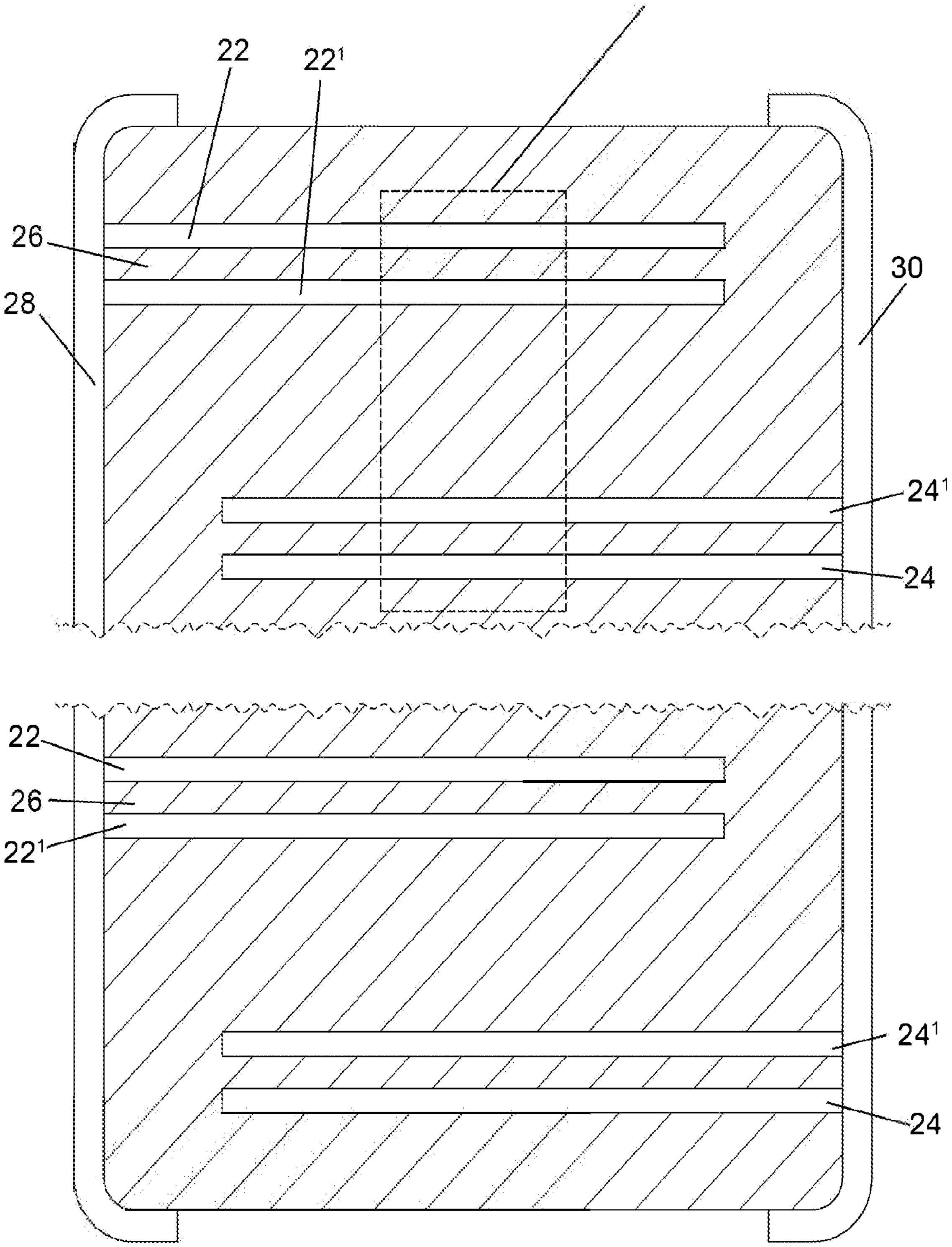

Fig. 4

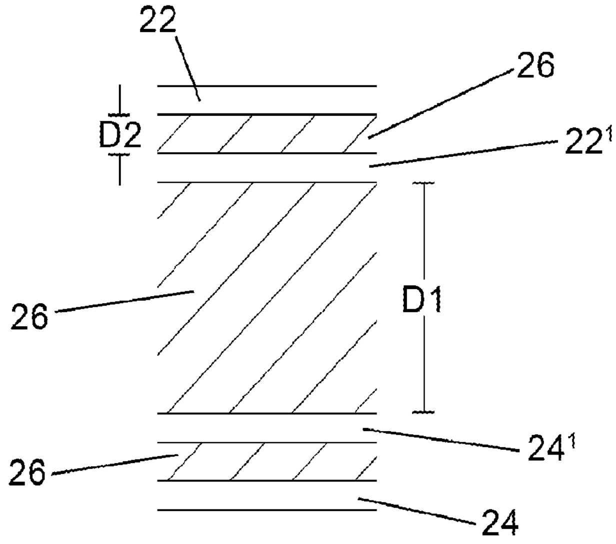

Fig. 5

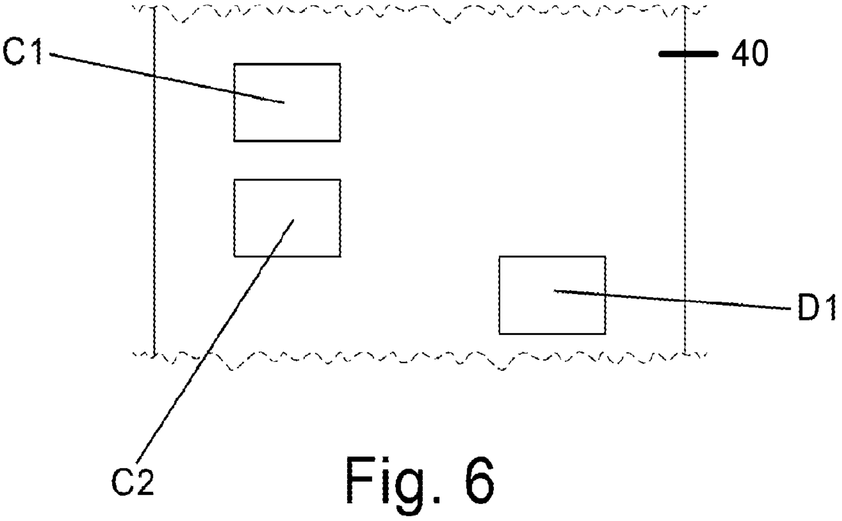

Fig. 6

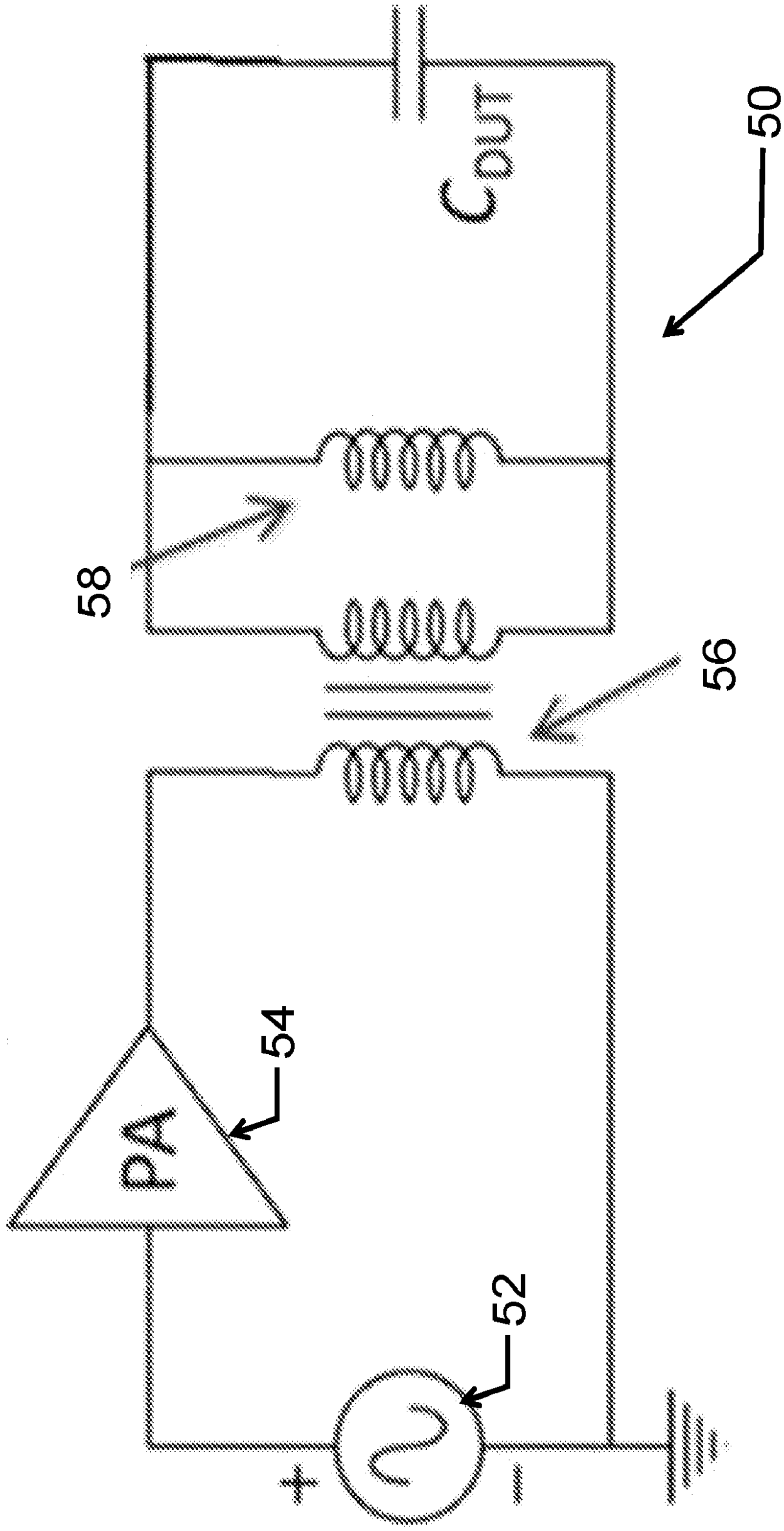

Fig. 7

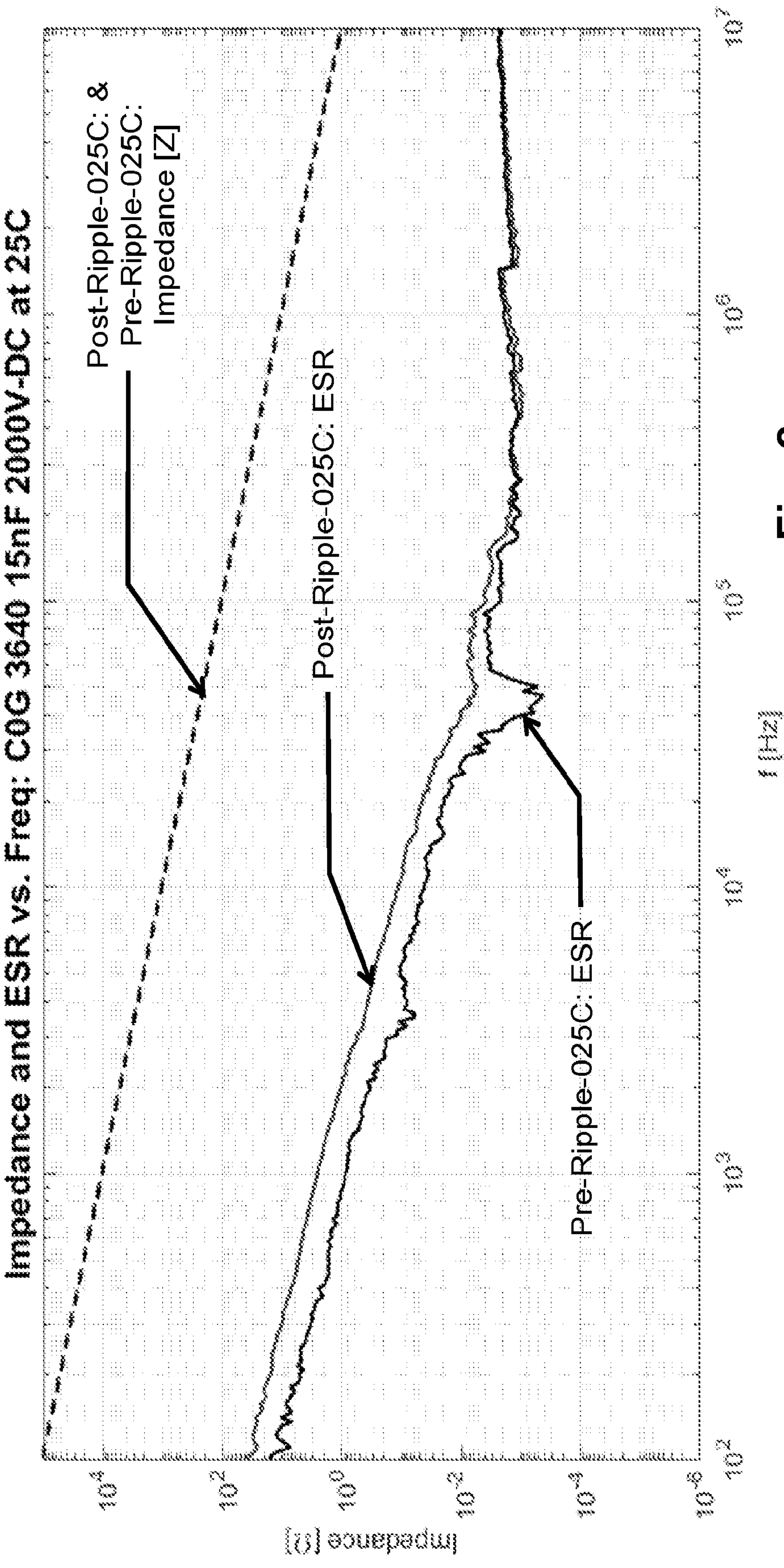
Impedance and ESR vs. Freq: C0G 3640 15nF 2000V-DC at 25C
Post-Ripple-025C: &
Pre-Ripple-025C:
Impedance [Z]
Post-Ripple-025C: ESR
Pre-Ripple-025C: ESR
Impedance [Ω]
10^4
10^2
10^0
10^{-2}
10^{-4}
10^{-6}
10^2
10^3
10^4
10^5
10^6
10^7
f [Hz]

Fig. 8

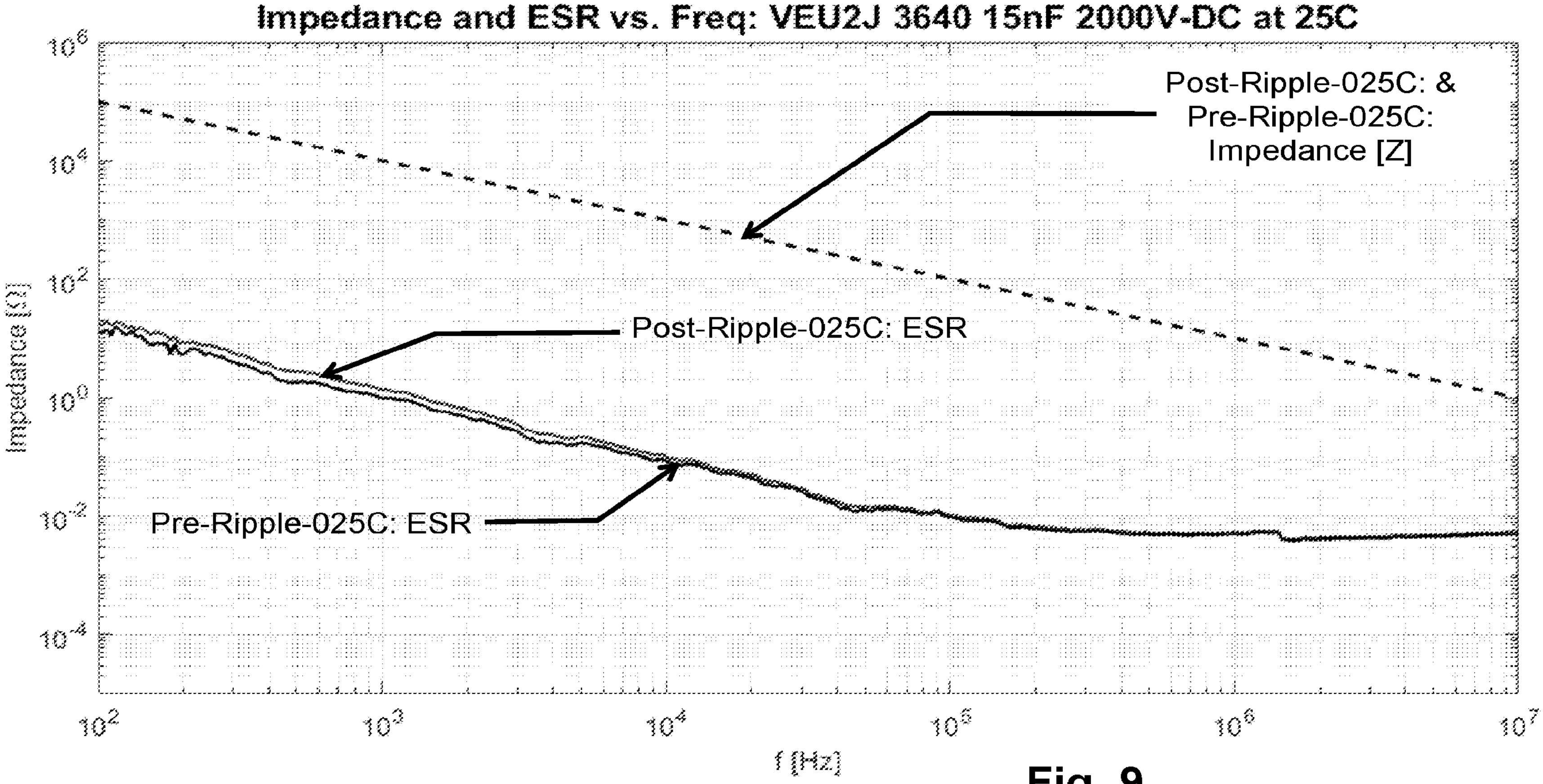
Impedance and ESR vs. Freq: VEU2J 3640 15nF 2000V-DC at 25C
Post-Ripple-025C: &
Pre-Ripple-025C:
Impedance [Z]
Post-Ripple-025C: ESR
Pre-Ripple-025C: ESR
Impedance [Ω]
10^6
10^4
10^2
10^0
10^{-2}
10^{-4}
10^2
10^3
10^4
10^5
10^6
10^7
f [Hz]

Fig. 9

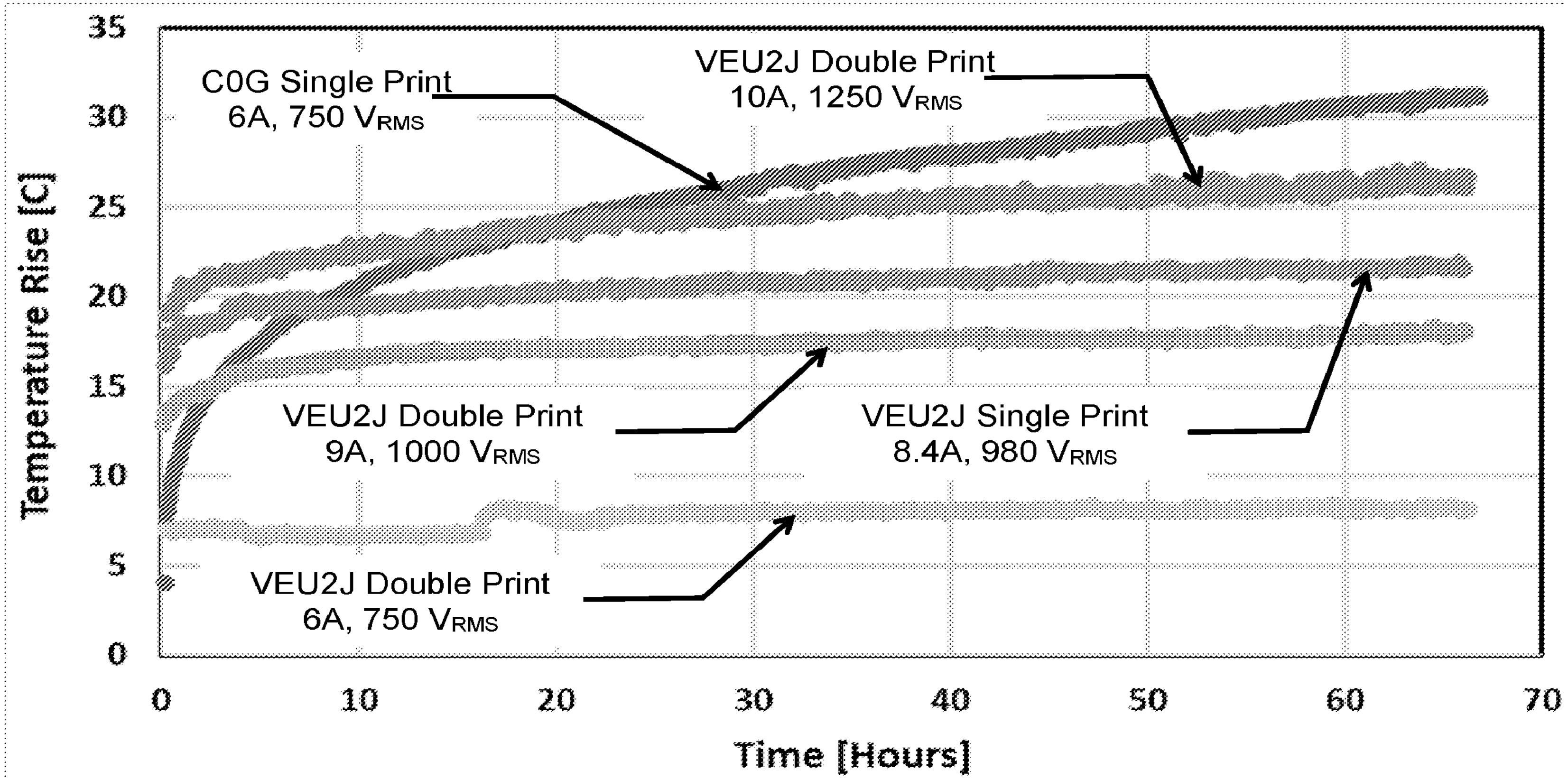
35
30
25
20
15
10
5
0
Temperature Rise [C]
0
10
20
30
40
50
60
70
Time [Hours]
C0G Single Print
6A, 750 V_{RMS}
VEU2J Double Print
10A, 1250 V_{RMS}
VEU2J Double Print
9A, 1000 V_{RMS}
VEU2J Single Print
8.4A, 980 V_{RMS}
VEU2J Double Print
6A, 750 V_{RMS}

Fig. 10

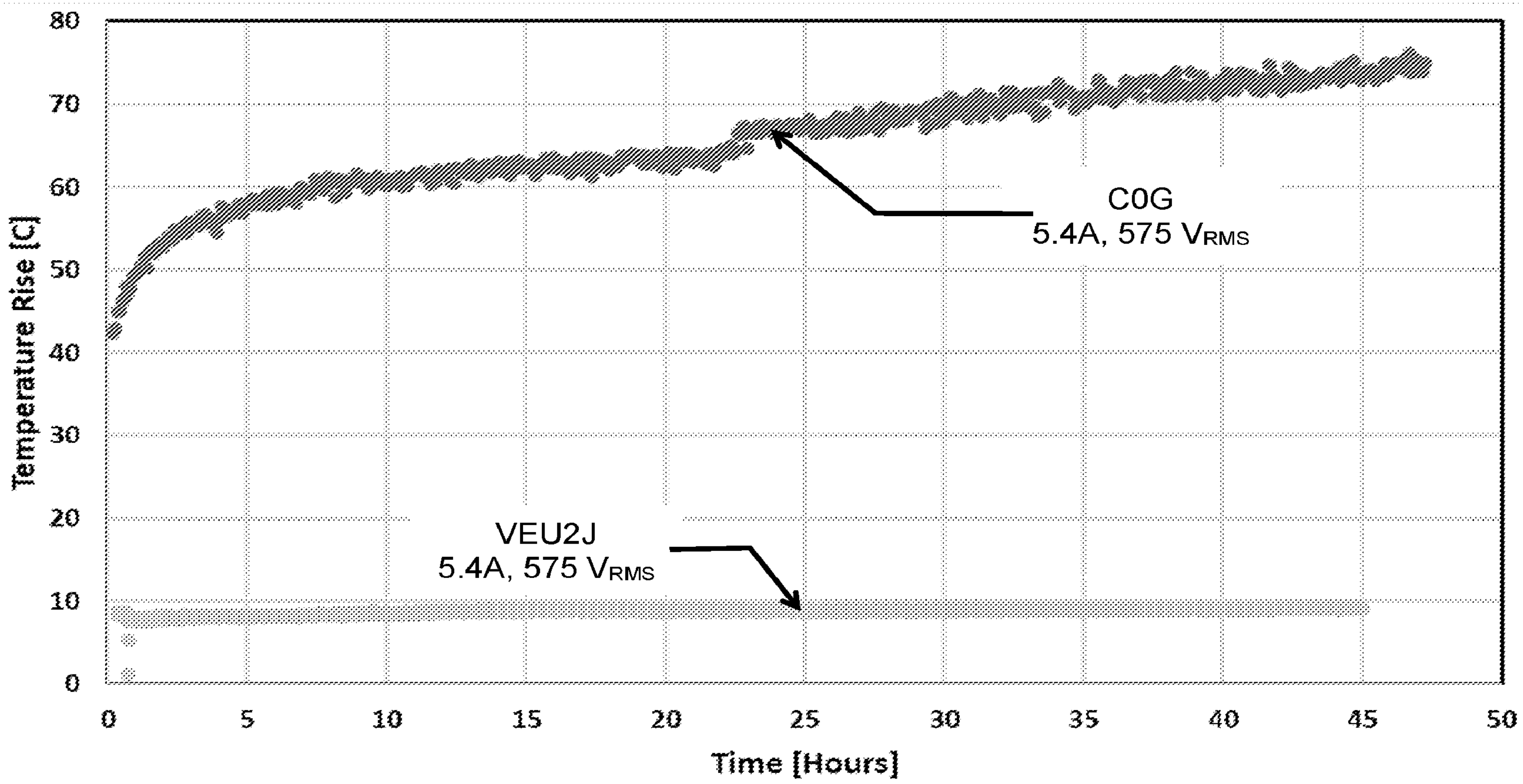
80
70
60
50
40
30
20
10
0
Temperature Rise [C]
0
5
10
15
20
25
30
35
40
45
50
Time [Hours]
C0G
5.4A, 575 V_{RMS}
VEU2J
5.4A, 575 V_{RMS}

Fig. 11

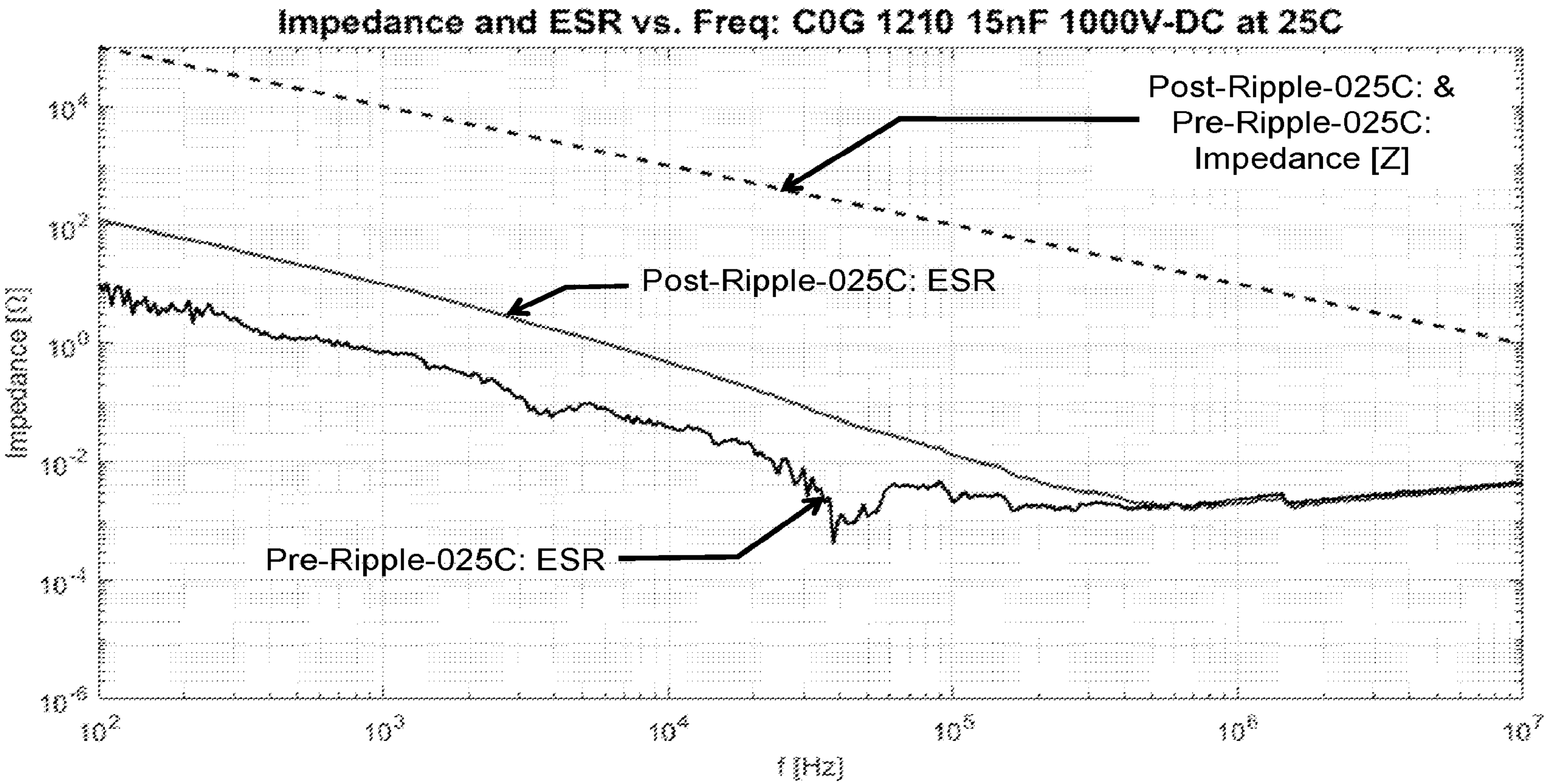
Impedance and ESR vs. Freq: C0G 1210 15nF 1000V-DC at 25C
Post-Ripple-025C: & Pre-Ripple-025C: Impedance [Z]
Post-Ripple-025C: ESR
Pre-Ripple-025C: ESR
Impedance [Ω]
10^4
10^2
10^0
10^{-2}
10^{-4}
10^{-6}
10^2
10^3
10^4
10^5
10^6
10^7
f [Hz]

Fig. 12

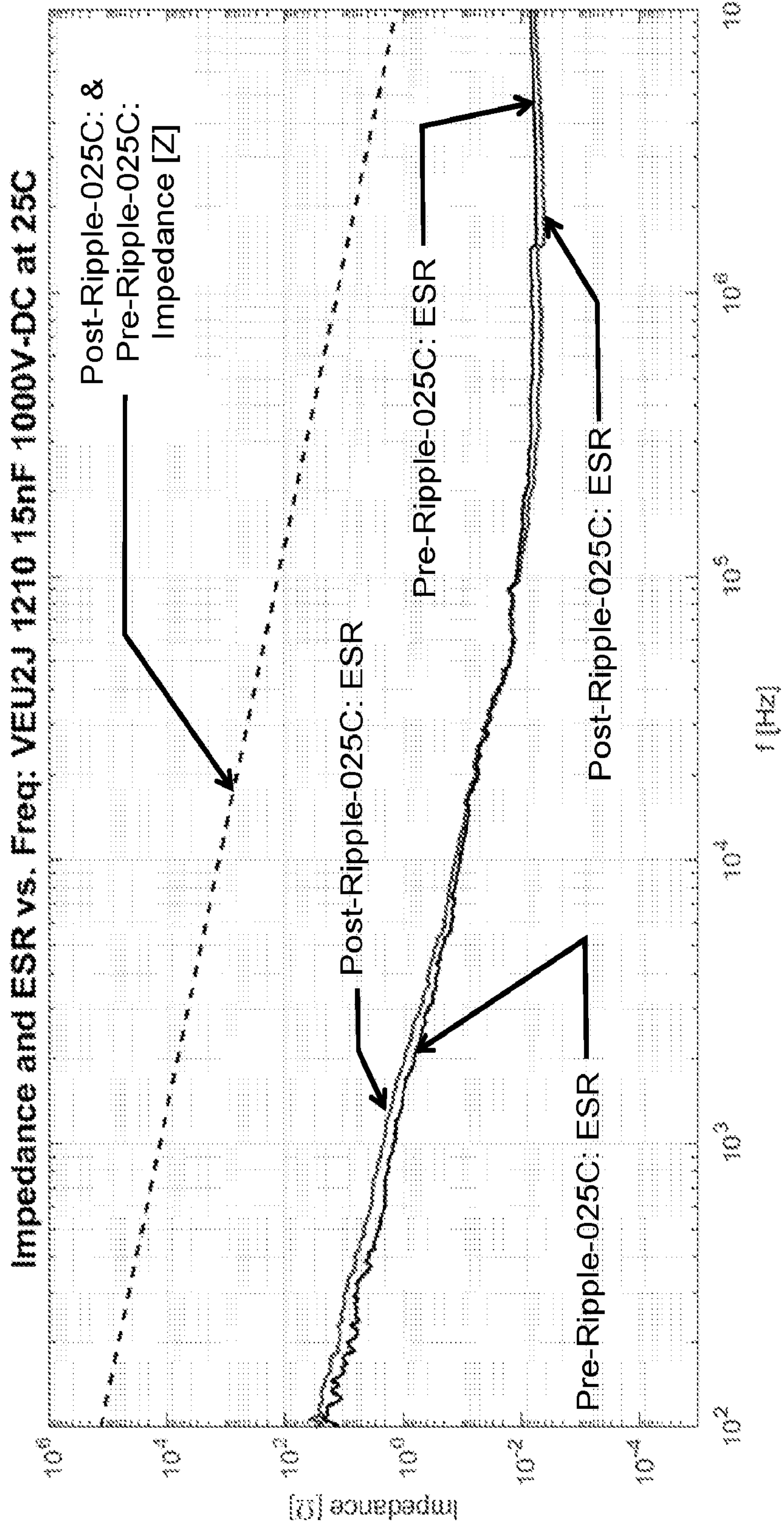
Impedance and ESR vs. Freq: VEU2J 1210 15nF 1000V-DC at 25C
Post-Ripple-025C: & Pre-Ripple-025C: Impedance [Z]
Post-Ripple-025C: ESR
Pre-Ripple-025C: ESR
Pre-Ripple-025C: ESR
Post-Ripple-025C: ESR
Impedance [Ω]
f [Hz]
10^6
10^4
10^2
10^0
10^{-2}
10^{-4}
10^2
10^3
10^4
10^5
10^6
10^7

Fig. 13

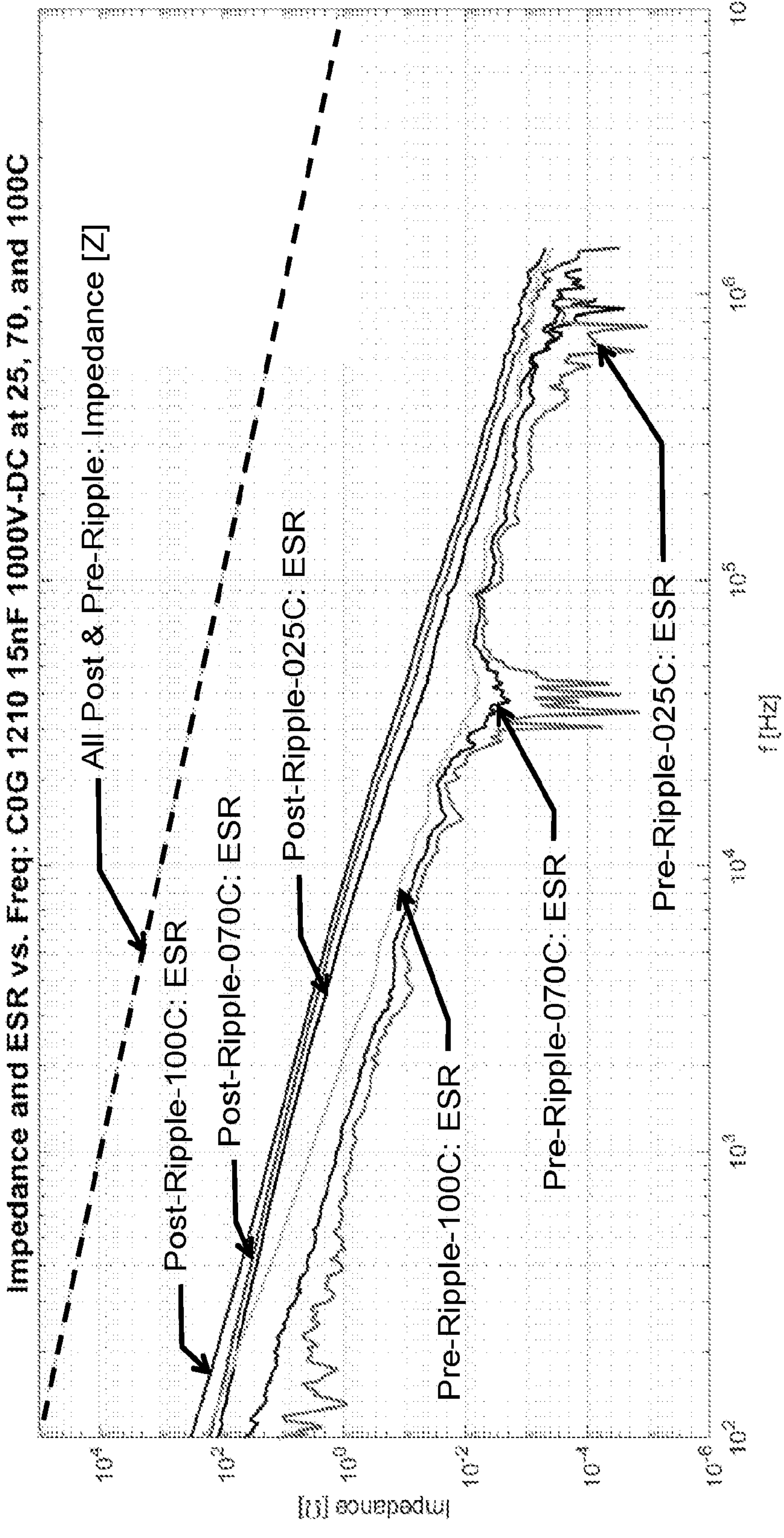
Impedance and ESR vs. Freq: C0G 1210 15nF 1000V-DC at 25, 70, and 100C
All Post & Pre-Ripple: Impedance [Z]
Post-Ripple-100C: ESR
Post-Ripple-070C: ESR
Post-Ripple-025C: ESR
Pre-Ripple-100C: ESR
Pre-Ripple-070C: ESR
Pre-Ripple-025C: ESR
Impedance [Ω]
10^4
10^2
10^0
10^{-2}
10^{-4}
10^{-6}
f [Hz]
10^2
10^3
10^4
10^5
10^6
10^7

Fig. 14

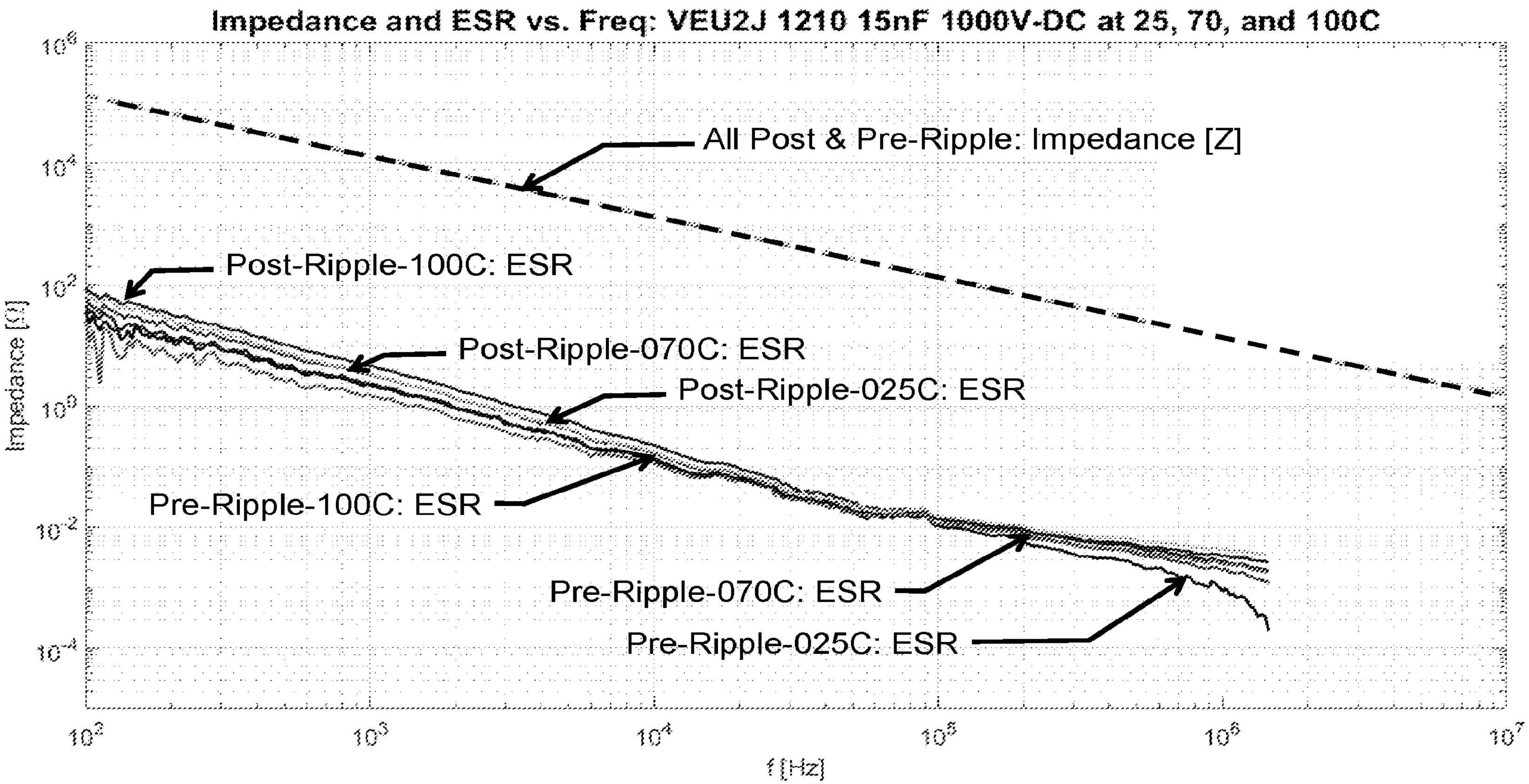
Impedance and ESR vs. Freq: VEU2J 1210 15nF 1000V-DC at 25, 70, and 100C
All Post & Pre-Ripple: Impedance [Z]
Post-Ripple-100C: ESR
Post-Ripple-070C: ESR
Post-Ripple-025C: ESR
Pre-Ripple-100C: ESR
Pre-Ripple-070C: ESR
Pre-Ripple-025C: ESR
Impedance [Ω]
10^6
10^4
10^2
10^0
10^{-2}
10^{-4}
f [Hz]
10^2
10^3
10^4
10^5
10^6
10^7

Fig. 15

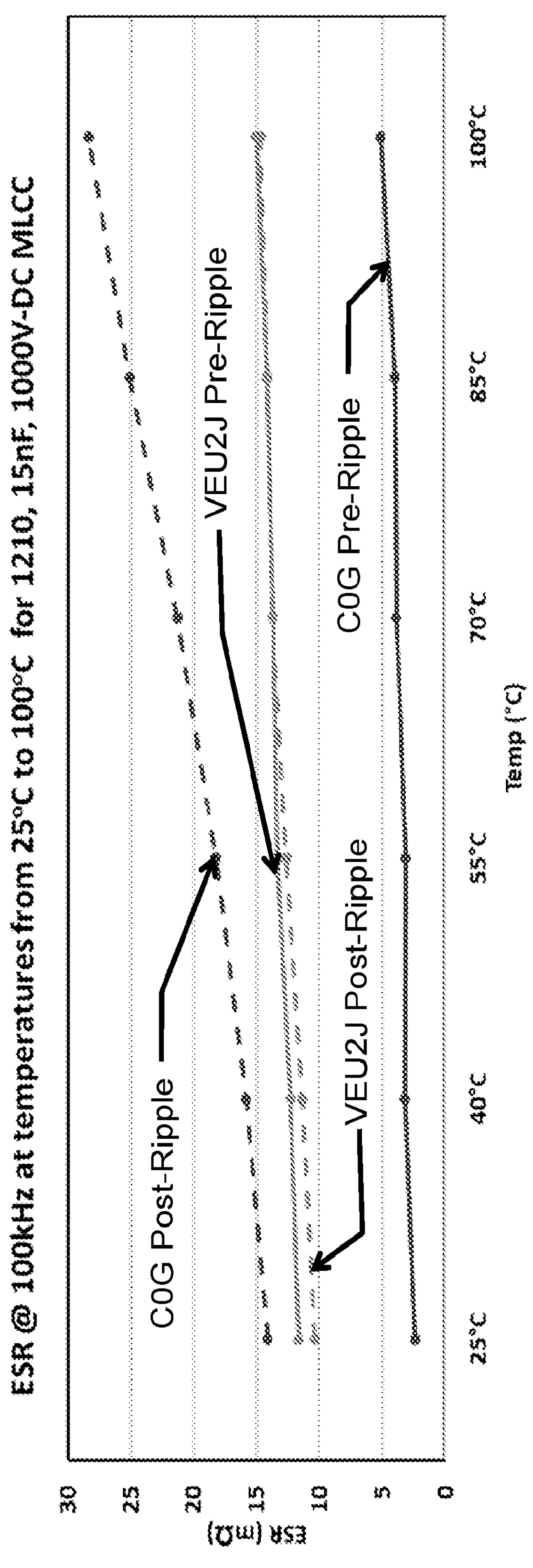
ESR @ 100kHz at temperatures from 25°C to 100°C for 1210, 15nF, 1000V-DC MLCC
ESR (mΩ)
30
25
20
15
10
5
0
25°C
40°C
55°C
70°C
85°C
100°C
Temp (°C)
C0G Post-Ripple
VEU2J Pre-Ripple
C0G Pre-Ripple
VEU2J Post-Ripple

Fig. 16

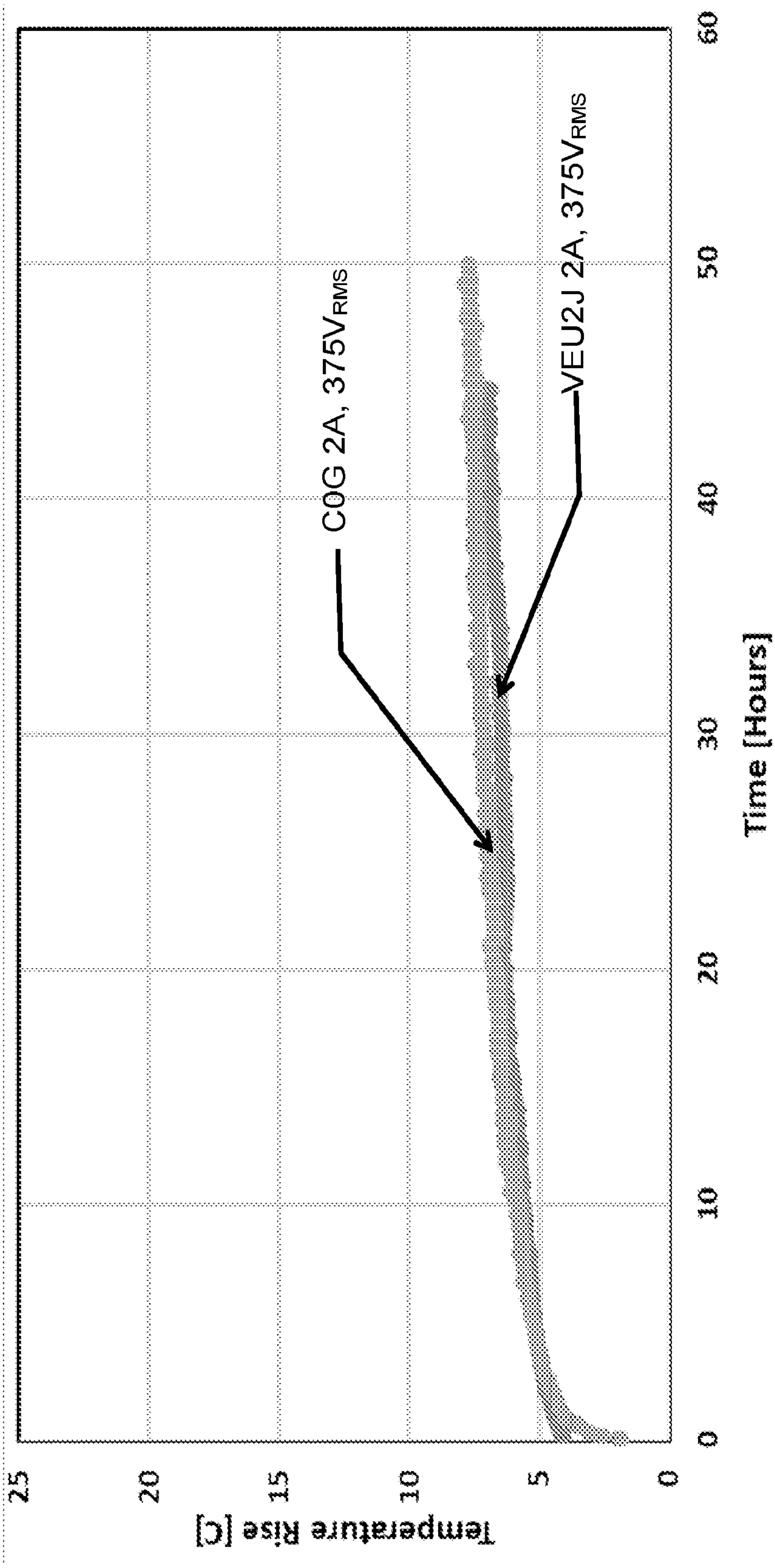
Temperature Rise [C]
0
5
10
15
20
25
Time [Hours]
0
10
20
30
40
50
60
C0G 2A, 375V_{RMS}
VEU2J 2A, 375V_{RMS}

Fig. 17

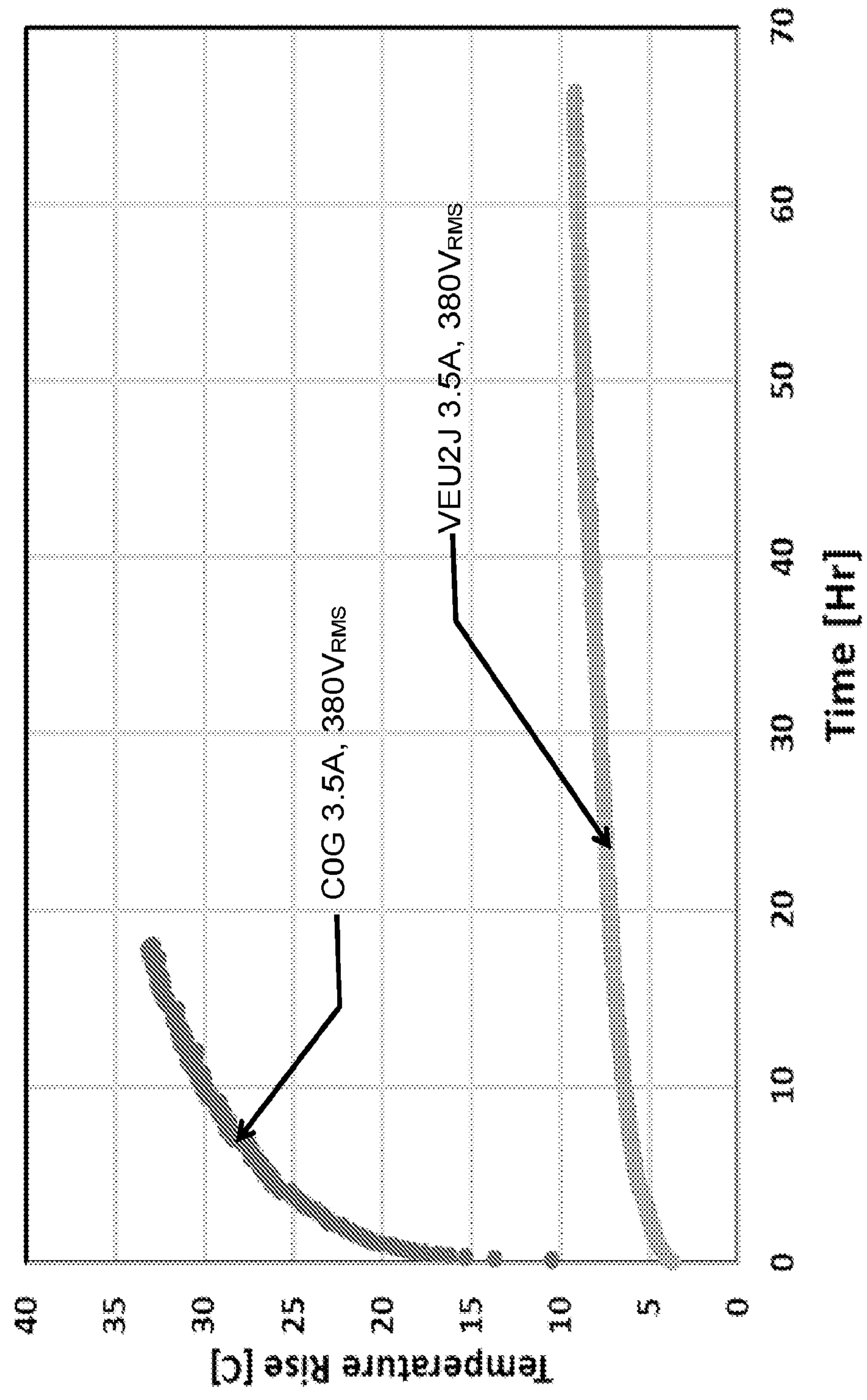
Temperature Rise [C]
0
5
10
15
20
25
30
35
40
Time [Hr]
0
10
20
30
40
50
60
70
C0G 3.5A, 380V_{RMS}
VEU2J 3.5A, 380V_{RMS}

Fig. 18

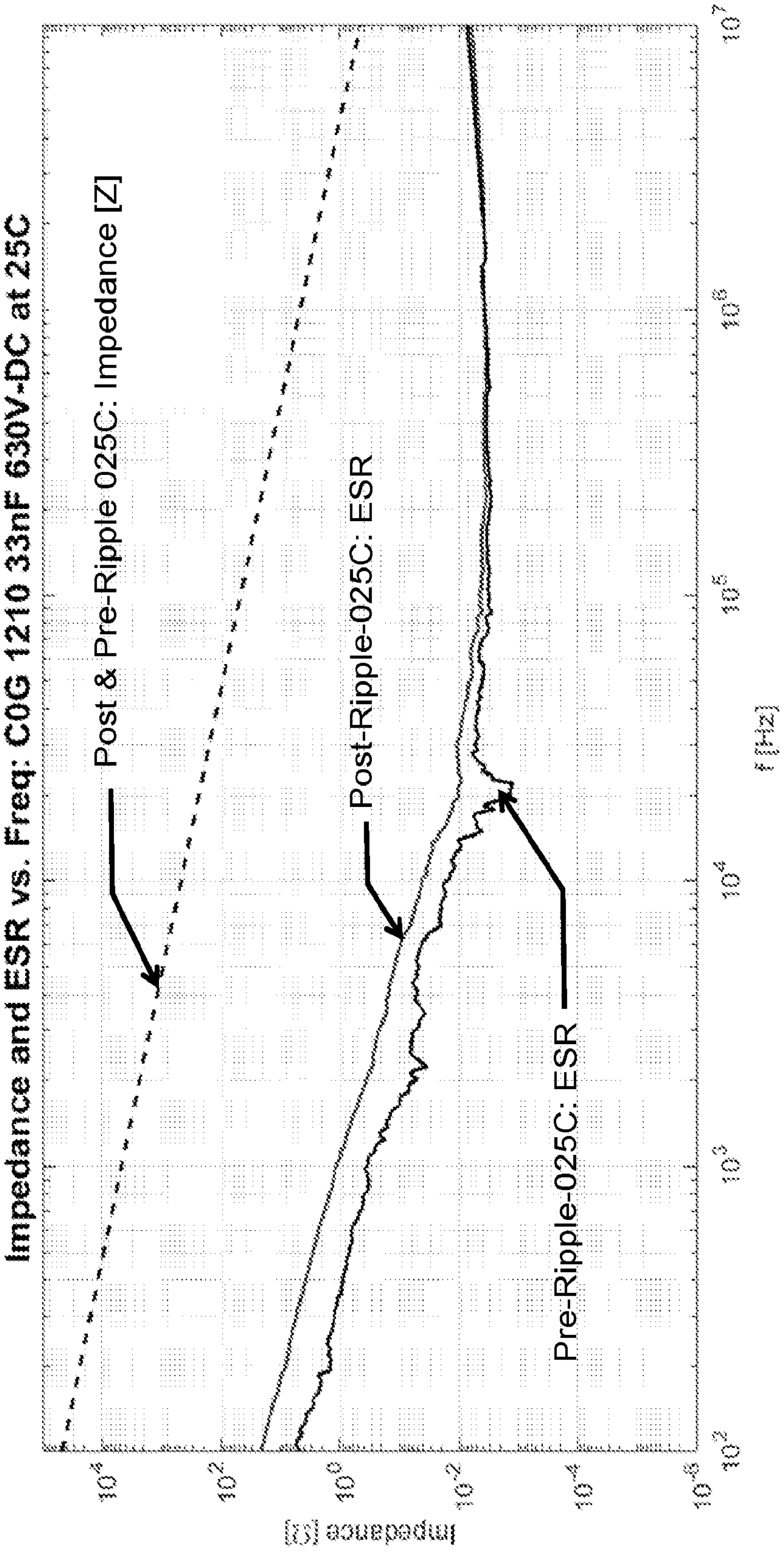
Impedance and ESR vs. Freq: C0G 1210 33nF 630V-DC at 25C
Post & Pre-Ripple 025C: Impedance [Z]
Post-Ripple-025C: ESR
Pre-Ripple-025C: ESR
Impedance [Ω]
10^{4}
10^{2}
10^{0}
10^{-2}
10^{-4}
10^{-6}
f [Hz]
10^{2}
10^{3}
10^{4}
10^{5}
10^{6}
10^{7}

Fig. 19

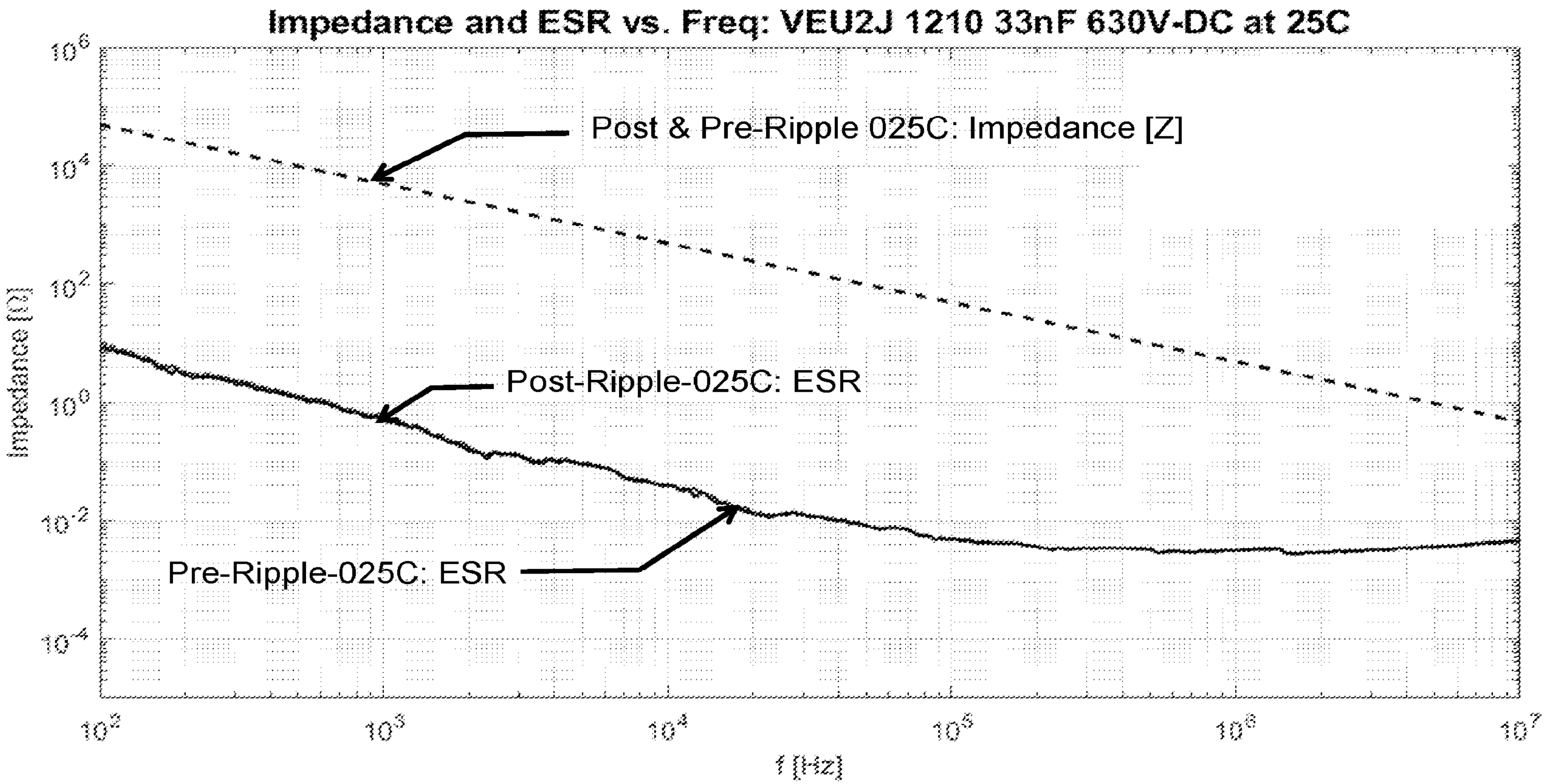
Impedance and ESR vs. Freq: VEU2J 1210 33nF 630V-DC at 25C
Post & Pre-Ripple 025C: Impedance [Z]
Post-Ripple-025C: ESR
Pre-Ripple-025C: ESR
Impedance [Ω]
10^6
10^4
10^2
10^0
10^{-2}
10^{-4}
10^2
10^3
10^4
10^5
10^6
10^7
f [Hz]

Fig. 20

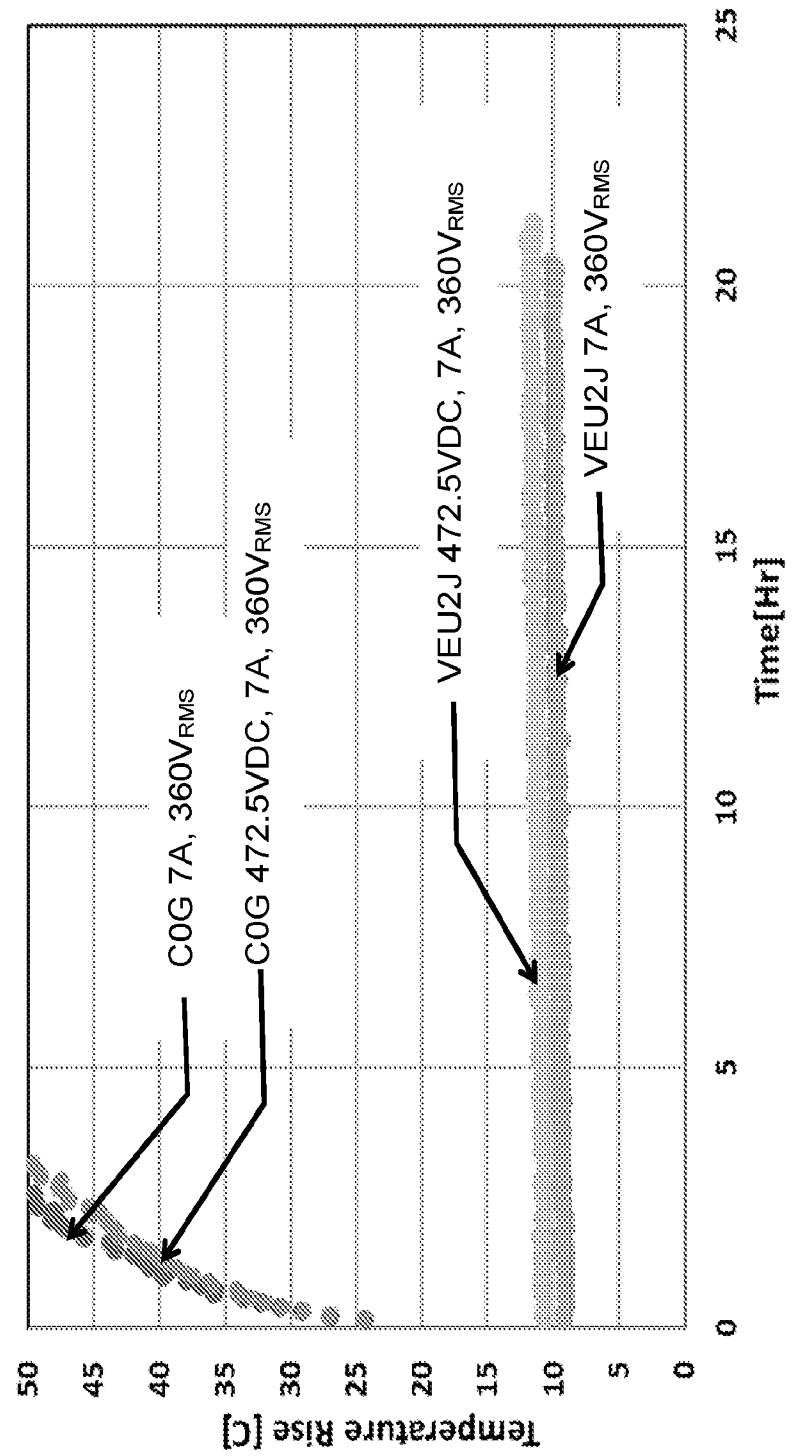
C0G 7A, 360V$_{RMS}$
C0G 472.5VDC, 7A, 360V$_{RMS}$
VEU2J 472.5VDC, 7A, 360V$_{RMS}$
VEU2J 7A, 360V$_{RMS}$
Temperature Rise [C]
50
45
40
35
30
25
20
15
10
5
0
Time[Hr]
0
5
10
15
20
25

Fig. 21

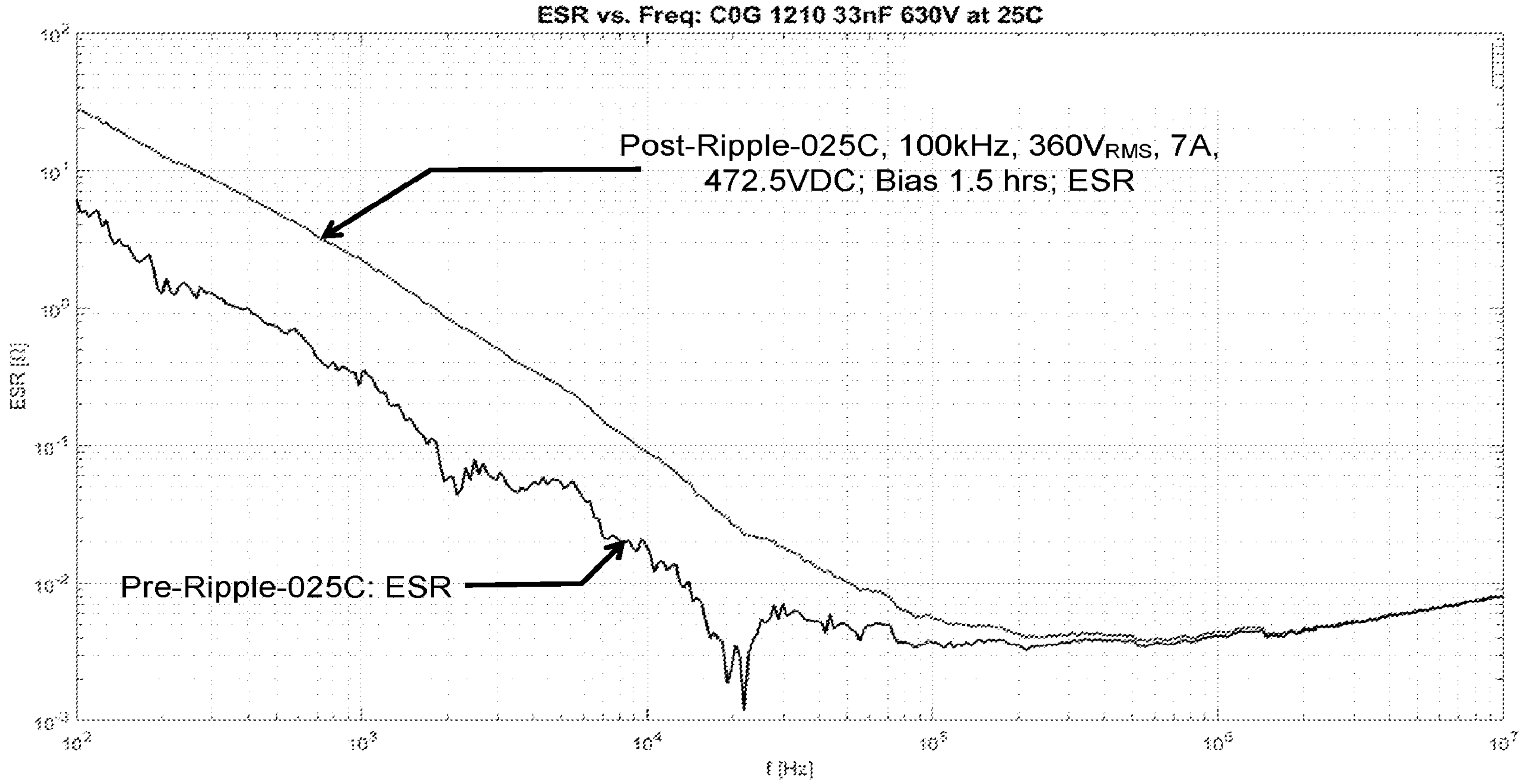
ESR vs. Freq: C0G 1210 33nF 630V at 25C
Post-Ripple-025C, 100kHz, 360V$_{RMS}$, 7A, 472.5VDC; Bias 1.5 hrs; ESR
Pre-Ripple-025C: ESR
ESR [Ω]
f [Hz]
10^{2}
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{2}
10^{3}
10^{4}
10^{5}
10^{6}
10^{7}

Fig. 22

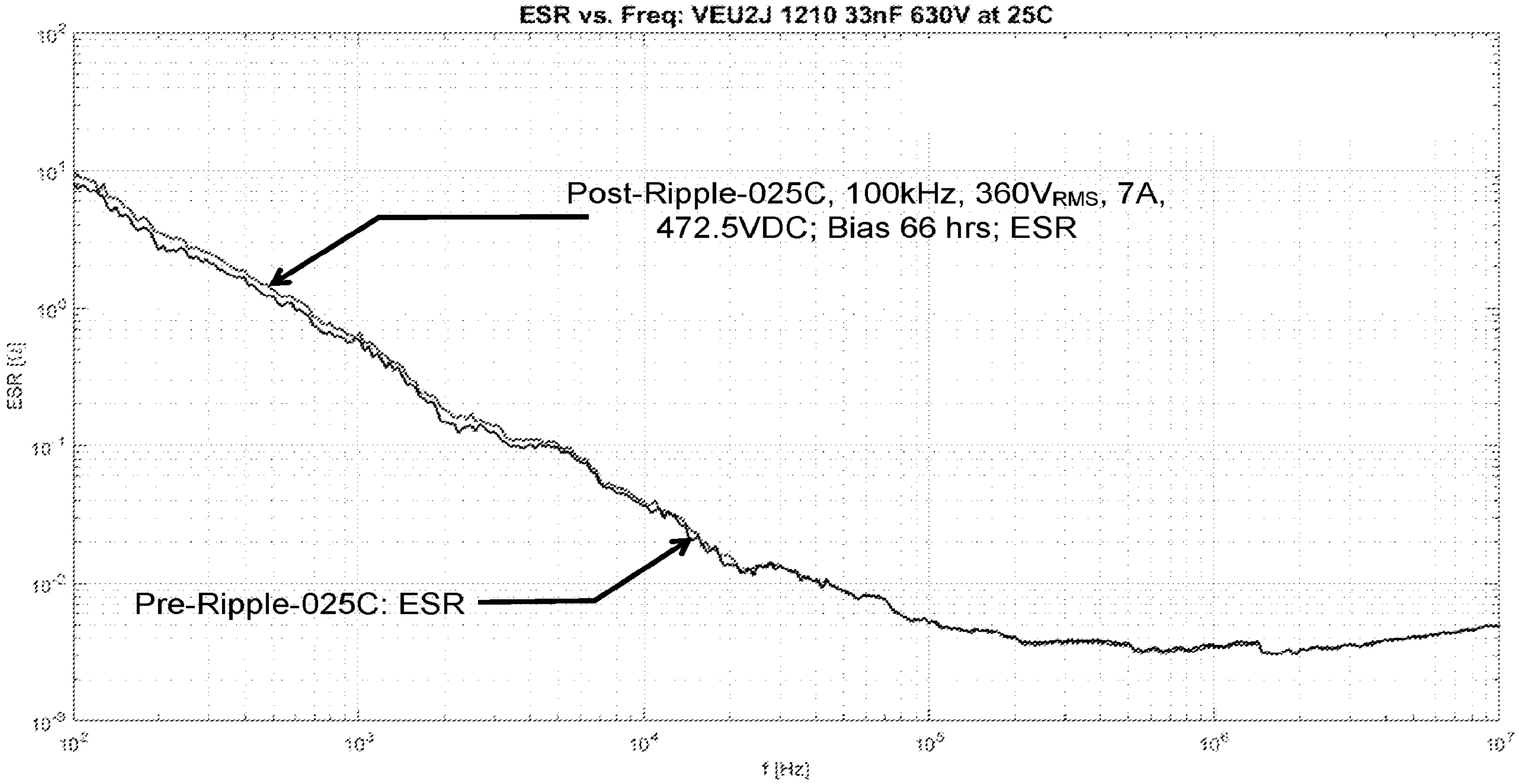
ESR vs. Freq: VEU2J 1210 33nF 630V at 25C
Post-Ripple-025C, 100kHz, 360V$_{RMS}$, 7A, 472.5VDC; Bias 66 hrs; ESR
Pre-Ripple-025C: ESR
ESR [Ω]
10^{2}
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
f [Hz]
10^{2}
10^{3}
10^{4}
10^{5}
10^{6}
10^{7}

Fig. 23

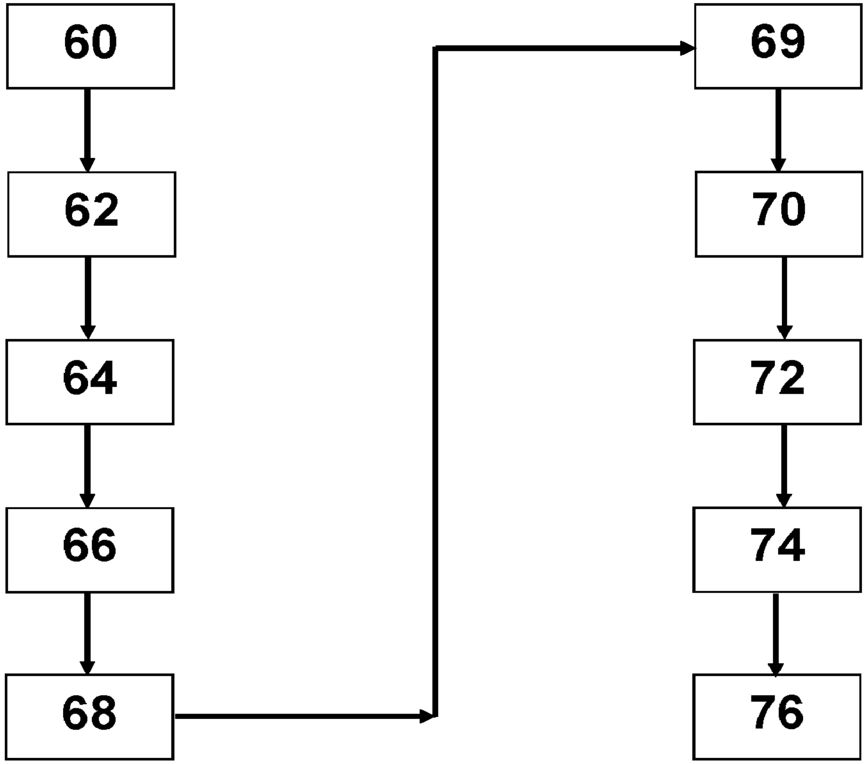

Fig. 24

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US21/49221

A. CLASSIFICATION OF SUBJECT MATTER

IPC - H01G 4/12; H01G 4/38; H01G 4/018; H01G 4/002 (2021.01)

CPC - H01G 4/12; H01G 4/1272; H01G 4/38; H01G 4/018; H01G 4/002

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2015/0070238 A1 (ROCHEMONT, L ET AL.) 12 March 2015; the entire document	1-152
A	US 2008/0107800 A1 (RANDALL, M ET AL.) 08 May 2008; the entire document	1-152
A	US 2002/0000825 A1 (SIRANE, T ET AL.) 03 January 2002; the entire document	1-152
A	US 2009/0207555 A1 (HACKENBERGER, W ET AL.) 20 August 2009; the entire document	1-152

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search 14 January 2022 (14.01.2022)	Date of mailing of the international search report FEB 07 2022
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Shane Thomas Telephone No. PCT Helpdesk: 571-272-4300

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
-***-Please See Supplemental Page-***-

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

-***-Continued From Box No. III: Observations where unity of invention is lacking-***-

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fee must be paid.

Group I: Claims 1-146 are directed towards a multilayer ceramic that has a rated DC voltage and a rated AC Vpp wherein said rated AC Vpp is higher than said rated DC voltage.
Group II: Claims 147-152 are directed towards a method of forming a multilayered ceramic capacitor comparing: forming a paraelectric ceramic dielectric defined by General Formula B as defined in the claim.

The inventions listed as Groups I-II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features.

Group I has at least at least first conductive plates electrically connected to first external terminations and second conductive plates electrically connected to second external terminations wherein said first conductive plates and said second conductive plates form a capacitive couple; the multilayer ceramic capacitor has a rated DC voltage and a rated AC Vpp wherein said rated AC Vpp is higher than said rated DC voltage, that Group II does not have.

Group II has; forming a paraelectric ceramic dielectric defined by General Formula B where the specific chemical composition and formula is given in the claim; forming a coating of said ceramic slip on a substrate; printing a pattern of conductive ink on said coating to form a printed coating; forming a stack comprising said printed coating wherein adjacent printed coatings are offset and alternated printed coatings are registration; forming a laminate of said stack; separating said laminate into green chips; sintering said green chips wherein said conductive ink forms first conductive plates and second conductive plates; and terminating said sintered green chips, that Group I does not have.

The common technical features of Groups I and II are a multilayer ceramic capacitor comprising first conductive plates and second conductive plates; a ceramic portion between said first conductive plates and said second conductive plates wherein said ceramic portion comprises paraelectric ceramic dielectric.

The common technical features are disclosed by US 2015/0070238 A1 to de Rochemont, L. (hereinafter "Rochemont"). Rochemont discloses a multilayer ceramic capacitor comprising first conductive plates and second conductive plates (a sheet capacitor 356 (multilayer) ceramic capacitor includes foil 360A and electroceramic 358A (first conductive plates) and foil 360b and electroceramic 358B (second plates); figures 18-19B; paragraphs [0106-0107]); a ceramic portion between said first conductive plates and said second conductive plates wherein said ceramic portion comprises paraelectric ceramic dielectric (a electroceramic 366 (ceramic portion) between the foil 360A and electroceramic 358A and foil 360b and electroceramic 358B, where the electrocermaic forms a paraelectric microstructure and is a dielectric material; figures 18-19B; paragraphs [0087, 0106-0108]).

Since the common technical feature is previously disclosed by the Rochemont reference, these common features are not special and so Groups I-II lack unity.