(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) **World Intellectual Property Organization**
International Bureau

(43) **International Publication Date**
12 June 2014 (12.06.2014)

(10) **International Publication Number**
WO 2014/088551 A1

(51) **International Patent Classification**:
H02M 7/483 (2007.01)

(21) **International Application Number**:
PCT/US2012/067715

(22) **International Filing Date**:
4 December 2012 (04.12.2012)

(25) **Filing Language**: English

(26) **Publication Language**: English

(71) **Applicant**: **OTIS ELEVATOR COMPANY** [US/US]; Ten Farm Springs Road, Farmington, Connecticut 06032 (US).

(72) **Inventors; and**

(71) **Applicants** *(for US only)*: **KOVACIC, Marinko** [HR/HR]; Horvacanska cesta 43, Zagreb, 10000 Zagrebacka (HR). **KRISHNAMURTHY, Shashank** [IN/US]; 205 Briarwood Court, Rocky Hill, Connecticut 06067 (US).

(74) **Agent**: **FOX, David, A.**; Cantor Colburn LLP, 20 Church Street, 22nd Floor, Hartford, Connecticut 06103 (US).

(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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(54) Title: GATE DRIVE POWER SUPPLY FOR MULTILEVEL CONVERTER

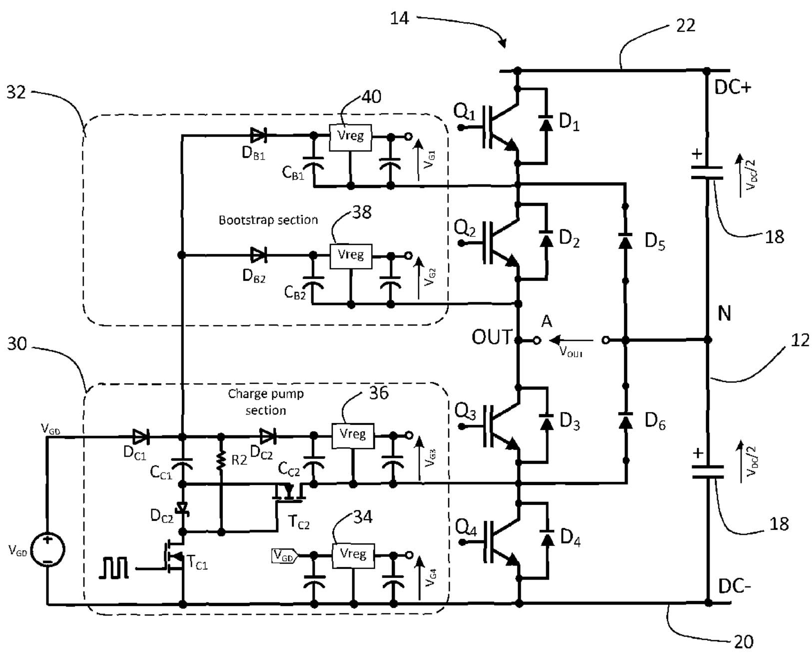

FIG. 2

(57) **Abstract**: A neutral point clamped, multilevel level converter including a DC voltage link having a positive rail and a negative rail; a phase leg coupled to an AC node, the phase leg having a first switch and a second switch in series between the negative rail and the AC node, the phase leg having a third switch and a fourth switch in series between the positive rail and the AC node; and a gate drive power supply having a charge pump section, the charge pump section generating a first gate drive voltage for the first switch and a second gate drive voltage for the second switch.

WO 2014/088551 A1

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *of inventorship (Rule 4.17(iv))*

Published:

- *with international search report (Art. 21(3))*

GATE DRIVE POWER SUPPLY FOR MULTILEVEL CONVERTER

FIELD OF INVENTION

[0001] The subject matter disclosed herein relates generally to the field of power conversion systems, and more particularly, to a gate drive power supply for a multilevel converter.

DESCRIPTION OF RELATED ART

[0002] Neutral point clamped (NPC) multilevel converters are used to convert a DC signal to an AC signal and to convert an AC signal to a DC signal. Three level NPC converters have a high acceptance by the industry, but require a higher number of switches than two level converters. A two level converter employs two switches per phase leg for a total of 6 switches for a 3 phase output. Three level NPC converters employ 4 switches in each phase leg, or twice the number of switches in a two level converter. Due to the increased number of active switches, the number of the gate drive units also has to be increased. Each of the gate drive units has its own floating power supply, such as a transformer isolated power supply for each switch. This approach increases the number of components and can negatively affect the total cost of the converter, particularly in low power applications.

BRIEF SUMMARY

[0003] According to an exemplary embodiment of the invention, a neutral point clamped, multilevel level converter including a DC voltage link having a positive rail and a negative rail; a phase leg coupled to an AC node, the phase leg having a first switch and a second switch in series between the negative rail and the AC node, the phase leg having a third switch and a fourth switch in series between the positive rail and the AC node; and a gate drive power supply having a charge pump section, the charge pump section generating a first gate drive voltage for the first switch and a second gate drive voltage for the second switch.

[0004] Other aspects, features, and techniques of embodiments of the invention will become more apparent from the following description taken in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Referring now to the drawings wherein like elements are numbered alike in the FIGURES:

[0006] FIG. 1 is a schematic diagram of an NPC multilevel converter in an exemplary embodiment;

[0007] FIG. 2 depicts a gate drive power supply in an exemplary embodiment; and

[0008] FIG. 3 depicts an initialization process in exemplary embodiment.

DETAILED DESCRIPTION

[0009] FIG. 1 is a schematic diagram of an NPC three phase, three level converter 10 in an exemplary embodiment. The converter 10 can operate in a generative mode or a regenerative mode. In generative mode, a DC signal from DC link 12 is converted to an AC signal. Two capacitors 18 are connected in series across the DC link 12, with the capacitor junction being referred to as the neutral point (NP). Converter 10 generates a single phase AC signal at each of AC nodes A, B and C. Each leg 14 of the converter 10 generates one of the AC phases. As known in the art, switches Q are controlled by a controller 16 to generate AC waveforms. Each leg 14 includes clamping neutral diodes, D, to clamp the leg output to a neutral point NP. In regenerative mode, an AC signal on one or more of AC nodes A, B and C is converted to a DC signal and supplied to DC link 12. In regenerative mode, switches Q are controlled by controller 16 to generate a DC signal at DC link 12. Switches Q may be transistors as known in the art. Controller 16 may be implemented using a general-purpose microprocessor executing a computer program stored on a storage medium to perform the operations described herein. Alternatively, controller 16 may be implemented in hardware (e.g., ASIC, FPGA) or in a combination of hardware/software.

[0010] FIG. 2 depicts an exemplary gate drive power supply for an NPC three phase, three level converter. Only one leg 14 is depicted in FIG. 2, for ease of illustration. DC link 12 includes a negative rail 20 and a positive rail 22. Capacitors 18 are connected in series between the negative rail 20 and positive rail 22, intersecting at a neutral point, N. Leg 14 includes four switches, Q_1-Q_4, which may be transistors. Switches Q_3-Q_4 are coupled in series from the AC node A to the negative rail 20. Switch Q_4 has a terminal connected to the negative rail 20 and switch Q_3 has a terminal connected to the AC node A. Clamping diode D_6 connects the junction of switches Q_3-Q_4 to the neutral point of the DC link 12. Flyback diodes D_3 and D_4 are positioned across terminals of switches Q_3 and Q_4, respectively.

[0011] Switches Q_1-Q_2 are coupled in series from the positive rail 22 to AC node A. Switch Q_1 has a terminal connected to the positive rail 22 and switch Q_2 has a terminal connected to the AC node A. Clamping diode D_5 connects the junction of switches Q_1-Q_2 to the neutral point of the DC link 12. Flyback diodes D_1 and D_2 are positioned across terminals of switches Q_1 and Q_2, respectively. The possible output states, V_{OUT} , at the AC node A are VDC+ (when switches Q_1 and Q_2 are closed), ZERO (when switches Q_2 and Q_3 are closed) and VDC- (switches Q_3 and Q_4 are closed).

[0012] Also shown in FIG. 2 is a gate drive power supply to provide a gate drive voltage to switches Q_1-Q_4. The gate drive power supply includes two sections, a charge pump section 30 and a bootstrap section 32. The charge pump section 30 provides gate drive voltages to switches Q_4 and Q_3. The bootstrap section 32 provides gate drive voltages to switches Q_1 and Q_2. Each leg 14 has a charge pump section 30 and a bootstrap section 32.

[0013] The charge pump section 30 includes a gate drive voltage source,V_{GD} , which is tied to the negative DC rail 20. The voltage output of gate drive voltage source V_{GD} is substantially larger than the desired voltage on the bootstrap capacitors C_{B1} and C_{B2}, due to the voltage drop on the diodes and active switches in the power supply.

[0014] Charge pump section 30 includes a voltage regulator 34 that receives an output from the gate drive voltage source V_{GD} and converts it to a first gate drive voltage, V_{G4}, for gate drive circuitry of switch Q_4.

[0015] Charge pump section 30 is also used to obtain a second gate drive voltage, V_{G3}, for the gate drive circuitry of switch Q_3. A pulsed gate drive signal is used to turn charge pump transistor T_{C1} on and off. The pulsed gate drive signal can be shared among all of the phase legs 14. In a charging mode, charge pump transistor T_{C1} is turned on and boost capacitor C_{C1} is charged by the gate drive voltage source V_{GD} through diodes D_{C1} and D_{C2}. Transistor T_{C2} and diode D_{C2} remain off since the gate-source voltage at transistor T_{C2} is forced to $-D_{C2}$ during the charging mode.

[0016] When charge pump transistor T_{C1} is turned off, the charge pump section 30 enters a boost mode. The voltage on boost capacitor C_{C1} starts to charge the gate capacitance of transistor T_{C2} through resistor R_2. The voltage at the negative (lower) terminal of boost capacitor C_{C1} rises from ground level to VDC+ as charge pump transistor T_{C1} turns off and the drain-source voltage of transistor T_{C2} decreases.

[0017] Once T_{C2} fully turns on, the power supply enters a pumping mode. Charge in the boost capacitor C_{C1} is transferred to the high-side capacitor C_{C2} that serves as the local supply for the gate of switch Q_3. A voltage regulator 36 receives an output from high-side capacitor C_{C2} and converts it to a second gate drive voltage, V_{G3}, for gate drive circuitry of switch Q_3. The pumping mode ends when charge pump transistor T_{C1} is turned on again by the external control. Continuous switching of charge pump transistor T_{C1} insures that gate drive charge is available at all times to the switch Q_3 without any interference with the desired phase-leg switching sequence. A benefit using charge pump section 30 is that transistors T_{C1} and T_{C2} can be rated to half of the DC link voltage. This is achieved because the voltage swing on transistor Q_4 is limited to the half of the DC link voltage ($V_{DC}/2$).

[0018] Once a stable second gate drive voltage, V_{G3}, is available at the source terminal of the transistor Q_3, gate drive voltages V_{G1} and V_{G2} for the switches Q_1 and Q_2, respectively, can be obtained from the second gate drive voltage V_{G3} using bootstrap section 32. As noted above, the gate drive voltage source, V_{GD}, provides voltage to create gate drive voltages V_{G1} and V_{G2}. Thus, a single power supply is used to generate all the gate drive voltages.

[0019] The bootstrap section 32 receives charge from the boost capacitor C_{C1} and charges bootstrap capacitors C_{B1} and C_{B2} using diodes D_{B1} and D_{B2}, respectively. Bootstrap capacitor C_{B2} is charged through the diode D_{B2} and charge pump transistor T_{C1} when switch Q_3 is closed. A voltage regulator 38 receives an output from bootstrap capacitor C_{B2} and converts it to a third gate drive voltage, V_{G2}, for gate drive circuitry of switch Q_2. Bootstrap capacitor C_{B1} is charged through the diode D_{B1} and charge pump transistor T_{C1} when switches Q_2 and Q_3 are closed. A voltage regulator 40 receives an output from bootstrap capacitor C_{B1} and converts it to a fourth gate drive voltage, V_{G1}, for gate drive circuitry of switch Q_1.

[0020] An initialization sequence is used at the startup of the converter 10 to ensure initial charging of capacitors in the charge pump and bootstrap sections. FIG. 3 depicts an initialization process in exemplary embodiments. The process beings at 100, where switches Q_3 and Q_4 are turned on with switches Q_1 and Q_2 off. This sets the output at AC node A to

VDC- for phase leg 14. The gate drive voltages for switches Q_3 and Q_4 are available from the gate drive voltage source V_{GD} and the charge pump section 30. At 102, bootstrap capacitor C_{B2} is charged through a current path from gate drive voltage source V_{GD} , capacitor C_{B2} and switches Q_3-Q_4.

[0021] At 104, switches Q_2 and Q_3 are turned on with switches Q_1 and Q_4 off. This sets the output at AC node A to zero for phase leg 14. The third gate drive voltage, V_{G2}, for switch Q_2 is available from bootstrap capacitor C_{B2} charged at 102. At 106, bootstrap capacitor C_{B1} is charged through a current path from gate drive voltage source V_{GD}, bootstrap capacitor C_{B1} and switches Q_2-Q_3. Once all the capacitors are charged, the converter can enter operational mode at 108.

[0022] Embodiments of the gate drive power supply provide several benefits. The topology reduces part count and the complexity of the gate drive circuitry. As the part count is smaller, the circuit board area and total weight are reduced. The gate drive power supply provides lower power loss at system stand-by as compared to transformer isolated power supplies. The gate drive power supply provides a reduction of the total price for low power three level units. The gate drive power supply makes three level NPC topology attractive and cost competitive to the standard two level converters, while offering better performance in terms of efficiency and EMI. Due to the usage of lower voltage rating devices, which have lower parasitic capacitances and lower gate charge, the gate drive power supply can be applied to higher power converters than bootstrap gate drive supplies applied to the standard two level converters.

[0023] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. While the description of the present invention has been presented for purposes of illustration and description, it is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications, variations, alterations, substitutions, or equivalent arrangement not hereto described will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. Additionally, while the various embodiments of the invention have been described, it is to be understood that aspects of the invention may include only some of the described embodiments. Accordingly, the invention is not to be seen as being limited by the foregoing description, but is only limited by the scope of the appended claims.

CLAIMS

1. A neutral point clamped, multilevel level converter, comprising:

a DC voltage link having a positive rail and a negative rail;

a phase leg coupled to an AC node, the phase leg having a first switch and a second switch in series between the negative rail and the AC node, the phase leg having a third switch and a fourth switch in series between the positive rail and the AC node; and

a gate drive power supply having a charge pump section, the charge pump section generating a first gate drive voltage for the first switch and a second gate drive voltage for the second switch.

2. The neutral point clamped, multilevel level converter of claim 1, wherein:

the gate drive power supply includes a single gate drive voltage source to supply the first gate drive voltage and the second gate drive voltage.

3. The neutral point clamped, multilevel level converter of claim 2, wherein:

the charge pump section includes a first voltage regulator for generating the first gate drive voltage from the single gate drive voltage source.

4. The neutral point clamped, multilevel level converter of claim 2, wherein:

the charge pump section includes a boost capacitor coupled to the single gate drive voltage source, the boost capacitor transferring voltage to a high-side capacitor to supply the second gate drive voltage.

5. The neutral point clamped, multilevel level converter of claim 4, wherein:

the charge pump section includes a second voltage regulator coupled to the high-side capacitor for generating the second gate drive voltage.

6. The neutral point clamped, multilevel level converter of claim 1, wherein:

the gate drive power supply includes a bootstrap section, the bootstrap section generating a third gate drive voltage for the third switch and a fourth gate drive voltage for the fourth switch.

7. The neutral point clamped, multilevel level converter of claim 6, wherein:

the gate drive power supply includes a single gate drive voltage source to supply the first gate drive voltage, the second gate drive voltage, the third gate drive voltage and the fourth gate drive voltage.

8. The neutral point clamped, multilevel level converter of claim 6, wherein:

the boot strap section includes a first bootstrap capacitor for supplying the third gate drive voltage.

9. The neutral point clamped, multilevel level converter of claim 8, wherein:

the boot strap section includes a third voltage regulator coupled to the first bootstrap capacitor for generating the third gate drive voltage.

10. The neutral point clamped, multilevel level converter of claim 8, wherein:

the boot strap section includes a second bootstrap capacitor for supplying the fourth gate drive voltage.

11. The neutral point clamped, multilevel level converter of claim 10, wherein:

the boot strap section includes a fourth voltage regulator coupled to the second bootstrap capacitor for generating the fourth gate drive voltage.

12. The neutral point clamped, multilevel level converter of claim 10, wherein:

the charge pump section operates an initialization process, the initialization process including closing the first switch and the second switch to charge the first bootstrap capacitor.

13. The neutral point clamped, multilevel level converter of claim 12, wherein:

the initialization process including closing the second switch and the third switch to charge the second bootstrap capacitor.

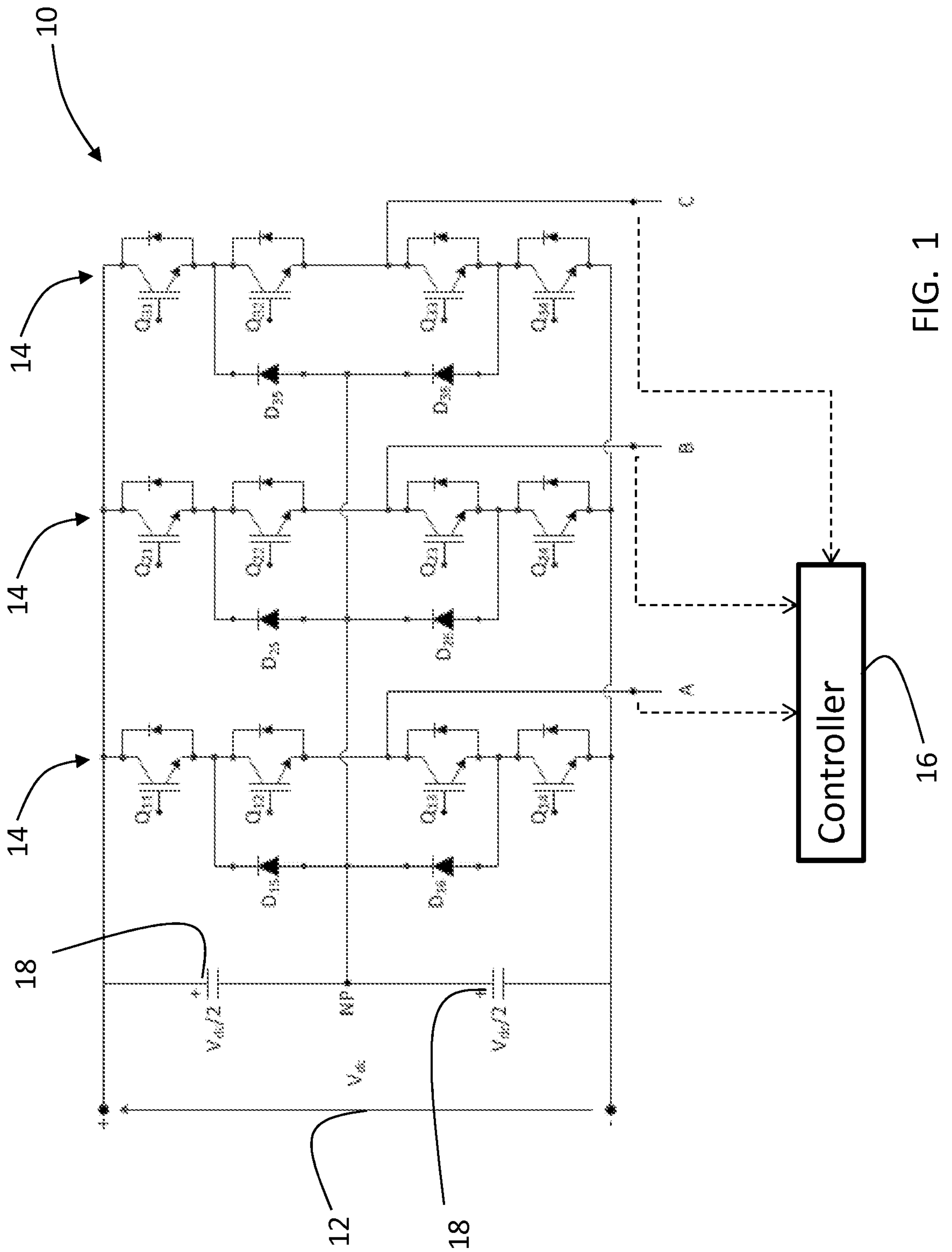
10
14
14
14
Q11
Q12
Q13
Q14
Q21
Q22
Q23
Q24
Q31
Q32
Q33
Q34
D15
D16
D25
D26
D35
D36
A
B
C
Controller
16
18
18
+
Vdc/2
NP
Vdc/2
Vdc
+
-
12

FIG. 1

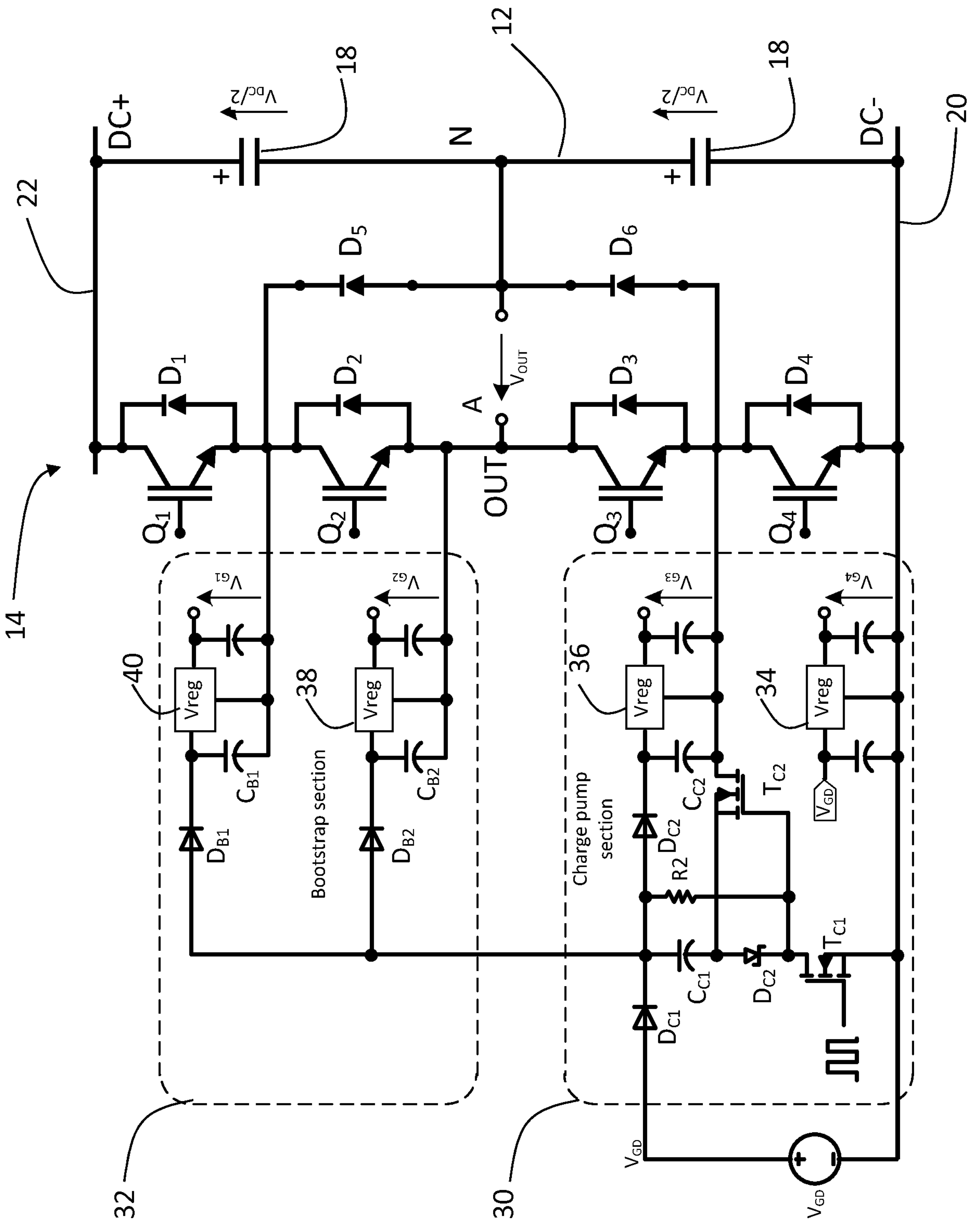
14
22
DC+
18
$V_{DC}/2$
+
12
N
18
$V_{DC}/2$
+
DC-
20
D_5
D_6
D_1
D_2
A
V_{OUT}
D_3
D_4
Q_1
Q_2
OUT
Q_3
Q_4
V_{G1}
V_{G2}
V_{G3}
V_{G4}
40
Vreg
38
Vreg
36
Vreg
34
Vreg
C_{B1}
C_{B2}
D_{B1}
D_{B2}
Bootstrap section
Charge pump section
C_{C2}
T_{C2}
V_{GD}
D_{C2}
R2
C_{C1}
D_{C2}
T_{C1}
D_{C1}
V_{GD}
V_{GD}
32
30

FIG. 2

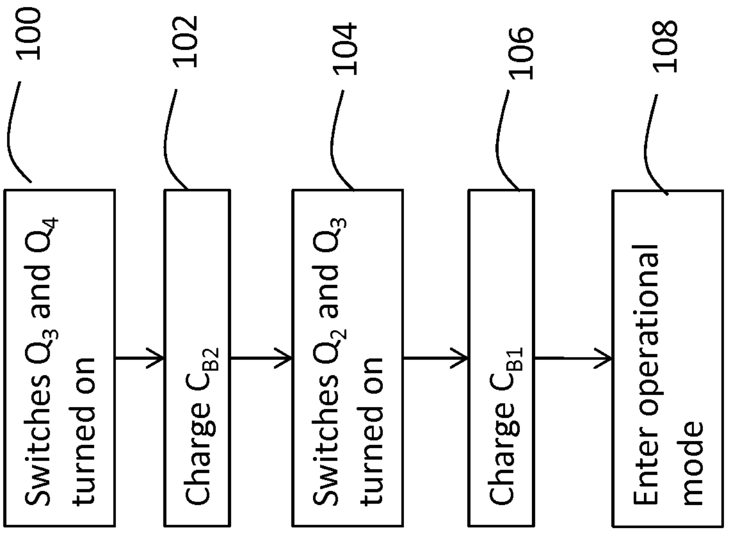
Switches Q_3 and Q_4 turned on
100
Charge C_{B2}
102
Switches Q_2 and Q_3 turned on
104
Charge C_{B1}
106
Enter operational mode
108

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/067715

A. CLASSIFICATION OF SUBJECT MATTER

H02M 7/483(2007.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M 7/483; H02M 7/537; H02M 7/44; H02M 7/48

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: neutral clamp converter, midpoint, charge pump, voltage doubler, voltage tripler, capacitor, switch, inverter

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WELCHKO, BRIAN A. et al. `A Three-Level MOSFET Inverter for Low-Power Drives` In: IEEE Transactions on Industrial Electronics, June 2004, Vol. 51, No. 3, pp. 669-674.	1-13
A	DE 102009002332 A1 (INFINEON TECHNOLOGIES AG) 14 October 2010 See abstract, paragraphs [0025]-[0037] and figures 2-4.	1-13
A	US 2011-0141779 A1 (JOSEPH, ALAN) 16 June 2011 See paragraphs [0018]-[0022], claim 1 and figures 2-5.	1-13
A	US 2012-0257430 A1 (TRUETTNER, DONALD J.) 11 October 2012 See paragraphs [0017]-[0023], [0027]-[0028], claims 1, 4 and figures 1-2, 4-5.	1-13
A	JP 05-015165 A (TOSHIBA CORP.) 22 January 1993 See abstract, paragraphs [0029]-[0045] and figures 1-5.	1-13

☐ Further documents are listed in the continuation of Box C.   ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"P" document published prior to the international filing date but later than the priority date claimed
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search 26 August 2013 (26.08.2013)	Date of mailing of the international search report **27 August 2013 (27.08.2013)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. +82-42-472-7140	Authorized officer PARK Hye Lyun Telephone No. +82-42-481-3463

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2012/067715

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 102009002332 A1	14/10/2010	None	
US 2011-0141779 A1	16/06/2011	None	
US 2012-0257430 A1	11/10/2012	US 8472223 B2	25/06/2013
JP 05-015165 A	22/01/1993	JP 3222489 B2	29/10/2001