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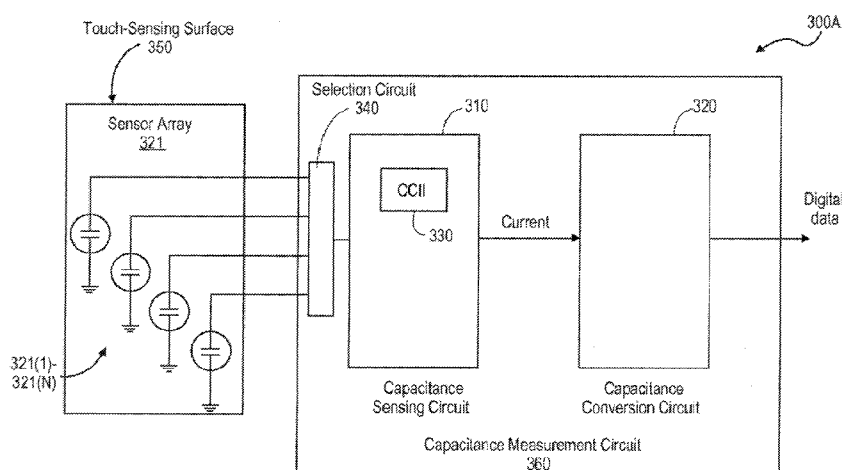


FIG. 3A

(57) Abstract: An apparatus for and a method of sensing capacitance of one or more sensor elements in multiple capacitance sensing modes, including a self-capacitance sensing mode and a mutual capacitance sensing mode.

MULTI-FUNCTIONAL CAPACITANCE SENSING CIRCUIT WITH A CURRENT CONVEYOR

TECHNICAL FIELD

[0001] The present invention relates generally to touch sensors and, more particularly, to capacitive touch sensors.

BACKGROUND

[0002] Capacitive touch sensors may be used to replace mechanical buttons, knobs and other similar mechanical user interface controls. The use of a capacitive sensor allows for the elimination of complicated mechanical switches and buttons, providing reliable operation under harsh conditions. In addition, capacitive sensors are widely used in modern customer applications, providing new user interface options in existing products.

[0003] Capacitive touch sensors can be arranged in the form of a sensor array for a touch-sensing surface. When a conductive object, such as a finger, comes in contact or close proximity with the touch-sensing surface, the capacitance of one or more capacitive touch sensors changes. The capacitance changes of the capacitive touch sensors can be measured by an electrical circuit. The electrical circuit, supporting one operation mode, converts the measured capacitances of the capacitive touch sensors into digital values.

[0004] There are two main operational modes in the capacitance sensing circuits: self-capacitance sensing and mutual capacitance sensing. The self-capacitance sensing mode is also called single-electrode sensing mode, as each sensor needs only one connection wire to the sensing circuit. For the self-capacitance sensing mode, touching

the sensor increases the sensor capacitance as added by the finger touch capacitance is added to the sensor capacitance.

[0005] The mutual capacitance change is detected in the mutual capacitance sensing mode. Each sensor uses at least two electrodes; one is a transmitter and the other is a receiver. When a finger touches a sensor or is in close proximity to the sensor, the capacitive coupling between the receiver and the transmitter of the sensor is decreased as the finger shunts part of the electric field to ground.

[0006] The capacitance sensing circuits used for the mutual capacitance sensing may have current or voltage inputs. The current input capacitance sensing circuits have low input impedance and provide best external noise suppression abilities. The voltage input capacitance sensing circuits have high input impedance and operate on the capacitive divider operation principle. The voltage input capacitance sensing circuits are suitable for sensing capacitance via high-resistance materials. However, the drawback is poor noise immunity, as potential input circuits may be too sensitive to environmental noise.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The present disclosure is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0008] Figure 1A illustrates a capacitance sensing circuit for sensing capacitance of C_s in a self-capacitance sensing mode using the charge accumulation operation sensing technique.

[0009] Figure 1B illustrates a capacitance-sensing circuit for sensing capacitance of C_s in a self-capacitance sensing mode using a sigma-delta modulator sensing technique.

[0010] Figure 2 illustrates a capacitance-sensing circuit for sensing mutual capacitance in a mutual capacitance sensing mode.

[0011] Figure 3A illustrates a block diagram of one embodiment of an electrical circuit having a capacitance measurement circuit for sensing capacitances on a touch-sensing surface using multiple sensor elements of a sensor array in a self-capacitance sensing mode.

[0012] Figure 3B illustrates a block diagram of another embodiment of an electrical circuit having a mutual capacitance measurement circuit for sensing capacitance on a touch-sensing surface using multiple sensor elements of a sensor array in a mutual capacitance sensing mode.

[0013] Figure 4A illustrates a capacitance sensing circuit for measuring capacitance of sensor elements in either a self-capacitance sensing mode or a mutual capacitance sensing mode, according to one embodiment.

[0014] Figures 4B-C illustrate the operation waveforms of the capacitance sensing circuit of Figure 4A for measuring capacitance of sensor elements in a self-capacitance sensing mode and a mutual capacitance sensing mode, respectively, according to embodiments.

[0015] Figure 5A illustrates an equivalent schematic of a second generation current conveyor (CCII), according to one embodiment.

[0016] Figure 5B illustrates a CMOS implementation of a second generation current conveyor, according to one embodiment.

[0017] Figure 6 illustrates the functional elements of capacitance sensing circuit of Figure 4A for measuring capacitance of sensor elements in the mutual capacitance sensing mode, according to one embodiment.

[0018] Figure 7 illustrates the functional elements of capacitance sensing circuit of Figure 4A for measuring capacitance of sensor elements in a single-ended, self-capacitance sensing mode, according to one embodiment.

[0019] Figure 8A illustrates a capacitance sensing circuit configurable for sensing either self-capacitance or mutual capacitance of sensor elements in dual-channel or single differential channel sensing modes, according to one embodiment.

[0020] Figure 8B illustrates a circuit configuration when the capacitance sensing circuit shown in Figure 8A operates in a dual channel voltage-based mutual capacitance sensing mode.

[0021] Figure 8C illustrates a circuit configuration when the capacitance sensing circuit shown in Figure 8A operates in a differential voltage-based mutual capacitance sensing mode.

[0022] Figure 8D illustrates a circuit configuration when the capacitance sensing circuit shown in Figure 8A operates in a dual-channel current-based mutual capacitance sensing mode.

[0023] Figure 8E illustrates a circuit configuration when the capacitance sensing circuit shown in Figure 8A operates in a differential channel single-ended self-capacitance sensing mode.

DETAILED DESCRIPTION

[0024] The following description sets forth numerous specific details such as examples of specific systems, components, methods, and so forth, in order to provide a good understanding of several embodiments of the present invention. It will be apparent to one skilled in the art, however, that at least some embodiments of the present invention may be practiced without these specific details. In other instances, well-known components or methods are not described in detail or are presented in a simple block diagram format in order to avoid unnecessarily obscuring the present invention. Thus, the specific details set forth are merely exemplary. Particular implementations may vary from these exemplary details and still be contemplated to be within the spirit and scope of the present invention.

[0025] References in the description to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase “in one embodiment” in various places in the specification do not necessarily all refer to the same embodiment.

[0026] Described herein are apparatuses and methods for sensing capacitance of one or more sensor elements in multiple capacitance sensing modes. In one embodiment, the multiple capacitance sensing modes include a self-capacitance sensing mode, and a mutual capacitance sensing mode. In one embodiment, the self-capacitance sensing mode is a single-electrode, single-ended sensing mode, and the mutual capacitance sensing mode is a dual-electrode, sensing mode. In another embodiment, the self-capacitance sensing mode is a dual-channel or a differential channel single-ended sensing mode, and

the mutual capacitance sensing mode is a dual-channel or a differential channel sensing mode. In one embodiment, a capacitance sensing circuit can sense capacitance in the multiple modes using a single current conveyor, for example, in the self-capacitance and mutual capacitance single-ended sensing modes. In another embodiment, the capacitance sensing circuit may include two current conveyors for sensing capacitance in either a dual-channel or a differential single-ended self-capacitance sensing mode, or in either a dual-channel or a differential channel mutual capacitance sensing mode. In yet another embodiment, the capacitance sensing circuit, when operating in either a dual-channel or a differential channel mutual capacitance sensing mode, supports voltage or current inputs.

[0027] There are various circuit implementations that may be used for sensing capacitance on sensor elements. Figure 1A illustrates a capacitance sensing circuit 100A for sensing capacitance of C_S 110 in a self-capacitance sensing mode. The capacitance sensing circuit 100A uses a charge accumulation or charge transfer sensing scheme to measure the self-capacitance of the capacitor C_S 110. The charge accumulation sensing scheme operates as follows: after resetting (i.e., discharging) the integration capacitor C_{INT} 120, the switches SW1 and SW2 operate in two non-overlapping phases PH1 and PH2, which are repeated in cycles. During phase PH1, i.e., when the clock signal to the capacitance sensing circuit 100A is high, the switch SW1 is on and the switch SW2 is off. During phase PH2, i.e., when the clock signal to the capacitance sensing circuit 100A is low, the switch SW2 is on and the switch SW1 is off. The switches SW1 and SW2 are not on at the same time. Thus, the sensing capacitor C_S 110 is charged to the supply voltage V_{DD} during phase PH1 and is discharged to the integration capacitor C_{INT} 120 during phase PH2. The self-capacitance sensed on C_S 110 may be determined by the

number of switching cycles used to get the integration capacitor C_{INT} 120 to a certain threshold value or by measuring the voltage on the integration capacitor C_{INT} 120 after executing predefined number of cycles.

[0028] With such a charge accumulation technique, the voltage on the integration capacitor C_{INT} 120 rises exponentially with respect to time (which can be measured by the cycle count). The relationship between the voltage on the integration capacitor C_{INT} 120 and the cycle count can be linearized for measurement methods where capacitance is calculated as a function of the voltage present on the integration capacitor after a predefined number of cycles.

[0029] The charge accumulation technique either converts the sensed capacitance to the time interval or voltage. Another self-capacitance sensing circuit, shown in Figure 1B, uses the sigma-delta modulator to convert the sensed capacitance to the bit stream density.

[0030] There are several possible implementations of how the sigma-delta modulation technique may be used for the capacitance sensing, a couple of possible examples are described in U.S. Patent Publication No. 2008/0111714, filed Nov. 14, 2006, and commonly assigned to the assignee of the present application.

[0031] Figure 1B illustrates a capacitance-sensing circuit 100B for sensing the capacitance of C_S 111 in a self-capacitance sensing mode using the sigma-delta modulator sensing technique. In Figure 1B, the switches SW1 and SW2 operate in two non-overlapping phases, PH1 and PH2, via the switches source 170. At phase PH1 (when clock signal is high), SW1 is on. At phase PH2 (when clock signal is low), SW2 is on. SW1 and SW2 are not on at the same time. The sensing capacitor C_S 111 is charged to

the supply voltage V_{DD} during phase PH1 and is discharged to the modulator capacitor C_{MOD} 183 during phase PH2.

[0032] The sigma-delta modulator 180 includes a comparator 181, a latch 182, a modulation capacitor C_{MOD} 183, and a discharge resistor R_B 184. When the modulation capacitor voltage V_{CMOD} reaches the comparator reference voltage V_{REF} , the comparator 181 toggles and, following a delay period provided by latch 182, enables the capacitor discharge resistor R_B when SW3 is on. As a result of the charge removed from C_{MOD} 183 through R_B 184, the voltage of the modulation capacitor C_{MOD} 183 starts dropping. When the voltage of the modulation capacitor C_{MOD} 183 falls below the reference voltage V_{REF} , the comparator 181 toggles and, following a delay period provided by latch 182, SW3 is off preventing the discharge of C_{MOD} 183 through resistor R_B 184. Thus, the modulation capacitor C_{MOD} 183 starts rising again, repeating the modulation capacitor C_{MOD} 183 charge/discharge cycles. The latch 182 makes comparator operation synchronous to the clock 190 and limits minimum discharge switch SW3 on/off time. The sigma-delta modulator 180 keeps the average modulation capacitor voltage V_{CMOD} close to the reference voltage V_{REF} by alternatively turning on/off the discharge switch SW3.

[0033] Figure 2 illustrates a capacitance sensing circuit 200 for sensing mutual capacitance of the capacitor C_M 210 in a mutual capacitance (transmitter-receiver or TX-RX) sensing mode. The capacitor C_{P1} 230 and C_{P2} 220 represent the parasitic capacitances of two sensor elements. The capacitance sensing circuit 200 may operate using two non-overlapping phases: PH1 and PH2, which cycle repeatedly. During PH1, the switches SW1 and SW3 are turned on, while during PH2, the switches SW2 and SW4 are turned on. The switches SW1 and SW2 function as a transmitter driver that charges

the capacitor C_M 210 during PH1 when SW1 and SW3 are turned on and discharges the capacitor C_M 210 during PH2 when SW2 and SW4 are turned on.

[0034] The switches SW3 and SW4 function as current demodulation receiver switches. The analog buffer 201 keeps the receiver electrode potential approximately the same during both PH1 and PH2 operation phases, shielding the circuit 200 from the C_{P1} parasitic capacitance change. It should be noted that the integration capacitor C_{INT} 206 is considered part of the capacitance sensing circuit 200 and is shown here for ease of explanation. During PH1, i.e., the charge cycle, the voltage potential for the capacitor C_M 210 is $V_{CM} = V_{DD} - V_{CENT}$, the voltage potential for the parasitic capacitors C_{P1} 230 and C_{P2} 220 are $V_{CP1} = V_{CENT}$, $V_{CP2} = V_{DD}$. During PH2, i.e., the discharge cycle, the voltage potential for the capacitor C_M 210 is $V_{CM} = V_{ABUF} = V_{CENT} = V_{CP1}$.

[0035] As discussed above, the capacitance sensing circuits 100A and 100B can only operate in a self-capacitance sensing mode and the capacitance sensing circuit 200 can only operate in a mutual capacitance sensing mode. The capacitance sensing circuits 100A, 100B, and 200 have variable input impedance at different operation phases, which causes possible parasitic external noise signal demodulation. For example, when none of the switches in a capacitance sensing circuit, such as the capacitance sensing circuit 100A, 100B, or 200, is turned on, the capacitance sensing circuit has high-impedance. It is supposed in the dead time no one switch is turned on. During this time the circuit is high-impedance circuit. If the very high-frequency RF noise (e.g. 1GHz signal, with periods comparable with dead time) with sufficient amplitude is applied during dead time, the body diode could turn on and analog multiplexer starts conduct, causing the

false capacitance sense system operation. If input circuit is low impedance input circuit all time, there is much less chances that RF noise could affect system operation.

[0036] Furthermore, the capacitance sensing circuits 100A, 100B, and 200 typically only provide half-wave rectification and demodulation of the sensing current, resulting in the low-frequency noise immunity degradation, especially noise from AC power, such as the high-amplitude noise at 110-230 V at 50/60 Hz. The term half-wave rectification and demodulation means that the circuit multiplies the noise signal, applied to C_S by factor 1 when C_S is connected with C_{MOD} and by factor 0 when C_S is connected to power supply. So, the noise signal comes to the following modulator/integration circuits without proper mixing up and suppressing by the integration circuit low-pass filter nature. The full-wave circuit multiples noise signal by factor ± 1 , mixing up it and suppressing the integration circuit filter. Noise may also be coupled from AC-DC power supplies, such as from AC-DC switching power converters having noise between 40 kHz-3MHz, depending on the switching power supply regulator. The main benefit of using full-wave demodulation is in the much better suppression of the AC noise and better suppression of the noise from switching regulators.

[0037] Furthermore, the above-mentioned circuits may be configured to sense the capacitance only in one self-capacitance (single-electrode) sensing mode or mutual capacitance (dual-electrode) sensing mode. Having a circuit with the ability to sense capacitance in both modes may provide some benefits, such as by improving the water rejection possibilities and touch coordinate resolution.

[0038] Figure 3A illustrates a block diagram of one embodiment of an electrical circuit 300A having a capacitance measurement circuit for sensing capacitances on a

touch-sensing surface using multiple sensor elements of a sensor array in a self-capacitance sensing mode. The electrical circuit 300A includes a capacitance measurement circuit 360 and a touch-sensing surface 350 (e.g., array of buttons, sliders, a touch screen, a touch pad).

[0039] The capacitance measurement circuit 360 includes a selection circuit 340, a capacitance sensing circuit 310, and a capacitance conversion circuit 320. The touch-sensing surface 350 may be coupled to the capacitance measurement circuit 360 via the selection circuit 340 (e.g., multiplexer). The selection circuit 340 allows the capacitance sensing circuit 310 to sense the capacitance on multiple sensor elements 321(1)-321(N). It is understood that the touch-sensing surface 350 may be coupled to one or more capacitance measurement circuits 360 via other means, e.g., one or more multiplexers, or without any multiplexers, as would be appreciated by one of ordinary skill in the art having the benefit of this disclosure. The capacitance sensing circuit 310 senses the self-capacitance of one or more sensor elements of the touch-sensing surface 350 in a single-ended, self-capacitance sensing mode by converting the sensed capacitance to current pulses. The capacitance conversion circuit 320, coupled to the capacitance sensing circuit 310, receives the current pulses input from the capacitance sensing circuit 310 and converts the current pulses into readable digital data.

[0040] In Figure 3A, the touch-sensing surface 350 is a two-dimensional user interface that uses a sensor array 321 to detect capacitance on the touch-sensing surface 350 in a self-capacitance sensing mode. In one embodiment, the sensor array 321 includes sensor elements 321(1)-321(N) (where N is a positive integer) that are disposed as a two-dimensional matrix (also referred to as an XY matrix). It should be noted that

the sensor array 321 depicts four sensor elements; however, in other embodiments, the sensor array 321 may include any number of sensor elements. The sensor elements 321(1)–321(N) are conductors that are coupled to the capacitance sensing circuit 310 of the capacitance measurement circuit 360 via the selection circuit 340. The conductors may be metal, or alternatively, the conductors may be conductive ink (e.g., carbon ink), conductive ceramic (e.g., transparent conductors of indium tin oxide (ITO)), conductive polymers, or the like. In Figure 3A, each sensor element 321(1)–321(N) is represented as a capacitor. The capacitance sensing circuit 310 includes at least one current conveyor 330. In one embodiment, the current conveyor 330 is a second generation current conveyor (CCII) implemented by CMOS technology, such as illustrated in Figure 5B.

[0041] Although Figure 3A describes the electrical circuit 300A having the capacitance measurement circuit 360 and the touch-sensing surface 350, in other embodiments, the capacitance measurement circuit may be implemented in other non-contact capacitance sensing devices that use proximity detection, which may not have a touch-sensing surface, as would be appreciated by one of ordinary skill in the art having the benefit of this disclosure.

[0042] Figure 3B illustrates a block diagram of one embodiment of an electrical circuit 300B having a mutual capacitance measurement circuit for sensing capacitances on a touch-sensing surface using multiple sensor elements of a sensor array in a mutual capacitance sensing mode. The electrical circuit 300B includes a capacitance measurement circuit 361 and a touch-sensing surface 351 (e.g., of a touch screen, a touch pad).

[0043] The capacitance measurement circuit 361 includes a multiplexer 370 and a demultiplexer 380, a capacitance sensing circuit 311, and a capacitance conversion circuit 321. The touch-sensing surface 351 is coupled to the capacitance measurement circuit 361 via the multiplexer 370 and the demultiplexer 380. Although Figure 3B shows the row sensor elements of the sensor array 322 are connected to the multiplexer 370 and the column sensor elements of the sensor array 322 are connected to the demultiplexer 380, alternatively, the row sensor elements of the sensor array 322 may be connected to the demultiplexer 380 and the column sensor elements of the sensor array 322 may be connected to the multiplexer 370, as would be appreciated by one of ordinary skill in the art having the benefit of this disclosure. It is also understood that the touch-sensing surface 351 could be coupled to the one or more capacitance measurement circuits 361 via other means, e.g., one multiplexer or more than two multiplexers, or without any multiplexers, as would be appreciated by one of ordinary skill in the art having the benefit of this disclosure. For example, one multiplexer may be used for the TX lines and the RX lines are connected to the receiver channels directly without a multiplexer or demultiplexer. The capacitance sensing circuit 311 senses the mutual capacitance formed between two sensor elements, which are located in an intersecting row and column of the touch-sensing surface 351, in a mutual capacitance sensing mode by converting the sensed mutual capacitance to current pulses. The capacitance conversion circuit 321, coupled to the capacitance sensing circuit 311, receives the current pulses input from the capacitance sensing circuit 311 and converts the current pulses into readable digital data.

[0044] In the embodiment shown in Figure 3B, the touch-sensing surface 351 is a two-dimensional user interface that uses the capacitance measurement circuit 361 to

detect mutual capacitance on the touch-sensing surface 351. The sensor array 322 includes sensor elements 322(1)-322(N) (where N is a positive integer) that are disposed in rows and columns. In one embodiment, the touch-sensing surface 351 uses ITO to form the electrically conductive sensor elements. Alternatively, other touch-sensing surfaces having other electrically conductive sensor elements may be used as would be appreciated by one of ordinary skill in the art having the benefit of this disclosure. It should be noted that the sensor array 322 depicts sensor elements 322(1)-322(N) disposed in 4 rows and 5 columns in Figure 3B; however, in other embodiments, the sensor array 322 may include any number of sensor elements that are disposed in any number of rows and columns. Although Figure 3B describes the electrical circuit 300B having the capacitance measurement circuit 361 and the touch-sensing surface 351, in other embodiments, the capacitance measurement circuit may be implemented in other non-contact capacitance sensing devices that use proximity detection, which may not have a direct touch-sensing surface, as would be appreciated by one of ordinary skill in the art having the benefit of this disclosure.

[0045] The sensor elements 322(1)-322(N) are conductors that are coupled to the capacitance sensing circuit 311 of the capacitance measurement circuit 361 via the multiplexer 370 and the demultiplexer 380. The conductors may be metal, or alternatively, the conductors may be conductive ink (e.g., carbon ink), conductive ceramic (e.g., transparent conductors of ITO), conductive polymers, or the like.

[0046] In Figure 3B, the mutual capacitance C_M is formed by electric field between two conductive objects, i.e., two sensor elements, one acting as a signal receiver and the other acting as a transmitter, in which some portion of the current passing through

one passes into the other. As shown, the mutual capacitance C_M occurs between two sensor elements that are located at the intersection of each row and column of the touch sensing surface 351. As a conductive object, such as a finger, presses down on a touch-sensing surface, the mutual capacitance formed between a receiver sensor element and a transmitter sensor element is decreased because the conductive object shunts part of the electric field to the ground. Although the parasitic capacitances of the receiver sensor element and the transmitter sensor element are increased at the same time the mutual capacitance decreases, the change of the parasitic capacitances should not affect the mutual capacitance sensing when the potential of the receiver sensor element is kept constant, which could be achieved when the capacitance sensing circuit receives current inputs.

[0047] The aforementioned circuits from Figure 1A, Figure 1B, and Figure 2 use the switching capacitor sensing principle. There is possible to build the capacitance sensing circuits, using the current conveyer as primary building block. There are several generation of the current conveyer circuits, this invention uses second generation of the current conveyer in one embodiment. In other embodiments, other generations of current conveyer circuits may be used.

[0048] Figure 5A illustrates a simplified schematic of a second generation current conveyer (CCII) 500A, according to one embodiment. The CCII 500A is a four-terminal device derived by interconnecting the voltage and the current followers. As shown in Figure 5A, the four terminals of the CCII 500A include: the voltage input terminal Y_V , the current input terminal X_I , the current output terminal I_{Z+} , and the current output terminal I_{Z-} . The voltage input terminal Y_V is a high-impedance terminal while the

current input terminal X_I is a low-impedance terminal. An input voltage (V_Y) applied to the voltage input terminal Y_V may be conveyed to the voltage V_X on the current input terminal X_I , i.e., $V_X = V_Y$. In addition, no current flows into the input terminal Y_V as Y_V is high impedance input.

[0049] An input current I_0 applied to the input terminal X_I is conveyed to the output current I_{Z+} at the output terminals I_{Z+} and I_{Z-} . The output terminals I_{Z+} and I_{Z-} are used for balanced current outputs, i.e., $I_{Z+} = -I_x$, $I_{Z-} = +I_x$.

[0050] The implementation of the bipolar current output of the CCII 500A helps with noise rejection and may be used for quasi-differential channels building. The output terminals I_{Z+} are high-impedance output terminals suitable for current output. The direction of the output current I_Z is relative to the input current at the current input terminal X_I . The input-output relation of the CCII 500A may be described by the following matrix equation:

$$[0051] \quad \begin{pmatrix} I_Y \\ V_X \\ I_{Z+} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ V_Z \end{pmatrix}$$

[0052] Using the CCII 500A for sensing capacitance in multiple modes of the capacitance sensing circuit may provide the following benefits. First, the CCII has the low-impedance current input X_I , which may provides good immunity to high-impedance noise signals, such as RF or ESD. Second, the voltage potential of the current input X_I is controlled by the high-impedance voltage input Y_V , allowing implementing optimal structures for multiple capacitance sensing modes (self capacitance sensing mode and mutual capacitance sensing mode). Third, the CCII 500A current outputs may be easily converted to measurable form by using charge integration/balancing circuits, such as a

sigma-delta modulator or simple charge integration circuits. Finally, the CCII 500A has the ability of operating without an external closed loop, providing stability at different sensor parasitic capacitances. The current conveyors are widely used inside the analog and mixed signal ASIC for signal amplification, filtering and rectification analog signals multiplication and division, building the trans-impedance and trans-conductance amplifiers, wideband line drivers. There are only few discrete implementation of the CCII, called sometimes as ideal transistor, e.g., the OPA860/861 from Texas Instruments.

[0053] In one embodiment, the CCII 500A may be an operational amplifier based architecture that uses a closed loop system. In another embodiment, the CCII 500A may use the translinear principle that uses an open loop architecture. Alternatively, other implementations of current conveyors may be used for sensing capacitance as would be appreciated by one of the ordinary skill in the art having the benefit of this disclosure.

[0054] Figure 5B illustrates a CMOS implementation of a second generation current conveyor (CCII) 500B implemented by translinear principle, according to one embodiment. The CCII 500B includes an input stage (transistors M1 and M12), a current bias sources stage (transistors M2 and M13), a voltage follower stage (transistors M8 through M11), multi output current mirrors M3-M4, M6, M14, M16, M17, and current mirrors M5, M7 and M15, M18. The voltage follower stage is represented by the transistors M8 through M11 forming a translinear loop stage. The current mirrors are used to convey the current passing through to the input terminal X_1 to the output terminals I_{Z+} and I_{Z-} . The CCII 500B may be implemented in the 0.35 μ m CMOS process. Alternatively, the CCII may be implemented using other CMOS or bipolar processes, as

well as using other configurations for the CCH as would be appreciated by one of ordinary skill in the art having the benefit of this disclosure.

[0055] Figure 4A illustrates a capacitance sensing circuit 400 for sensing capacitance of one or more sensor elements in either a self-capacitance (single-electrode) sensing mode or a mutual capacitance sensing mode, according to one embodiment. The capacitance sensing circuit 400 includes a driver circuit 410 for sensing mutual capacitance, a sensor element circuit 420, a CCH 430, a synchronous demodulation circuit 440, a clock source 450, a delay element 460, and a signal selection circuit 470. The CCH 430 generates balanced current outputs (I_{z+} , I_{z-}), which are used as inputs for the demodulation circuit 440. In one embodiment, the synchronous demodulation circuit 440 is a full-wave synchronous demodulation circuit. Alternatively, other synchronous demodulation circuits could be used for the capacitance sensing circuit 400, as would be appreciated by one of ordinary skill in the art having the benefit of this disclosure.

[0056] In one embodiment, the multiple capacitance sensing modes include a self-capacitance (single-electrode, single-ended) sensing mode and a mutual capacitance sensing mode. In one embodiment, the capacitance sensing circuit 400 may be switched between a self-capacitance sensing mode and a mutual capacitance sensing mode using the mode selection signal 480.

[0057] The clock source 450 generates a clock signal for the synchronous demodulation circuit 440, the mode selection circuit 470, and the driver circuit 410. In one embodiment, the clock source 450 is a spread spectrum clock source. The delay element 460 is used to delay the clock signal generated by the clock source 450 to make sure that the delayed clock signal 490 is applied to the signal selection circuit 470 and the

driver circuit 410, after the synchronous demodulation circuit 440 is switched to accept proper input current polarity. The capacitance sensing circuit 400 acts as differentiator network, forming the largest peak current values immediately after rising and falling edge of the TX signal, taking into account finite on/off switching time the synchronous demodulation circuit 440 is needed prior to the edge of the TX signal. Alternatively, the capacitance sensing circuit 400 does not include the delay element 460.

[0058] In Figure 4A, the mode selection circuit 470 is a multiplexer 471 having two inputs: the delayed clock 490 and a reference voltage V_{REF} 473. The mode selection signal 480 functions as a selection line for the multiplexer 471. The output of the multiplexer 471 is coupled to the input terminal Y_V , i.e., the voltage input of the CCII 430. The input terminal X_I , i.e., the current input, of the CCII 430 is coupled to a terminal of the sensor element circuit 420, e.g., one terminal of the capacitor (C_M) to be measured. The balanced outputs (I_{z+} , I_{z-}) of the CCII 430 are coupled to the synchronous demodulation circuit 440, which in turn generates a current output I_{OUT} . In another embodiment, other selection circuits may be used to switch between the sensing modes, for example, a logic state machine. Various techniques for the synchronous detector output current measurement could be used, e.g., the techniques of converting current in the voltage using the resistive circuits with following filtering, integrating current and charge time measurement, and supplying current to the sigma-delta modulator circuits and convert it to the bit-stream density.

[0059] The driver circuit 410 includes an AND gate 411, a NAND gate 412, switches SW1 and SW2, and a voltage source V_{DD} . The driver circuit 410 may be used to charge and discharge the capacitors in the sensor element circuit 420. The charge and

discharge are repeated in cycles. During the charge cycle, the switch SW1 of the driver circuit 410 is turned on and the switch SW2 of the driver circuit 410 is turned off. The switch SW1 is controlled by the output of the NAND gate 412 and the switch SW2 is controlled by the output of the AND gate 411. The timing of the switching of SW1 and SW2 are controlled so as to prevent any interval where both SW1 and SW2 are closed at the same time. One input of each of the AND gate 411 and the NAND gate 412 is coupled to the mode selection signal 480 and another input of each of the AND gate 411 and the NAND gate 412 is coupled to the delayed clock 490. Alternatively, the driver circuit 410 may include other circuit components than those illustrated in Figure 4A, as would be appreciated by one of ordinary skill in the art having the benefit of this disclosure.

[0060] The sensor element circuit 420 may include one or more sensor elements. In one embodiment, when the circuit 400 operates in a self-capacitance sensing mode, the sensor element circuit 420 may include one sensor element with a sensing capacitor C_s (as shown in Figure 7). In another embodiment, when the circuit 400 operates in a mutual capacitance sensing mode, the sensor element circuit 420 may include two sensor elements as a mutual capacitor C_M along with two parasitic capacitors C_{P1} and C_{P2} (as shown in Figure 6) are formed between those two sensor elements that are located in an adjacent intersection of a row and a column of a sensor array. Alternatively, the sensor elements circuits 420 may include more than two sensor elements, as would be appreciated by one of ordinary skill in the art having the benefit of this disclosure.

[0061] Figures 4B-C illustrate the operation waveforms of the capacitance sensing circuit of Figure 4A for measuring capacitance of sensor elements in a self-capacitance

sensing mode and a mutual capacitance sensing mode respectively, according to embodiments. As shown in Figure 4B, in the self-capacitance sensing mode, the CCH 430 voltage input reference Y_V is not kept constant, which is because the driver circuit 410 is disabled in the self capacitance sensing mode; therefore, the sensor element circuit 420 is driven and sensed through the X_I current pin of the CCH 430. As shown in Figure 4C, in the mutual capacitance sensing mode, the CCH 430 voltage input reference Y_V is kept constant at V_{REF} , which is because the driver circuit 410 is enabled to drive the sensor element circuit 420 in the mutual capacitance sensing mode.

[0062] Figure 6 illustrates the capacitance sensing circuit 400 of Figure 4A when configured to operate in a mutual capacitance sensing mode, according to one embodiment. As discussed above, the capacitance sensing circuit 400 shown in Figure 4A may sense capacitance for one or more sensor elements in multiple sensing modes, one of which is a mutual capacitance sensing mode. It should be noted that scanning multiple sensor elements could be done using multiple parallel channels or scanning sensor elements in series using analog switches. Figure 6 shows a simplified form of the capacitance sensing circuit 400 of Figure 4A when the mutual capacitance sensing mode is selected via the signal selection circuit 470, e.g., via the mode selection signal 480, in Figure 4A. As shown in Figure 4A, when the mode selection signal 480 indicates to the signal selection circuit 470 to operate in a mutual capacitance sensing mode, the multiplexer 471 of the signal selection circuit 470 will select the constant reference voltage V_{REF} as its output. As a result, as shown in Figure 6, the V_{REF} is coupled to the voltage input terminal Y_V of the CCH 430, and the delayed clock 490, generated from the clock source 450 via the delay element 460, is coupled to the driver circuit 410'. The

driver circuit 410' is equivalent to the driver circuit 410 in Figure 4A when the mutual capacitance sensing mode is selected, e.g., the mode selection signal is set to logic high. Because the voltage input terminal Y_V of the CCII 430 is held at a constant potential V_{REF} , the CCII 430, acting as a current amplifier, receives a current input from the sensor element circuit 420 and generates a current output for the synchronous demodulation circuit 440.

[0063] As shown in Figure 6, the sensor element circuit 420 includes the mutual capacitor C_M and two parasitic capacitors C_{P1} and C_{P2} . As described above, a mutual capacitor is formed between two sensor elements that are located at the intersection of each row and column of a touch-sensing surface. One terminal of the capacitor C_M in the sensor element circuit 420 is coupled to the current input terminal X_I , i.e., the low impedance current input of the CCII 430, while the other terminal of the capacitor C_M in the sensor element circuit 420 is coupled to the driver circuit 410'.

[0064] The driver circuit 410' charges and discharges the capacitor C_M of the sensor element circuit 420, and the charge and discharge are repeated in cycles. During the charge cycle, the switch SW1 of the driver circuit 410' is closed and the switch SW2 of the driver circuit 410' is open. Because the terminal of the capacitor C_M , which is connected to the current input X_I of the CCII 430, is fixed at the potential V_{REF} , due to the fact that V_{REF} is connected to the voltage input Y_V of the CCII 430, the capacitor C_M in the sensor element circuit 420 is charged to have a voltage potential of the voltage difference between V_{DD} and V_{REF} . During the discharge cycle, the switch SW2 of the driver circuit 410' is closed and switch SW1 of the driver circuit 410' is open. Accordingly, the capacitor C_M is discharged to have a voltage potential of $-V_{REF}$, because

the terminal of the capacitor C_M , which is connected to the current input X_I of the CCH 430, is fixed at the potential V_{REF} . In one embodiment, as illustrated in Figure 3B, a multiplexer 370 may be used to input signals from the sensor element circuit 420 to the CCH 430 and a demultiplexer 380 may be used to output signals from the driver circuit 410' to the sensor element circuit 420 when the circuit 400 operates in a mutual capacitance sensing mode.

[0065] Figure 7 illustrates the capacitance sensing circuit 400 of Figure 4A for sensing self capacitance of one or more sensor elements in a self-capacitance, single-ended sensing mode, according to one embodiment. As discussed above, the capacitance sensing circuit 400 shown in Figure 4A may sense capacitance for one or more sensor elements in multiple sensing modes, one of which is a self-capacitance, single-ended sensing mode. Figure 7 shows a simplified view of the capacitance sensing circuit 400 when the self capacitance, single-ended sensing mode is selected via the signal selection circuit 470 shown in Figure 4A. In Figure 4A, when the mode selection signal 480 indicates to the signal selection circuit 470 to operate in a self-capacitance, single-ended sensing mode, the multiplexer 471 of the signal selection circuit 470 will select the delayed clock 490 as its output, and the driver circuit 410 is disabled. As a result, as shown in Figure 7, the delayed clock 490 is coupled to the voltage input terminal Y_V of the CCH 430. Thus, the CCH 430, keeping the voltage potential of the low-impedance current input terminal X_I the same as that of the voltage input terminal Y_V , functions as a driver circuit to the sensor element circuit 420, and converts the charge and discharge currents of the sensor element circuit 420 to the balanced outputs I_{z+} and I_{z-} . In one embodiment, as illustrated in Figure 3A, a selection circuit 340 may be used to input and

output signals between the sensor element circuit 420 and the CCH 430 when the circuit 400 operates in a self-capacitance sensing mode.

[0066] The implementation of the CCH 430 of Figure 4A in a capacitance sensing circuit makes the electrode impedance of the sensor element circuit 420 constantly low during all operation phases and different sensing modes, and requires one charge and one discharge cycle for each operation period, allowing the capacitance sensing circuit 400 to operate at twice the frequency than previously known four-phase or multi-phase circuits. The ability to sense both sensor element charge and discharge current allows the output current within a given time window to be doubled, resulting in smaller number of charge/discharge cycles and improving signal-to-noise ratio.

[0067] The capacitance sensing circuits 400, 600, and 700 shown in Figures 4A, 6, and 7 respectively, may be used to implement one channel capacitance sensing operation. In another embodiment, a capacitance sensing circuit may operate in a differential sensing mode, forming the output signal proportional to the capacitance difference between two sensor elements. The differential sensing mode is especially useful for the working with the noisy signals, where noise is applied to two input terminals at same time.

[0068] Figure 8A illustrates a capacitance sensing circuit 800 for sensing capacitance of sensor elements in single-ended and differential (dual-channel) sensing modes, according to one embodiment. As shown, the capacitance sensing circuit 800 includes the CCH 810, the CCH 820, the synchronous demodulation circuit 830, the synchronous demodulation circuit 840, and four multiplexers M1, M2, M3, and M4. In one embodiment, each of the synchronous demodulation circuits 830 and 840 is a full-wave synchronous demodulation circuit. Alternatively, other synchronous demodulation

circuits could be used for the capacitance sensing circuit 800, as would be appreciated by one of ordinary skill in the art having the benefit of this disclosure

[0069] The outputs of M1 and M2 are coupled to the voltage input terminal Y_V and current input terminal X_I of the CCII 810, respectively; the outputs of M3 and M4 are coupled to the voltage input terminal Y_V and the current input terminal X_I of the CCII 820, respectively. Each of the multiplexers M1, M2, M3, and M4 has four inputs. Each of the multiplexers M1 and M3 receives four inputs: one input IN_A from the channel A, one input IN_B from the channel B, and one clock input. The fourth input of the multiplexers M1 and M3 are grounded. Each of the multiplexers M2 and M4 receives two inputs: one input IN_A from the channel A and one input IN_B from the channel B. The third and the fourth inputs of the multiplexers M2 and M4 are connected via the resistor R_G to some intermediate voltage potential (e.g. analog ground or reference source V_{REF}). The value of the resistor R_G determines the circuit current gain level (transconductance). The resistors R_B are bias resistors, which determine the CCII Y_V input potential in the mutual capacitance sensing modes. The input IN_A from channel A accepts either a current or voltage input from a first set of one or more sensor elements, and the input IN_B from channel B (CH2) accepts either a current or voltage input from a second set of one or more sensor elements, and passes same to the associated current conveyor.

[0070] In one embodiment, the inputs to both channels are voltage inputs. In another embodiment, the inputs to both channels are current inputs. The capacitance sensing circuit 800 is capable of operating in six different sensing modes, as noted in the table which is part of Figure 8A: a dual-channel single-ended self-capacitance sensing mode, a differential channel single-ended self-capacitance sensing mode, a dual-channel

current-based mutual capacitance sensing mode, a dual-channel voltage-based mutual capacitance sensing mode, a differential channel current-based mutual capacitance sensing mode, and a differential channel voltage-based mutual capacitance sensing mode. It is possible to pair two channels to get differential sensing modes for each dual channel sensing mode, resulting in having one differential channel.

[0071] The balanced outputs of the CCH 810 and CCH 820 are coupled to the synchronous demodulation circuits 830 and 840 respectively. The switch SM 870 selects which pair of current outputs is going to be used for the current outputs of the capacitance sensing circuit 800.

[0072] The capacitance sensing circuit 800 may receive either current inputs or voltage inputs from the two input channels, i.e., from the IN_A input terminal and the IN_B input terminal. In one embodiment, the capacitance sensing circuit 800 receives two current inputs when the capacitance sensing circuit 800 is configured as a low-impedance receiver. In another embodiment, the capacitance sensing circuit 800 receives two voltage inputs when the capacitance sensing circuit 800 is configured as a high-impedance receiver. It should be noted that, in the current-based sensing mode, the capacitance sensing circuit input is a low-impedance receiver and the input signal is current, flowing into or out of the receiver. In the voltage-based sensing mode the capacitance sensing circuit input is a high-impedance receiver and the input signal is voltage, applied to the receiver input. It should be noted that various capacitance sensing circuits use the current-based sensing mode due better immunity to the noise, but some capacitance sensing circuits use voltage-based sensing mode, especially when operating

with high resistance materials or when used differentially where coupled common mode noise may be rejected by the differential receiver.

[0073] The simplified schematics of the capacitance sensing circuit 800 in various sensing modes are shown in Figure 8B – Figure 8E. Figure 8B shows the circuit configuration when the capacitance sensing circuit 800 operates in a dual-channel, voltage-based mutual capacitance sensing mode. As shown in Figure 8B, one terminal of each of the mutual capacitors C_{MA} and C_{MB} of the sensor element circuit 880 is directly connected to the high-impedance input of the CCH 810 and CCH 820, respectively. The resistors R_B set DC component of inputs. The resistors R_G determine circuit gain in the dual-channel voltage-based mutual capacitance sensing mode, and CCH 810 and CCH 820 act as voltage to current translators with transconductance:

$$[0074] \quad g_{om} = \frac{1}{R_G}$$

[0075] Figure 8C shows the circuit configuration when the capacitance sensing circuit 800 operates in a differential voltage-based mutual capacitance sensing mode. As shown, the difference between Figure 8B and 8C is that the balanced outputs of the synchronous demodulation circuits 830 and 840 in Figure 8C are connected in opposite way, the resulted output current is difference between synchronous demodulation circuits 830 and 840 output currents.

[0076] Figure 8D shows the circuit configuration when the capacitance sensing circuit 800 operates in a dual-channel current-based mutual capacitance sensing mode. As shown in Figure 8D, the high-impedance voltage input terminal Y_V of each of the

CCII 810 and CCII 820 is connected to the constant voltage reference V_{REF} , and the current input terminal X_I of each of the CCII 810 and CCII 820 receives current input.

[0077] Figure 8E shows the circuit configuration when the capacitance sensing circuit 800 operates in a differential channel single-ended self-capacitance sensing mode. As shown, the delayed replica of the clock signal is applied to the high-impedance voltage input terminal Y_V of each of the CCII 810 and CCII 820. The CCII 810 and CCII 820 translates the voltage received from their respective voltage input terminal into the current input at the current input terminal X_I of each of the CCII 810 and CCII 820, causing the sensor element circuit 890 excitation. Then, each of the CCII 810 and CCII 820 subtracts the signals received from two channels (CH A and CH B).

[0078] The circuit configuration for the capacitance sensing circuit 800 operating in a dual-channel single-ended self-capacitance sensing mode is similar to the one shown in Figure 8E, and the difference between those two circuit configurations are that the outputs of the synchronous demodulation circuits 830 and 840 are not joined together when the capacitance sensing circuit 800 operates under the dual-channel single-ended self-capacitance sensing mode. In one embodiment, the capacitance sensing circuit 800, when operating in the single electrode sensing mode, may include a level translator, which translates the digital clock levels into the voltage applied to the voltage input of each of the CCII, e.g. supplying the predefined REF_HI level of the voltage to CCII at High level of the clock signal and applying the predefined REF_LO level at low.

[0079] The other embodiments of the proposed invention are possible, for example, there is possible to exchange the synchronous detector and differential mode switch.

[0080] Embodiments of the present invention, described herein, include various operations. These operations may be performed by hardware components, software, firmware, or a combination thereof. As used herein, the term “coupled to” may mean coupled directly or indirectly through one or more intervening components. Any of the signals provided over various buses described herein may be time multiplexed with other signals and provided over one or more common buses. Additionally, the interconnection between circuit components or blocks may be shown as buses or as single signal lines. Each of the buses may alternatively be one or more single signal lines and each of the single signal lines may alternatively be buses.

[0081] Certain portions of the embodiments may be implemented as a computer program product that may include instructions stored on a computer-readable medium. These instructions may be used to program a general-purpose or special-purpose processor to perform the described operations. A computer-readable medium includes any mechanism for storing or transmitting information in a form (e.g., software, processing application) readable by a machine (e.g., a computer). The computer-readable storage medium may include, but is not limited to, magnetic storage medium (e.g., floppy diskette); optical storage medium (e.g., CD-ROM); magneto-optical storage medium; read-only memory (ROM); random-access memory (RAM); erasable programmable memory (e.g., EPROM and EEPROM); flash memory, or another type of medium suitable for storing electronic instructions. The computer-readable transmission medium includes, but is not limited to, electrical, optical, acoustical, or other form of propagated signal (e.g., carrier waves, infrared signals, digital signals, or the like), or another type of medium suitable for transmitting electronic instructions.

[0082] Additionally, some embodiments may be practiced in distributed computing environments where the computer-readable medium is stored on and/or executed by more than one computer system. In addition, the information transferred between computer systems may either be pulled or pushed across the transmission medium connecting the computer systems.

[0083] Although the operations of the method(s) herein are shown and described in a particular order, the order of the operations of each method may be altered so that certain operations may be performed in an inverse order or so that certain operation may be performed, at least in part, concurrently with other operations. In another embodiment, instructions or sub-operations of distinct operations may be in an intermittent and/or alternating manner.

[0084] In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will be evident, however, that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative sense rather than a restrictive sense.

CLAIMS

What is claim is:

1. An apparatus, comprising
a capacitance sensing circuit comprising a current conveyor, the
capacitance sensing circuit configured to sense capacitance of one or more sensor
elements in a plurality of capacitance sensing modes, wherein a first of the
plurality of capacitance sensing modes is a self-capacitance sensing mode, and a
second of the plurality of capacitance sensing modes is a mutual capacitance
sensing mode.
2. The apparatus of claim 1, wherein the capacitance sensing circuit further
comprises a signal selection circuit configured to select one of the plurality of
capacitance sensing modes.
3. The apparatus of claim 1, wherein the capacitance sensing circuit further
comprises a synchronous demodulation circuit coupled to a current output of the
current conveyor, and wherein the synchronous demodulation circuit is configured
to generate a current output.
4. The apparatus of claim 1, wherein the self-capacitance sensing mode is a single-
electrode, single-ended sensing mode, and the mutual capacitance sensing mode is
a dual-electrode, single-ended sensing mode.

5. The apparatus of claim 4, wherein a voltage input of the current conveyor is coupled to a clock signal and a current input of the current conveyor is coupled to the one or more sensor elements when the single-electrode, single-ended sensing mode is selected.
6. The apparatus of claim 4, wherein a voltage input of the current conveyor is coupled to a constant reference voltage and a current input of the current conveyor is coupled to a first terminal of the one of more sensor elements when the dual-electrode, single-ended sensing mode is selected.
7. The apparatus of claim 6, wherein a second terminal of the one or more sensor elements is coupled to a driver circuit, and wherein the driver circuit receives a clock signal and uses the clock signal to repeatedly charge and discharge the one or more sensor elements to be sensed when the dual-electrode, single-ended sensing mode is selected.
8. The apparatus of claim 1, wherein the current conveyor is a second generation current conveyor (CCII).
9. The apparatus of claim 1, further comprising a capacitance conversion circuit coupled to the capacitance sensing circuit, wherein the capacitance conversion circuit converts a current received from the capacitance sensing circuit into digital data.

10. An apparatus, comprising:

a first current conveyor coupled to a first set of one or more sensor elements; and

a second current conveyor coupled to a second set of one or more sensor elements, wherein the first and the second current conveyors are configured to sense capacitance on the first and the second sets of one or more sensor elements, respectively, in a plurality of capacitance sensing modes, and wherein a first of the plurality of capacitance sensing modes is a self-capacitance sensing mode, and a second of the plurality of capacitance sensing modes is a mutual capacitance sensing mode.

11. The apparatus of claim 10, wherein the self-capacitance sensing mode is a dual-channel or a differential channel single-ended sensing mode and the mutual capacitance sensing mode is a dual-channel or a differential channel sensing mode.

12. The apparatus of claim 10, further comprising:

a first synchronous demodulation circuit coupled to the first current conveyor, wherein the first synchronous demodulation circuit is configured to generate a first current output; and

a second synchronous demodulation circuit coupled to the second current conveyor, wherein the second synchronous demodulation circuit is configured to generate a second current output.

13. The apparatus of claim 10, further comprising a signal selection circuit having a first, a second, a third, and a fourth multiplexers, wherein the first and the second multiplexers are coupled to a voltage input and a current input of the first current conveyor respectively, and the third and the fourth multiplexers are coupled to a voltage input and a current input of the second current conveyor respectively.
14. The apparatus of claim 10, wherein each of the first and the second current conveyors is a second generation current conveyor (CCII).
15. A method of measuring capacitance, comprising:
 - selecting one of a plurality of capacitance sensing modes; and
 - sensing capacitance of one or more sensor elements based on the selected one of the plurality of capacitance sensing modes, wherein a first of the plurality of capacitance sensing modes is a self-capacitance sensing mode, and a second of the plurality of capacitance sensing modes is a mutual capacitance sensing mode.
16. The method of claim 15, wherein the self-capacitance sensing mode is a single-electrode, single-ended sensing mode and the mutual capacitance sensing mode is a dual-electrode, single-ended sensing mode.

17. The method of claim 16, further comprising:

sensing the capacitance on the one or more sensor elements by using a current conveyor; and
generating a current output by the current conveyor.

18. The method of claim 15, further comprising:

charging the one or more sensor elements by using a driver circuit when in the mutual capacitance sensing mode; and
charging the one or more sensor elements by using the current input of the current conveyor.

19. The method of claim 15, wherein the self-capacitance sensing mode is a dual-channel or a differential channel single-ended sensing mode and the mutual capacitance sensing mode is a dual-channel or a differential channel sensing mode.

20. The method of claim 19, further comprising:

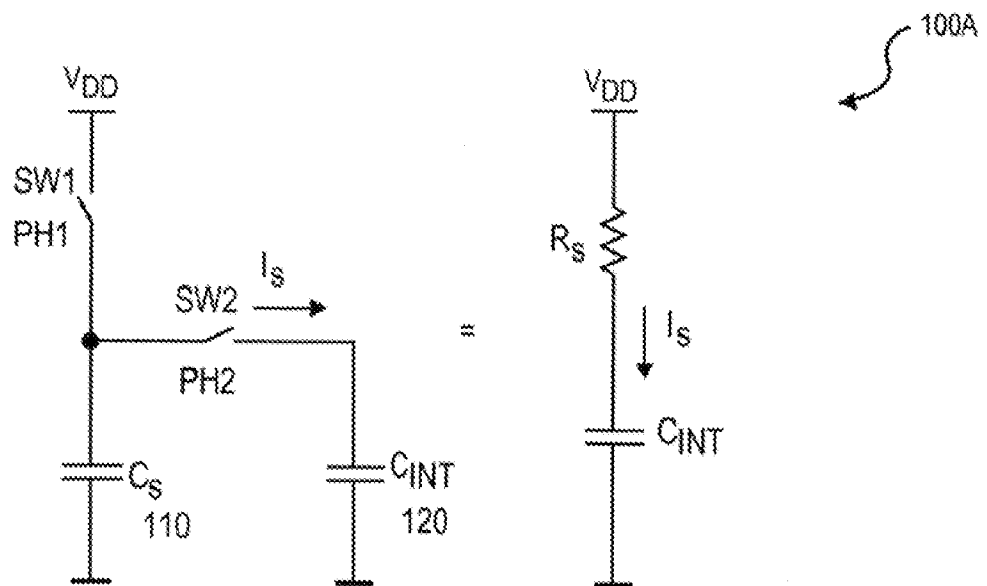
sensing the capacitance on a first set of the one or more sensor elements by using a first current conveyor;
sensing the capacitance on a second set of the one or more sensor elements by using a second current conveyor;
generating a first current output by the first current conveyor; and

generating a second current output by the second current conveyor.

21. An apparatus, comprising

a capacitance sensing circuit comprising a current conveyor, the capacitance sensing circuit configured to sense capacitance of a sensor element in a self-capacitance sensing mode.

22. The apparatus of claim 21, wherein the capacitance sensing circuit is further configured to sense capacitance of two or more sensor elements in a mutual capacitance sensing mode.

**FIG. 1A**

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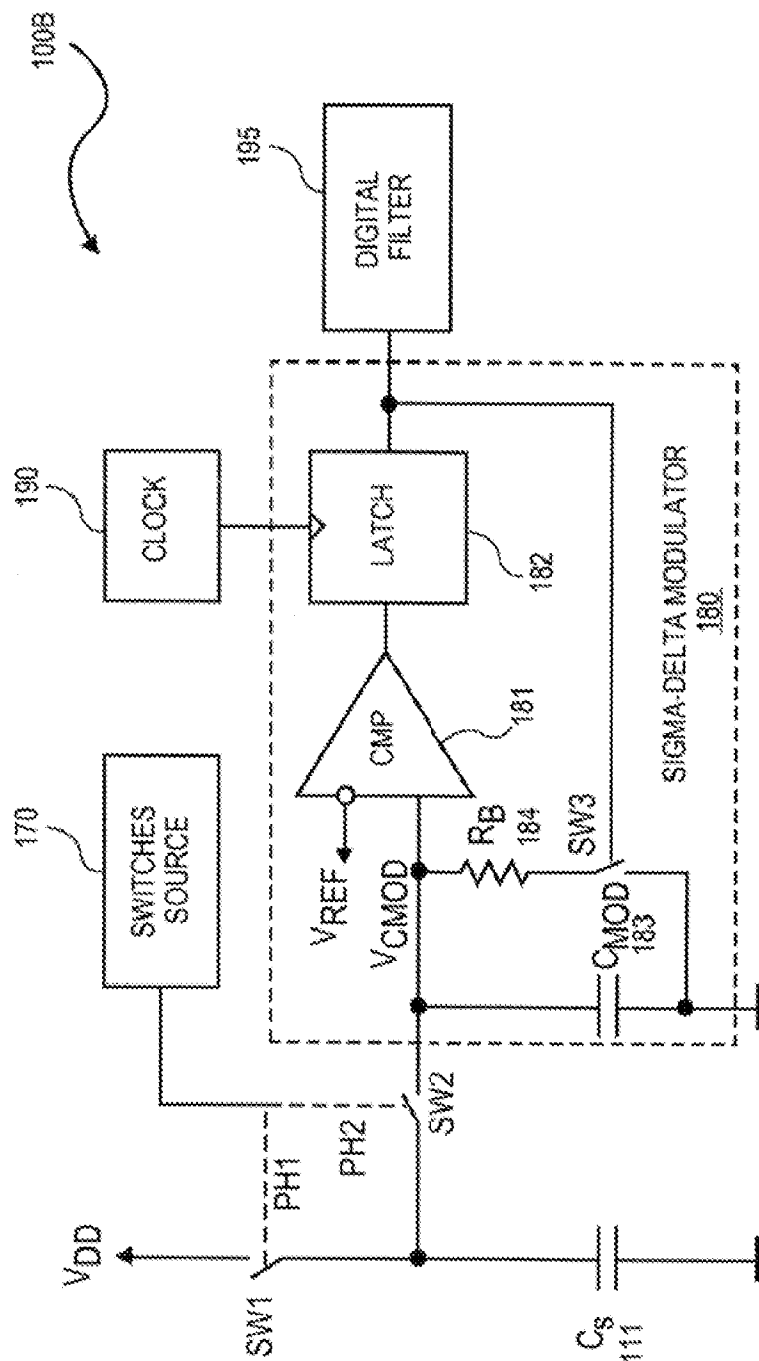
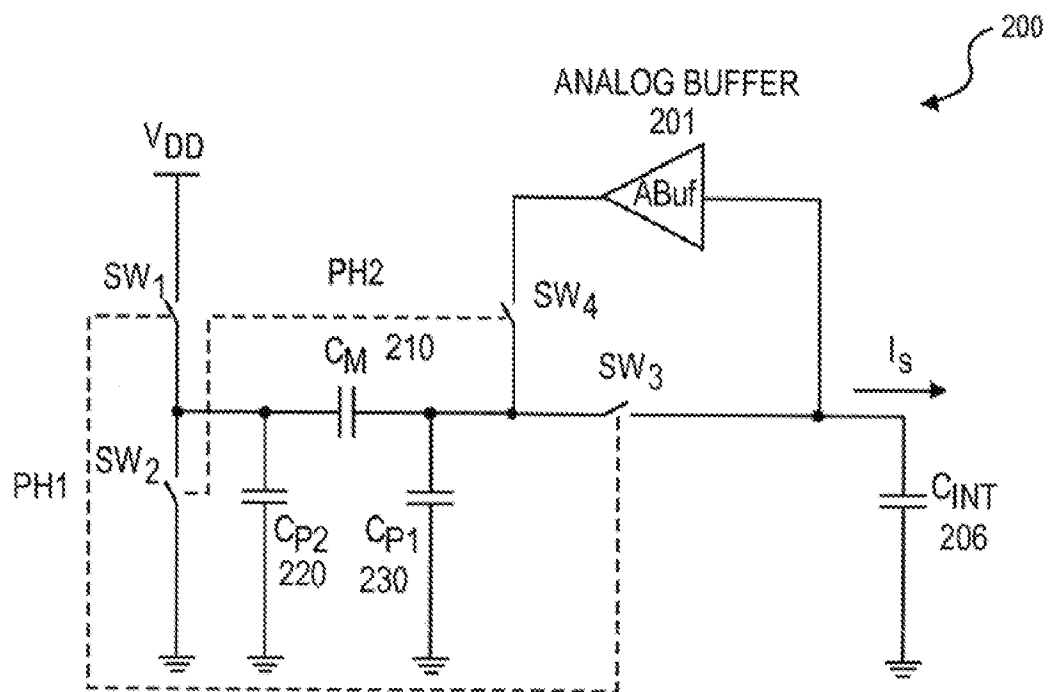


FIG. 1B

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**FIG. 2**

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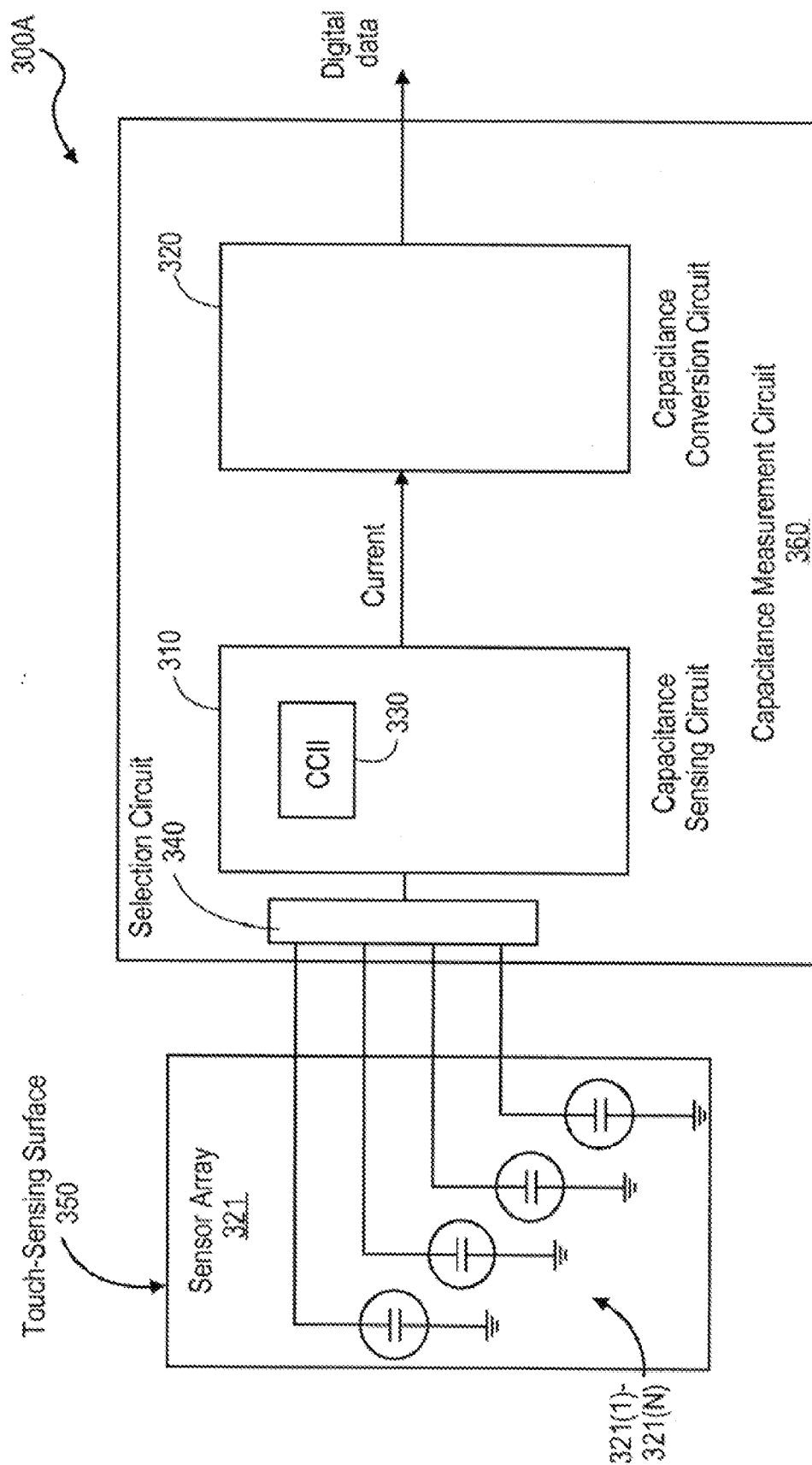


FIG. 3A

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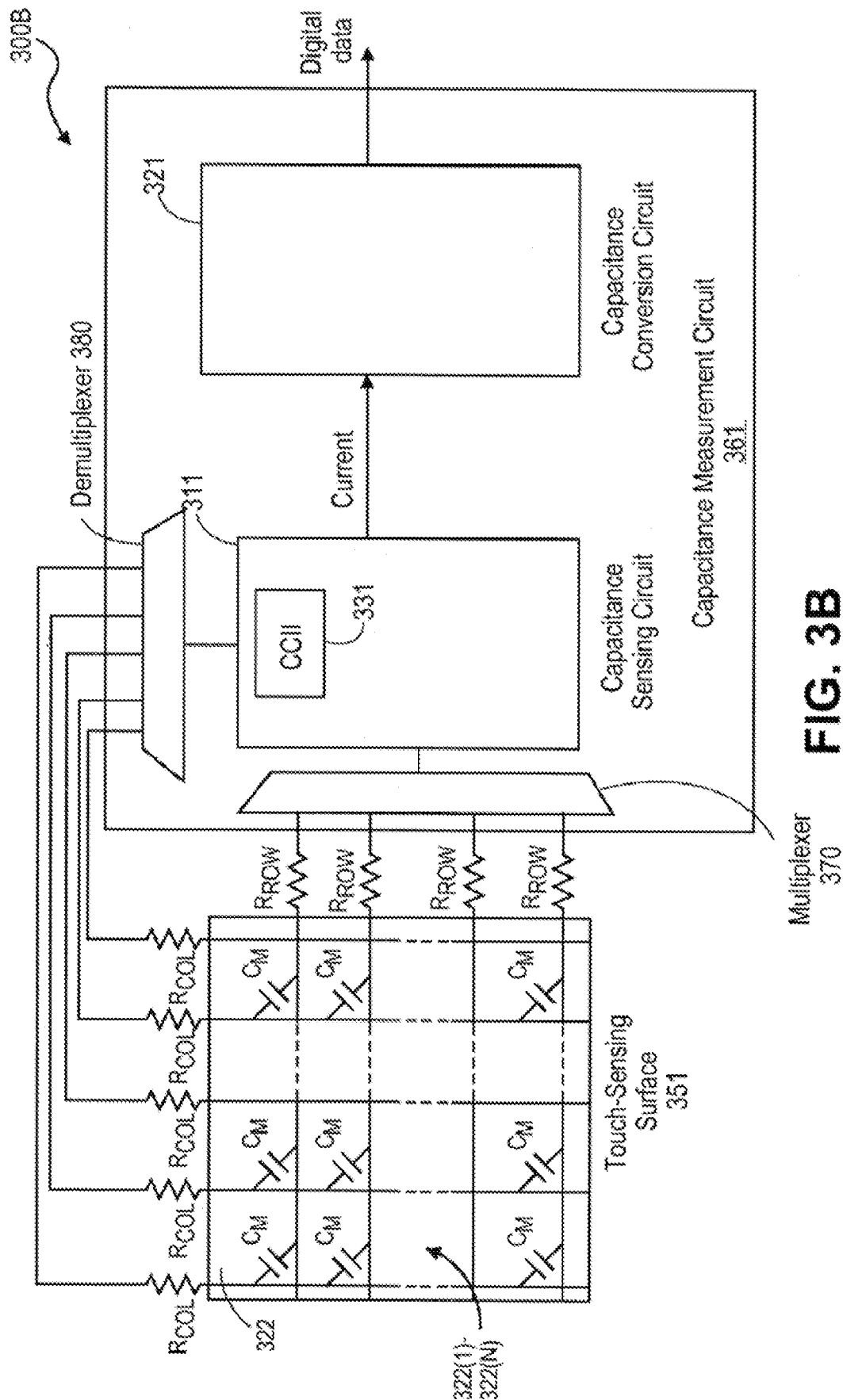


FIG. 3B

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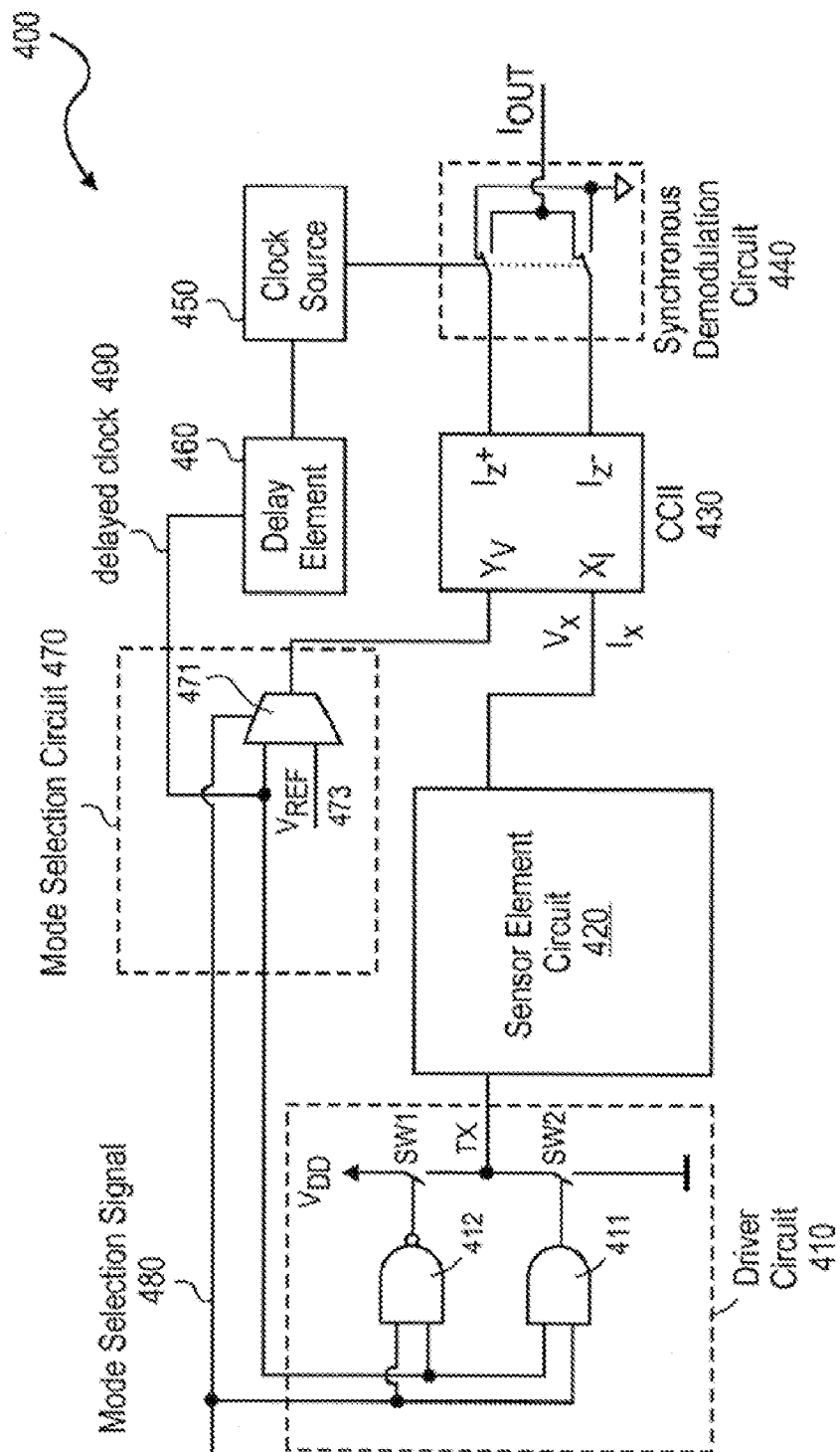


FIG. 4A

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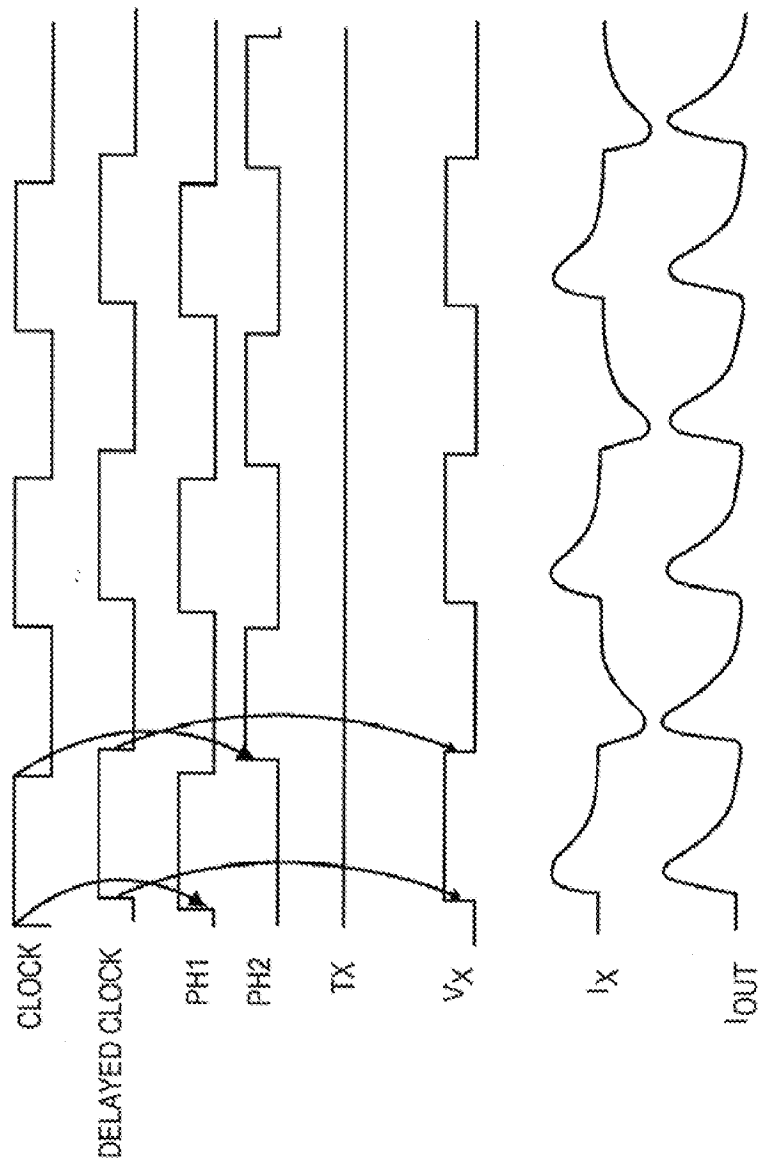


FIG. 4B

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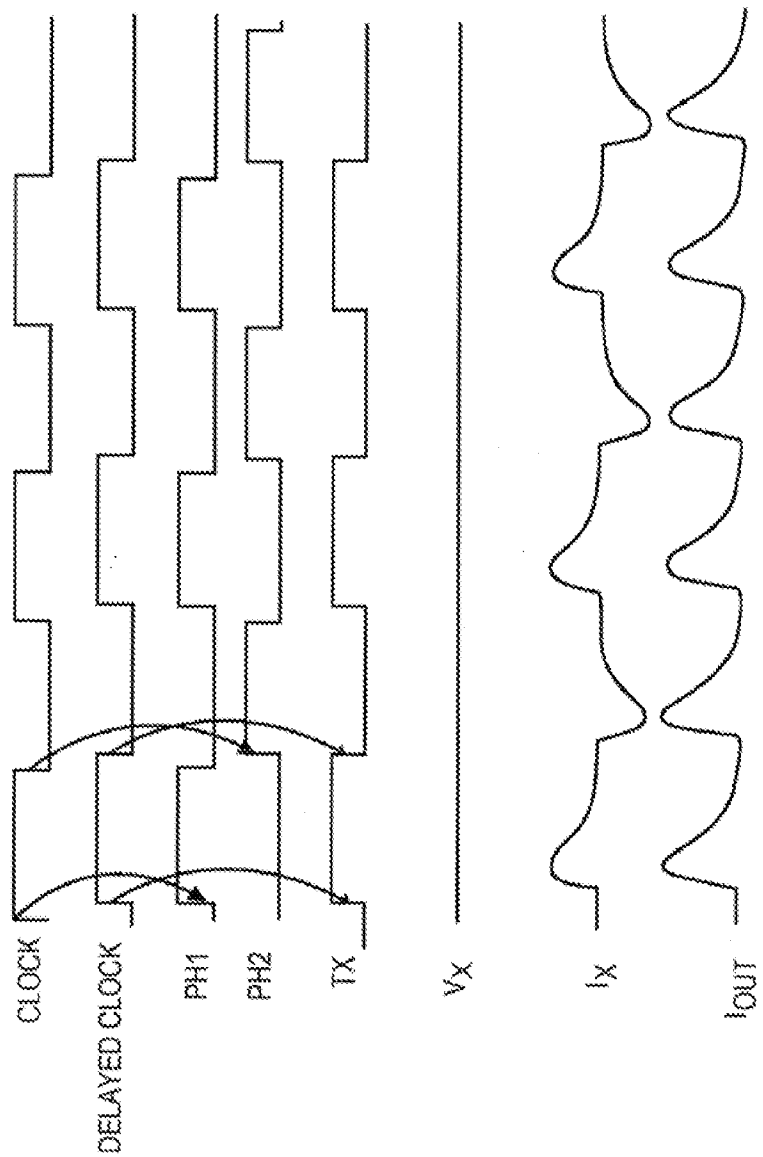


FIG. 4C

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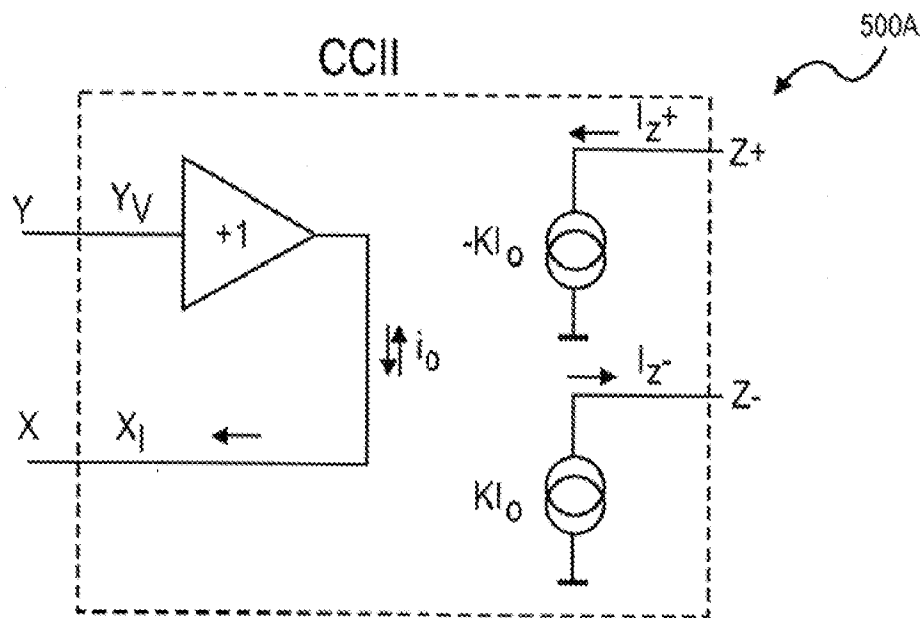


FIG. 5A

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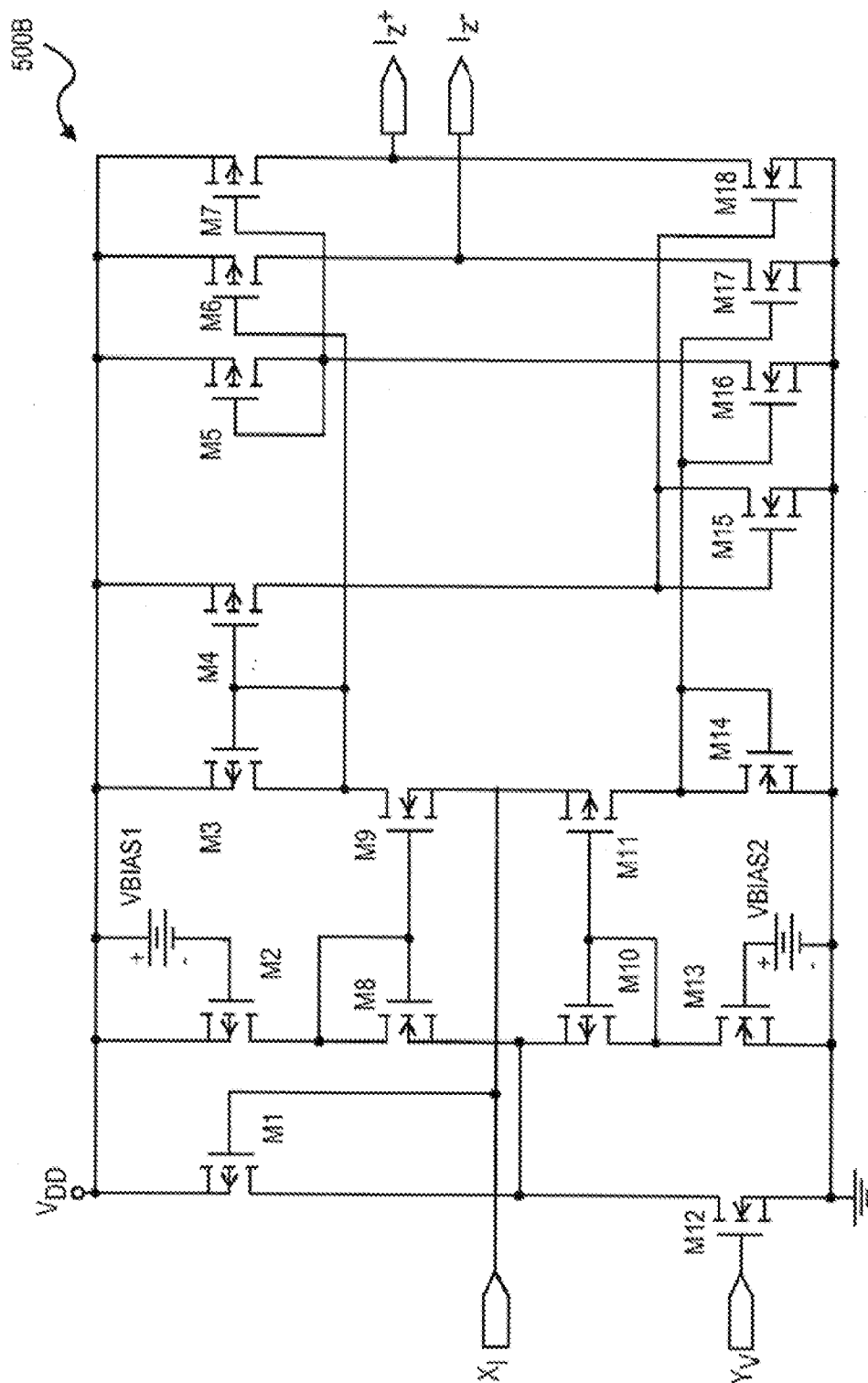


FIG. 5B

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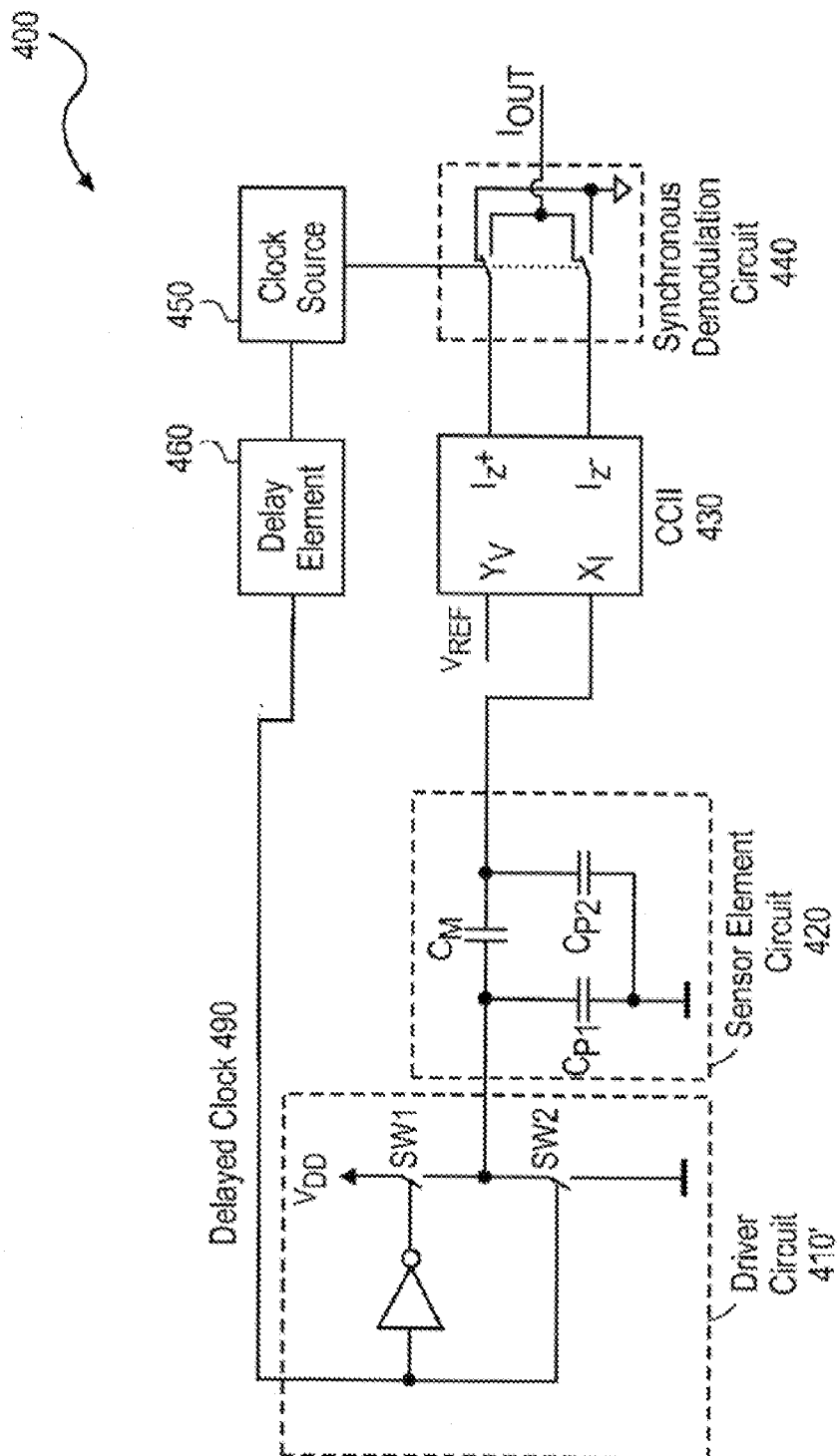


FIG. 6

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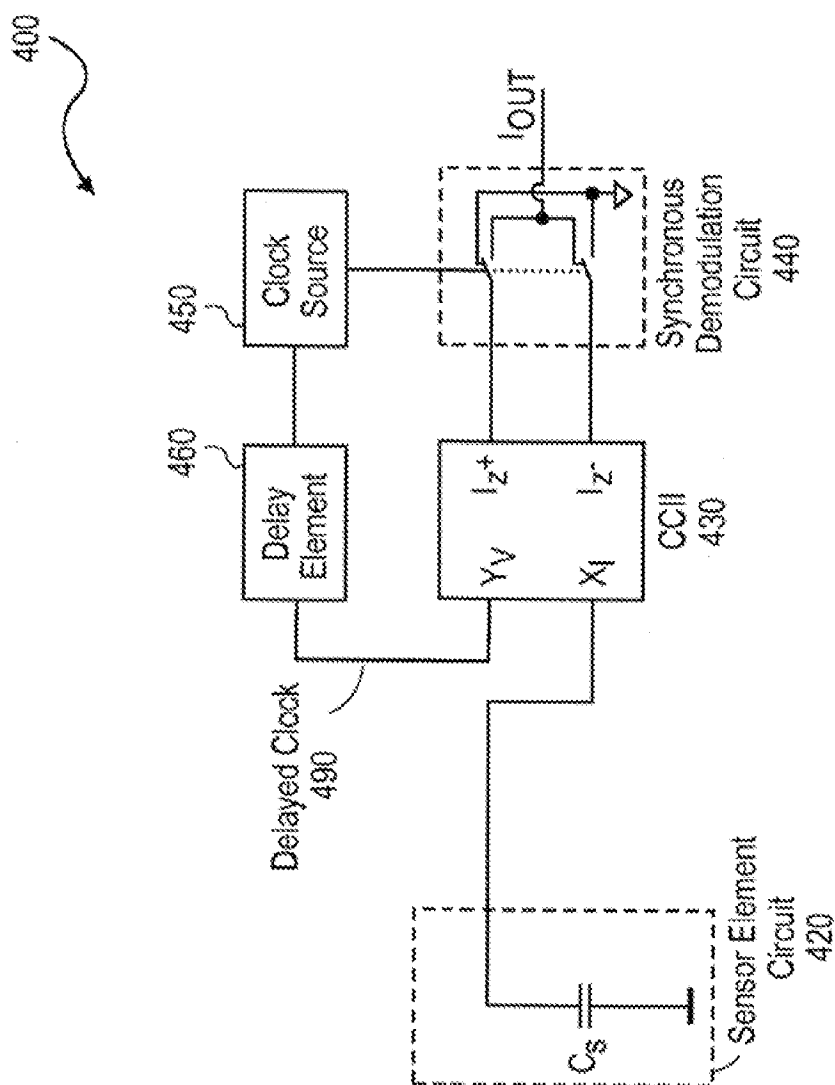
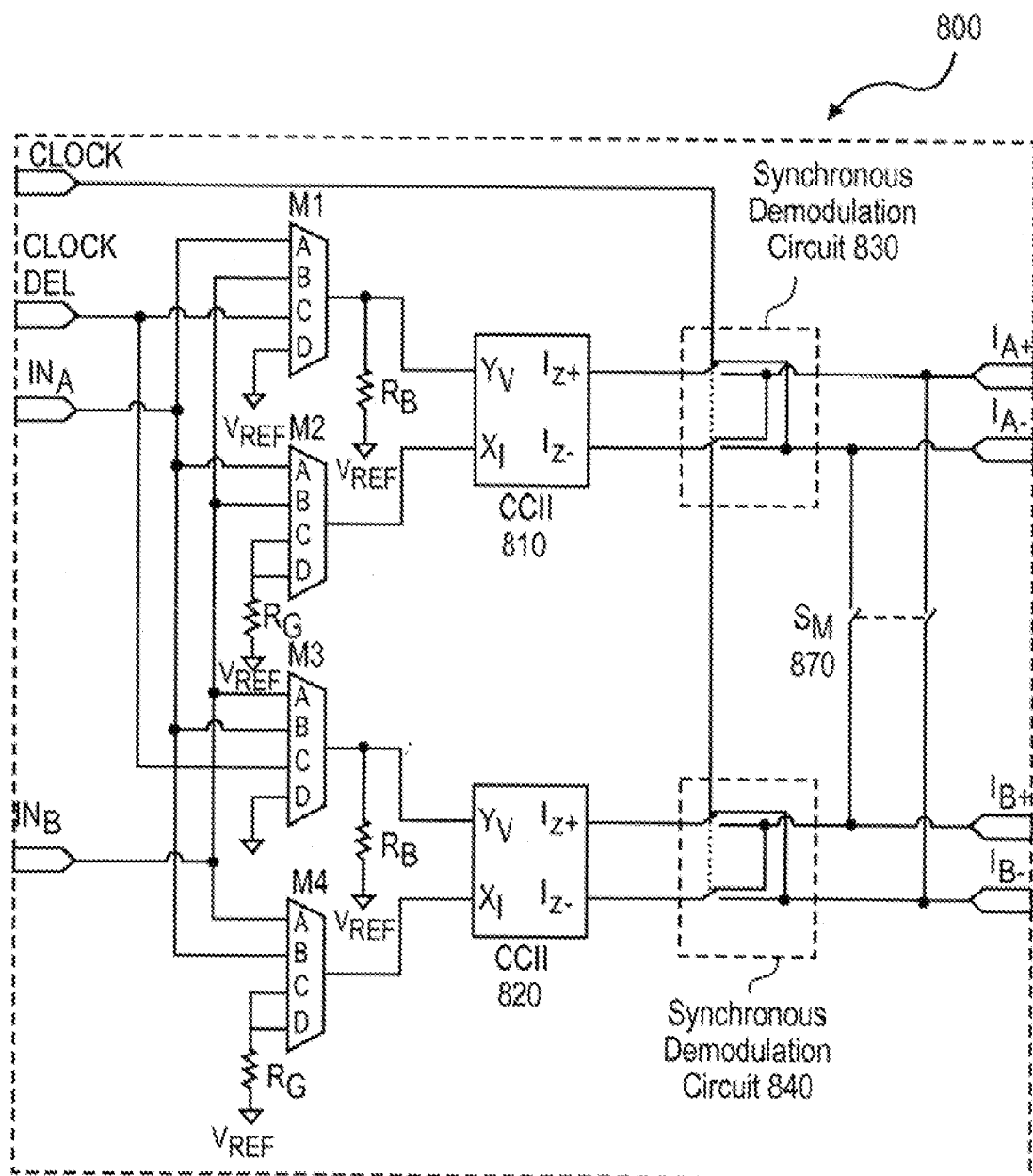


FIG. 7

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#	Mode	CHANNELS	M1	M2	M3	M4	S_M
1	Self-Capacitance	2	C	A	C	A	OFF
2	Self-Capacitance Differential	1	C	A	C	A	ON
3	Mutual Capacitance, Voltage Input	2	A	C	A	C	OFF
4	Mutual Capacitance, Current Input	2	D	A	D	A	OFF
5	Mutual Capacitance, Voltage Input, Differential	1	A	C	A	C	ON
6	Mutual Capacitance, Current Input, Differential	1	D	A	D	A	ON

FIG. 8A

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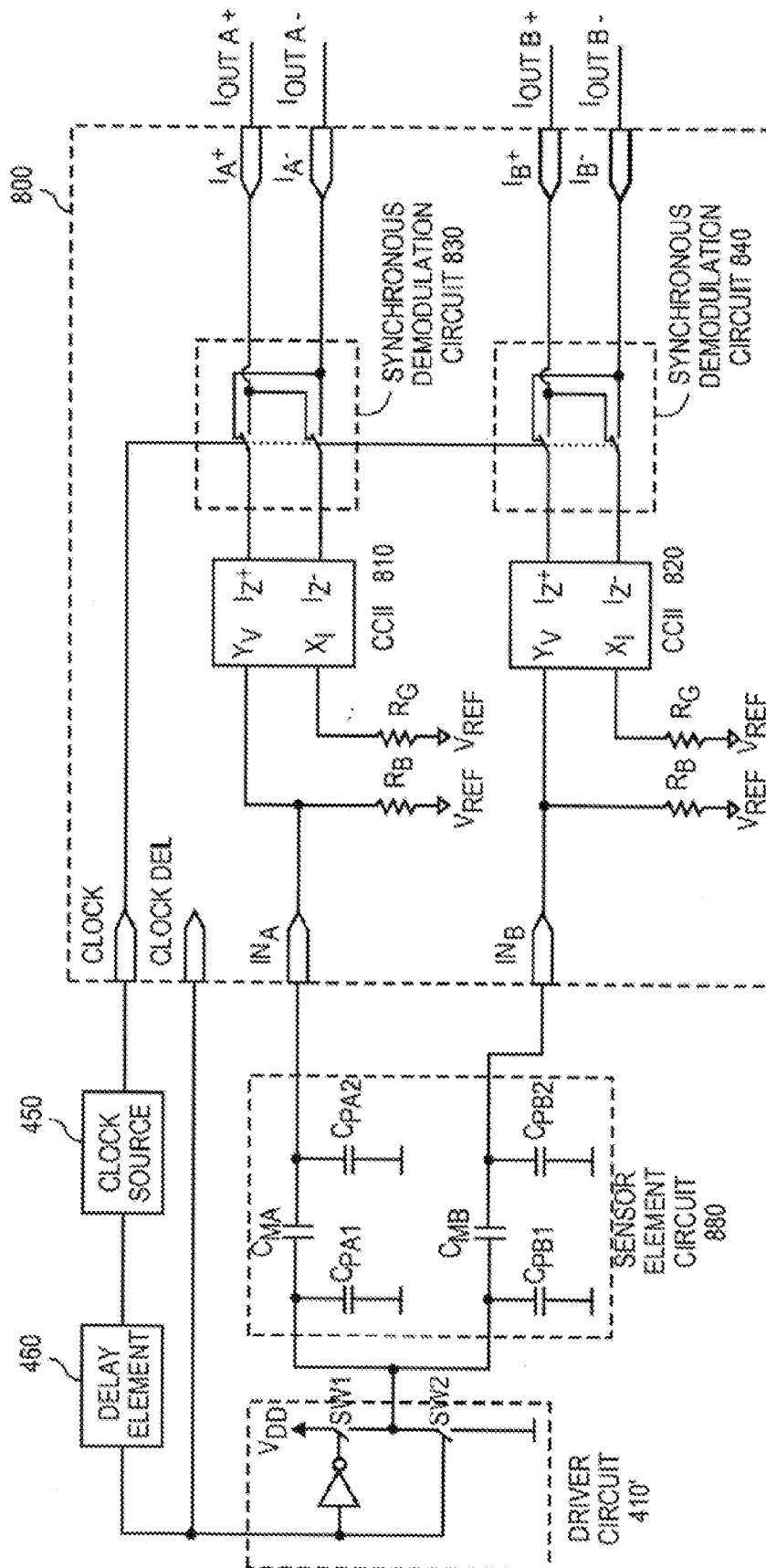


FIG. 8B

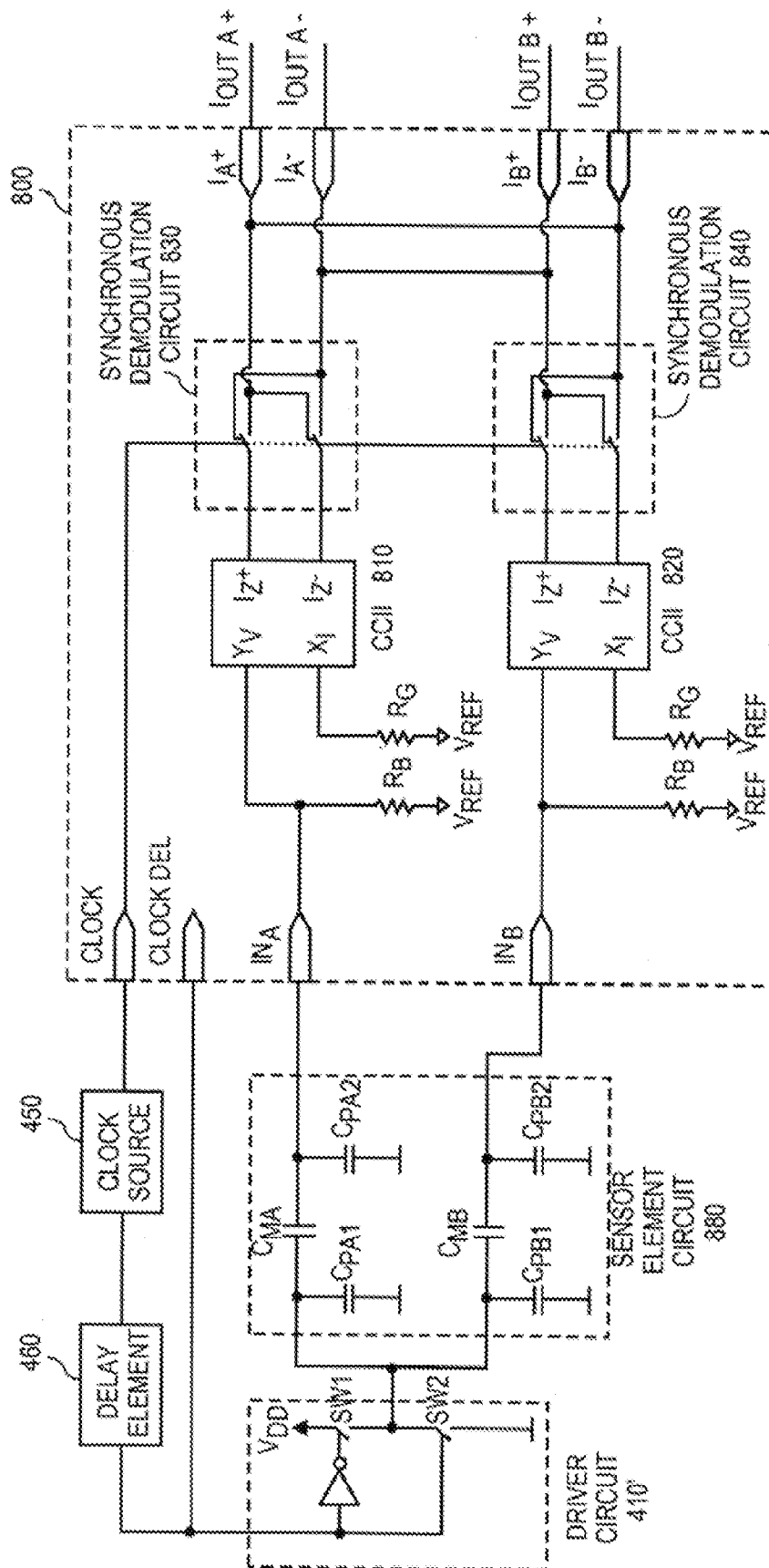


FIG. 8C

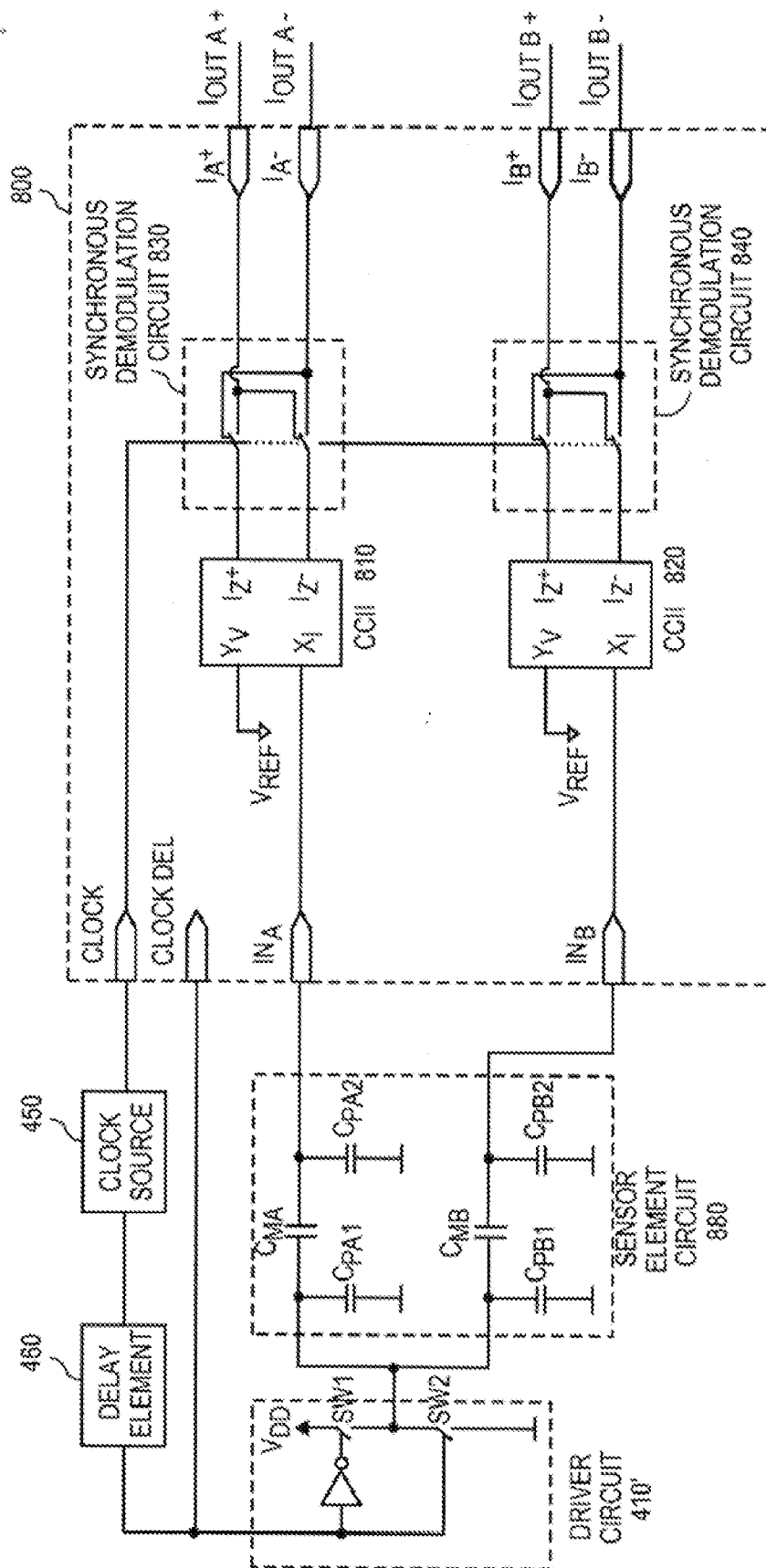


FIG. 8D

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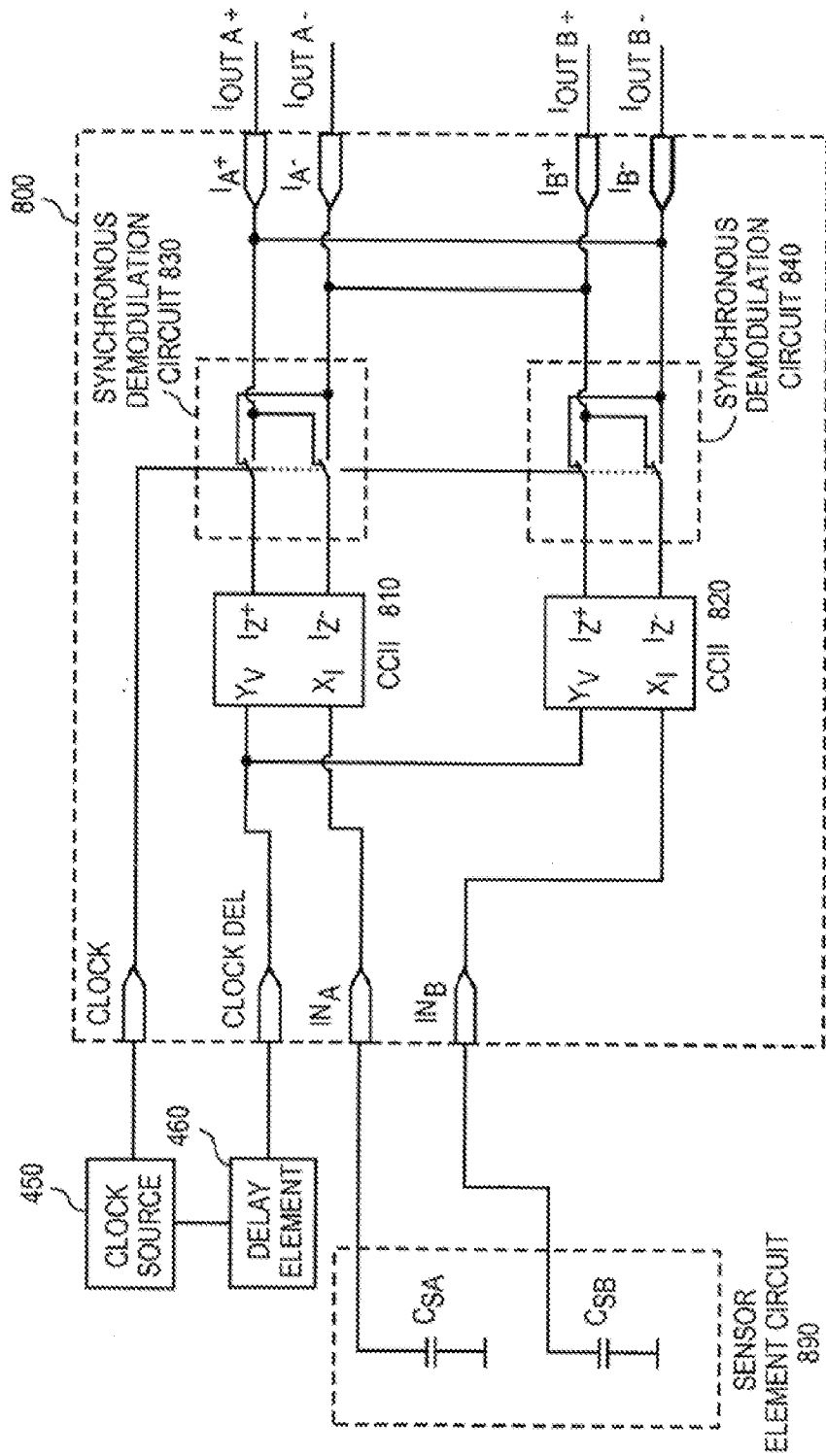


FIG. 8E

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 10/28943

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G01R 27/26 (2010.01)

USPC - 324/658

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

USPC: 324/658

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 324/658,663,686 (text search - see terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PubWEST(USPT,PGPB,EPAB,JPAB); Google

Search Terms: self, mutual, capacitance, sensing, sensor, current, conveyor, dual, mode, electrode, sigma delta, multiplex\$, modulai\$, second generation

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2006/0138574 A1 (SAITO et al.) 29 June 2006 (29.06.2006), entire document especially the Abstract; paras [0004], [0010], [0082], [0100]-[0104], [0107]	1-22
Y	US 2009/0058802 A1 (ORSLEY) 05 March 2009 (05.03.2009), entire document especially paras [0038], [0103]	1-22
Y	WO 2008/085720 A1 (KRAH et al.) 17 July 2008 (17.07.2008), entire document especially paras [0072]-[0073]	1-22
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Date of mailing of the international search report

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