Title: TAPPED TRANSMISSION LINE STRUCTURE, TEST BOARD, AUTOMATED TEST EQUIPMENT AND METHOD FOR PROVIDING SIGNALS TO A PLURALITY OF DEVICES

Abstract: A tapped transmission line structure (1) for providing an electrical connection between a driver terminal (110) and a plurality of device connections (120a, 120b) comprises a main transmission line (130) and a plurality of branching structures (142a, 142b). The branching structures couple the main transmission line (130) with the device connections at different distances (II, 12) from the driver terminal (110) and have associated therewith signal transmission portions. Different of the signal transmission portions are designed to have different signal transmission characteristics in order to counteract differences of signal characteristics at different device connections.

FIG 1
Tapped transmission line structure, test board, automated test equipment and
method for providing signals to a plurality of devices

Background of the invention

Embodiments of the invention are related to a tapped transmission line structure for
providing an electrical connection between a driver terminal and a plurality of device
connections. Other embodiment according to the invention is related to a test board for
coupling a plurality of devices-under-test with an automated test equipment. Further
embodiments according to the invention are related to an automated test equipment. Yet
further embodiments according to the invention are related to methods for providing
signals to a plurality of devices.

Another embodiment is related to a method to improve the signal integrity of testing
multiple high-speed double-data-rate (DDR) memory integrated circuits (IC's) using a
tapped transmission line approach.

In many cases, it is desirable to connect a plurality of devices to a single driver. While this
can be implemented easily for low speed devices, things become more and more difficult
as the speed of the devices and the data rate of the data to be transmitted to the devices
increases. In the following, some concepts will be discussed for connecting a plurality of
memory devices to a driver. However, the present invention is applicable to other devices
as well.

High-speed memory applications, like applications using devices that obey the so-called
"double-data-rate 3" (DDR3) standard, use so-called "stub-series terminated logic" (SSTL)
to connect the various memory integrated circuits in a dual-inline-memory-module
(DIMM) to the memory controller for control lines like "ADDRESS", which is
topologically equivalent to a tapped transmission line structure. For details regarding this
concept, reference is made to Fig. 13.

Fig. 13 shows a schematic representation of an application, in which multiple DRAMs are
coupled to a common memory controller. As can be seen in Fig. 13, an application 1300
typically comprises a memory controller 1310 and a plurality of dynamic-random-access-
memory devices (also briefly designated as DRAMs) 1320a, 1320b, 1320c. Signals are
provided from the memory controller 1310 to the dynamic random access memory devices
1320a, 1320b, 1320c, like, for example, an address signal "ADDRESS_0". Said address signal may be routed from the memory controller 1310 to a first branching point 1340a via a first transmission line portion 1330a. An address input of the first dynamic random access memory device 1320a may be coupled to the first branching point 1340a via an appropriate electrical connection. In addition, a second transmission line portion 1330b typically connects the first branching point 1340a with a second branching point 1340b. An address input of the second dynamic random access memory device 1320b may be connected with the second branching point 1340b via an appropriate electrical connection. Further, an address input of the third dynamic random access memory device 1320c may be coupled with the second branching point 1340b via a third transmission line portion 1330c, and possibly an additional electrical path. The transmission line is terminated by a termination resistor $R_t$ connected to a termination voltage $V_t$.

The type of data bus (or address bus) design shown in Fig. 13 can have significant signal integrity issues for high-data rates (for example above 2 gigabit per second) and/or when there is a large number of integrated circuits that hang on the data bus or address bus (for example 8 integrated circuits instead of 4 integrated circuits).

However, the technology described with reference to Fig. 13 has been successful in the current generation of dual-inline-memory-module (DIMM) designs (for example according to the standard DDR3), and in the context of production test of double-data-rate memories (DDR memories) it has been leveraged as a way to test multiple double-date-rate integrated circuits using a smaller number of automated test equipment channels, as will be discussed taking reference to Fig. 14.

Figs. 14a and 14b show block schematic diagrams of circuit arrangements for production testing of dynamic random access memories (DRAMs). Fig. 14a shows a block schematic diagram of a simple arrangement for a production testing of DRAMs according to a first option. As can be seen, separate automated-test-equipment channels 1410a, 1410b, 1410c can be used to provide separate signals (for example "ADDRESS_0") for the individual dynamic random access memory devices 1420a, 1420b, 1420c, which act as devices-under-test ("dut1", "dut2", "dut3"). However, the concept shown in Fig. 14a is very resource-inefficient and requires a high number of costly automated-test-equipment channels 1410a, 1410b, 1410c.

Fig. 14b shows a block schematic diagram of an arrangement for a more resource-efficient production testing of dynamic random access memories, according to a second option. As
can be seen, a common automated-test-equipment channel 1460 is used to provide a signal (for example "ADDRESS_0") to a plurality of dynamic random access memories 1470a, 1470b, 1470c. The common automated-test-equipment channel 1460 is connected to inputs of the dynamic random access memory devices 1470a, 1470b, 1470c (or, more generally, to inputs of a plurality of devices-under-test) via a common signal transmission structure.

However, it should be noted that there are important signal integrity issues to be solved. In particular, it should be noted that the requirements regarding the signal integrity (and signal predictability) are much more demanding in the test of devices than in the normal operation of devices. It should be noted that some techniques have been developed to improve the signal integrity on the so-called "SSTL" ("stub-series terminated logic") interface for a dual-inline-memory-module, but it should also be noted that these techniques are very simplistic in their approach and not targeted to integrated circuit production testing.

In the following, a simple architecture and the problems associated therewith will be described taking reference to Fig. 15. Fig. 15 shows a schematic diagram with an automated-test-equipment configured for testing a plurality of devices-under-test (in the following also designated as "duts"). As can be seen in Fig. 15, an automated-test-equipment driver 1510 is connected to a driver terminal 1522 of a tapped transmission line 1520 having a plurality of transmission line segments 1520a, 1520b, 1520c, 1520d with branching points 1524a, 1524b, 1524c in between adjacent transmission line segments. An end 1526 of the transmission line 1520 is terminated, i.e. connected to a termination voltage $V_t$ via a termination resistor $R_{t,\text{rm}}$.

The first branching point 1524a is coupled to a dut input 1540a of a first dut 1542a via an electrically conducting structure, which may comprise a via 1530a. A dut input 1540b of a second dut 1542b is coupled with the second branching point 1524b via an electrically conducting structure 1530b. Similarly, a dut input 1540c of a third device-under-test 1542c is coupled with the third branching point 1524c via an electrically conducting structure 1530c.

An electrical behavior of the dut inputs 1540a, 1540b, 1540c of the duts 1542a, 1542b, 1542c may be modeled, for example, using a series connection of an inductance, a resistance and a capacitance, thereby describing an inductance of any connections (for example package pads, bond wires and so on), an unavoidable parasitic series resistance and an input capacitance of input transistors.
The challenge with a tapped transmission line approach for double-data-rate testing (DDR testing) is that multiple device pins (for example inputs 1540a, 1540b, 1540c) are connected to a single automated test equipment (ATE) driver 1510, and that each device-under-test input 1540a, 1540b, 1540c is not terminated (or not terminated with an appropriate impedance to avoid reflections), so that there is no amplitude reduction (or only a limited amplitude reduction). This in turn creates several reflections that travel across the entire signal path until they are absorbed by the automated test equipment driver 1510 or the termination $R_{term}$ at the end 1526 of the signal path 1520a, 1520b, 1520c, 1520d. The reflections will become worse with additional devices-under-test or faster rise times associated with higher data rates. Second, signals launched from the ATE driver are attenuated on the way to the termination, due to the dut-taps themselves, as well as resistive loss, skin effect loss and dielectric loss. The reflections and attenuations cause different signals to appear at each dut which leads to the fact that each dut 'sees' a different signal and therefore behave differently, which makes correlation of the dut's test-results very difficult.

For details, reference is made to Fig. 15.

In view of the above discussion, there is a need for a concept which allows for an improvement of the signal integrity in an environment in which multiple device inputs are connected to a common driver.

**Summary of the invention**

This problem is solved by a tapped transmission line structure according to claim 1, a test board according to claim 10 or claim 13, an automated test equipment according to claim 14 and a method according to claim 17.

An embodiment according to the invention creates a tapped transmission line structure for providing an electrical connection between a driver terminal and a plurality of device connections. The tapped transmission line structure comprises a main transmission line and a plurality of branching structures coupling the main transmission line with the device connections at different distances from the driver terminal. The branching structures have associated therewith respective signal transmission portions. Different of the signal transmission portions are designed to have different signal transmission characteristics in order to counteract differences of signal characteristics at different device connections.
It is the key idea of the present invention that a signal integrity, for example a signal uniformity across multiple device connections, can be improved by providing a plurality of different signal transmission portions, each associated with one of the branching structures. In this way, it can be achieved that differences of signal characteristics (for example rise times, or eye-openings), which conventionally appear at device inputs of devices connected to a tapped transmission line at different distances from the driver terminal of the tapped transmission line, are reduced by the differences of the signal transmission portions associated with the different branching structures.

Accordingly, the different signal transmission portions associated with the different branching structures may, for example, be configured to at least partially compensate for a degradation of rise times of signals traveling along the main transmission line, thereby resulting in more uniform signals at inputs of different devices coupled to the main transmission line.

Also, the different signal transmission portions associated with the different branching structures may, for example, be configured to at least partially compensate for a degradation of an eye opening of a data signal at a remote device connection when compared to an eye opening at a closer device connection (wherein it is assumed that the remote device connection is electrically further away from the driver terminal than the closer device connection).

Accordingly, the inventive concept improves the signal degradation in a tapped transmission line approach to test multiple DDR memory duts with a reduced number of channels. Thus, the inventive concept generally allows to connect multiple devices to a common driver. When applied on a test board of an automated test equipment, the inventive concept allows to test multiple devices, for example, double data rate memory devices, with a reduced number of channels. Also, in some cases the inventive approach allows to test devices at higher data rate when compared to a conventional approach.

Typically, the inventive concept improves the correlation of signals at different DUT connections. For testing multiple devices in parallel it is critical that the signal at all DUT's is (at least approximately) the same, i.e. having some DUT's receiving a good performance signal and some a bad performance signal is not acceptable for production testing. All DUT's need to receive (at least approximately) the same signal quality even if that means degrading the signal for some of the DUT's.
In embodiments of the invention, the different characteristics of the signal transmission portions contribute to obtaining a balance between the signal characteristics at different duty cycles, thereby counteracting differences of signal characteristics at different device connections.

Further details and advantages of the inventive concept will subsequently be described taking reference to specific embodiments.

Another embodiment according to the invention creates a test board for coupling a plurality of devices-under-test with an automated test equipment. The test board comprises a plurality of device-under-test sockets for contacting the devices-under-test. The test board also comprises a tapped transmission line structure as discussed above. The tapped transmission line structure is configured to forward a signal from the automated test equipment (or an automated test-equipment interface) to a plurality of the device-under-test sockets.

Another embodiment according to the invention creates a test board coupling a plurality of devices-under-test with an automated test equipment. The test board comprises a plurality of device-under-test and a tapped transmission line structure as discussed above. The branching structures of the tapped transmission line structure are configured to couple inputs of a plurality of the devices-under-test to the main transmission line. A signal transmission portion of a first branching structure is configured to form a first low pass filter with an input capacitance of an input of a first device-under-test, which is coupled to the main transmission line via the first branching structure. A signal transmission portion of a second branching structure is configured to form a second low pass filter with an input capacitance of an input of a second device-under-test, which is coupled to the main transmission line via the second branching structure. The time constant of the first low pass filter is larger than the time constant of the second low pass filter, and a first branching point, at which the first branching structure branches from the main transmission line, is closer to the driver terminal than a second branching point, at which the second branching structure branches from the main transmission line.

The discussed test board allows to exploit the input capacitances of the devices-under-test such that the complexity of the branching structure can be kept low. Also, by using a first low pass filter having a higher time constant in the proximity of the driver terminal and a
second low pass filter having a smaller time constant at a larger distance from the driver terminal, the degrading impact of the main transmission line and the branching structures on the signal integrity (causing a variation of signal characteristics across the devices) can be compensated at least partially. In other words, the different time constants of the low pass filters counteract differences of the signal characteristics at different device connections, which would occur in the absence of filters having different time constants or in the presence of identical filters.

Another embodiment according to the invention creates an automated test equipment comprising a test board, as discussed before. The automated test equipment is configured to test in parallel a plurality of devices-under-test attached to the test board. For this purpose, the automated test equipment is configured to apply a test signal to the tapped transmission line structure having a bit rate of larger than 1 gigabit per second. In such a test system, the advantages of the inventive tapped transmission line structure bring along a significant improvement of the signal integrity, because the inventive concept is particularly efficient for high bit rates and fast rise times.

Another embodiment according to the invention creates a method for providing signals to a plurality of devices using a common main transmission line, to which devices are coupled via a plurality of branching structures. The method comprises forwarding a signal from a driver terminal to a first of the devices via the main transmission line and a first branching structure coupling the first device to the main transmission line. The method also comprises forwarding the signal from the driver terminal to a second of the devices via the main transmission line and a second branching structure coupling the second device to the main transmission line. When being forwarded, the signal is shaped by a first signal transmission portion associated with the first branching structure and by a second signal transmission portion associated with the second branching structure, such that the signal shaping by the first signal transmission portion and by the second signal transmission portion counteracts differences of signal characteristics at different device connections.

This method realizes the advantages discussed above.

**Brief description of the figures**

Fig. 1 shows a schematic representation of a tapped transmission line structure, according to a first embodiment of the invention;
Fig. 2a shows a schematic representation of a test board, according to a second embodiment of the invention;

Fig. 2b shows a schematic representation of a test board, according to a third embodiment of the invention;

Fig. 3 shows a schematic representation of an automated test equipment, according to a fourth embodiment of the invention;

Fig. 4 shows a schematic representation of a tapped transmission line structure, according to a fifth embodiment of the invention;

Figs. 5a, 5b, 5c show schematic representations of structural elements for the implementation the signal transmission portions;

Fig. 6 shows a schematic representation of a tapped transmission line structure, according to a sixth embodiment of the invention;

Fig. 7 shows a schematic representation of a tapped transmission line structure, according to a seventh embodiment of the invention;

Fig. 8 shows a graphical representation of eye-diagrams of signals at different device connections in the absence of signal shaping resistors;

Fig. 9 shows a graphical representation of eye-diagrams of signals at different device connections in the presence of signal shaping resistors;

Fig. 10 shows a schematic cross-sectional view of a test arrangement, according to an embodiment of the invention;

Fig. 11 shows a three-dimensional view of a test board and an interposer board, according to an embodiment of the invention;

Fig. 12 shows a graphical representation of eye-diagrams at different signal connections in the absence of a interposer and in the presence of an interposer;
Fig. 13 shows a schematic representation of a topology for connecting dynamic random access memories to a memory controller;

Fig. 14 shows a schematic representation of different approaches for a production testing of dynamic random access memories;

Fig. 15 shows a schematic representation of a transmission line structure for connecting devices to a driver; and

Fig. 16 shows a schematic representation of a Y-shaped tapped transmission line structure, according to an embodiment of the invention.

**Detailed description of the embodiments**

**Embodiment according to Fig. 1**

Fig. 1 shows a schematic representation of a tapped transmission line structure 100, according to a first embodiment of the invention. The tapped transmission line structure 100 is configured for providing an electrical connection between a driver terminal 110 and a plurality of device connections 120a, 120b. The tapped transmission line structure comprises a main transmission line 130 and a plurality of branching structures 140a, 140b coupling the main transmission line 130 with the device connections 120a, 120b at different distances \( l_1, l_2 \) from the driver terminal 110.

The branching structures 140a, 140b have associated therewith signal transmission portions. For example, the first branching structure 140a has associated therewith a signal transmission portion 142a and/or a signal transmission portion 144a. Similarly, the second branching structure 140b has associated therewith a signal transmission portion 142b and/or a signal transmission portion 144b. Generally speaking, the one or more signal transmission portions 142a, 144a associated with the first branching structure 140a may be part of the first branching structure 140a, or may be adjacent to the first branching structure 140a. As can be seen, the signal transmission portion 142a is part of the branching structure 140a. The signal transmission portion 144a is arranged in an environment of a branching point, at which the branching structure 140a branches from the main transmission line 130. However, it should be noted that the presence of one of the signal transmission portions 142a, 144a associated with the first branching structure 140a is sufficient. Nevertheless, both signal transmission portions may be present simultaneously.
in an embodiment. Similarly, one or more signal transmission portions 142b, 144b are associated with the second branching structure 140b. As can be seen, the signal transmission portion 142b may be part of the branching structure 140b. Alternatively, the signal transmission portion 144b may be arranged in an environment of a branching point, at which the second branching structure 140b branches from the main transmission line 130.

Moreover, it should be noted that different signal transmission portions 142a, 144a, 142b, 144b are designed to have different signal transmission characteristics in order to counteract differences of signal characteristics at different device connections 120a, 120b. In other words, the signal transmission portion 142a associated with the first branching structure 140a may comprise different signal transmission characteristics when compared to the signal transmission portion 142b, which is associated with the second branching structure 140b. Similarly, the signal transmission portions 144a, 144b, which are associated with the first branching structure 140a and the second branching structure 140b, may optionally comprise different transmission characteristics (if the signal transmission portions 144a, 144b are present).

Regarding the functionality of the tapped transmission line structure 100, it should be noted that the tapped transmission line structure 100 typically forwards a signal from the driver terminal 110 to the first device connection 120a and to the second device connection 120b. However, the first branching structure 140a branches from the main transmission line 130 at a distance \( l_1 \) from the driver terminal 110, while the second branching structure 140b branches from the main transmission line 130 at a distance \( l_2 \) from the driver terminal 110.

Assuming now - as a comparison example - that the first branching structure 140a and the second branching structure 140b were identical, it is easy to understand that a signal component arriving at the second device connection 120b in response to a signal injected at the driver terminal 110 would be more severely degraded by imperfections of the tapped transmission line structure than a signal component arriving at the first device connection 120a. This is due to the fact that the propagation along the main transmission line 130 brings along a certain frequency-dependent attenuation, which tends to degrade edges (for example by increasing the rise time). Accordingly, the degradation would increase with increasing propagation length along the main transmission line 130. In addition, the signals arriving at the second device connection 120b are also degraded by signal reflections occurring, for example, at the first device connection 120a. Accordingly, it can be said that the signal characteristics (for example a steepness of the edges, or an eye-opening) would
be significantly worse for a signal arriving at the second device connection 120b when compared to signals arriving at the first device connection 120a.

However, according to the present invention, the signal transmission portions (for example signal transmission portions 142a, 142b and/or signal transmission portions 144a, 144b) are designed to be different (i.e. to have different signal transmission characteristics), such that a signal component propagating from the driver terminal 110 to the first device connection 120a is affected (or shaped) differently by the signal transmission portion 142a (and/or by the signal transmission portion 144a) when compared to a shaping, by means of the signal transmission portion 142b (and/or the signal transmission portion 144b), of a signal component traveling from the driver terminal 110 to the second device connection 120b.

For example, the signal transmission portion 142a of the first branching structure 140a may be configured to reduce a steepness of edges by more than the signal transmission portion 142b of the second branching structure 140b. Alternatively, or in addition, the signal transmission portion 142a may be configured to effect a stronger reduction of an eye-opening than the signal transmission portion 142b. Alternatively, or in addition, the signal transmission portion 142a may be configured to attenuate the signal component traveling from the driver terminal 110 to the first device connection 120a more than the signal transmission portion 142b attenuates a signal component traveling from the driver terminal 110 to the second device connection 120b. One or more of the above mentioned characteristics of the signal transmission portions 142a, 142b are adapted to counteract differences of signal characteristics at the different device connections 120a, 120b (for example in comparison to a case in which the branching structures have identical signal transmission characteristics).

In a preferred embodiment, different branching structures 140a, 140b comprise, as the signal transmission portions 142a, 142b (or as a part of the signal transmission portions), resistors of different resistances circuited in series between the main transmission line 130 and the device connections 120a, 120b. By doing so, it is possible to implement low pass filters of different time constants. Accordingly, it is possible to adapt a signal rise time (or an eye opening) seen at the second device connection 120b to a signal rise time (or an eye opening) seen at the first device connection 120a, thereby counteracting a difference of rise time (or eye openings) at the first and second device connections 120a, 120b when compared to the situation in the absence of different signal transmission portions.
In another preferred embodiment, a series resistor of a signal transmission portion 142a of the first branching structure 140a, which branches from the main transmission line 130 at a first branching point, comprises a larger resistance (for example by at least 10% larger, or even by at least 30% larger, or even by 100% larger) than a series resistor of the signal transmission structure 142b of a second branching structure 140b, which branches from the main transmission line 130 at a second branching point, wherein the second branching point is electrically spaced further away from the driver terminal 110 than the first branching point. By choosing a smaller series resistor in the branching structure 140b, which is further away from the driver terminal 110 (when compared to resistor of a branching structure 140a closer to the driver terminal 110), a signal edge degradation which increases with increasing propagation length, can be at least partially compensated, thereby counteracting differences of the signal characteristics (edge steepness and/or eye opening) at the different device connections 120a, 120b.

In a further preferred embodiment, the signal transmission portions 142a, 142b of the branching structures 140a, 140b comprise low pass filters circuited between the main transmission line 130 and the device connections 120a, 120b. The time constants of the low pass filters decrease with increasing electrical distance \( l_1, l_2 \) of the branching points, at which the branching structures 140a, 140b branch from the main transmission line 130, from the driver terminal 110.

It should be noted here that in some embodiments, the different signal transmission characteristics of the different signal transmission portions 142a, 142b may be obtained by using different resistors for obtaining different low pass filters, depending on the requirements. If only different resistors are used, low pass filter characteristics may be obtained in combination with input capacitances of devices connected to the device connections 120a, 120b. However, if it is not desired to rely on the input capacitances of the devices, complete low pass filters may also be used to implement the signal transmission portions 142a, 142b.

In a preferred embodiment, the tapped transmission line structure further comprises a high pass filter arranged between the driver terminal 110 and a first branching point, at which the first branching structure 140a (when seen from the driver terminal 110) branches from the main transmission line 130. The high pass filter is preferably configured to at least partially compensate for an effect of the one or more low pass filters.

In such an arrangement, the effect of the low pass filter in the first branching structure 140a can be partially compensated, such that a degradation of an edge steepness caused by
the low pass filter of the first branching structure 140a is at least partially compensated. Accordingly, steep edges can be observed at the first device connection 120a even in the presence of a low pass filter (circuited into the first branching structure 140a).

In a preferred embodiment, the high pass filter is an equalization-type high pass filter configured to reduce a rise time of a signal.

In a preferred embodiment, the signal transmission portions 144a, 144b associated with the branching structures 140a, 140b comprise portions of the main transmission line 130 arranged adjacent to (or in an environment of) branching points, at which the branching structures 140a, 140b branch from the main transmission line 130. The portions of the main transmission line comprise an increased impedance when compared to the rest of the main transmission line. Using such signal transmission portions, an effect of an additional capacitance (in particular a reflection of signals), which occurs at the branching point, can be reduced.

In some embodiments, the signal transmission portions 142a, 142b associated with the branching structures comprise vias extending from the transmission line to another layer of a multi-layer circuit board, and pads in an electrical contact with the vias, thereby forming capacitances. By introducing capacitances into the branching structures 140a, 140b, the desired low pass characteristic of the branching structures 140a, 140b can be obtained, wherein the low pass filter time constant of the different branching structures 140a, 140b may be chosen differently, such that the branching structure 140a, which is closer to the driver terminal 110, comprises a longer low pass filter time constant than the branching structure 140b, which is further away from the driver terminal 110.

Embodiment according to Fig. 2a

Fig. 2a shows a schematic representation of a test board 200 for coupling a plurality of devices-under-test with an automated test equipment. The test board 200 comprises a plurality of device-under-test sockets 210a, 210b for contacting the devices-under-test. The test board 200 also comprises a tapped transmission line structure 100, as discussed above. The tapped transmission line structure is configured to forward a signal from the automated test equipment (received, for example, at the driver terminal 110) to a plurality of the device-under-test sockets 210a, 210b.

In a preferred embodiment, the test board 200 comprises an interposer-type printed circuit board arranged between a main printed-circuit board carrying the main transmission line
130 and at least one of the device-under-test sockets 210a, 210b. In this case, the branching structure 140a coupling a pad of the device-under-test socket 210a with the main transmission line 130 comprises a vertical resistor extending between a first surface of the interposer-type printed-circuit-board and a second opposite surface of the interposer-type printed-circuit-board, thereby electrically coupling a surface of the main printed-circuit-board with the device-under-test socket 210a. Details regarding this arrangement will be described later on taking reference to Fig. 10.

Embodiment according to Fig. 2b

Fig. 2b shows a schematic representation of a test board 250 for coupling a plurality of devices-under-test 260a, 260b with an automated test equipment. Test board 250 comprises the devices-under-test 260a, 260b. The test board also comprises a tapped transmission line structure 100, as discussed above. The branching structures 140a, 140b of the tapped transmission line structure are configured to couple inputs 262a, 262b of a plurality of the devices-under-test 260a, 260b to the main transmission line 130. A signal transmission portion 142a of the first branching structure 140a is configured to form a first low pass filter with an input capacitance of the input 262a of the first device-under-test 260a, which first device-under-test is coupled to the main transmission line 130 via the first branching structure 140a. A signal transmission portion 142b of the second branching structure 140b is configured to form a second low pass filter with an input capacitance of the input 262b of a second device-under-test 260b, which second device-under-test is coupled to the main transmission line 130 via the second branching structure 140b. A time constant of the first low pass filter is larger than a time constant of the second low pass filter, wherein a first branching point, at which the first branching structure 140a branches from the main transmission line 130, is closer to the driver terminal 110 than a second branching point, at which the second branching structure 140b branches from the main transmission line 130.

Within this concept, the input capacitances of the devices-under-test 260a, 260b are exploited for the implementation of different signal transmission characteristics to counteract differences of signal characteristics (e.g. rise times or eye-openings) at device connections (or inputs 262a, 262b) of the different devices-under-test 260a, 260b.

In a preferred embodiment, inputs of one or more of the devices-under-test (e.g. the input of the dut 260a) are coupled to the main transmission line 130 via one or more branching structures (e.g. the branching structure 140a) branching from the main transmission line 130 comparatively closer to the driver terminal 110. In this embodiment, inputs of one or more of the devices-under-test (e.g. the input 262b of the dut 260b) are coupled to the main
transmission line 130 via one or more branching structures (e.g. the branching structure 140b) branching from the main transmission line 130 comparatively further away from the driver terminal 110. The one or more branching structures 140a branching from the main transmission line comparatively closer to the driver terminal 110 comprise a series resistance larger than 20 Ohm, and the one or more branching structures 140b branching from the main transmission line 130 comparatively further away from the driver terminal 110 comprise a series resistance smaller than 4 Ohm. In this embodiment, the significant difference of the series resistances of the branching structures helps to counteract differences of the signal characteristics at different device connections. It has been found, that for devices being coupled to the main transmission line 130 comparatively closer to the driver terminal 110, it is important to reduce reflections and to slow down the rise time. In contrast, for devices coupled with the main transmission line 130 further away from the driver terminal 110, it is preferred to avoid a slow down of the rise time and it is also not necessary to attenuate reflections as strongly as it is desired closer to the driver terminal. Accordingly, a strong difference of the series resistances has shown to bring along well-balanced signal characteristics at inputs of different devices-under-test.

In a preferred embodiment, the devices-under-test 260a, 260b are double-data-rate memory devices, wherein double-data-rate inputs are coupled to the transmission line structure 100.

**Embodiment according to Fig. 3**

Fig. 3 shows a schematic representation of an automated test equipment, according to an embodiment of the invention. The automated test equipment 300 comprises an automated test equipment channel 310 and a test board 320. The test board 320 may be identical to the test board 200 described with reference to Fig. 2a or the test board 250 described with reference to Fig. 2b. An output driver 312 of the automated test equipment 210 may, for example, be coupled with the driver terminal 110 of the main transmission line 130 via a so-called "POGO PIN" connection 316. In addition, there may be additional connections between outputs of the devices-under-test and the automated test equipment, thereby allowing a test of the devices. However, the automated test equipment 300 is preferably configured to test in parallel a plurality of devices-under-test attached to test board 320. Also, the automated test equipment is preferably (but not necessarily) configured to apply a test signal to the tapped transmission line structure 100 having a bit rate of larger than one gigabit per second. Accordingly, the automated test equipment 300 as a whole is capable of a reliable parallel testing of a plurality of devices-under-test even at high bit rates.
Embodiment according to Fig. 4

In the following, a tapped transmission line structure 400 will be described taking reference to Fig. 4. The tapped transmission line structure 400 is based on the transmission line structure 1500 shown in Fig. 15.

However, as discussed above, the reflections become bad with additional devices-under-test or faster rise times (associated with higher data rates) in the transmission line structure 1500 of Fig. 15. Nevertheless, since there is a significant advantage in being able to test a higher number of duts at higher data rates using the approach discussed with reference to Fig. 15, and given the fact that in a double-data-rate (DDR) production test board there is more freedom and less cost pressures than on a dual-inline-memory-module design for an end user application, it is possible to use a more complex design to improve the signal integrity. According to the invention, it has been found that it is an advantageous approach to design a series of filters that can be (or are) added after the automated test equipment driver and before each device-under-test coupled to a tapped transmission line.

In the following, some details regarding this approach will be discussed with reference to Fig. 4. The tapped transmission line structure 400 shown in Fig. 4 comprises a main transmission line 430, which comprises a plurality of main transmission line segments 430a, 430b, 430c, 430d. A first main transmission line segment 430a is circuited between a driver terminal 432 of the tapped transmission line structure and a first branching point (or branching node) 434a. At the first branching point 434a, a branching structure 436a branches from the main transmission line 430, wherein the main transmission line 430 continues from the first branching point 434a via a second main transmission line segment 430b. The branching structure 436a, which couples a device input 442a of a first device 440a with the branching point 434a, comprises a filter 450 and, optionally, a via 452. The filter 450 and the optional via 452 are circuited in series between the branching point 434a and the device input 442a.

An additional branching point 434b is arranged further downstream the main transmission line 430, for example between a third main transmission line segment 430c and an (optional) fourth transmission line segment 430d. The second branching point 434b is coupled to an input 442b of a second device 440b using a second branching structure 436b.

The second branching structure 436b comprises a filter 460 and, optionally, a via 462. The filter 460 and the optional via 462 are circuited in series between the branching point 434b and the input 442b of the device 440b.
In addition, the main transmission line 430 may be terminated. For example, an end 433 of
the main transmission line 430 may be coupled to a termination potential \( V_e \) using a
termination resistor \( R \).

Moreover, the tapped transmission line structure may optionally comprise an equalization
filter 470, which may be circuited between the driver terminal 430 and the first branching
point 444a. However, the equalization filter 470 may also be part of a driver driving the
tapped transmission line structure.

In the following, details regarding the filters 450, 460 and the functionality thereof may be
described. It should be noted here that the filter 450, which is included in the first
branching structure 436a, is preferably a low pass filter. Accordingly, a frequency
transmission in response is typically monotonically decaying with increasing frequency,
such that the filter 450 comprises a low insertion attenuation for low frequencies and an
increasing insertion attenuation for increasing frequencies. Similarly, the filter 460 is
preferably a low pass filter comprising an insertion loss that increases with frequency.

However, the filter 450 of the first branching structure 436a typically comprises a longer
low pass filter time constant (or smaller cutoff frequency) than the low pass filter 460 of
the second branching structure 436b. A low pass filter time constant is defined as a delay
time after which an output of the low pass filter reaches a predetermined percentage (e. g.
50 % or 63 %) of an input signal value for a step signal applied at the filter input. In other
words, it is preferred that a threshold frequency (e. g. a 3dB threshold frequency, or a 6dB
threshold frequency, or a 10dB threshold frequency or a 20dB threshold frequency) of the
filter 450 of the first branching structure 436a is lower than the corresponding threshold
frequency of the filter 460 of the second branching structure 436b. In this way, it can be
achieved that signals arriving at the dut inputs 442a, 442b comprise similar signal
characteristics.

Optionally, the high pass filter 470 further contributes to an improvement of signal
characteristics of signals arriving at the device inputs 442a, 442b. For example, the filter
470 may comprise a high pass characteristic, such that a predetermined range of higher
frequencies is emphasized over a range of lower frequencies. For example, there may be a
first frequency range, ranging from DC to a first given frequency, in which the filter 470
may comprise an approximately constant amplitude transmission. There may be a second
frequency range following (in a direction of increasing frequency) the first frequency
range, in which second frequency range the filter 470 exhibits an emphasized amplitude
response, which is larger than the amplitude response in the first frequency range. For
frequencies above the second frequency range, the amplitude response of the filter 470 may decay. Accordingly, the filter 470 may be considered as an equalization-type high pass filter, which is configured to reduce rise times of signal transitions.

5 Filter implementation

In the following, some details regarding the implementation of the filters as described above will be explained. It should be noted that it is very critical how these filters are implemented, since large structure will tend to degrade the signal integrity much more than any possible benefit from the filters 450, 460. It is preferred to do the filter design using techniques that do not imply a large performance price.

Some of those techniques are to change the thickness of the signal trace (for example of the main transmission line 430) before the via (e.g. before the via 452, or before the via 462) to the device (or device-under-test) 440a, 440b to either add inductance or capacitance, to add copper pads on the via 452, 462 to add capacitance, or to add a series resistor to the via 452,462 by using an embedded passive on the printed circuit board.

Naturally, the above techniques (changing the thickness of the signal trace before the via, adding a copper pad to the via, adding a series resistor to the via) which will be explained in detail taking reference to Figs. 5a, 5b and 5c, can also be combined.

Fig. 5a shows a schematic representation of a first technique for implementing a filter, for example the filter 450 or the filter 460. As can be seen in Fig. 5, the first segment 430a of the main transmission line 430 may comprise a width Wo. Also, a second segment 430b of the main transmission line 430 may comprise the same width Wo. However, in an environment 510 of the via 452, which couples the branching point 434a to the device input 442a, the width of the main transmission line 430 may be reduced to a width W_{ext} over a length l_{int}. This reduction of the width of the main transmission line 430 in the environment of the branching point 434a may effectively act as a series inductance circuited between the first main transmission line segment 430a and the branching point 434a, and also as a series inductance circuited between the branching point 434a and the second main transmission line segment 430b. Similarly, another narrowed portion of the main transmission line may be arranged in an environment 512 of the second branching point 434b, if desired.

Another technique to implement the filters 450, 460 is to add a pad to one or more to the vias 452, 462, which brings along an additional capacitance. For example, a copper pad
540, which is electrically coupled to the via 452, may be added. Accordingly, the via 452, or at least a portion thereof, may be electrically in between the pad 540 and the main transmission line 430. Accordingly, the via 452 (or the portion of the via 452) may act as an inductance, which is circuited between the main transmission line 430 and the capacitance constituted by the pad 540. Accordingly, the combination of the via 452 and the pad 540 may act as a low pass filter structure (also designated as a "signal transmission portion" herein).

A further technique to implement the filters 450, 460 is shown in Fig. 5c. As can be seen, the branching point 434a is connected to the device input 442a using a via 452, which via is considered to establish a "vertical" connection through one or more printed circuit board layers, approximately perpendicular to a plane, in which the main transmission line extends. The via 452 comprises a resistor (or dedicated resistor) 570. A resistance of the resistor 570 may be chosen such that the specific resistance (per unit length) of the resistor 570 is at least by a factor of 10 larger than a specific resistance of a normal low-resistance via material. Typically, a resistance of the resistor 570 is larger than 5 Ohms, or even larger than 10 Ohms, which is significantly higher than a "normal" resistance of a "good" via. However, the resistor 570 may act, in combination with an additional capacitance (e.g. as shown in Fig. 5b, or implemented by the input capacitance of a device), as a low pass filter.

It should be noted here that the techniques shown with respect to Figs. 5a, 5b and 5c can be combined in order to implement the filters 450, 460. However, in other embodiments a single one of the concepts shown in Figs. 5a, 5b and 5c may be sufficient to implement the different signal transmission portions discussed above. Also, in some cases, different of the concepts of Figs. 5a, 5b and 5c may be applied for different signal transmission portions associated with different branching structures (or different devices). Also, in some embodiments completely different concepts may be used to implement the signal transmission portions associated with the branching structures.

**Embodiment according to Fig. 6**

Fig. 6 shows a schematic representation of a tapped transmission line structure 600, according to a sixth embodiment of the invention.

It should be noted here that the general typology of the transmission line structure 600 of Fig. 6 is very similar to the typology of the transmission line structure 400 of Fig. 4.
Accordingly, identical reference numerals will be used for identical features. Accordingly, reference is made to the above description for the sake of brevity.

As can be seen in Fig. 6, the optional filter 470, which has been described with reference to Fig. 4, can be omitted. Also, it can be seen from Fig. 6 that the vias 452, 462, which have been described with reference to Fig. 4, can be omitted in some cases. The filter 450 can be replaced by a low pass filter 650, and the filter 460 can be replaced by a low pass filter 660. Thus, the low pass filter 650 is circuited between the branching point 434a and the device input 442a of the first device 440a. Similarly, the low pass filter 660 is circuited between the branching point 434b and the device input 442b of the second device 440b.

The structure of Fig. 6 addresses the finding that in the case of a tapped transmission line structure to test multiple double-data-rate memories, the challenge is that the first (one or more) devices under test after the automated test equipment driver 431 (for example the first dut 440a) will (conventionally) see a much faster rise-time than the devices under test at the end 433 (or in the proximity of the end 433) of the tapped transmission line 430 (for example the dut 440b).

However, it has been found that, when testing several devices, it is desirable to provide well-controlled and (at least approximately) identical conditions (e.g. signal characteristics) to a plurality of devices, such that the testing conditions (e.g. signal characteristics) are well reproducible and (at least approximately) identical for any devices.

One approach to solve this issue using the technique described in Fig. 4 is to add a low pass filter 650, 660 before each dut 440a, 440b with the low pass filter time constant being reduced as we move to the end 433 of the tapped transmission line. For details, reference is made, for example, to Fig. 6.

Specific reference is also made to a graphical representation of the frequency behavior of the low pass filters 650, 660. A frequency response of the first low pass filter 650 is shown in a graphical representation at reference numeral 652, and a frequency response of the second low pass filter 660 as shown in a graphical representation at reference numeral 662. An abscissa 652a describes a frequency, and an ordinate 652b describes an amplitude response. Similarly, an abscissa 662a describes the frequency and an ordinate 662b describes the amplitude response. Curves 652c, 662c describe the evolution of the amplitude responses over the frequency for the filters 650, 660. As can be seen, the second low pass filter 660 is configured to have a higher bandwidth than the first low pass filter
In other words, the amplitude response of the first low pass filter 650 decays faster with frequency than the amplitude response to the second filter 660.

**Embodiment according to Fig. 7**

In the following, a possible implementation will be described in detail taking reference to Fig. 7. As the tapped transmission line structure 700 of Fig. 7 is very similar to the tapped transmission line structure 600 of Fig. 7, identical reference numerals are used to designate identical features.

As can be seen, the tapped transmission line structure 600 comprises a main transmission line 430, which comprises a plurality of main transmission line segments 430a-430d. As can also be seen in Fig. 7, a resistor $R_i$ and a via 750 are circuited in series between the branching point 434a and an input (or a device connection) 442a of (or for) a first device 440. Similarly, a resistor $R_o$, and a via 760 are circuited in series between the branching point 434b and an input (or device connection) 442b of (or for) a device 440b. Again, it is assumed that the input 442a of the device 440a can be modeled, at least approximately, by a series connection of an inductance $L_{out}$, a resistance $R_{out}$ and an input capacitance $C_{out}$.

In addition, the tapped transmission line structure 700 optionally comprises a high-pass filter 770, which is connected between a driver terminal 432 of the tapped transmission line structure 700 and the branching node 434a. However, the high pass filter 770 may optionally be part of the automated test equipment driver 431 driving the tapped transmission line structure.

The optional high-pass filter 770 may, for example, comprise a T-structure. For example, a first high-pass filter resistor 772 is circuited between an input 780 of the high-pass filter and a central node 782 of the high-pass filter. A second high-pass filter resistor 774 is circuited between the central node 782 and an output 784 of the high-pass filter. In addition, a third high-pass filter resistor 776 and a high-pass filter inductor 778 are circuited in series between the central node 782 and a reference potential connection GND. In addition, a high-pass-filter bypass capacitor 779 is circuited between the high-pass filter input 780 and the high-pass filter output 784. Accordingly, the high-pass filter 770 may attenuate DC signals and low-frequency signals having frequencies for which the high-pass filter capacitor 779 comprises an impedance, which is larger than the resistance $R$ of the high-pass filter resistors 772, 774, 776. In contrast, the high-pass filter 770 may pass high frequencies, for example, frequencies, for which the impedance of the high-pass filter capacitor 779 is smaller than the resistance $R$ of the high-pass filter resistors 772, 774, 776.
Accordingly, the high-pass filter 770 may be configured to emphasize edges or transitions over steady signals, thereby reducing a rise-time of the filtered signal, which is forwarded via the man transmission line 430. Additionally, the $R,L,C$ values of the filter may be chosen so that the impedance of the high-pass filter is equal or similar to the impedance of the main transmission line.

In the following, the concept of the circuit of Fig. 7 will be briefly summarized. One approach to implement the low-pass behavior, which has been discussed with reference to Fig. 6, is to use an embedded resistor (for example the resistors $R_j$ to $R_n$) before the via (for example vias 750, 760) to each device-under-test (for example devices 440a, 440b), wherein each resistor value (for example values $R_i$ to $R_N$) is different depending on the device-under-test position along the tapped transmission line to generate the required time constant for the low-pass filter.

The interaction of this resistor (for example of the resistors $R_i$ to $R_N$) with the input capacitance (for example $C_{Dn}$) of the device-under-test (e.g. 444a, 444b) will generate a low-pass filter. By selecting appropriately the resistor value (e.g. $R_1$ to $R_N$), it is possible to tune the time constant of this filter for each device-under-test.

The performance can be further improved by adding the equalization-type high-pass filter 770 after the automated test equipment driver 431, so that a faster rise-time is available at the last devices-under-test (e.g. device 440b and possibly adjacent devices) of the tapped transmission line without adverse consequences to the first devices-under-test (for example device 440a and possibly adjacent devices) because of the low-pass behavior of the $R/C$ circuit (comprising, for example, the resistor $R_1$ and the input capacitance $C_{out}$ of the device 440a) at the initial (close to the driver terminal 432) devices-under-test. Details regarding this arrangement have been shown in Fig. 7.

Performance discussion with reference to Figs. 8 and 9

In the following, the performance improvements, which can be achieved by the inventive concept, will be discussed in detail with reference to Figs. 8 and 9. Fig. 8 shows a graphical representation of simulation results for the circuit setup of Fig. 7 with eight devices-under-test, where each device-under-test is assumed to have an input capacitance of 1.3 pF and a resistance of 5 $\Omega$ and an inductance of 0.5 nH. Also, for the simulations, the results, which are shown in Fig. 8, the socket (which connects the dut 440a, 440b with the test board or the via 750,760) is assumed to have an inductance of 1 nH. Also, it was
assumed that no high-pass filter 770 was used after the automated test equipment driver 431. All transmission lines have a 50 Ohm impedance.

For a reference simulation, the results of which are shown in Fig. 8, it was assumed that the resistors \( R_1 \) to \( R_N \) were negligible, i.e. that the resistances of the resistors \( R_i \) to \( R_N \) were equal to 0. For a simulation of the inventive concept, the results of which are shown in Fig. 9, the following resistor values (of the resistors \( R_i \) to \( R_N \)) were added for each device-under-test (DUT):

\[
\begin{align*}
\text{DUT1:} & \; 70 \, \Omega; \; \text{DUT2:} \; 30 \, \Omega; \; \text{DUT3:} \; 0 \, \Omega; \; \text{DUT4:} \; 0 \, \Omega; \\
\text{DUT5:} & \; 0 \, \Omega; \; \text{DUT6:} \; 0 \, \Omega; \; \text{DUT7:} \; 0 \, \Omega; \; \text{DUT8:} \; 0 \, \Omega.
\end{align*}
\]

Here, it is assumed that DUT1 is the device, which is electrically closest to the driver terminal 432, and that the device DUT8 is electrically furthest away from the driver terminal 432. In other words, the branching point 434a, at which a branching structure coupling the input 442a of the first DUT 440a (DUT1) branches from the main transmission line, is closer to the driver terminal 432 than the branching point 434b, at which the branching structure coupling the input 442b of the DUT 440b (DUT8) branches from the main transmission line.

Fig. 8 shows a graphical representation of eye diagrams, which represent the signals at the device connections 442a, 442b of eight devices-under-test DUT1 to DUT8. Thus, Fig. 8 shows the data eye at each device-under-test (for DUT1 to DUT8) and the rise times if no resistor was added (i.e. if resistors \( R_i \) to \( R_N \) were omitted).

Fig. 9 shows a graphical representation of the data eyes at each DUT with the added resistors (as discussed above). Also, Fig. 9 shows results for the rise-times.

As can be seen in Fig. 8, which shows the data eye in the absence of the resistors \( R_i \) to \( R_N \), the eye opening is significantly larger for the first device-under-test DUT1 (which is closest to the driver terminal) than for the last device-under-test DUT8 (which is electrically farthest away from the driver terminal). Also, it can be seen that in the absence of the resistors \( R_i \) to \( R_N \), the rise-time varies significantly, by a factor of more than 2, between the first device DUT1 (97 picoseconds) and the last device DUT8 (199 picoseconds).

In contrast, Fig. 9 shows a significant improvement in terms of uniformity for the case in which the above-mentioned resistors \( (R_i = 70 \, \Omega, \; R_2 = 30 \, \Omega, \; R_3 \ldots \; R_8 = 0 \, \Omega) \) are added.
As can be seen, the data eye openings are significantly more uniform across the devices DUT1 to DUT8. Also, the rise-times are significantly more uniform. A variation of the rise-times is reduced to a range between 146 picoseconds (for DUT1) and 206 picoseconds (for DUT8).

Thus, it can be seen that the implementation of the inventive concept, to add resistors of different values into the branching structures coupling inputs of the devices with the main transmission line, brings along a significant improvement in uniformity of the signals present at the inputs of the devices. It allows testing a plurality of devices in parallel, because meaningful and reliable testing results can only be obtained if the signals at the different devices to be tested comprise similar characteristics. Also, as the rise-times at the first one or more devices (electrically closest to the driver terminal) are increased, reflections are reduced and the signal integrity, in particular for the more remote devices, is increased. As can be seen in Fig. 9, the data eye at the DUT8 is more "smooth" in the presence of said resistors Ri, RN when compared to the situation in the absence of the resistors Ri, ..., RN, which is shown in Fig. 8.

To summarize, Fig. 8 shows the data eye at each device-under-test in the rise-times if no resistor was added, while Fig. 9 represents the results with the added resistors. The results of Fig. 9 show a smaller variation in the rise-time (across the devices) and a better data eye correlation across the eight devices-under-test.

Implementation Details - Usage of an interposer shown in Figs. 10 and 11

In the following, a possible implementation for the above-described tapped transmission line structure will be discussed taking reference to Figs. 10 and 11.

Fig. 10 shows a cross-sectional view of a tapped transmission line structure, according to an embodiment of the invention. The tapped transmission line structure 1000 shown in Fig. 10 comprises a main printed-circuit-board (pcb) 1010. A main transmission line 430 comprising a plurality of transmission line segments 430a, 430b, 430c, 430d is embedded on an inner or outer layer of the main printed circuit board 1010. For example, the main transmission line 430 may be implemented as a strip line or micro strip line, which is embedded between two or more layers of the main printed circuit board 1010. Further, the main print circuit board 1010 comprises a plurality of vias 750, 760, which typically extend from the main transmission line 430 to a main surface 1011 of the main printed circuit board 1010. The vias typically extend approximately perpendicularly to the main surface 1011 of the main printed circuit board 1010, thereby establishing an electrical
coupling between the main transmission line 430 and pads 1050, 1060 on the main surface of the main print circuit board 1010. A plurality of vias, two of which are designated with 750 and 760, branch from the main transmission line 430 at different distances from a driver terminal 432 of the main transmission line 430. In addition, another via 1070 extends between the driver terminal 432 of the main transmission line 430 and a driver pad 1072 arranged on a second main surface 1012 of the main printed circuit board 1010. An automated testing equipment channel 431 (or an output driver thereof) may be connected to the driver pad 1072, for example via a so-called "POGO ASSEMBLY" cable.

An interposer (or interposer printed-circuit-board) 1080 is arranged on the first main surface 1011 of the main printed circuit board 1010, such that the interposer 1080 neighbors the first main surface 1011 of the main printed circuit board 1010 in an environment of the pad 1050. A device-under-test socket 1090 is stacked onto the interposer 1080, such that the interposer 1080 is sandwiched by the device-under-test socket 1090 and the main printed circuit 1010. Interposer 1080 comprises an embedded resistor 1082, which extends "vertically", i.e. approximately perpendicular to the main surface 1011 of the main printed circuit board 1010, from a lower surface of the interposer 1080 (which lower surface is in contact with the main printed circuit board 1010) to an upper surface of the interposer 1080 (which upper surface of the interposer 1080 is in contact with the device-under-test socket 1090). Accordingly, the embedded resistor 1082 is configured to establish an electrical connection between the pad 1050 and an electrical connection 1092 of the DUT socket 1090. Accordingly, the arrangement is configured such that an electrical connection is established between the main transmission line 430 and a device connection 1096 of a device 1094, if the device 1094 is inserted into the DUT socket 1090. The electrical connection between the main transmission line 430 and the DUT connection 1096 may be established via the via 750, the pad 1050, the embedded resistor 1082 and the DUT socket connection 1092. Accordingly, the via 750 and the embedded resistor 1082 may be considered as a signal transmission portion in the sense of the present application.

In addition, it should be noted that different interposers, i.e. interposers having embedded therein resistors of different resistance values, may be used. Accordingly, DUT sockets (not shown in Fig. 10), which are coupled to the main transmission line 430 close to the end 433 of the main transmission line 430 (for example via the via 760 and the tap 1060), may see a smaller series resistance circuited between the DUT socket and the corresponding branching point of the main transmission line than DUT sockets (e.g. the DUT socket 1090) coupled to the main transmission line close to the driver terminal 432. Accordingly, the further away (in an electrical sense) a DUT socket is arranged from the
driver terminal 432, the smaller is the resistance of the embedded resistor in the corresponding interposer. In some cases, one or more of the dut sockets, which are coupled to the main transmission line 430 close to the end 433 of the main transmission line 430, may be coupled to the main transmission line without an interposer, or using an interposer without an embedded resistor.

Fig. 11 shows a three-dimensional representation of the main printed circuit board 1010 and the interposer 1080, which interposer is not yet attached to the main printed circuit board. As can be seen, a contact pattern 1120 of the interposer 1080 is at least approximately identical to a contact pattern 1110 of the main printed circuit board 1010. Accordingly, the interposer 1080 is configured to vertically route through signals from a pad 1050 on the first main surface 101 of the main printed circuit board 1010 to the device socket 1090 to be attached to the top surface of the interposer 1080. When routing through a signal vertically, the resistor 1082 may be involved, which resistor 1082 is embedded in the interposer 1080, as discussed with reference to Fig. 10.

However, different implementations of the interposer are possible. For example, another possible implementation is that the interposer is embedded on the PCB socket board. For example, the top layer (for example of the PCB socket board) is designed to serve the same functionality as the interposer described above by having the resistor integrated there. This would save the need to use the separate interposer but would require a more complex manufacturing process on the socket board.

To summarize the above, the technique, to introduce different resistors into the branching structures branching from the main transmission line has been implemented on a real prototype using a Verigy pin electronics board that already includes a high-pass type active equalization filter in the pin electronics (for example in the automated test equipment driver 431). The needed resistor (for example the resistor R1 shown in Fig. 7) was implemented on an interposer type printed circuit board 1080, which is arranged (in operation) between the printed circuit board socket board that connects to the automated test equipment system (for example the main printed circuit board 1010) and the device under test socket 1090, as shown in Fig. 10. This resistor R1 can be implemented as an embedded passive component 1082 in a very thin interposer 1080 for a maximum signal integrity, as shown in Fig. 11. The interposer board is commercially available.
Measured Results in the presence of an interposer layer

In the following, some measured results will be discussed. Fig. 12 shows a graphical representation of measured results for an eight device-under-test tapped transmission line where a single 33 Ω resistor was set on the DUT1 position. Fig. 12 shows, in a first graphical representation 1210, a data eye at the DUT1 position, which is obtained without using an interposer, and, in a graphical representation 1220, a data eye at the DUT8 position obtained without using an interposer. In addition, Fig. 12 shows, in a graphical representation 1230, a data eye at the DUT1 position obtained in the presence of an interposer, and, in a graphical representation 1240, a data eye at the DUT8 position obtained in the presence of the interposer. As can be seen in the graphical representations 1210, 1220, the data eye is significantly different at the DUT1 position and at the DUT8 position in the absence of an interposer. A difference of the eye openings is 85 picoseconds in the absence of an interposer. In contrast, the graphical representations 1230 and 1240 show that the eye openings at the DUT1 position and the DUT8 position are more similar in the presence of an interposer (which is arranged at the DUT1 position). A difference of the eye openings is only 29 picoseconds in this case. Accordingly, it can be clearly seen from Fig. 12 that the usage of the interposer improves the signal correlation at different DUT positions.

To summarize the above, Fig. 12 shows the measured results for an eight device-under-test tapped transmission line, where a single 33 Ω resistor was set on the DUT1 position. A significant improvement is seen on the rise time correlation between DUT1 and DUT8.

Even though the results shown in Fig. 12 already demonstrate significant improvements, it should be noted that the techniques shown in Fig. 5 can be further used to tune each of the filters to the best response, including the optimization of the termination resistor at the end of the tapped transmission line. Accordingly, even better results can be obtained in some embodiments.

Y-shaped tapped transmission line

It should be noted that the inventive concept can also be applied for a tapped transmission line structure, as will be explained taking reference to Fig. 16, which shows a schematic representation of such a tapped transmission line structure 1600.
The tapped transmission line 1600 comprises a first main transmission line 430, and a second main transmission line 1630, both branching from a common line portion 1620 at a Y branching-point 1622.

The first main transmission line 430 and the branching structures coupled therewith may comprise any of the features and functionalities discussed above. For the sake of simplicity, identical reference numerals are used to designate identical means in the embodiment of Fig 16, as discussed above.

The second main transmission 1630 line may for example be symmetrical with respect to the first main transmission line 430, having portions 1630a, 1630b, 1630c. Similarly, branching structures comprising low pass filter structures 1650, 1660 may branch from the main transmission line 1630 at branching points 1634a, 1634b.

To summarize, the Y-shaped transmission line constitutes an additional topology. This topology has been verified, and it could be seen that it also provides significant improvements. The topology has a "Y-sharing tapped transmission line". A disadvantage of this topology is the fact that there is a signal amplitude loss from the Y-sharing circuit. Nevertheless, since each branch has a smaller number of duts (e.g. 4 duts per branch or "main transmission line") to achieve an 8 parallel dut configuration, compared with 8 in case of the normal tapped line), this topology allows for better signal integrity improvements and/or allows to test a higher number of duts compared with a standard tapped transmission line.

The above discussion demonstrates, that the inventive concept can be applied in numerous different topologies, some of which have been described herein. Nevertheless, the application of the inventive concept is not limited to the topologies discussed herein.
Claims

1. A tapped transmission line structure (100; 400; 600; 700) for providing an electrical connection between a driver terminal (110; 432) and a plurality of device connections (120A, 120B; 442A, 442B; 1096), the tapped transmission line structure comprising:

- a main transmission line (130; 430); and
- a plurality of branching structures (140A, 140B; 436A, 436B; 650, 660; R1, 750, RN, 760) coupling the main transmission line with the device connections at different distances (t1, t2) from the driver terminal and having associated therewith signal transmission portions (142A, 144A, 142B, 144B; 450, 452; 460, 462; Ri, 750, RN, 760),

wherein different of the signal transmission portions are designed to have different signal transmission characteristics in order to counteract differences of signal characteristics at different device connections.

2. The tapped transmission line structure (100; 400; 600; 700) according to claim 1, wherein different of the branching structures (140A, 140B; 436A, 436B; 750, 760; Ri 750, RN, 760) comprise, as the signal transmission portions or as a part of the signal transmission portions, resistors (R1, RN) of different resistance values circuited in series between the main transmission line (130; 430) and the device connections (120A, 120B; 442A, 442B).

3. The tapped transmission line structure (100; 400; 600; 700) according to claim 2, wherein a series resistor R1 of a signal transmission portion (142a) of a first branching structure (140a, 436a), which branches from the main transmission line (430) at a first branching point (434A), comprises a larger resistance value than a series resistor RN of a signal transmission portion (142b) of a second branching structure (140b, 436b), which branches from the main transmission line at a second branching point (434B), which second branching point (434B) is electrically spaced further away from the driver terminal (432) than the first branching point (434A).

4. A tapped transmission line structure (100; 400; 600; 700) according to one of claims 1 to 3, where the signal transmission portions of the branching structures (140A, 140B; 436A, 436B; 650, 660) comprise low pass filters (450, 460; 650, 660)
circuited between the main transmission line (130; 430) and the device connections (120A, 120B; 442A, 442B), wherein time constants of the low pass-filters decrease with increasing electrical distance of the branching points 434A, 434B), at which the branching structures branch from the main transmission line, from the driver terminal (110; 432).

5. The tapped transmission line structure (100; 400; 600; 700) according to claim 4, wherein the tapped transmission line structure further comprises a high-pass filter (470; 770) arranged between the driver terminal (432) and the first branching point (434A), at which a first branching structure (436A; 650; Ri, 750), when seen from the driver terminal (432), branches from the main transmission line (130; 430), and wherein the high-pass filter is configured to at least partially compensate for an effect of the low-pass filters (450, 460; 650, 660).

6. The tapped transmission line structure (100; 400; 600; 700) according to claim 5, wherein the high-pass filter (470; 770) is an equalization-type high-pass filter configured to reduce a rise time of a signal passing through the high-pass filter.

7. The tapped transmission line structure (100; 400; 600; 700) according to one of claims 1 to 6, wherein the signal transmission portions (142A, 144A, 142B, 144B; 450, 452, 460, 462; 650, 660; R1, 750, RN, 760) associated with the branching structures comprise portions (510, 512) of the main transmission line (130; 430) arranged adjacent to branching points (434A, 434B), at which the branching structures branch from the main transmission line, which portions (510, 512) of the main transmission line comprise an increased impedance when compared to a rest of the main transmission lines.

8. The tapped transmission line structure (100; 400; 600; 700) according to one of claims 1 to 7, wherein the signal transmission portions (142A, 144A, 142B, 144B; 450, 452, 460, 462; 650, 660; R1, 750, RN, 760) associated with the branching structures comprise vias (452, 462; 750, 760) extending from the main transmission line (130; 430) to another layer of a multi-layer circuit board (1010), and pads (540) in electrical contact with the vias and forming capacitances.

9. A Y-shared tapped transmission line (1600), comprising:
a driver terminal (1601) copied to a Y-branching point (1622) of the Y-shared tapped transmission line (1600);

a first tapped transmission line structure (100;400;600;700) according to one of claims 1 to 8, wherein the main transmission line of the first tapped transmission line structure branches from the Y branching point (1622); and

a second tapped transmission line structure (100;400;600;700) according to one of claims 1 to 8, wherein the main transmission line of the second tapped transmission line structure branches from the Y branching point (1622).

10. A test board (200; 1000) for coupling a plurality of devices-under-test with an automated test equipment, the test board comprising:

a plurality of device-under-test sockets (210a, 210b; 1080) for contacting the devices-under-test (1094); and

a tapped transmission line structure (100; 400; 600; 700) according to one of claims 1 to 9, wherein the tapped transmission line structure is configured to forward a signal from the automated test equipment (431) to a plurality of the device-under-test sockets (1080).

11. The test board (200; 1000) according to claim 10, wherein the test board comprises an interposer-type printed circuit board (1080) arranged between a main printed circuit board (1010) carrying the main transmission line (130; 430) and at least one of the device-under-test sockets (1090); and

wherein the branching structure (750, 1082) coupling a pad (1092) of the device-under-test socket (1090) with the main transmission line (130; 430) comprises a vertical resistor (1082) extending between a first surface of the interposer-type printed circuit board (1080) and a second opposite surface of the interposer-type printed circuit board (1080), thereby electrically coupling a surface (1011) of the main printed circuit board (1010) with the device-under-test socket (1090).

12. The test board according to claim 10, wherein the test boards comprises, as a top layer or embedded therein, an interposer layer,
wherein the interposer layer comprises a resistor extending between a first surface of the interposer layer and a second opposite surface of the interposer layer; and

wherein the branching structure (750, 1082) coupling a pad (1092) of the device-under-test socket (1090) with the main transmission line (130; 430) comprises the resistor (1082) extending between the first surface of the interposer layer and the second opposite surface of the interposer layer, thereby electrically coupling main transmission line with the device-under-test socket (1090).

13. A test board (250; 1000) for coupling a plurality of device-under-test (260A, 260B) with an automated test equipment, the test board comprising:

a plurality of devices-under-test (260A, 260B); and

a tapped transmission line structure (100; 400; 600; 700) according to one of claims 1 to 9;

wherein the branching structures (140A, 140B) of the tapped transmission line structure are configured to couple inputs (262a, 262b) of a plurality of the devices-under-test to the main transmission line (130; 430); and

wherein a signal transmission portion (142a) of a first branching structure (140A) is configured to form a first low pass filter with an input capacitance of an input (262a) of a first device-under-test (260A), which is coupled to the main transmission line (130; 430) via the first branching structure (140A);

wherein a signal transmission portion (142b) of a second branching structure (140B) is configured to form a second low pass filter with an input capacitance of an input (262b) of a second device-under-test (260B), which is coupled to the main transmission line (130; 430) via the second branching structure (140B); and

wherein a time constant of the first low-pass filter is larger than a time constant of the second low-pass filter, wherein a first branching point, at which the first branching structure branches from the main transmission line, is closer to the driver terminal than a second branching point, at which the second branching structure branches from the main transmission line.
14. The test board (250; 1000) according to claim 13, wherein inputs (262a) of one or more of the devices-under-test (260A) are coupled to the main transmission line (130) via one or more branching structures (140a) branching from the main transmission line (130;430) comparatively closer to the driver terminal (110),

wherein inputs of one or more of the devices-under-test (260B) are coupled to the main transmission line (130) via one or more branching structures (140b) branching from the main transmission line (130;430) comparatively further away from the driver terminal (110); and

wherein the one or more branching structures (140a) branching from the main transmission line comparatively closer to the driver terminal (110) comprise a series resistance larger than 20 Ohm, and

wherein the one or more branching structures (140b) branching from the main transmission line comparatively further away from the driver terminal comprise a series resistance smaller than 4 Ohm.

15. The test board (250; 1000) according to claim 13 or 14, wherein the devices-under-test (260A, 260B) are double-data-rate memory devices, and

wherein double-data-rate inputs (262a, 262b) are coupled to the tapped transmission line structure (100).

16. An automated test equipment (300) comprising a test board (200; 250; 1000) according to one of claims 11 to 15,

wherein the automated test equipment is configured to test in parallel devices-under-test (210A, 210B; 260A, 260B; 1094) attached to the test board; and

wherein the automated test equipment is configured to apply a test signal to the tapped transmission line structure (100) having a bit rate larger than 1 Gbit per second.

17. A method for providing signals to a plurality of devices using a common main transmission line, to which the devices are coupled via a plurality of branching structures, the method comprising:
forwarding a signal from a driver terminal to a first one of the devices via the main transmission line and a first branching structure coupling the first device to the main transmission line; and

forwarding the signal from the driver terminal to a second one of the devices via the main transmission line and a second branching structure coupling the second device to the main transmission line;

wherein the signal is shaped by a first signal transmission portion associated with the first branching structure and by a second signal transmission portion associated with the second branching structure, such that the signal shaping by the first signal transmission portion and by the second signal transmission portion counteracts differences of signal characteristics at different device connections.
FIG 9A

DUT 1

DUT 2

DUT 5

DUT 6

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<p>| rise time | 146ps | 147ps | 134ps |</p>
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FIG 12

measurement done on a bench setup using a serial burst and a 60PS rise time limiter

1230
with interposer

1210
no interposer

1220
1240
FIG 13

production testing

option 1

option 2

FIG 14A

FIG 14B
INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/067780

A. CLASSIFICATION OF SUBJECT MATTER

INV. G11C29/56 G11C5/06
ADD. G06F13/40 G01R31/319

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C G06F G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<td>US 6 366 972 Bl (GREBENKEMPER C JOHN [US]) ET AL) 2 April 2002 (2002-04-02)</td>
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<td>US 2003/126338 Al (D0DD JAMES M [US] ET AL) 3 July 2003 (2003-07-03) paragraph [0017] - paragraph [0023]; figures 3,4</td>
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Date of the actual completion of the international search: 26 March 2010

Date of mailing of the international search report: 06/04/2010

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"%" document member of the same patent family
**INTERNATIONAL SEARCH REPORT**

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