

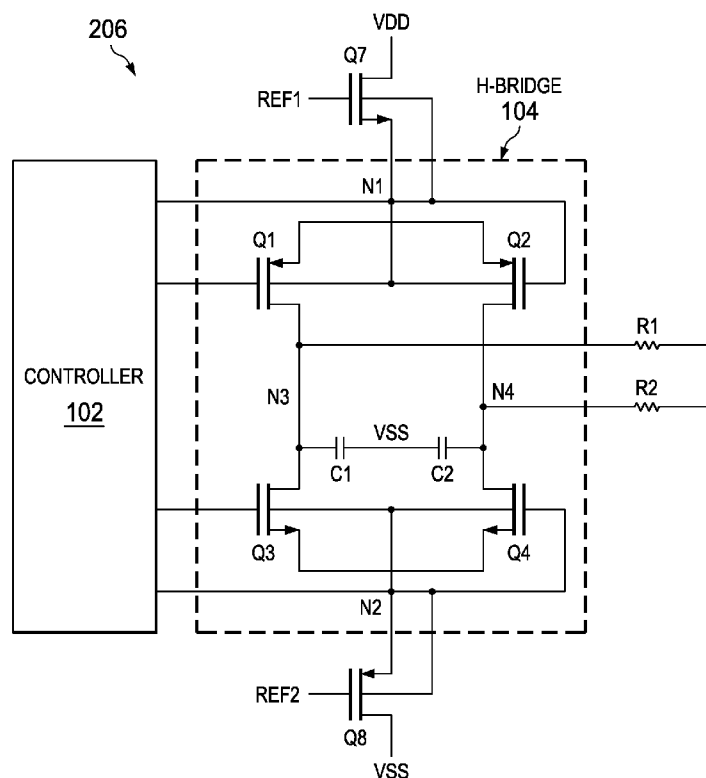


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(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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[Continued on next page]

(54) **Title:** SOURCE-FOLLOWER BASED VOLTAGE MODE TRANSMITTER

(57) **Abstract:** An apparatus has an H-bridge with a first switch (Q1) coupled between first and third nodes (N1, N3), a second switch (Q2) coupled between first and fourth nodes (N1, N4), a third switch (Q3) coupled between second and third nodes (N2, N3), and a fourth switch (Q4) coupled between second and fourth nodes (N2, N4). A first source-follower (Q7) coupled to the first node (N1) and a first supply rail (VDD) is configured to receive a first reference signal (REF1). A second source-follower (Q8) coupled to the second node (N2) and a second supply rail (VSS) is configured to receive a second reference signal (REF2).

**Declarations under Rule 4.17:**

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

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SOURCE-FOLLOWER BASED VOLTAGE MODE TRANSMITTER

[0001] This relates generally to transmitter and, more particularly, to voltage mode transmitter having an H-bridge that uses source-followers.

BACKGROUND

[0002] FIG. 1 shows an example conventional driver 100. In operation, controller 102 provides complementary drive or control signals to H-bridge 104 (which generally comprises transistors Q1 to Q4 and capacitors C1 and C2). Specifically, these complementary signals are provided to transistor pair Q1 and Q2 (which, as shown, are PMOS transistors) and transistor pair Q3 and Q4 (which, as shown, are NMOS transistors) in order to generate output signals for resistors R1 and R2 (which are typically impedance matching resistors) and the transmission channel (not shown). This means that controller 102 provides a logic high or “1” signal to transistors Q1 and Q4 (while providing a logic low or “0” signal to transistors Q2 and Q3) to create one current path and visa versa for another current path. With either current path, there is a loss that occurs as result of using transistors Q5 and Q6; namely, there is high output impedance and a slow response due to transistors Q5 and Q6 operating as current sources. Therefore, there is a need for a driver having improved performance.

[0003] Some examples of conventional circuits are described in U.S. Patent No. 6,917,169; U.S. Patent No. 5,689,144; U.S. Patent Pre-Grant Publ. No. 2008/0252372; and Krenzk et al., “A 36-V H-BRIDGE DRIVER INTERFACE IN A STANDARD 0.35- μ m CMOS PROCESS,” IEEE Intl. Symposium on Circuits and Systems 2005, Vol. 4, May 23-26 2005, pp. 3651-3554.

SUMMARY

[0004] In one aspect, the invention provides an apparatus.

[0005] A described embodiment of the apparatus comprises a first supply rail; a second supply rail; an H-bridge having: a first node; a second node; a third node; a fourth node; a first switch that is coupled between the first and third nodes; a second switch that is coupled between

the first and fourth nodes; a third switch that is coupled between the second and third nodes; and a fourth switch that is coupled between the second and fourth nodes; a first source-follower that is coupled to the first node of the H-bridge, that is coupled to the first supply rail, and that is configured to receive a first reference signal; and a second source-follower that is coupled to the second node of the H-bridge, that is coupled to the second supply rail, and that is configured to receive a second reference signal.

[0006] In specific implementations, the first and second switches may further comprise first and second PMOS transistors, wherein each of the first and second PMOS transistors are coupled to the first node at its source. The third and fourth switches may further comprise first and second NMOS transistors, wherein each of the first and second NMOS transistors are coupled to the second node at its source. The first source-follower may further comprise a third NMOS transistor that is coupled to the first node at its source and body, that is coupled to the first supply rail at its drain, and that is configured to receive the first reference signal at its gate. The second source-follower may further comprise a third PMOS transistor that is coupled to the second node at its source and body, that is coupled to the second supply rail at its drain, and that is configured to receive the second reference signal at its gate. The third NMOS and third PMOS transistors are depletion mode transistors.

[0007] In another aspect an apparatus is provided that comprises a first supply rail; a second supply rail; a transmitter having: a transmit circuit; an H-bridge having: a first node; a second node; a third node; a fourth node; a first switch that is coupled between the first and third nodes and that is controlled by the transmit circuit; a second switch that is coupled between the first and fourth nodes and that is controlled by the transmit circuit; a third switch that is coupled between the second and third nodes and that is controlled by the transmit circuit; and a fourth switch that is coupled between the second and fourth nodes and that is controlled by the transmit circuit; a first source-follower that is coupled to the first node of the H-bridge, that is coupled to the first supply rail, and that is configured to receive a first reference signal; and a second source-follower that is coupled to the second node of the H-bridge, that is coupled to the second supply rail, and that is configured to receive a second reference signal; an transmission channel that is coupled to the third and fourth nodes; and a receiver that is coupled to the interconnect.

[0008] In specific implementations, the transmit circuit may further comprise an input circuit; and a write circuit that is coupled to the input circuit and the gates of the first and second PMOS transistors and the gates of the first and second NMOS transistors. The transmission channel may further comprise an interconnect. The receiver may further comprise a magnetic head. The write circuit may further comprise a driver that is coupled to the gates of the first and second PMOS transistors and the gates of the first and second NMOS transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 is a diagram of an example of a conventional H-bridge transmitter.

[0010] FIG. 2 is a diagram of system in accordance with the invention.

[0011] FIG. 3 is diagram of an example implementation of the system of FIG. 2.

[0012] FIG. 4 is a diagram of an example of a driver of the systems of FIGS. 2 and 3.

[0013] FIG. 5 is a diagram comparing the performance of the drivers of FIGS. 1 and 4.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0014] FIG. 2 illustrates an example of a system 200 in accordance with the invention. In operation, transmitter 202 (and transmit circuit 204, in particular) receives an input signal IN. The transmit circuit 204 (which, can, for example, perform wave-shaping operations) provides control signals to driver 206 that permit a signal to be driven over the transmission channel 208. The receiver 210 can then generate an output signal OUT based on the signal received from the transmission channel 208.

[0015] One example implementation of the system 200 can be seen in FIG. 3. In this example, the system 200 is implemented as a write channel for a hard disk drive or HDD (which is labeled 300). For the system 300, a write signal is received from the HDD channel by the preamplifier 301 (namely the input circuit 302). Collectively, the input circuit 302 and write circuit 304 can perform wave-shaping so as to allow driver 206 to transmit a write signal over interconnect 308 to the magnetic head 310. Based on this write signal, the magnetic head 310 can write to an HDD platter.

[0016] The driver 206 (which can be seen in greater detail in FIG. 4) is used in systems 200 and 300. Driver 206 has a similar construction driver 100, except that current sources (i.e., transistors Q5 and Q6) have been replaced with source-followers (i.e., transistors Q7 and Q8), which are coupled to nodes N1 and N2 of H-bridge 104. Source-followers respond very quickly (compared to current sources) to changes in the source voltage (which occur during switching of

H-bridge 104). Since the gates of transistors Q7 and Q8 are generally held at fixed reference voltages REF1 and REF2, any source voltage changes results in an increase of the gate-source voltage of transistors Q7 and Q8, which prompts a rapid increase in drain-to-source current. Thus, driver 206 more rapidly charges and discharges the output nodes N3 and N4 compared to driver 100, improving efficiency.

[0017] Moreover, by using source-followers (i.e., transistors Q7 and Q8), the common source impedance Z_{OUT} looking back into the H-bridge 104 is also decreased. Looking back to driver 100, impedance $Z_{OUT,100}$ is:

$$(1) \quad Z_{OUT,100} = Z_{SWITCH} + Z_{CS} = Z_{SWITCH} + \frac{V_A}{I_D},$$

where Z_{SWITCH} is the switch impedance (i.e., on-resistance of one of transistors Q1 to Q4), Z_{CS} is current source impedance, V_A is the Early voltage of transistor Q5 or Q6, and I_D is the drain current of transistor Q5 or Q6. This means that for an Early voltage of about 10V and a drain current I_D of about 50mA, impedance $Z_{OUT,100}$ is about 200Ω (which is very high). With driver 206, the impedance $Z_{OUT,206}$ is

$$(2) \quad \begin{aligned} Z_{OUT,200} &= Z_{SWITCH} + Z_{SF} = Z_{SWITCH} + \frac{1}{g_m} \\ &= Z_{SWITCH} + \frac{1}{\sqrt{\frac{2W}{L} C_{OX} \mu I_D}}, \end{aligned}$$

where Z_{SF} is source-follower impedance, W/L is the aspect ratio of transistor Q7 or Q8, C_{OX} is the oxide unit capacitance of transistor Q7 or Q8, μ is the carrier mobility, and I_D is the drain current of transistor Q7 or Q8. The impedance $Z_{OUT,206}$ is comparative much smaller, being about $1-5\Omega$ with a drain current I_D of about 10mA. This lower impedance can, therefore, move the resulting parasitic pole out to a higher frequency so as to permit higher frequency operation.

[0018] To further improve performance, transistors Q7 and Q8 can be depletion mode transistors. Depletion mode devices (i.e., depletion mode NMOS or PMOS transistors) have a negative threshold voltage V_T . This allows the source-followers (i.e., transistors Q7 and Q8) to achieve a maximum output swing (which, theoretically, is a dynamic range from the voltage on rail VSS plus a drain-source voltage drop across transistor Q8 to the voltage on rail VDD minus

a drain-source voltage drop across transistor Q7) without having to provide reference voltage REF1 and REF2 that exceed the voltages on rails VDD and VSS (which is usually accomplished with charge pumps).

[0019] Turning to FIG. 5, a comparison of the drivers 100 and 206 can be seen. As shown, driver 206 settles much more quickly than driver 100. As a result the efficiency of driver 206 is greatly improved over that of driver 100.

[0020] Those skilled in the art will appreciate that modifications may be made to the described example implementations, and also that many other embodiments are possible, within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:
 - a first supply rail;
 - a second supply rail;
 - an H-bridge having a first node; a second node; a third node; a fourth node; a first switch that is coupled between the first and third nodes; a second switch that is coupled between the first and fourth nodes; a third switch that is coupled between the second and third nodes; and a fourth switch that is coupled between the second and fourth nodes;
 - a first source-follower that is coupled to the first node of the H-bridge, that is coupled to the first supply rail, and that is configured to receive a first reference signal; and
 - a second source-follower that is coupled to the second node of the H-bridge, that is coupled to the second supply rail, and that is configured to receive a second reference signal.
2. The apparatus of Claim 1, wherein the first and second switches further comprise first and second PMOS transistors, wherein each of the first and second PMOS transistors are coupled to the first node at its source.
3. The apparatus of Claim 2, wherein the third and fourth switches further comprise first and second NMOS transistors, wherein each of the first and second NMOS transistors are coupled to the second node at its source.
4. The apparatus of Claim 3, wherein the first source-follower further comprises a third NMOS transistor that is coupled to the first node at its source and body, that is coupled to the first supply rail at its drain, and that is configured to receive the first reference signal at its gate.
5. The apparatus of Claim 4, wherein the second source-follower further comprises a third PMOS transistor that is coupled to the second node at its source and body, that is coupled to

the second supply rail at its drain, and that is configured to receive the second reference signal at its gate.

6. The apparatus of Claim 5, wherein the third NMOS and third PMOS transistors are depletion mode transistors.

7. The apparatus of Claim 6, further comprising:
a transmitter having a transmit circuit including the H-bridge;
an transmission channel that is coupled to the third and fourth nodes; and
a receiver that is coupled to the interconnect.

8. The apparatus of Claim 7, wherein the transmit circuit further comprises:
an input circuit; and
a write circuit that is coupled to the input circuit and the gates of the first and second PMOS transistors and the gates of the first and second NMOS transistors.

9. The apparatus of Claim 8, wherein the transmission channel further comprises an interconnect.

10. The apparatus of Claim 8, wherein the receiver further comprises a magnetic head.

11. The apparatus of Claim 8, wherein the write circuit further comprises a driver that is coupled to the gates of the first and second PMOS transistors and the gates of the first and second NMOS transistors.

12. The apparatus of Claim 1, wherein the transmit circuit further comprises:
an input circuit; and
a write circuit that is coupled to the input circuit and the gates of the first and second PMOS transistors and the gates of the first and second NMOS transistors.

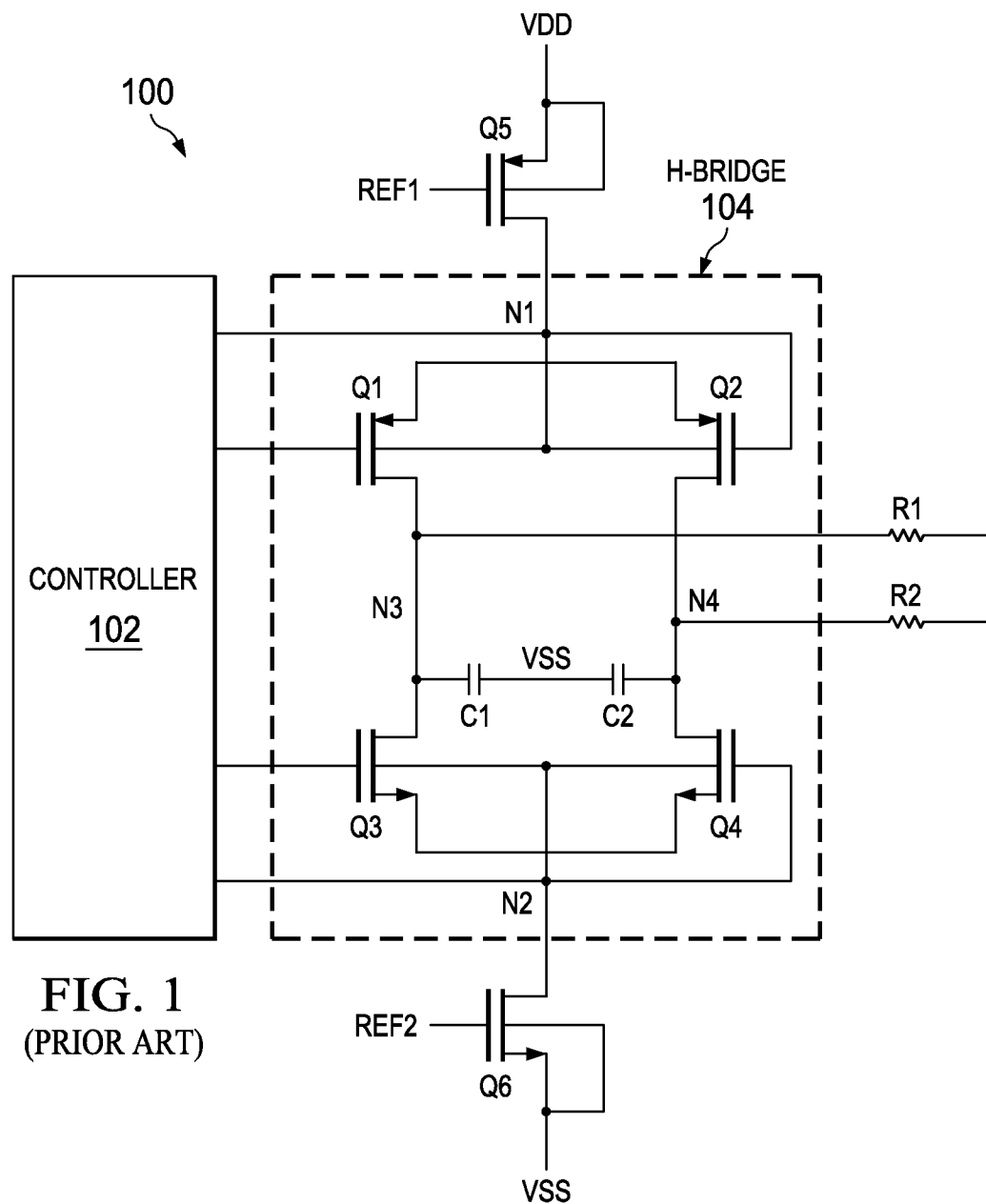


FIG. 1
(PRIOR ART)

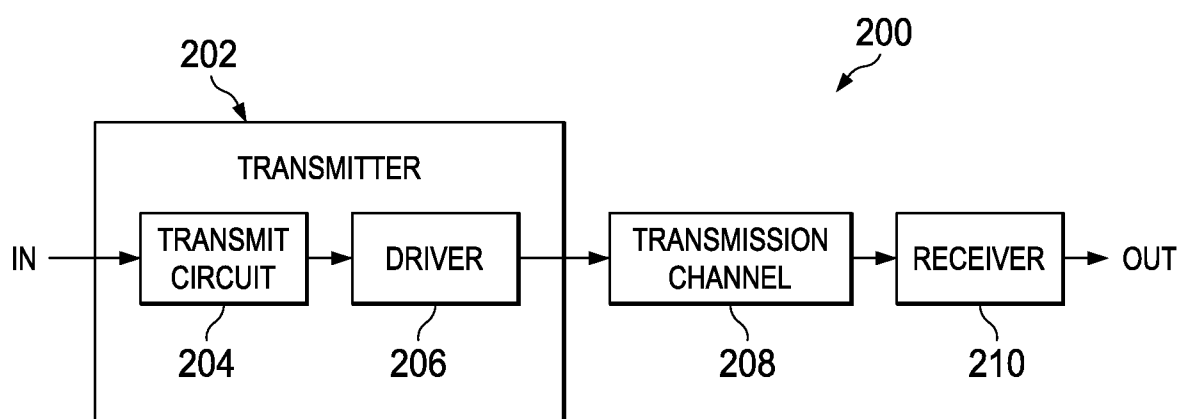
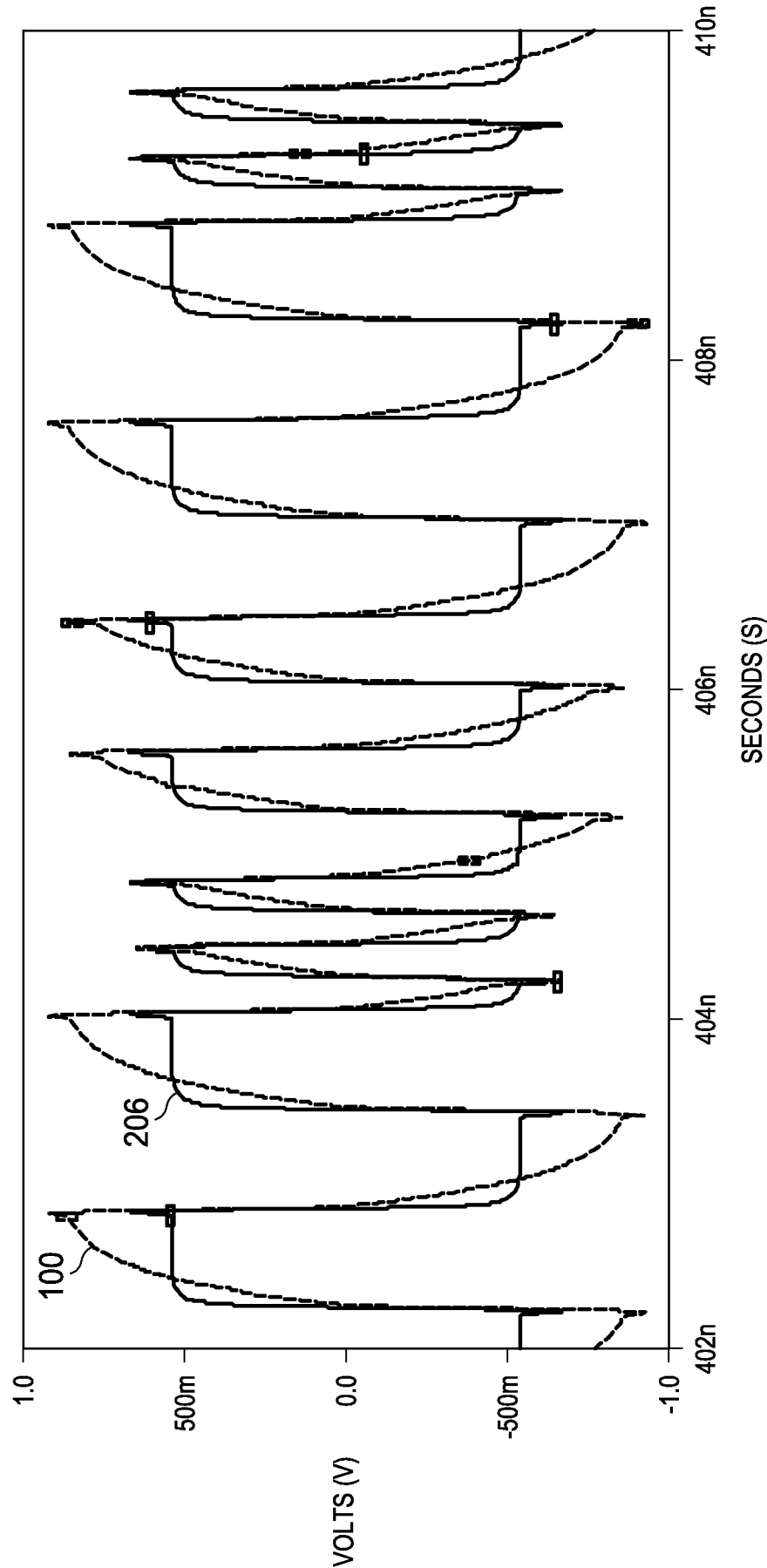


FIG. 2

FIG. 5



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/034800**A. CLASSIFICATION OF SUBJECT MATTER****H03K 19/0185(2006.01)i, H04L 25/02(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03K 19/0185; G05F 1/40; H03B 1/00; G11B 5/09; G01R 19/00; H04L 25/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: voltage mode transmitter, source-follower, H-bridge

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005-0013029 A1 (JASON P. BRENDEN) 20 January 2005 See abstract, claims 1, 6, paragraph [0013] and figures 1-4.	1-12
A	US 6720805 B1 (DAVID JAMIE HAAS) 13 April 2004 See abstract, claims 1, 4-7 and figures 1A-3.	1-12
A	WO 99-39437 A1 (TELEFONAKTIEBOLAGET LM ERICSSON (PUBL)) 05 August 1999 See abstract, claims 1-2 and figures 1a-4.	1-12
A	US 6636024 B2 (KLAUS ZAMETZKY) 21 October 2003 See abstract, claims 1-4 and figures 4-8.	1-12
A	US 2011-0221421 A1 (RICHARD K. WILLIAMS) 15 September 2011 See abstract, claims 1-4 and figures 6A-7C.	1-12



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

09 July 2013 (09.07.2013)

Date of mailing of the international search report

10 July 2013 (10.07.2013)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/034800

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