

June 2, 1970

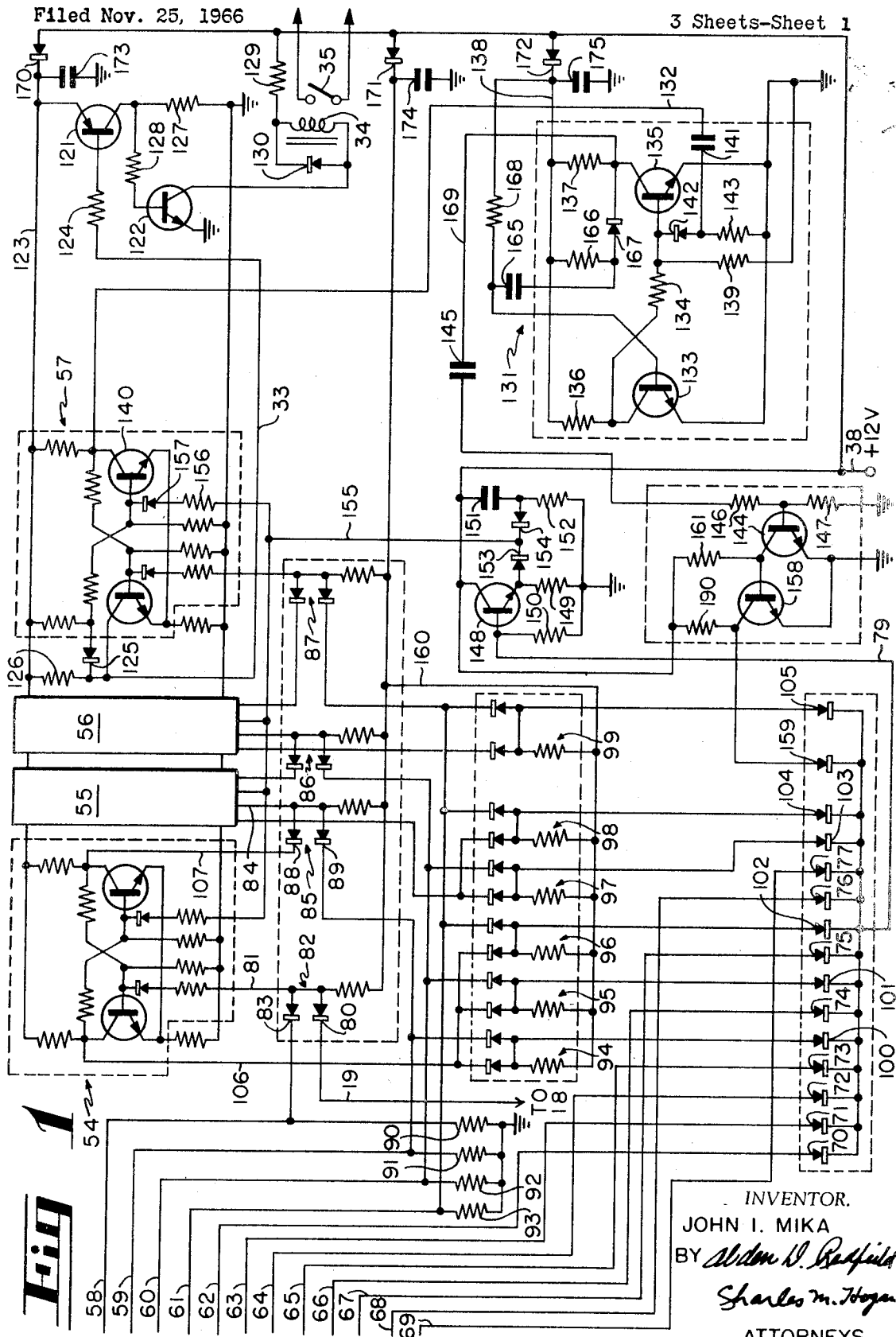
J. I. MIKA

3,515,340

DIGITAL CODED SECURITY SYSTEM

Filed Nov. 25, 1966

3 Sheets-Sheet 1



June 2, 1970

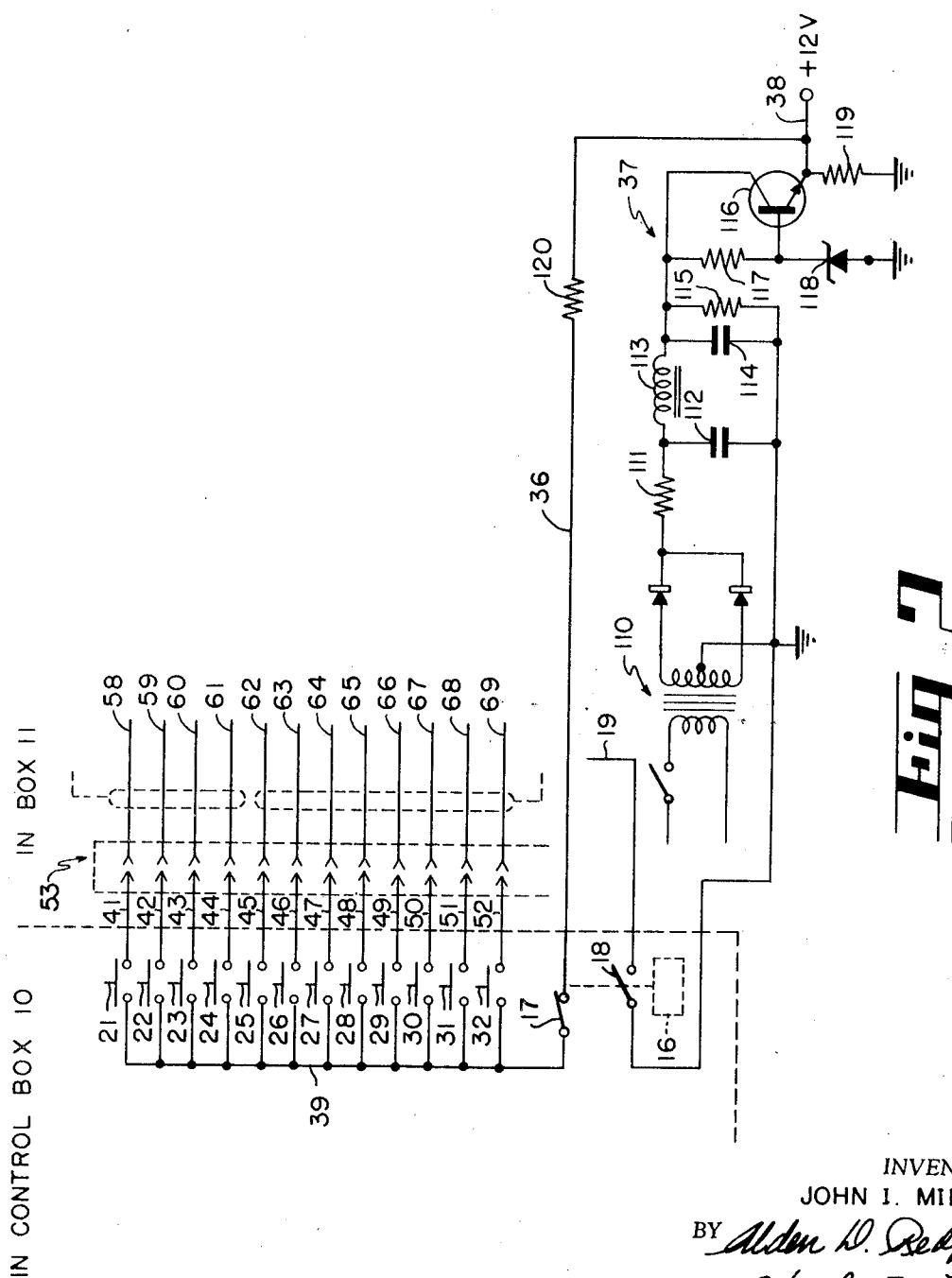
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DIGITAL CODED SECURITY SYSTEM

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3 Sheets-Sheet 2



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3 Sheets-Sheet 3

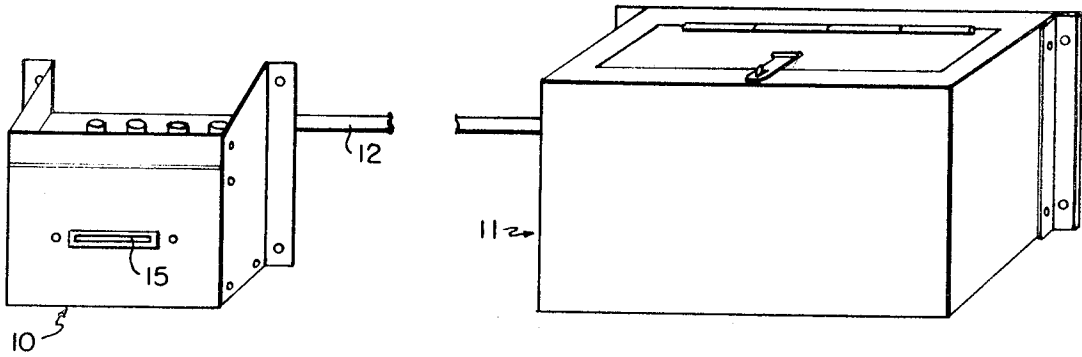


Fig 3

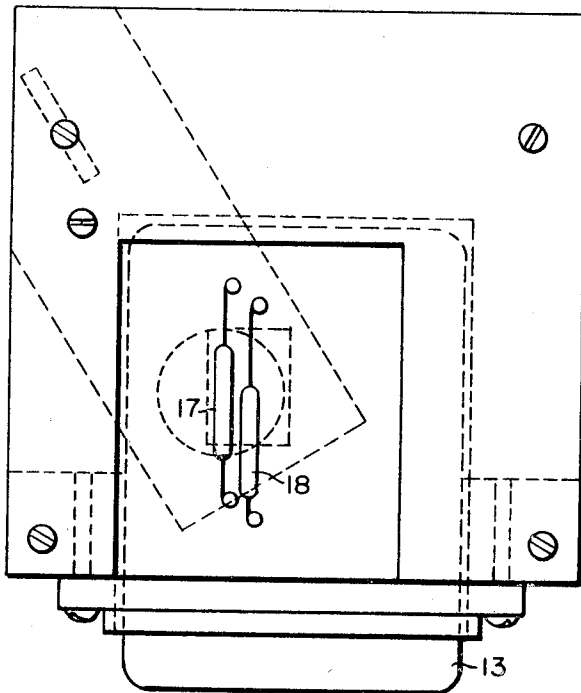


Fig 4

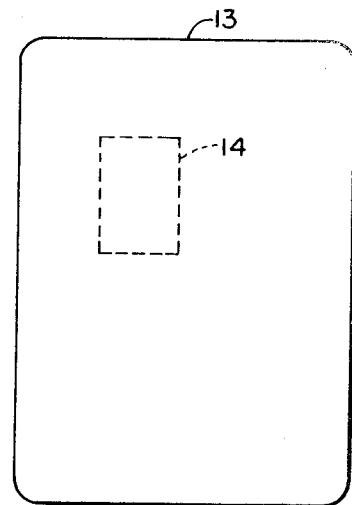


Fig 6

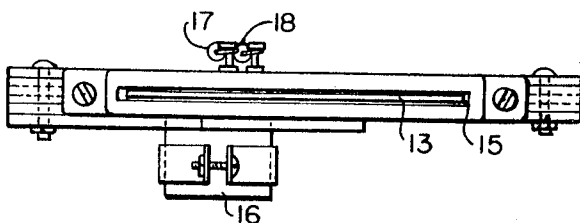


Fig 5

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3,515,340

DIGITAL CODED SECURITY SYSTEM

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U.S. Cl. 235—61.7

1 Claim

ABSTRACT OF THE DISCLOSURE

This is a security system for permitting access to secured premises. Satisfaction of a code card provides energy for a plurality of push button switchable lines. Input lines and output lines on a patch board provide for selection of a switch code involving energizing of a selected few of the output lines in sequence. The selected lines are individually applied to the stages of a register of cascaded binary devices. In response to successive energization of the selected lines, in accordance with the switch code, the binary devices are successively set and the final binary device activates a qualifying device permitting access for a limited time. The disclosure includes an OR gate which so gates false signals on the non-selected output lines of the patch board as to cause reset. The disclosure features AND circuit means for causing resetting upon sensing coincidence between a reset state of any binary device, and an out-of-sequence signal applied over one of the selected lines to any of the succeeding binary devices.

The present invention provides an improved digital coded security system of the type employed to control entry into secured areas, vaults, safes or similar places requiring protection.

The principal object of the invention is to provide a novel security system which employs the combination of a key code, built into a card in the possession of an authorized user, and a coded combination of manual operations, such as the depression of a sequence of push buttons, i.e., a switch code. These codes set up electrical circuitry which controls the operation of a door latch or like entry-permitting mechanism.

Another object of the invention is to provide a security system of such fool-proof character that access is negated if a non-coded button is depressed or if a coded button is depressed out of its proper sequence or if the key code is not satisfied.

Another object of the invention is to provide an improved security system in which the switch code may readily be changed, the system affording a large number of code selections.

It is also an object of the present invention to provide simplified circuitry for limiting the access-permitting operations to a predetermined period.

For a better understanding of the invention, together with other and further objects, advantages and capabilities thereof, reference is made to the following description of the accompanying drawings, in which:

FIG. 1 is a circuit diagram of a complete security system in accordance with the invention (with the exception of the FIG. 2 circuitry). The FIG. 1 elements are in box 11;

FIG. 2 is a schematic diagram of the circuitry in the control box 10 and also the patch board in box 11;

FIG. 3 is a perspective view of the control box and the cabinet containing the processing circuitry;

FIGS. 4 and 5 are top plan and side views of the assembly of switches which are actuated by the key card; and

FIG. 6 is a top plan view of the key card.

The digital code security system in accordance with

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the invention prevents unauthorized personnel (those not possessing the key code or those not knowing the switch code) from gaining entry or access to a protected area. Only an authorized person, in possession of a key code or card code and with knowledge of the switch code, can gain access to the secured area and then only by performing the requisite operations.

The system is packaged in two containers 10 and 11 (FIG. 3). The encoder or control box 10 houses the devices on which the operator performs manual operations. For convenience this container 10 is located at the entrance port.

The other container 11 houses the circuitry (FIG. 1) which causes to be operated the latching and unlatching mechanism through which access to the secured area is obtained or barred, as the case may be. The container 11 (FIG. 3) is preferably installed inside the protected area. The container 11 also houses the mechanism utilized to change the switch code. The two boxes 10 and 11 are interconnected by an appropriate cable 12.

A system in accordance with the invention utilizes two codes, a key code and a switch code. The key or card code is provided by a magnetically coated portable card 13 (FIG. 6), which is made of plastic material, is carried around by the operator and has imbedded in it a ferro-magnetic element 14, the position of which is code-significant. The control box 10 is formed with an opening 15 into which the card is inserted. If the element 14 on the card registers positionally with a magnet 16 (FIG. 5) then reed switches 17 and 18 are operated in the manner described and supply power to and permit the operation of the FIG. 1 system.

A valid key code supplies power to the FIG. 1 circuitry and unlocks the digital circuitry. A valid switch code sets up the circuitry so that the entrance to the secured area is unlocked for a predetermined time. Then the FIG. 1 circuitry is reset. Entry is permitted only during a predetermined interval.

As previously indicated, the control box 10 contains the card insertion aperture 15 and the card detection magnet which actuates the reed switches 17 and 18. Additionally, the twelve push-button switches 21-32 (of which four are used in any one of the selected switch codes) are also mounted on the box 10. The container 11 houses all of the elements in FIG. 1, excepting cable 12, which are not included in the control box 10. The container 11 houses the processing circuitry and the patch board and plug-in devices which are employed in the predetermination of the desired switch code, i.e., the push buttons depressed and the sequence according to which they are to be depressed. In order to gain access to the secured area the following sequence of events must occur:

First, the authorized person or operator inserts the code card 13 in the slot 15. The placement of the ferro-magnetic insert 14 on the card is such that the card is compatible to the particular security system and registers with the magnet 16. Parenthetically, it will be understood that the magnet 16 and the magnetic element 14 may be placed in any desired position width-wise or length-wise, the point being that they register when compatible.

Note that with the code card out, both of the normally open reed switches 17 and 18 (FIGS. 4 and 5) are actuated and held in the closed position by the permanent magnet 16 that is located under them. When the code card 13 is inserted, reed switches 17 and 18 will open up as the card slides into place, due to the magnetic shielding effect of the insert 16. If the card is a correct card for the particular box, reed switch 18 will stay open but reed switch 17 will again close when the card is fully inserted into its slot 15. This operation of the reed switches is caused by the unique location of the piece of magnetic material 14 in the code card. If the

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card is compatible with the system, then the switch 18 will stay open but the switch 17 will again close when the card is fully inserted into the slot. The opening of switch 18 allows the switch code to be read into the processing circuitry, because it ungrounds a line 19 which would otherwise prevent the code from being read into the first binary device described below.

Second, the proper switch code is satisfied by depressing the switch buttons in the required sequence. The twelve available push-button switches are numbered 21-32, and they are used four at a time, for example 21-24 in the particular embodiment shown. That is, the switch code is selected by putting the plugs for wires 41-44 into the jacks for wires 58-61. The plugs for wires 45-52 are arranged as shown in FIG. 2.

Third, the electrical processing circuit generates an output command on line 33 which causes to be energized a port-unlatching solenoid 34. The period of the unlatching is approximately eight seconds. After this eight-second period the system is automatically reset.

In order to provide satisfactory security, a two-part code philosophy is employed. The first part of the two-part code is the simple code card 13 which must be inserted; the second part of the code is the four-out-of-twelve push-button switch arrangement which is activated in the proper sequence. The chance of a successful opening by an unauthorized person who has obtained the code card is one out of the combination of twelve things taken four at a time. This figure is $(12)(11)(10)(9) = 11,880$. The number of possible chances is at least doubled by the use of the code card; hence, the security against unauthorized entry is at least 1 out of 23,760 trials.

A word is in order at this time about some additional security features of this system. One of these is provided because the processing circuitry is located inside of locked box 11 and within the secured area. This tends to prevent tampering. The wiring from the control box is housed in a protective conduit 12. Additionally, the impedance of each of the input wires from the control box to the processing circuitry is matched, and this fact renders compromise more difficult.

Referring now specifically to FIG. 2, it will be seen that all read-in power is supplied through switch 17, which switch is connected by line 36 to the regulator 37 included in the power supply, which regulator supplies 12 volts on line 38. When read switch 17 is closed, 12 volts is accordingly available on bus bar 39. When power is available on bus bar 39, energy is supplied to the inputs of all of the switchable circuits including the push buttons 21-32. Parenthetically, in the event that a piece of ferro-magnetic material is inserted in slot 15 in lieu of the code card 13, the switches 17 and 18 will open and remain open, thereby keeping bus bar 39 de-energized and preventing effective use of the push-button switches. On the other hand, after a correct code card 13 has been inserted, then bus bar 39 is energized and the operator can activate the system by correctly operating the four selected push-button switches. Depression of any of these switches causes a 12 volt signal to appear on its respective output line. These lines are numbered 41 through 52. Only the lines 41-44 are used to provide the switch code input to the processing box in the following description of operation here given.

Included in the box 11 is a code-selecting patch board 53 which comprises simply twelve jacks and plugs. The output of the patch board goes to the processing circuitry.

The purposes of the processing circuitry are these: first, to set up in response to the proper switch code; second, to provide an output to unlock the door when the correct codes have been provided; third, to generate a reset signal and return to a passive state whenever the wrong button is depressed or whenever a correct code button is depressed in the wrong sequence; and fourth, to generate an automatic resetting signal in any event after a sufficient time for entry or access has elapsed.

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The principal wiring diagram of the system is shown in FIGS. 1, 2. In the particular embodiment here presented there are twelve push-button switches 21-32 in the control box 10 and the ultimate operation, i.e., the opening of an entrance door, etc., is performed only when four flip-flops 54-57 are set. In other words, the preferred embodiment is concerned with permutations of twelve things taken four at a time.

Now the elements which do the "taking" are four flip flops, variously referred to as binary devices or binaries, these being numbered 54, 55, 56 and 57. These four binaries will make transitions from "zero" or reset state to a "one" or set state as they do the "taking," that is, provided that the lines 58, 59, 60 and 61 are activated in sequence. These lines are activated or energized in sequence by closing the push-button switches so as to accomplish that sequence. To that end the lines 41, 42, 43 and 44 are run into a patch board for connection by plugs and jacks to lines 58-61. This patch board will accept any combination or permutation of the four push-button switches. Those push-button switches 25-32 which are not used for the security code and which should not be pressed may, however, be pressed and are employed to reset the binary devices. In other words, if one of these push-button switches is depressed then any of the binary devices which is in the one state is reset back to zero, thus effectively preventing code discovery by "trial and error" methods.

Parenthetically, the mode of accomplishment of the last mentioned function is quite simple and will be described at this time. The switches 25-32 are plugged in on the patch board 53 to jacks which are connected by wires 62-69 to diodes 70-77 and all of these diodes (collectively referred to as "error detection gate") are so poled and the switches so connected to the bus bar 39 that in the event of the depression of any one of the switches 25-32 a positive potential is impressed on line 79, which potential is used for resetting purposes as will later appear.

It is a condition of the setting of binary circuit 54 that the ground be removed from diode 80 by opening switch 18, also that push button 21 be pressed. The corresponding conditions for changing the binaries 55, 56 and 57 to the one state are as follows: (a) as to binary 55—that push button 23 be pressed and that the preceding binary device 54 be in the one state; (b) as to binary 56—that push button 23 be pressed and that the preceding binary device 55 be in the one state; and (c) as to binary 57—that push button 24 be pressed and that the preceding binary device 56 be in the one state.

It has been seen that the input circuit 81 to the first binary device 54 is activated only in response to two conditions. The first of these conditions, as has been stated, is that line 58 is energized and the second of these conditions is that the ground connection be removed by switch 18 from diode 80. Accordingly, an "and" gate 82 constitutes the read-in circuit for bistable device 54 and diode 83 is the read-in diode. The diode 80 functions as an inhibiting input until switch 18 opens. Each of the other binary devices 55, 56 and 57 is provided with an input circuit such as 84 which comprises the output of an "and" gate such as 85 comprising two diodes, such as 88 and 89, poled to pass only coincident positive levels or rather a positive pulse on top of a positive level. Only one of the gates 85, 86, and 87 is described in detail because the operation of all is the same. The sequential binaries 54-57 and the activating inputs provided by AND gates 82, 85, 86 and 87 are collectively a conventional subcombination.

Parenthetically, resistors 90, 91, 92 and 93 are individually connected between the inputs of the read-in diodes and ground. The gates at the inputs to the binary devices 55, 56 and 57 are numbered 85, 86 and 87. Each of the read-in diodes (say 89) of gates 82 and 85-87 is connected to that line (say 59) which when energized by depression of a push button (say 22) is intended to activate the associated binary device (say 55). The other

diode (say 88) of each gate, is connected to an output circuit of the preceding bistable device (say 54), with the exception of the first binary device 54, and as to that one, the diode is connected to the reed switch 18.

Thus the first binary device 54 changes from the zero to the one state when line 58 is energized after the ground is removed from diode 80. The second binary device 55 changes to the one state on condition that the line 59 is energized when the binary device 54 is in its one state. Binary device 56 changes to the one state on the condition that line 60 is energized when the second binary device is in its one state. Binary device 57 changes to the one state if line 61 is energized while device 56 is in the one state. In other words each binary device responds to logical "and" information to change from a zero to a one state and the four elements of the switch code, being potentials on lines 58, 59, 60 and 61, have to be presented in sequence before they are "taken."

It has already been pointed out that the diodes 70-77 constitute error-detection gates which cause the four binary devices to be reset to the zero state in the event of an inadvertent or purposeful depression of a push-button switch not employed in the desired code. More specifically, the OR gate having an output at 79 comprises a first plurality of diodes 70-77 individually connected to the false signal lines 62-69 for causing resetting of all the binary devices in the event of a signal on one of the false signal lines. To give an example of a false signal, depression of button 32 would put a false signal on line 69.

Further in accordance with the invention there are provided sequence error-detection gate circuits which assure that the bistable devices can be operated only in the proper sequence, 54, 55, 56, 57. All of the gate circuits 94-99 are normally conductive and when any of them becomes nonconductive the 12 volt potential on line 160 is applied to the reset line 79. The proper sequence must be maintained.

This is accomplished by a combination of six "and" gates numbered 94, 95, 96, 97, 98, and 99, having outputs connected to diodes 100, 101, 102, 103, 104, and 105. Each one of these gates has two diodes of which one is connected to the read-in line of a binary device and of which the other is connected to an output line of a preceding binary device. The logical "and" is satisfied on the condition that an effort is made to activate a binary device when a preceding binary device is in its zero state. Each of "and" gates 94-99 functions to sense any coincidence that there may be with respect to the reset state of an associated binary device and an out-of-sequence signal on any of the true signal lines appurtenant to any of the succeeding binary devices. This undesired contingency can occur in six different ways: Attempts to set the second, third and fourth binary devices before the first, or to set the third or fourth binary device before the second, or to set the fourth binary device before the third. Accordingly, six "and" gates 94-99 are provided, one for each undesired contingency. That is, if in the wrong sequence an effort is made to activate binary device 57 before binary device 56 is activated then gate 99 will cause resetting, passing a positive output through diode 105 to line 79. If in the wrong sequence an effort is made to activate binary device 57 before binary device 54 is activated then gate 98 will cause resetting, passing a positive output through diode 104 to line 79. If in the wrong sequence an effort is made to activate binary device 57 before binary device 55 is activated then gate 97 will cause resetting, passing a positive output through diode 103 to line 79. If in the wrong sequence an effort is made to activate binary device 56 before binary device 55 is activated then gate 96 will cause resetting, passing a positive output through diode 102 to line 79. If in the wrong sequence an effort is made to activate binary device 56 before binary device 54 is activated then gate 95 will cause resetting, passing a positive output through diode

101 to line 79. If in the wrong sequence an effort is made to activate binary device 55 before binary device 54 is activated then gate 94 will cause resetting, passing a positive output through diode 100 to line 79.

The binary devices are generally similar and only one is discussed as representative. It is a simple NPN transistor binary quite similar to that shown in Fig. 10-7 at p. 371 of the text entitled "Pulse, Digital and Switching Wave Forms," Millman and Taub, McGraw-Hill Book Company, 1965, New York. A positive-going pulse supplied at 81 changes this binary from the zero to the one state. When the binary 54 is in the zero state a positive potential of approximately 12 volts is available at its collector output 106 which is coupled to the sequence error-detection gates 94, 95 and 96. On the other hand, when the binary is in the one state a positive potential of approximately 12 volts is available in its output 107 which is coupled to the next binary 55. Thus each binary either "tells" the sequence error-detection gates that it has not yet changed from zero to one or it goes to a one state to enable the next binary device.

When binary device 57 assumes its one state it transmits a negative level via line 33 to a transistorized relay driving system which comprises transistors 121 and 122. The emitter of transistor 121 is connected to the positive supply line 123. Its base is connected via resistor 124 to line 33 and the junction of diode 125 and resistor 126. A collector load resistor 127 is connected between its collector and ground. The collector is coupled by resistor 128 to the base of a grounded emitter transistor 122, the collector of which is in series circuit with the coil 34 of a solenoid, with resistor 129 and with the positive supply line 38, the solenoid being shunted by diode 130 for purposes of transient suppression. The solenoid actuates an armature 35 closing a circuit which is arranged to control an entrance door release or unlatching mechanism. Such unlatching mechanisms and releases and their input circuits are well known to those of skill in the art and need not be described in detail herein. The group of elements activated by line 33, i.e., 121, 122, 124, 127, 128, 129, 130, 34 and 35 is collectively referred to as a qualifying device. These elements collectively operate to qualify the person seeking admission and to permit access for a period of time.

The overall circuit functions as follows: When a correct code sequence is generated, the first code switch 21 output sets the first flip flop 54. An output level from this flip flop enables one side 88 of a two-side "and" gate 85 connected to the input of the next flip flop 55 and disables the error-detection gates 94, 95, 96 associated with first flip flop. Operation of the next correct code switch 22 on the control box 10 enables the other side of this previously mentioned two-side gate 85. The output now provided through this two-side gate sets the second flip flop 55 and disables its error-detection gate circuits 97-98. This process continues on 60 and 61 for the next two input pulses. On the fourth pulse the last flip flop 57 of the series is set, and an output pulse is coupled into both the relay driver 121, etc., and a monostable multivibrator delay circuit 131. The closure of the relay contacts 35 supplies a voltage which is then applied to a door unlatching device.

The circuit 131 is a monostable device and its function is to establish a predetermined access interval during which the solenoid 34 is energized. In this monostable configuration a positive triggering signal on line 132 induces a transition from the stable state to the quasi-stable state. The diode 142 carries a positive pulse to the base of transistor 135 but prevents negative voltages from reaching the transistor. The monostable circuit 131 remains in its quasi-stable state for a time which is very long in comparison with transition between states. Eventually, however, it automatically returns from the quasi-stable state to its stable state.

The monostable device herein shown comprises a first

NPN transistor 133 which has its collector coupled by resistor 134 to the base of a second NPN transistor 135. The emitters are grounded and the collectors of the transistors are provided with collector load resistors 136 and 137 connected to the 12 volt line 138. Transistor 135 has a base resistor 139 coupled between its base and ground.

The trigger circuit input 132 to the monostable device 131 originates at the collector of the output transistor 140 of the last binary device 57 and it passes, via capacitor 141, to the junction of a diode 142 and resistor 143, the latter two elements being connected between the base of transistor 135 and ground. An input signal to this monostable device 131 causes it to assume its quasi-stable state. After a predetermined time it returns to its stable state and applies to the base of transistor 144 via series capacitor 145 and series resistor 146 and shunt resistor 147, a signal which causes resetting to occur. The monostable device comprising the transistors 133 and 135 and all elements grouped between the input 132 and the output 169 are collectively referred to as a timer or timing means. This group of elements provides a signal that insures that the binary devices will be reset and the function of the qualifying device terminated, thereby limiting access to a short period of time.

The description now proceeds to the details of the arrangement by which the four binary devices are reset. All of the diodes 70-77 and 100-105 and 159 are connected to a common line 79 which constitutes the base input of a transistor 148. This is the reset driver transistor. An emitter resistor 149 is connected between its emitter and ground and a base resistor 150 is connected between its base and ground. The transistor is of an NPN type and is rendered conductive by a positive potential applied to its base. The collector of 148 goes to the supply line 38. Between line 38 and ground is disposed a time constant circuit comprising a capacitor 151 and a resistor 152. A pair of diodes 153 and 154 are connected in a chain with opposite polarity between the junction of 151, 152 and the emitter of 148. The junction of the cathodes of these diodes is connected to the principal reset line 155, which in turn is coupled to the bases of the right-hand transistors of each of binary devices 54-57. For example, the reset line 155 is coupled to the base of transistor 140 by the series combination of resistor 156 and diode 157. A positive pulse appearing on line 155 causes all of the bistable devices to be reset.

A positive pulse may be caused to occur on line 155 in either of two ways. Whenever the wrong push button is depressed or a proper push button (such as one of 21-24) is depressed out of the proper sequence, a positive potential appears on line 79 and this renders conductive the transistor 148 and it applies, via diode 153, a positive pulse to the reset line 155. The second mode in which the pulse can be applied to line 155 is associated with the first application of power (i.e., the turning on of the entire system) to line 38, whereupon a charging current flows through the time constant circuit 152, 151, applying a positive pulse, via diode 154, to line 155, thus assuring that whenever power is turned on all of the binary devices will be reset. The elements including transistor 148, having an input at line 79 and an output at reset line 155, constitute a reset driver, essentially an amplifier or repeater, i.e., effectively a part of the coupling between the principal OR gate and the common reset circuitry for the binary devices.

Reference is now made to the double inverter circuitry comprising transistor 158 and transistor 144. The function of this circuitry is to receive a pulse via 145, to amplify it and to apply it with proper polarity to line 79 via diode 159 at the termination of the predetermined access time. The transistors 158 and 144 have their emitters connected together and to ground, the base of transistor 158 being connected to the collector of transistor 144 and the collector of the transistor 158 being connected to diode 159. These transistors have collector load

resistors 190 and 161 and the base of the input transistor is provided with a base resistor 147. The elements 145, 146 and 147 constitute a differentiating circuit. The elements having an input at resistor 146 and an output connected to diode 154 constitute essentially an amplifier or repeater, in the coupling between the timer and input 159 of the OR gates.

The regulated rectifier system here employed is conventional and comprises a transformer 110 having a primary connected to the supply line and a secondary connected to a full wave rectifier network which feeds into a filter comprising series resistor 111, shunt capacitor 112, series filter choke 113, shunt capacitor 114, shunt resistor 115, and a regulator circuit 37 which includes transistor 116. The collector of transistor 116 is connected to the high potential terminal of resistor 115. A resistor 117 is inserted between its base and collector and a Zener stabilizing diode 118 between its base and ground. An emitter resistor 119 is connected between the emitter and ground and the 12 volt supply line 38 originates at this emitter; that line is connected via resistor 120 to line 36 and the reed switch 17 to supply power to bus bar 39.

A word is now in order about the operation of the monostable circuit 131. At the time that the last binary device 57 is set it applies to the base of transistor 135 a positive pulse, via line 132, capacitor 141, and positive pulse steering diode 142, which renders transistor 135 conductive, its collector simultaneously dropping in voltage and producing the leading edge of a square wave pulse. This pulse is a measure of the time delay between the setting of the last binary 57 and the resetting of all the binaries. The trailing edge of this square wave pulse is differentiated and the positive portion of the differentiated wave form is applied, via differentiating circuit 145, 146, 147 to the base of transistor 144 of the double inverter circuit which comprises transistors 158 and 144. The output of this double inverter is applied via diode 159 to line 79 to activate the reset driver to cause all of the binary devices to be reset. Thus all binary devices are automatically reset after a predetermined time delay following the setting of the last binary 57. This action limits the access time, i.e., the energization of solenoid 34, to a predetermined interval, which interval is substantially equal to the length of the square wave output occurring at the collector of transistor 135, which output is representative of the quasi-stable state of the monostable 131.

As transistor 135 becomes conductive, at the beginning of the quasi-stable state aforesaid, transistor 133 is cut off. During the stable state of the monostable, capacitor 165 had charged up, via the circuit comprising line 138, resistor 166, capacitor 165, the base emitter circuit of transistor 133, and ground, but when the transistor 133 was cut off, at the beginning of the quasi-stable state, then the capacitor slowly discharges through its time constant discharge circuit which includes resistors 168 and 166. At the end of the discharge of capacitor 165, transistor 133 becomes conductive and transistor 135 is cut off and the monostable resumes its stable state. As the transistor 135 is cut off its collector rises in voltage, terminating the square wave output, and it is this rise which is differentiated as stated aforesaid. As the rise occurs the diode 167 isolates the time constant discharge circuit of capacitor 165 from the collector, the diode then being cut off.

The three diodes numbered 170, 171 and 172 prevent equalizing currents from being exchanged among shunt filter capacitors 173, 174 and 175 in the voltage supply network, as to which the element 38 is the bus bar.

Thus it will be seen that the invention comprises, in a security system, the combination of a normally disabled switch-coded system (FIGS. 1-2, generally) and means including two complementary elements 14, 16 (FIGS. 5-6) for enabling the switch-coded subsystem only in response to a proper relative placement of those

elements by a carrier of one of them, 14. The normally disabled switch-coded subsystem comprises all of the parts of the system with the exception of the card 14 and the switching devices 17, 18 which are illustrated in FIGS. 4 and 5. The two complementary elements are the ferromagnetic insert in the card 13 and the magnet 16 with which the element 14 registers. One of these complementary elements is carried by the authorized employee. Only in response to the proper relative placement of the elements 14 and 16 by this employee is the subsystem enabled by reason of the closure of switch 17 (FIG. 2), which supplies power, and the opening of switch 18, removing the disabling ground connection from the input 80 of the first binary device 54.

The switch-coded subsystem comprises the larger number of individually manually operable switch elements 21-32 (FIG. 2), each adapted to energize lines, and a smaller number of true signal lines 58-61 (FIGS. 1-2) adapted to be energized in sequence and to be coupled by the patch board 53 (FIG. 2) to selected ones of the switch elements (21-24 in the embodiment herein shown) in accordance with a selected permutation representative of a switch code (the permutation here being 21-22-23-24). The subsystem also includes a plurality of false signal lines 62-69 (FIGS. 1-2) and means in the patch board 53 for coupling the non-selected manually operable switch elements 25-32 to the false signal lines 62-69. A plurality of binary devices 54-57 (FIG. 1) are cascaded to be activated in sequence as the signal lines 58-61 are energized by manipulation of the selected manually operable switch elements 21-24.

The subsystem further included error-detecting means 70-77 (FIG. 1) in circuit with the false signal lines 62-69 for detecting operation of any one of the non-selected manually operable switch elements 25-32. The system further includes means (i.e., the reset driver 148, etc.) responsive to the error-detecting means for resetting the binary devices.

An additional feature of the subsystem is the sequence error-detecting means which comprises a plurality of gates 94-99 (FIG. 1), each having two inputs, the gates being associated with all of the binary devices except the first. In any one of the gates, such as 99, one of the inputs is connected to the signal line (such as 61) for the binary device (such as 57) sought to be set and the other of the inputs is connected to an output of a preceding binary device, for example device 56. Each of such gates functions in such a manner that the binary device sought to be set (for example 57) cannot be set unless all of the preceding binary devices have been set. The inputs of all of the binary devices comprise individual "and" gates. Each of these "and" gates, for example gate 85, has two inputs. One input (for example 89) is connected to the appropriate signal line (59) and (except in the case of the gate 82 for the first binary device) the other input is connected to the output (for example 107) of the preceding binary device. In the case of gate 82, the other input is inhibited, except when switch 18 removes a ground from it. In the preferred embodiment of the invention all of the binary devices are transistorized flip flops.

While there has been shown and described what is at present considered to be the preferred embodiment of the invention, it will be understood by those skilled in the art that various changes and modifications may be made therein without departing from the scope of the invention as defined by the appended claims.

I claim:

1. In a security system, a sequence detector comprising:

- a plurality of true signal lines adapted to be energized in sequence in accordance with a selected code,
- a plurality of false signal lines each adapted when energized to provide a false signal,
- a plurality of binary devices arranged in a series, each binary device having

a two-terminal AND circuit set input and a reset input and a principal output, each binary device except the last having a state-indicating output, one terminal of each AND circuit set input being connected to its respective one of said true signal lines, the other terminal of the first AND circuit set input being adapted to be utilized for enabling and inhibiting as desired, the other terminals of the remaining AND circuit set inputs being severally connected to the principal outputs of the respective preceding binary devices so that in response to energizing of said true signal lines in sequence the binary devices are set in sequence,

a qualifying device coupled to the principal output of the last binary device and responsive to setting of the last binary device to perform its qualifying function, and

error-detecting and sequence-error-detecting means responsive to a false signal or to a departure from the desired sequence of true signals for resetting all of said binary devices comprising:

an OR gate having an output coupled to all of said reset inputs, said OR gate also having a first plurality of inputs individually connected to said false signal lines so that resetting occurs in response to a false signal,

said error detecting means further comprising:

a plurality of two-terminal input AND gates in number corresponding to the varieties of sequence errors that can occur, the last-mentioned AND gates having output circuits and

said OR gate having a second plurality of inputs individually connected to said output circuits, said last-mentioned AND gates being arranged in a sequence of groups, the groups being individually associated with all of the binary devices excepting the last, each group having collective input terminal connections to the state-indicating output of the associated binary device and each group having input connections in severality to the true signal lines of the succeeding binary devices so that the groups are normally enabled but are successively disabled as their associated binary devices are set and as true signals are received in proper sequence, a logical AND not being satisfied, but so that in response to the satisfaction of a logical AND by reason of an erroneous-sequence signal delivered over a true signal line a logical AND will be satisfied and a signal will be applied by one of said last-mentioned AND gates through said OR gate to cause resetting of all binary devices to occur.

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