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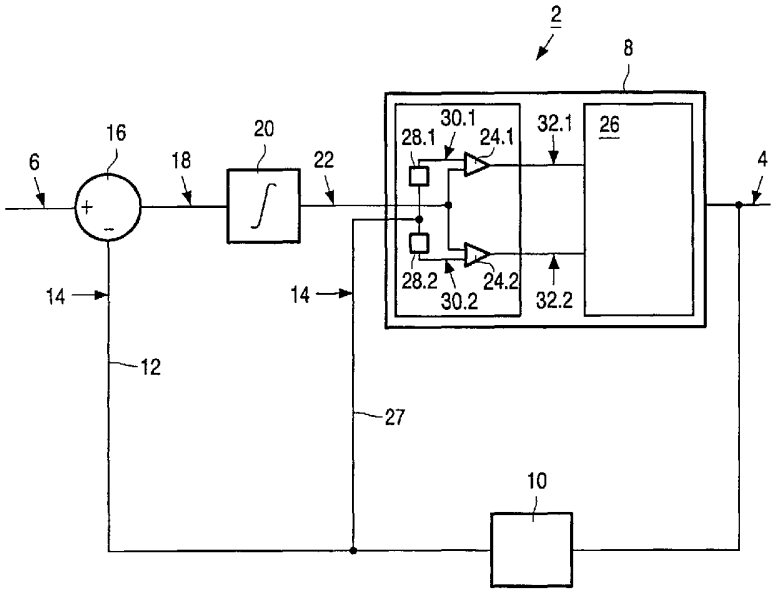
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(54) Title: SIGMA DELTA A/D CONVERTER WITH PSEUDO FLASH CONVERTER



(57) Abstract: The invention relates to a Sigma Delta A/D converter (2) for generating a N-bits digital output signal (4) on the basis of an analogue input signal (6), comprising a control loop which comprises a quantizer (8) comprising at least a comparator (24.1, 24.2) for generating the N-bits digital output signal (4) and a D/A converter (10) in a first feedback loop (12) of the control loop for generating an analogue version (14) of the N-bits digital output signal (4) on the basis of the N-bits digital output signal (4), wherein the quantizer (8) also comprises an Up-Down counter (26) which is coupled to the comparator (24.1, 24.2), wherein the D/A converter (10) is coupled to the comparator (24.1, 24.2) in a second feedback loop (27) of the control loop.

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Sigma Delta A/D converter with pseudo flash converter

The invention relates to a Sigma Delta A/D converter for generating a N-bits digital output signal on the basis of an analogue input signal, comprising a control loop which comprises a quantizer comprising at least a comparator for generating the N-bits digital output signal and a D/A converter in a first feedback loop of the control loop for generating an analogue version of the N-bits digital output signal on the basis of the N-bits digital output signal.

The said Sigma Delta A/D converter is known in actual practice. A particular example of the known Sigma Delta A/D converter can be found in United States Patent 5,982,313.

Sigma Delta A/D converters have come into wide spread use. With relative simple circuitry Sigma Delta A/D converters can achieve a relatively high accuracy. A simple circuitry can be achieved if the said quantizer is a 1-bit A/D converter. An advantage of the 1-bit A/D converter is that it has a perfect linearity. A disadvantage of the 1-bit A/D converter is that it generates large quantization errors. In principle, these large quantization errors result in a poor accuracy of the Sigma Delta A/D converter. However, according to Sigma Delta technology, an oversampling is applied (sampling rate greater than the Nyquist rate). As a consequence of this a large part of the quantization noise is shifted outside the signal bandwidth. This is called noise-shaping which allows subsequent filtering of the noise. In this way a relatively high accuracy and a relatively high Signal-to-Noise ratio can be achieved.

In order to further increase the Signal to Noise Ratio of the Sigma Delta A/D converter the loopfilter order and/or the oversampling ratio can be increased. Furthermore it is possible to increase the number of quantification levels which yields a multi-bit Sigma Delta A/D converter.

Increasing the number of quantization levels may be achieved by applying a quantizer comprising a multi-bit comparator, preferably a multi-bit flash comparator. An advantage of a flash comparator is that it adds a negligible delay in the control loop. However, a disadvantage of a N-bits flash comparator is that it requires many 1-bit comparators (for example [M-1] comparators for M different signal levels of an N-bits flash

comparator, wherein $M=2^N$ for M, N integers). Therefore, the flash comparator makes the Sigma Delta converter sizeable, expensive and the circuitry of the Sigma Delta complex.

It is an object of the invention to provide a multi-bit Sigma Delta A/D converter which is relatively compact and simple and which has a relative high signal bandwidth and a high SNR. For this, the invention provides a Sigma Delta A/D converter which is characterised in that the quantizer also comprises an Up-Down counter which is coupled to the comparator, wherein the D/A converter is coupled to the comparator in a second feedback loop of the control loop. The D/A converter is part of the first feedback loop of the control loop and is also part of the second feedback loop. The second feedback loop is a direct loop from the Up-Down counter to the comparator. As a consequence of the direct feedback of the second feedback loop, the combination of the comparator and the Up-Down counter acts as a flash comparator. The number of comparators in the Sigma Delta converter according to the invention is independent of the number of signal levels of the quantizer and generally much less than the number of comparators in the known Sigma Delta converter. Thus, according to the invention an effective, simple and compact multi-bit Sigma Delta A/D converter is achieved.

An embodiment of the Sigma Delta converter according to the invention is characterised in that the Sigma Delta A/D converter also comprises a combiner for generating a combined signal by combining the analogue input signal with the analogue version of the N-bits digital output signal, and a loopfilter for generating a filtered combined signal by filtering the combined signal, wherein the comparator is arranged for generating a control signal on the basis of the filtered combined signal and the analogue version of the N-bits digital output signal, and wherein the Up-Down counter is arranged for generating the N-bits digital output signal on the basis of the control signal. If the filtered combined signal is significantly greater (smaller) that the analogue version of the N-bits digital output signal then the control signal will control the Up-Down counter in such a way that it counts up (count down) with one unit for the next sample period. In this way the N-bits digital output signal can be increased or decreased for the subsequent sample period with one unit with respect to the current sample period.

A preferred embodiment according to the invention is characterised in that the quantizer comprises two comparators which are coupled to the Up-Down counter. With the first comparator it is checked whether the filtered combined signal is greater than the analogue version of the N-bits digital output signal plus a first pre-determined threshold value. This results in a first control signal. With the second comparator it is checked whether

the filtered combined signal is less than the analogue version of the N-bits digital output signal minus a second pre-determined threshold value. This results in a second control signal. The first and second control signals are fed to the Up-Down counter. If the filtered combined signal is greater (smaller) than the analogue version of the N-bits digital output signal plus (minus) the threshold value then the Up-Down counter counts up (down) with one unit for the next sample period. If the filtered combined signal lies within the interval determined by the first and second threshold values then the Up-Down counter keeps its value for the next sample period.

Preferably, the loopfilter of the Sigma Delta converter is a cascade of integrators depending on the order of the loopfilter for obtaining a rapid response of the Sigma Delta A/D converter to fluctuations of the analogue input signal.

In the accompanying drawing, in which a preferred embodiment of the Sigma Delta converter according to the present invention is shown for illustrative purposes:

The sole figure is a schematic overview of an embodiment of the Sigma Delta A/D converter according to the invention.

In the figure a schematic overview of a Sigma Delta A/D converter 2 according to the invention is shown. The Sigma Delta A/D converter 2 can generate a N-bits digital output signal 4 on the basis of an analogue input signal 6. The Sigma Delta A/D converter 2 comprises a control loop with a multi-bit quantizer 8 for generating the N-bits digital output signal 4. Furthermore, the control loop comprises a D/A converter 10 in a first feedback loop 12 for generating an analogue version 14 of the N-bits digital output signal on the basis of the N-bits digital output signal 4.

The Sigma Delta A/D converter 2 also comprises a combiner 16 for generating a combined signal 18 by combining the analogue input signal 6 with the analogue version 14 of the N-bits digital output signal. Furthermore, the Sigma Delta A/D converter 2 comprises a loopfilter 20 for generating a filtered combined signal 22 by filtering the combined signal 18. In this example the loopfilter 20 is an integrator.

The quantizer 8 comprises two comparators 24.1, 24.2 and an Up-Down counter 26. The combination of the two comparators 24.1, 24.2 and the Up-Down counter 26 acts as a flash converter and can be called a pseudo multi-bit flash comparator. The operation of the combination of the comparators 24.1, 24.2 and the Up-Down counter 26 will be discussed in more detail hereinafter.

The Sigma Delta A/D converter 2 comprises a second feedback loop 27. The analogue version 14 of the N-bits digital output signal can be fed to the quantizer 8 via the

second feedback loop 27. The time constant of the second feedback loop 27 is negligible to the time constant of the first feedback loop 12. Therefore, the quantizer 8 can dispose over the analogue version 14 of the N-bits digital output signal in a relative short time after the N-bits digital output signal 4 has been output of the Sigma Delta A/D converter 2. This is an important aspect of the Sigma Delta A/D converter 2 since it enables the quantizer 8 to operate as a multi-bit flash converter while only two comparators 24.1 and 24.2 are used.

In the quantizer 8 the analogue version 14 is fed to a first threshold setting block 28.1 and to a second threshold setting block 28.2 via the second feedback loop 27. The first threshold setting block 28.1 adds a positive predetermined first threshold value to the analogue version 14 of the N-bits digital output signal for generating a first reference signal 30.1. Subsequently, the first reference signal 30.1 is fed to the first comparator 24.1. The second threshold setting block 28.2 subtracts a positive predetermined second threshold value for generating a second reference signal 30.2. The second reference signal 30.2 is fed to the second comparator 24.2.

The first comparator 24.1 generates a first control signal 32.1 on the basis of the filtered combined signal 22 and the first reference signal 30.1. If the filtered combined signal 22 is greater than the first reference signal 30.1 then the first control signal 32.1 is set to logic value 1 by the first comparator 24.1. If the filtered combined signal 22 is less than the first reference signal 30.1 then the first control signal 32.1 is set to logic value 0. In an analogous way the second comparator 24.2 generates a second control signal 32.2 on the basis of the filtered combined signal 22 and the second reference signal 30.2. If the filtered combined signal 22 is greater than the second reference signal 30.2 then the second control signal 32.2 is set to logic value 1 by the second comparator 24.2. If the filtered combined signal 22 is less than the second reference signal 30.2 then the second control signal 32.2 is set to logic value 0.

The comparators 24.1, 24.2 are connected with the Up-Down counter 26 such that the first and second control signals 32.1, 32.2 can be fed to the Up-Down counter 26. If the first and second control signal 32.1, 32.2 are both equal to logic value 1 then the Up-Down counter 26 counts up with one unit. Consequently, the N-bits digital output signal 4 is increased with one unit. If the first and second control signal 32.1, 32.2 are both equal to logic value 0 then the Up-Down counter 26 counts down with one unit, such that the N-bits digital output signal 4 is decreased with one unit. If the first control signal 32.1 is equal to logic value 0 and the second control signal 32.2 is equal to logic value 1 then the Up-Down counter 26 maintains it value, such that the N-bits digital output signal is unchanged.

The Sigma Delta A/D converter 2 is connected to a system clock which is not depicted in the drawing for reasons of simplicity. The system clock is responsible for the timing of for example the comparators 24.1, 24.2, the Up-Down counter 26 and the D/A converter 10. Generally, the sample period of the system clock is chosen small enough to enable the Sigma Delta A/D converter 2 to follow rapid signal fluctuations of the analogue input signal 6. Each sample period the respective comparators 24.1, 24.2 generate the respective control signals 32.1, 32.1 which are subsequently fed to the Up-Down counter 26, and each sample period the Up-Down counter 26 can change one unit such that the N-bits digital output signal 4 is changed with one unit. In this way the Up-Down counter 26 can count up an down in a pre-determined interval. This pre-determined interval is the range of the N-bits digital output signal 4. Often, the interval of the Up-Down counter 26 is related to the number of bits N of the N-bits digital output signal 4.

The invention has been described according to a preferred embodiment. However, it should be noted that the invention can be practised otherwise than as specifically illustrated and described without departing from its spirit or scope. It is noted that in alternative embodiments of the Sigma Delta A/D converter according to the invention the multi-bit quantizer can also be provided with only one, three or more comparators.

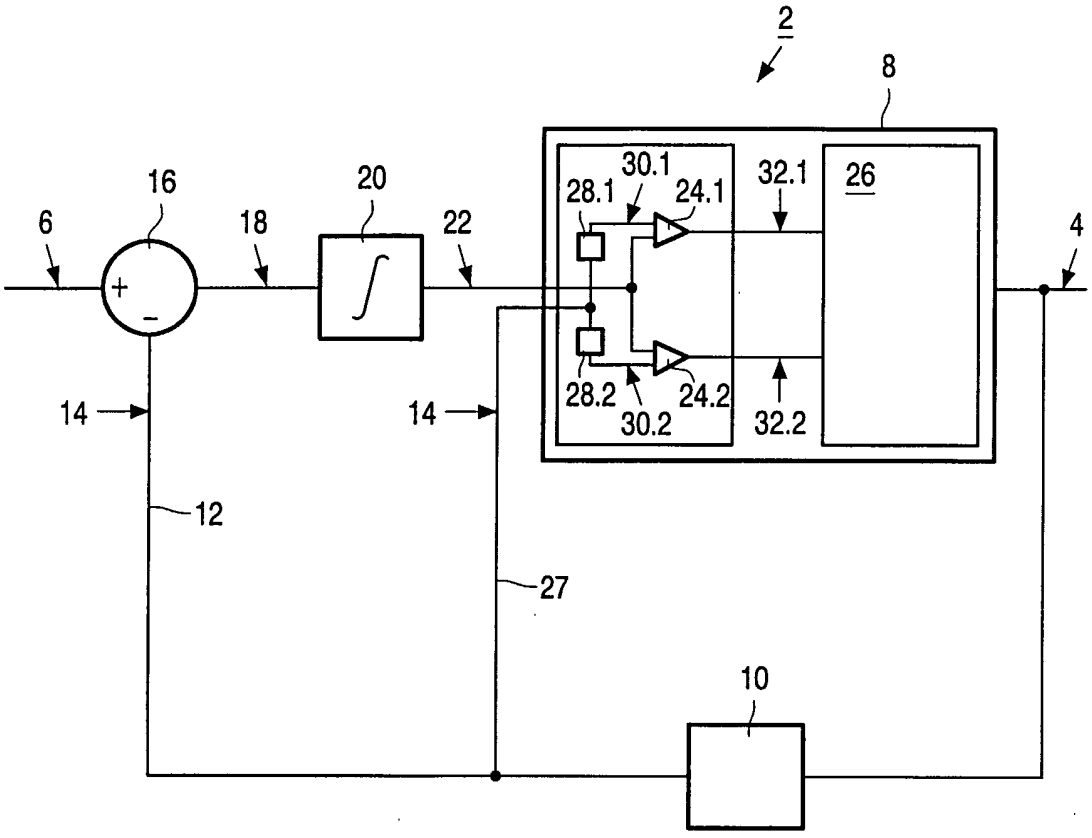
CLAIMS:

1. A Sigma Delta A/D converter (2) for generating a N-bits digital output signal (4) on the basis of an analogue input signal (6), comprising a control loop which comprises a quantizer (8) comprising at least a comparator (24.1, 24.2) for generating the N-bits digital output signal (4) and a D/A converter (10) in a first feedback loop (12) of the control loop for generating an analogue version (14) of the N-bits digital output signal (4) on the basis of the N-bits digital output signal (4),characterised in that, the quantizer (8) also comprises an Up-Down counter (26) which is coupled to the comparator (24.1, 24.2), wherein the D/A converter (10) is coupled to the comparator (24.1, 24.2) in a second feedback loop (27) of the control loop.

2. A Sigma Delta A/D converter according to claim 1, characterised in that, the Sigma Delta A/D converter (2) also comprises a combiner (16) for generating a combined signal (18) by combining the analogue input signal (6) with the analogue version (14) of the N-bits digital output signal, and a loopfilter (20) for generating a filtered combined signal (22) by filtering the combined signal (18), wherein the comparator (24.1, 24.2) is arranged for generating a control signal (32.1, 32.2) on the basis of the filtered combined signal (22) and the analogue version (14) of the N-bits digital output signal, and wherein the Up-Down counter (26) is arranged for generating the N-bits digital output signal (4) on the basis of the control signal (32.1, 32.2).

3. A Sigma Delta A/D converter according to claim 2, characterised in that, the loopfilter (20) is an integrator.

4. A Sigma Delta A/D converter according to one of the preceding claims, characterised in that, the quantizer (8) comprises two comparators (24.1, 24.2) which are coupled to the Up-Down counter (26).


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28.2
30.2
24.2
32.2
12
27
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INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/IB 03/02008

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03M3/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	US 2002/186776 A1 (COSAND ALBERT E) 12 December 2002 (2002-12-12) page 1 -page 4; figure 3	1-4
X	AZEREDO LEME C ET AL: "Oversampled interface for IC sensors" INSTRUMENTATION AND MEASUREMENT TECHNOLOGY CONFERENCE, 1994. IMTC/94. CONFERENCE PROCEEDINGS. 10TH ANNIVERSARY. ADVANCED TECHNOLOGIES IN I & M., 1994 IEEE HAMAMATSU, JAPAN 10-12 MAY 1994, NEW YORK, NY, USA,IEEE, 10 May 1994 (1994-05-10), pages 652-655, XP010121989 ISBN: 0-7803-1880-3 page 652 -page 655; figures 1-3	1-4

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
7 October 2003	17/10/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Morrish, I

INTERNATIONAL SEARCH REPORT

Int[illegible]onal Application No
PCT/IB 03/02008

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 736 953 A (YAMAGUCHI MOTOI) 7 April 1998 (1998-04-07) column 1 -column 10; figures 1-5	1-4
A	EP 0 454 407 A (HUGHES AIRCRAFT CO) 30 October 1991 (1991-10-30) page 3 -page 7; figure 1	1-4

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte onal Application No
PCT/IB 03/02008

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