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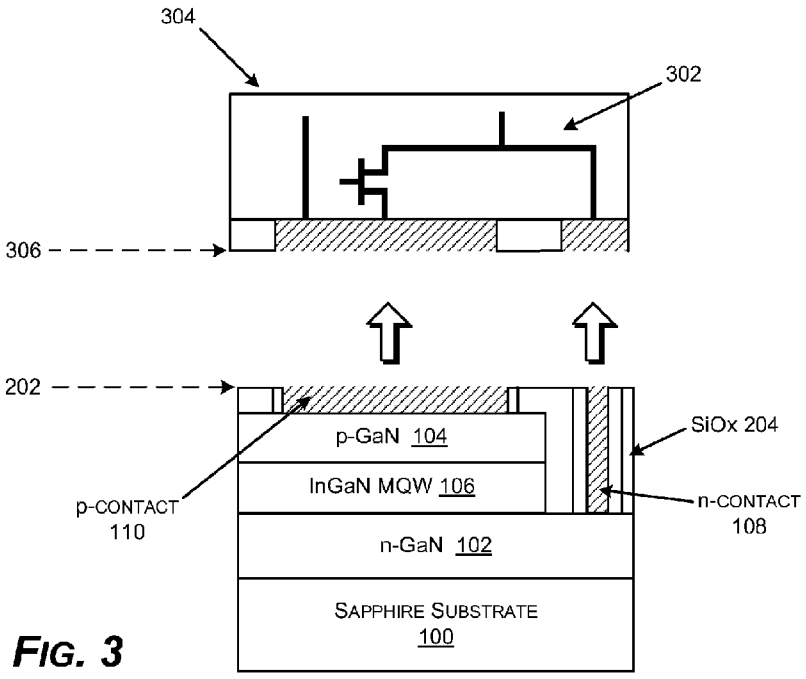

FIG. 3

(57) Abstract: Direct- bonded LED arrays and applications are provided. An example process fabricates a LED structure that includes coplanar electrical contacts for p-type and n-type semiconductors of the LED structure on a flat bonding interface surface of the LED structure. The coplanar electrical contacts of the flat bonding interface surface are direct-bonded to electrical contacts of a driver circuit for the LED structure. In a wafer-level process, micro-LED structures are fabricated on a first wafer, including coplanar electrical contacts for p-type and n-type semiconductors of the LED structures on the flat bonding interface surfaces of the wafer. At least the coplanar electrical contacts of the flat bonding interface are direct-bonded to electrical contacts of CMOS driver circuits on a second wafer. The process provides a transparent and flexible micro-LED array display, with each micro-LED structure having an illumination area approximately the size of a pixel or a smallest controllable element of an image represented on a high-resolution video display.

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DIRECT-BONDED LED ARRAYS AND APPLICATIONS

RELATED APPLICATIONS

[0001] This patent application claims the benefit of priority to U.S. Provisional Patent Application No. 62/472,363 to Tao et al., entitled "Direct Bonded LED Arrays and Applications," filed March 16, 2017 and incorporated by reference herein, in its entirety.

BACKGROUND

[0002] MicroLEDs, also known as micro-LEDs, μLEDs, and "mLEDs" as used herein, are gaining significant attraction as an emerging flat panel display technology. But as of yet, mLED displays have not been mass-produced or commercialized widely. The mLED displays are arrays of microscopic LEDs forming individual pixel elements. Compared to the widespread LCD technology, mLED displays provide greater contrast and faster response times, while using less energy.

[0003] Along with organic light-emitting diodes (OLEDs), in which a film of organic compound is stimulated to emit electroluminescence, mLEDs can be used in small low-energy devices such as smart phones and smart watches, where battery power is at a premium.

[0004] Both mLEDs and OLEDs require less energy than conventional LCD systems. Unlike OLEDs, however, the mLED technology utilizes conventional III-V inorganic semiconductor materials (GaN, InGaN, etc.) for use as self-emissive LEDs for lighting and display, which can offer higher overall brightness (e.g., 30x over OLEDs) and higher contrast than OLED products, with higher efficiency in lux per watt (lux/W) light output. The mLED technology can also provide a longer working life for the product that is hosting the mLED

technology. Versions of this mLED array technology may be ideal for automotive, virtual reality, and augmented reality displays.

SUMMARY

[0005] Direct-bonded LED arrays and applications are provided. An example process fabricates a LED structure that includes coplanar electrical contacts for p-type and n-type semiconductors of the LED structure on a flat bonding interface surface of the LED structure. The coplanar electrical contacts of the flat bonding interface surface are direct-bonded to electrical contacts of a driver circuit for the LED structure. In a wafer-level process, micro-LED structures are fabricated on a first wafer, including coplanar electrical contacts for p-type and n-type semiconductors of the LED structures on the flat bonding interface surfaces of the wafer. At least the coplanar electrical contacts of the flat bonding interface are direct-bonded to electrical contacts of CMOS driver circuits on a second wafer. The process provides a transparent and flexible micro-LED array display, with each micro-LED structure having an illumination area approximately the size of a pixel or a smallest controllable element of an image represented on a high-resolution video display.

[0006] This summary is not intended to identify key or essential features of the claimed subject matter, nor is it intended to be used as an aid in limiting the scope of the claimed subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Certain embodiments of the disclosure will hereafter be described with reference to the accompanying drawings, wherein like reference numerals denote like elements. It should be understood, however, that the accompanying figures illustrate the various implementations described herein and are not meant to limit the scope of various technologies described herein.

[0008] Fig. 1 is a diagram of an example conventional nitride light emitting diode (LED).

[0009] Fig. 2 is a diagram of an example LED structure suitable for direct-bonding of electrical contacts enabling wafer level, chip array-level, and individual chip-level construction of direct-bonded micro-LED structures.

[0010] Fig. 3 is a diagram of the example LED structure of Fig. 2, in a direct-bonding operation with driver circuitry.

[0011] Fig. 4 is a diagram of an example process of fabricating the LED structure of Fig. 2.

[0012] Fig. 5 is a diagram of a first stage of fabricating an example LED array display.

[0013] Fig. 6 is a diagram of a second stage of fabricating the example LED array display.

[0014] Fig. 7 is a diagram of a third stage of fabricating the example LED array display.

[0015] Fig. 8 is a diagram of a fourth stage of fabricating the example LED array display.

[0016] Fig. 9 is a diagram of a fifth stage of fabricating the example LED array display.

[0017] Fig. 10 is a diagram of a completed LED array display and optional components.

[0018] Fig. 11 is a block diagram of an example process of making a direct-bonded LED structure.

DESCRIPTION

[0019] This disclosure describes example direct-bonded light emitting diode (LED) arrays and applications. New processes for forming actively driven mLED (microLED) structures and display cells are described, including example processes of array-bonding III-V compound semiconductor mLEDs to silicon driver chips to form actively driven mLED display cells. Some of these processes may be used to mass-produce mLED array displays.

Example Processes and Structures

[0020] Fig. 1 shows an example of a conventional epilayer structure 50 of a light emitting diode (LED) over a sapphire substrate 100, illustrating and comparing some LED components used in example structures and processes described herein. The example conventional LED structure 50 may produce green or blue light, for example. Semiconductor materials are layered on a carrier, such as a sapphire substrate 100. The large mismatches in lattice constants and thermal expansion coefficients between GaN and sapphire 100 would cause high crystalline defect densities in the GaN films, which leads to degradation of device performance; hence a lattice and CTE matched buffer material 101 is deposited on sapphire 100 to grow GaN. Optoelectronic devices like the conventional LED structure 50 utilize semiconductor doping, for example, a small amount of silicon or germanium is added to gallium nitride (GaN) to make the GaN a conductor for electrons (n-type) n-GaN 102, and a small amount of magnesium is added to the gallium nitride (GaN) to make the GaN into a conductor for holes (electron holes) (p-type) p-GaN 104. Between the layer of n-GaN 102 and the layer of p-GaN 104 is sandwiched an ultrathin layer of a light-producing quantum well or multiple quantum well (MQW) material, that has a smaller band gap (and slightly less conductivity) than either the n-GaN 102 and the p-GaN 104, such as indium gallium nitride InGaN, a semiconductor material made of a mix of gallium nitride (GaN) and indium nitride (InN). InGaN is a ternary group III/group V direct band gap

semiconductor. The example InGaN/GaN or InGaN MQW layer 106 provides quantum confinement, or discrete energy subbands, in which the carriers can have only discrete energy values, providing better performance in optical devices. Conventional LED structures 50 may have many variations in the number or layers used, and the materials used for each layer. In Fig. 1, the layers, and especially the MQW layer 106, are not shown to relative scale.

[0021] The example conventional LED structure 50 is characterized by an n contact 108 and a p contact 110 at different vertical levels on different surfaces of the conventional LED structure 50. The difference in vertical heights between p contact 110 and n contact 108 is conventionally compensated for by wire bond or solder connections. Or, an example conventional structure 50 may have an n contact 108 that is not exposed (not shown).

[0022] Figs. 2-3 show an example LED structure 200 and process overview, for direct-bonding LED components containing III-V semiconductor elements to driver circuitry, for making mLED array displays. The example LED structure 200 provides an ultra-flat bonding interface 202, made flat by chemical-mechanical polishing (CMP) for example, with both n contact 108 and p contact 110 surrounded by an insulator 204, such as a silicon oxide, and exposed on the ultra-flat bonding interface 202 with respective coplanar conductive footprints 206 & 208 on the ultra-flat bonding interface 202.

[0023] The n contact 108 and p contact 110 may be made of a metal, or combination of alloyed metals, or laminated metals that enhance direct bonding. Besides metal composition, the ultra-flat bonding interface 202 itself also facilitates direct bonding between the n and p contacts 108 & 110 and respective conductive surfaces being bonded to. The ultra-flat bonding interface 202 fabricated by damascene methods, for example, is also ultra-clean, and flat within a few tens of nanometers, such as less than 1/4 the wavelength of an illumination source of monochromatic green light at the 546.1 nm or helium-neon red laser light at 632.8 nm. In some embodiments the roughness of the

flat polished surface 202 is less than 5% of the wavelength of an illumination source and preferably less than 10 nm.

[0024] Fig. 3 shows an example direct-bonding process 300 between the example LED structure 200 of Fig. 2, and a driver circuit 302 on a chip 304, to form LED circuitry, such as thin-film transistor (TFT) drivers. The example direct-bonding process 300 can be performed at the level of individual chips, or at a chip array level, or at wafer level. For subsequent lift-off and thinning, wafer level direct-bonding may be the best approach.

[0025] In an implementation, the mLED ultra-flat bonding interface 202 can be bonded to the respective ultra-flat bonding interface 306 of a silicon-based driver integrated circuit (IC) 304, for example. The ultra-flat bonding interface 306 may have a contacting surface that is topped with a flat silicon oxide layer and copper (Cu) pads to facilitate direct-bonding, for example direct-bonding via a ZiBond® brand process or a DBI® brand process, to form LED circuitry (Xperi Corporation, San Jose, CA). In an implementation, the sapphire substrate 100 may then be laser-lifted off. If desirable, both top and bottom sides can be thinned further to make the entire stack flexible.

[0026] Fig. 4 shows stages of example structure fabrication, illustrating an example process flow for making an LED structure 200 suitable for direct-bonding with a silicon driver ICs 304, for example.

[0027] In a first stage 400 of the example process flow, an example wafer, such as a sapphire substrate 100, is built up with beginning epitaxial layers of n-GaN 102, InGaN MQW 106, and p-GaN 104.

[0028] In a second stage 402 of the example process flow, the top epitaxial layers are patterned and etched to expose the n-GaN layer 102 at specific locations 404. Although the single exposed location 404 is shown at the edge at the die, there may be more than one location. For example, one or more through-vias may expose the n-GaN layer 102. The patterning resist can be left on.

[0029] In a third 406 stage of the example process flow, an insulator or dielectric, such as a silicon oxide layer 204 is deposited to cover both the exposed p-GaN 104 and the exposed n-GaN 102, at least at the location of the contacting pads.

[0030] In a fourth stage 408 of the example process flow, the silicon oxide layer 204 is patterned and etched over the p-GaN 104 and n-GaN 102 layers to make cavities 410 through the silicon oxide 204 for conductive metals to become the electrodes of the LED structure 200. In an implementation, the total thickness of the p-GaN 104 layer and the MQW 106 layer is approximately 2μm, making the structure at this stage suitable for one-step etching and metallization (MQW layer 106 not shown to scale). One or more of such cavities 410 can be formed to form one or more electrodes contacting the n-GaN 102 layer and the p-GaN 104 layer.

[0031] In an alternative implementation, the example process deposits a flat silicon oxide layer 204 as in the third stage 406 above, then bonds this oxide surface directly with the driving chip(s) 304 using a ZiBond® brand direct-bonding process, or other direct bonding technique. Then, through-silicon-vias (TSVs) are drilled to create the electrical connectivity from the n contact 108 and the p contact 110 to the driver chip 304.

[0032] In a fifth stage 412 of the example process flow, the cavities 410 can be metalized with a conductive material 414. In an implementation, barrier and seed layer coatings 416 may be applied and formed, then cavities filled with the conductor 414, followed by annealing, and chemical-mechanical planarization (CMP). In an implementation, a low melting temperature metal, such as indium, may be coated in the cavities.

[0033] In a sixth stage 418 of the example process, a top surface of the example LED structure 200 is plasma-activated 420 for the direct-bonding operation. Plasma-activation 420 may be optional for some types of direct-bonding techniques, while in others, the plasma-activation step 420 enhances the bond strength between two metal surfaces, for example, during contact

bonding. Plasma-activation 420 may also be applied to the opposing surfaces to be bonded on the driver chip(s) 304.

[0034] In various implementations, the example process flow depicted in Fig. 4 may include picking and transferring many small LED chips with high throughput, and direct-bonding at very fine pitch, for example at a pitch of less than 1 mm (even smaller pitch for making micro-projectors), and at a 0.05 mm spacing, and in various implementations all the way down to a 12 um pitch with 6um bump. The pixel array optics achieve high parallelity of the LED dies 200 to the Si dies 304. Post-processing, such as thinning and laser lift-offs, can be accomplished because the direct-bonding applied results in the flat topography and strong bonding interfaces achieved.

[0035] Figs. 5-9 show an example process for creating a thin, transparent, and flexible mLED array display 500, in which a wafer 502 with the LED structures 200 made by the process of Fig. 4 are now bonded to (for example) a CMOS driver chip wafer 504 to make the transparent and flexible array display 500.

[0036] In Fig. 5, in an implementation, after the flat and activated surface on the LED device wafer 502 is formed, the CMOS wafer 504 is planarized with CMP or other means of obtaining an ultra-flat surface, and plasma-activated 420.

[0037] In Fig. 6, the two wafers 502 & 504 are bonded. For example, the first wafer 502 with the LED structures 200 and with coplanar bonding surfaces of the n contacts 108 and p contacts 110, and the second wafer 504 with CMOS driver chips 304, are brought together for direct-bonding between metallic conductors and in an implementation, between nonmetallic dielectric surfaces 602 also. Exposed silicon oxide of the first wafer 502 in contact with exposed silicon oxide of the second wafer 504 bonds first through oxide bonding, as with a ZiBond® brand direct-bonding process. The metal contact pads of the respective wafers 502 & 504 form a metal-to-metal bond during higher-than-room-temperature annealing, as with a DBI® brand direct-bonding process.

The bonding interface 604 may be annealed at approximately 100-200 °C to form a strong direct bond interface, such as the ZiBond® or DBI® brand direct-bond interface.

[0038] An optical reflective coating, such as distributed Bragg reflector (DBR) 606 (not shown to relative scale), can be deposited to increase light output of the package by choosing different types and thickness of the dielectric layers on top of wafer 502 at the interface (606) between the first wafer 502 and the second wafer 504. Alternatively, the DBR 606 could also be formed on top of the second wafer 504 prior to bonding. In this orientation of a DBR 606, light can escape from the sapphire side of the device. If DBRs 606 are formed on the first wafer 502, then the thin dielectrics need to be deposited at the end of the second stage 402 or the third stage 406 of the process shown in Fig. 4. The DBR 606 is a structure formed from multiple layers of alternating materials with varying refractive index, or by periodic variation of some characteristic, for example, thickness of the dielectrics, resulting in periodic variation in the effective refractive index. These thin layers of dielectric coatings may be the combination of silicon oxide, magnesium fluoride, tantalum pentoxide, zinc sulfide, and titanium dioxide, for example. A silicon oxide SiOx layer on a top surface of the compound wafer 502 can also serve as the last of the coatings which is then bonded directly with direct bonding techniques, such as a ZiBond® or a DBI® process, to wafer 504.

[0039] In another embodiment, DBR may be formed at between sapphire and n-GaN. In this orientation, the light will be reflected towards CMOS wafer 504. However, less amount of light will escape as CMOS chip would be obstructing the escape route.

[0040] In Fig. 7, the thin-film transistor (TFT) backplane can be thinned 702, which can be facilitated by a ZiBond® brand direct-bonding process. Then the non-transistor parts 704 of the thinned backplane can also be etched away. In this embodiment, the location of one or more n-contacts 108 and p-contacts 110 can be designed such that they may be exposed from the backside after etching

of the backplane; and hence can be contacted for power delivery from the back side.

[0041] In Fig. 8, the thinned and etched transistor surface may be coated with a polyimide (PI) layer 802 or any other dielectric material for protection.

[0042] In Fig. 9, a laser-lift-off of the sapphire substrate layer 100 may be performed, and this exposed side of the wafer 502 then coated with a flexible organic substrate 902.

[0043] In another embodiment, the process to etch and backfill by the transistor backplane by PI may be skipped before a laser-lift-off of the sapphire substrate layer 100. In this embodiment, one or more through- electrodes may be needed in the backplane for power delivery to the electrodes.

[0044] Fig. 10 shows operational access available on all sides of example transparent and flexible mLED array displays 500 created with direct-bonding. This versatility is due at least in part to the strong bonds possible with direct bonding, such as DBI® and ZiBond® brand bonding processes, which result in a final structure able to tolerate further processing on multiple sides of the structure 500. For example, besides lifting off the transparent (e.g., sapphire) substrate 100 to make a flexible display 500 bonded to a flexible organic substrate 902, post grinding may be applied and further lift-off performed to make the display thinner, more transparent, and more flexible.

[0045] The backside of the mLED array display 500 may be added onto with backside build-up layers 1002 for further 3D integration to attach to memory, printed circuit boards (PCBs), tactile and other sensors, and so forth.

[0046] One or more optical waveguides 1004 may be integrated on top of the transparent substrate 902 to transmit optical signals from the LED elements, and also lines for electrical signals may be added. In an implementation, the one or more optical waveguides 1004 are attached to the example LED array display 500 by a direct-bonding technique.

[0047] On the sides of the example mLED array display 500, an edge emitting configuration 1006 may be added, and/or optical waveguides on the

sides, similar to the one or more optical waveguides 1004 on top. In this embodiment, reflectors may be needed on both sides of the LED devices 200, at layer 902, as well as at the direct-bond (e.g., ZiBond®) interface 604 / 606.

[0048] The structure of the example mLED array display 500 enables multi-junction stacking of compound semiconductors, for solar cells and solar panels, for example.

[0049] The sides of the example mLED array display 500 can also accommodate cooling structures 1008.

[0050] After removing sapphire layer 100, as in Fig. 8, the surface may be roughened and indium tin oxide (ITO) added to improve the electrical conductivity of the LEDs.

[0051] The example steps just described and illustrated above provide direct-bonded light emitting diode (LED) arrays 500, for example arrays of mLEDs, wherein group III-V semiconductor elements are direct-bonded to LED driver circuitry, in wafer-level processes, for example. The arrays 500, made through a direct-bonding process, may be flexible, and possess an optically transparent surface.

[0052] In general, the example compound semiconductor-based LED array devices 500 are made with a flat surface composed of coplanar metal regions and dielectric regions. The coplanar metal regions are electrically connected to the active regions of the compound semiconductors of each LED element.

[0053] The above compound semiconductor-based LED array structures 500 may include bonds to a CMOS based device connected in a direct-bonding manner. The metal regions and the dielectric regions of the compound semiconductor-based LED array device 500 may be bonded directly to the respective metal regions and dielectric regions of the CMOS based device. Although described with respect to a wafer level process, the example process of Figs. 5-9 can be used not only for wafer-to-wafer (W2W) processes, but also die-to-die (D2D), or one or multiple dies-to-wafer (D2W) processes.

[0054] The resulting example LED array structures 500 may also have other characteristics and features:

[0055] The resulting LED array structures 500 may have an absence of substrate where the group III-V-based semiconductor light-emitting devices are grown. Further, a surface of the microstructure of the group III-V semiconductor-based light-emitting devices can be advantageously roughened for improved light extraction.

[0056] The electrode shape for electrically connecting to the n-GaN 102 and p-GaN 104 active regions via a direct-bonding process, such as a DBI® brand direct-bonding process, can be specially designed, such as frame-traced dot arrays for the electrode or contact 108 of the n-GaN 102 region, and a dot array in a circular or square area for the electrode or contact 110 of the p-GaN 104 region.

Example Processes

[0057] Fig. 11 shows an example method 1100 of making a direct-bonded LED structure. In the flow diagram, operations of the example method 1100 are shown in individual blocks.

[0058] At block 1102, a LED structure is fabricated with electrical contacts to p-type and n-type semiconductor elements coplanar on a first surface comprising a flat bonding interface of the LED structure.

[0059] At block 1104, the first surface is direct-bonded to a second surface comprising a flat bonding interface of a driver circuit for the LED structure.

[0060] The direct-bonding operation used in the example method 1100, such as a ZiBond® or a DBI® brand direct-bonding process, may be applied in a wafer level, single chip-level, or a chip array-level process.

[0061] In the specification and appended claims: the terms “connect,” “connection,” “connected,” “in connection with,” and “connecting,” are used to mean “in direct connection with” or “in connection with via one or more

elements." The terms "couple," "coupling," "coupled," "coupled together," and "coupled with," are used to mean "directly coupled together" or "coupled together via one or more elements."

[0062] While the present disclosure has been disclosed with respect to a limited number of embodiments, those skilled in the art, having the benefit of this disclosure, will appreciate numerous modifications and variations possible given the description. It is intended that the appended claims cover such modifications and variations as fall within the true spirit and scope of the disclosure.

CLAIMS

1. An apparatus, comprising:

a direct-bonded light emitting diode (LED) array; and

a flat bonding interface of at least one LED element in the direct-bonded LED array, each flat bonding interface comprising at least first and second coplanar conductive areas comprising electrical contacts of each LED element.

2. The apparatus of claim 1, wherein each first coplanar conductive area in each flat bonding interface comprises an electrical contact to an n-type layer of a group III-V semiconductor of each LED element; and

wherein each second coplanar conductive area in each flat bonding interface comprises an electrical contact to a p-type layer of a group III-V semiconductor of each LED element.

3. The apparatus of claim 2, wherein the first coplanar conductive area comprises multiple conductive contacts to the n-type layer, and the second coplanar conductive area comprises multiple conductive contacts to the p-type layer.

4. The apparatus of claim 2, where in the first coplanar conductive area is electrically connected to the n-type layer at multiple locations, and the second coplanar conductive area is electrically connected to the p-type layer at multiple locations.

5. The apparatus of claim 2, further comprising a frame-traced dot array electrode as the coplanar electrical contact to n-type layer of the group III-V semiconductors of each LED element; and

a circular or square dot array electrode as the coplanar electrical contact to p-type layer of the group III-V semiconductors of each LED element.

6. The apparatus of claim 1, further comprising at least a third coplanar conductive area electrically isolated from the first conductive area and the second conductive area, the third coplanar conductive area for thermal dissipation, for connecting to an electrical ground, or for conducting a signal.

7. The apparatus of claim 1, wherein each LED in the direct-bonded LED array comprises a micro-LED having an illumination area approximately a size of a pixel of a high-resolution video display, or an illumination area approximately a size of a smallest controllable element of an image represented on the high-resolution video display.

8. The apparatus of claim 1, further comprising at least a direct metal-to-metal contact bond between each first and second conductive area in each flat bonding interface of each LED element, and respective conductive contacts of driver circuitry for each LED element, the driver circuitry direct-bonded to each flat bonding interface of each LED element.

9. The apparatus of claim 8, further comprising a direct dielectric-to-dielectric contact bond between dielectric areas of each flat bonding interface of each LED element and respective dielectric areas of each flat bonding interface of each instance of the driver circuitry.

10. The apparatus of claim 9, wherein each direct dielectric-to-dielectric contact bond comprises at least one plasma-activated surface of the direct dielectric-to-dielectric contact bond.

11. The apparatus of claim 1, further comprising a flexible organic substrate of the direct-bonded LED array providing a flexible and transparent direct-bonded LED array display.

12. The apparatus of claim 1, further comprising a distributed Bragg reflector (DBR) located at a top of each LED element, at a bottom of each LED element, or integrated in the flat bonding interface of each LED element.

13. The apparatus of claim 1, further comprising an optical waveguide bonded to a top surface or a side surface of the direct-bonded LED array.

14. The apparatus of claim 1, further comprising a semiconductor element bonded to a top surface or a side surface of the direct-bonded LED array.

15. A process, comprising:

fabricating a LED structure to include coplanar electrical contacts for p-type and n-type semiconductors of the LED structure on a first bonding surface of the LED structure; and

direct-bonding at least the coplanar electrical contacts of the first bonding surface to electrical contacts of a driver circuit for the LED structure.

16. The process of claim 15, further comprising performing the direct-bonding between a first wafer having an array of the LED structures and a second wafer having a corresponding array of instances of the driver circuit.

17. The process of claim 16, wherein the first wafer comprises an array of micro-LED structures, each micro-LED structure having an illumination area approximately a size of a pixel of a high-resolution video

display, or an illumination area approximately a size of a smallest controllable element of an image represented on the high-resolution video display.

18. The process of claim 15, further comprising performing the direct-bonding between a first single chip comprising the LED structure and a second single chip comprising the driver circuit, or between a first chip array comprising instances of the LED structure and a second chip array comprising instances of the driver circuit.

19. A process, comprising:

providing a first wafer;

building semiconductor layers of LED structures on the first wafer;

patterning the first wafer with a resist and etching the wafer to expose an n-type semiconductive layer of each LED structure;

depositing a silicon oxide layer to cover both a p-type semiconductive layer and the exposed n-type semiconductive layer of each LED structure;

patterning and etching the silicon oxide over the p-type semiconductive layer and the n-type semiconductive layer of each LED structure to form cavities in the silicon oxide down to the surfaces of the p-type semiconductive layer and the n-type semiconductive layer of each LED structure;

metalizing the cavities in the silicon oxide;

planarizing the silicon oxide and the metalized cavities to make a flat bonding surface with coplanar contacts of the p-type semiconductive layer and the n-type semiconductive layer of each LED structure;

plasma-activating a surface of the first wafer;

bonding the activated surface of the first wafer to the surface of the second wafer; and

annealing the bonded wafers to make a direct-bonded LED array display.

20. The process of claim 19, wherein each LED structure of the first wafer is direct-bonded to a CMOS based device of the second wafer, wherein metal regions and dielectric regions of each LED structure on the surface of the first wafer are direct-bonded to metal regions and dielectric regions, respectively, of the CMOS based devices of the second wafer.

21. The process of claim 19, further comprising thinning a thin-film transistor (TFT) backplane of the direct-bonded LED array display.

22. The process of claim 21, further comprising coating the thinned backplane with a polyimide (PI) layer for protection.

23. The process of claim 15, further comprising removing the first wafer through a laser-lift-off and coating the remaining surface with a flexible organic substrate, to make a transparent and flexible direct-bonded LED array display.

24. A process, comprising:

forming semiconductor layers of LED structures on a first wafer;

forming an exposed n-type semiconductive layer of each LED structure;

forming an exposed p-type semiconductive layer of each LED structure;

forming a planarized damascene layer with respective coplanar conductive areas of the planarized damascene layer contacting the exposed n-type semiconductive layer and the exposed p-type semiconductive layer of each LED structure;

plasma-activating a surface of the planarized damascene layer of the first wafer;

bonding the plasma-activated surface of the first wafer to a surface of a second wafer; and

annealing the bonded wafers to make a direct-bonded LED array display.

25. An apparatus, comprising:

a direct-bonded light emitting diode (LED) array; and

a planarized interface of at least one LED element in the direct-bonded LED array, each planarized interface comprising at least first and second coplanar conductive areas comprising electrical contacts of each LED element.

26. The apparatus of claim 25, further comprising a direct dielectric-to-dielectric contact bond between dielectric areas of each planarized interface of each LED element and respective dielectric areas of each planarized interface of each instance of a driver circuitry.

27. The apparatus of claim 25, wherein each direct dielectric-to-dielectric contact bond comprises at least one plasma-activated surface of the direct dielectric-to-dielectric contact bond.

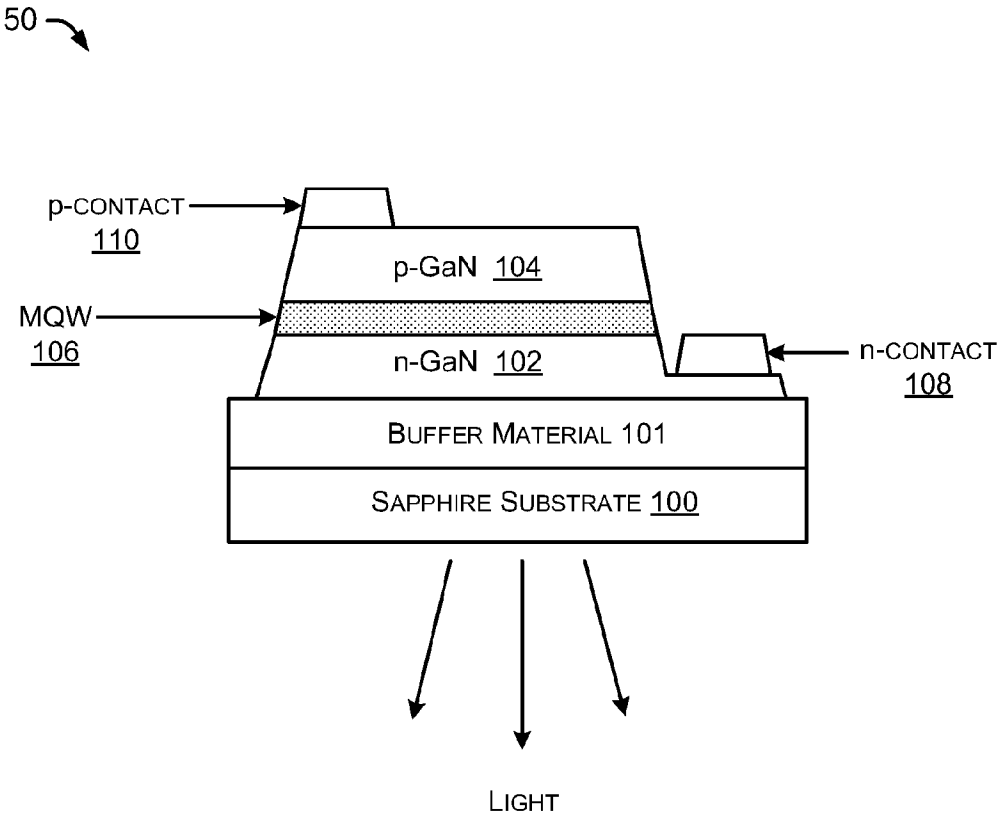

FIG. 1
(PRIOR ART)

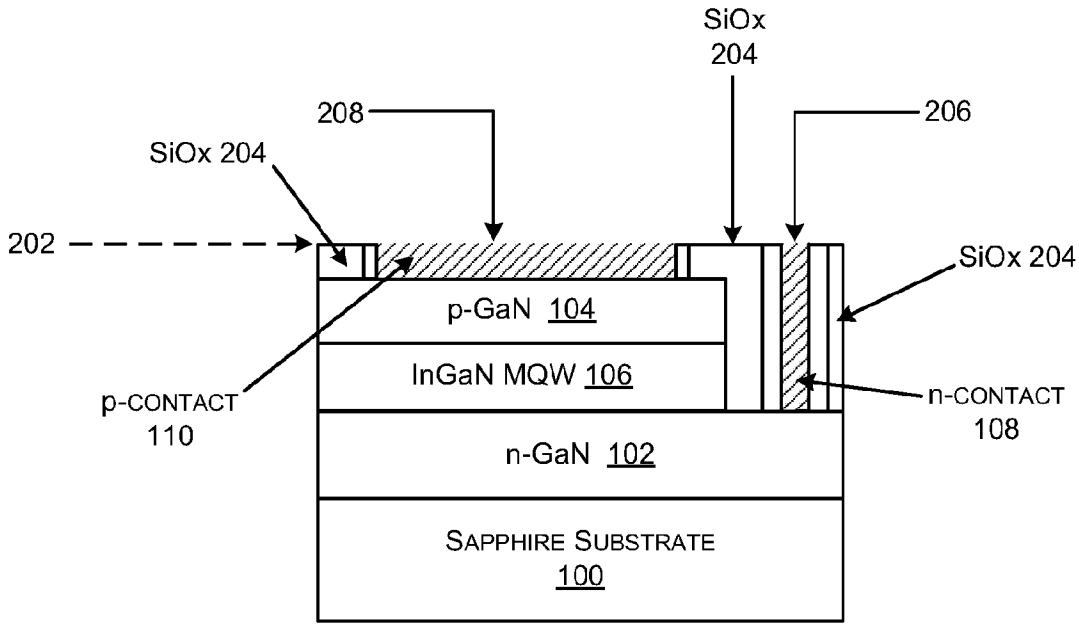
SiOx
204
208
206
SiOx 204
202
SiOx 204
p-GaN 104
InGaN MQW 106
p-CONTACT
110
n-CONTACT
108
n-GaN 102
SAPPHIRE SUBSTRATE
100

FIG. 2

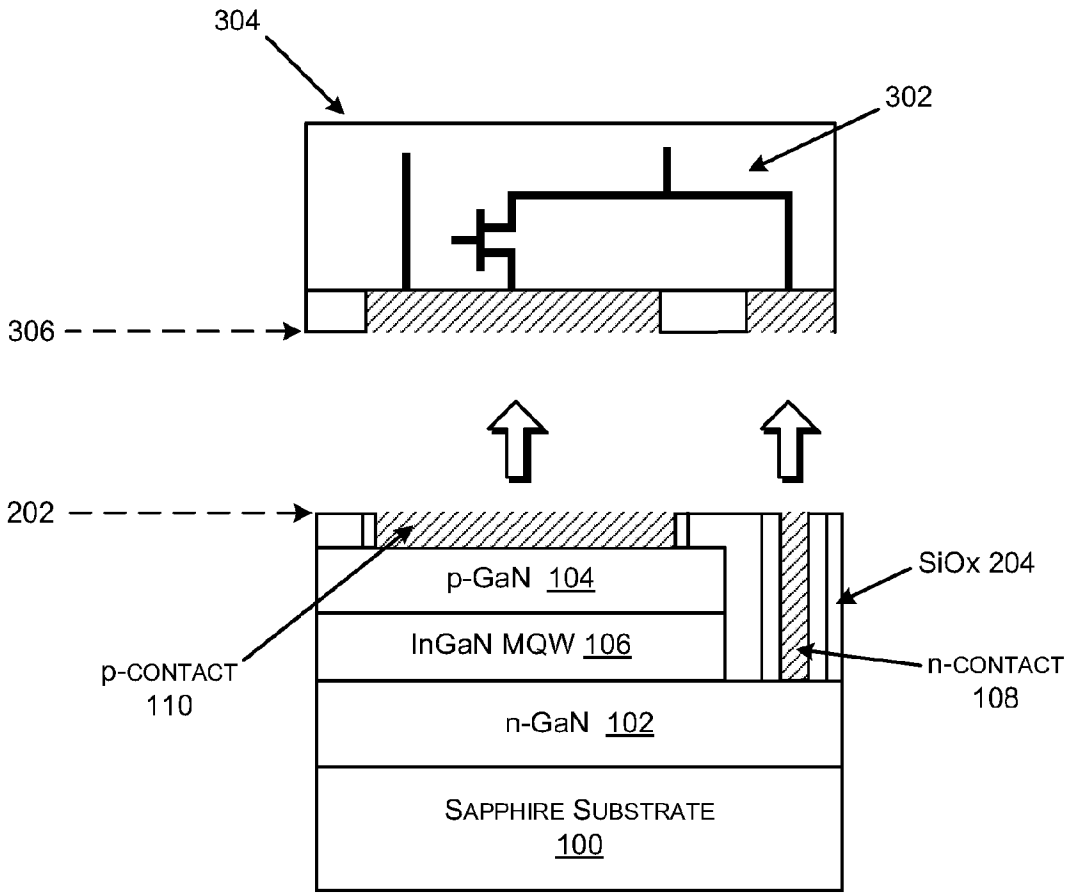
304
302
306
202
p-GaN 104
InGaN MQW 106
n-GaN 102
SAPPHIRE SUBSTRATE
100
SiOx 204
p-CONTACT
110
n-CONTACT
108

FIG. 3

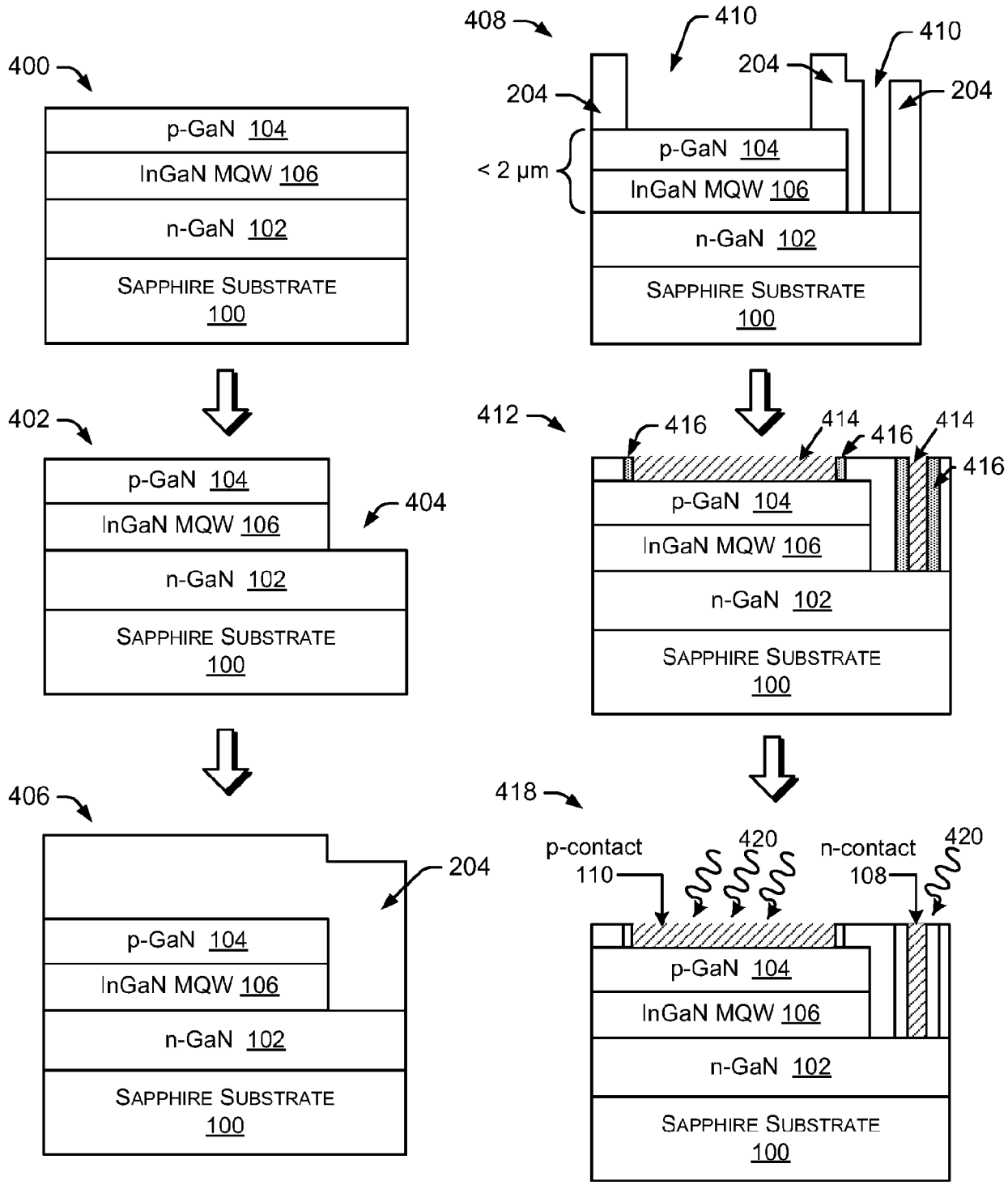
400
p-GaN 104
InGaN MQW 106
n-GaN 102
SAPPHIRE SUBSTRATE 100
402
p-GaN 104
InGaN MQW 106
n-GaN 102
SAPPHIRE SUBSTRATE 100
404
406
204
p-GaN 104
InGaN MQW 106
n-GaN 102
SAPPHIRE SUBSTRATE 100
408
410
204
410
204
204
< 2 μm
p-GaN 104
InGaN MQW 106
n-GaN 102
SAPPHIRE SUBSTRATE 100
412
416
414
416
414
416
p-GaN 104
InGaN MQW 106
n-GaN 102
SAPPHIRE SUBSTRATE 100
418
p-contact 110
420
n-contact 108
420
p-GaN 104
InGaN MQW 106
n-GaN 102
SAPPHIRE SUBSTRATE 100

FIG. 4

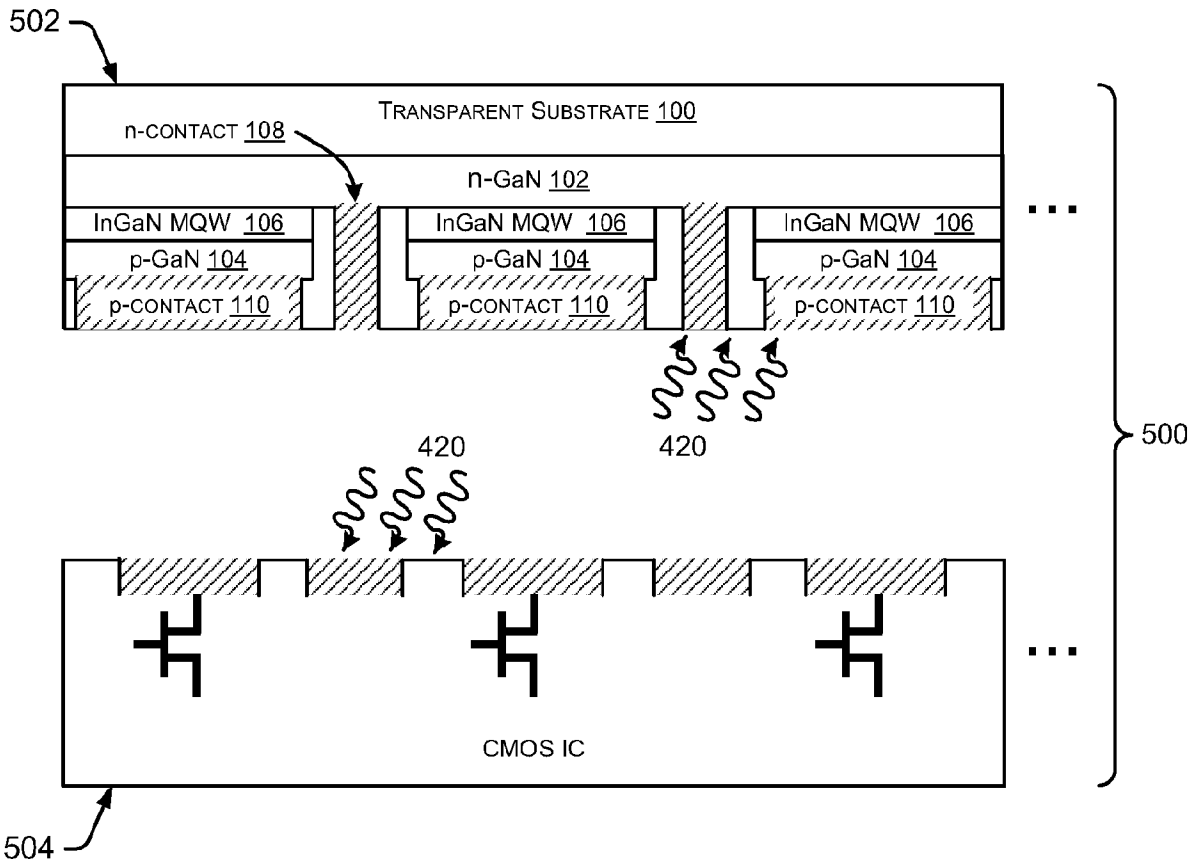
502
TRANSPARENT SUBSTRATE 100
n-CONTACT 108
n-GaN 102
InGaN MQW 106
InGaN MQW 106
InGaN MQW 106
p-GaN 104
p-GaN 104
p-GaN 104
p-CONTACT 110
p-CONTACT 110
p-CONTACT 110
420
420
500
CMOS IC
504

FIG. 5

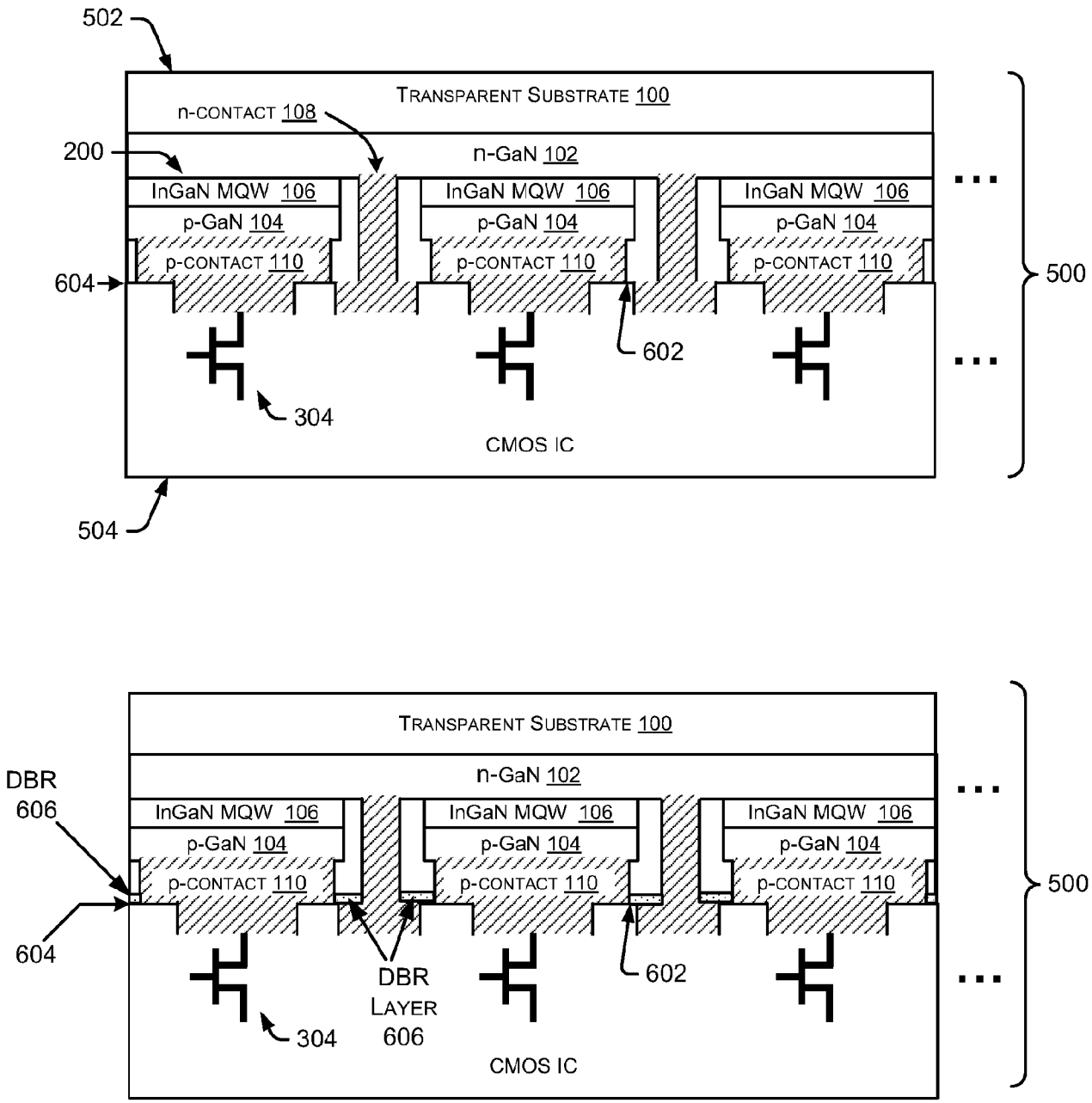
502
TRANSPARENT SUBSTRATE 100
n-CONTACT 108
200
n-GaN 102
InGaN MQW 106
p-GaN 104
p-CONTACT 110
604
602
304
CMOS IC
500
504
DBR
606
DBR
LAYER
606

FIG. 6

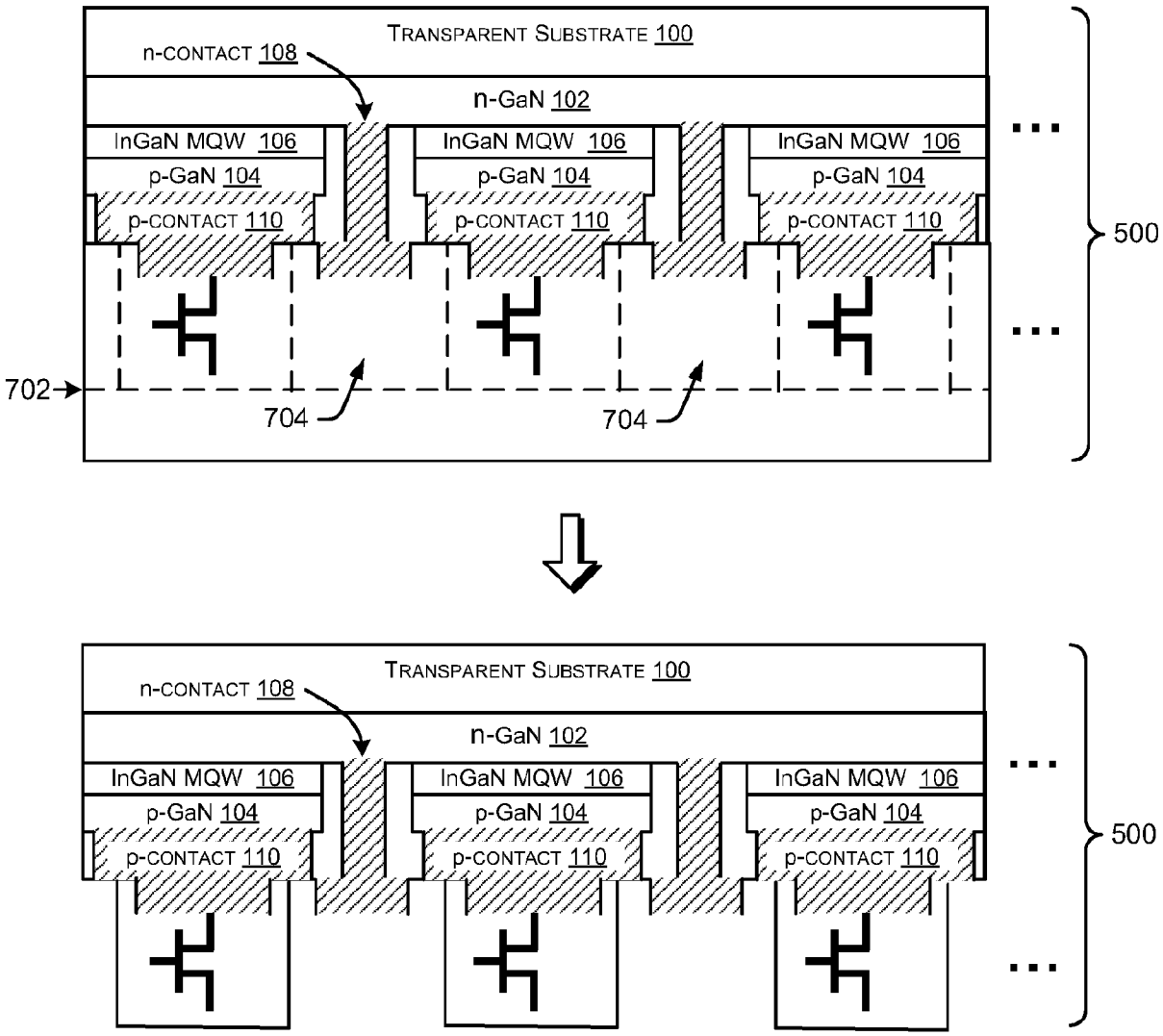
TRANSPARENT SUBSTRATE 100
n-CONTACT 108
n-GaN 102
InGaN MQW 106
p-GaN 104
p-CONTACT 110
500
702
704
704
TRANSPARENT SUBSTRATE 100
n-CONTACT 108
n-GaN 102
InGaN MQW 106
p-GaN 104
p-CONTACT 110
500

FIG. 7

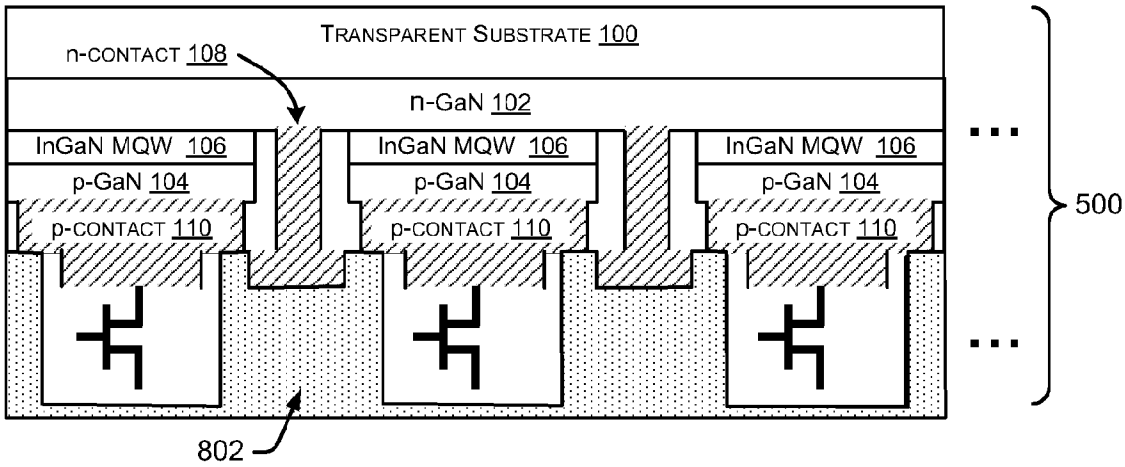
TRANSPARENT SUBSTRATE 100
n-CONTACT 108
n-GaN 102
InGaN MQW 106
InGaN MQW 106
InGaN MQW 106
p-GaN 104
p-GaN 104
p-GaN 104
p-CONTACT 110
p-CONTACT 110
p-CONTACT 110
500
802

FIG. 8

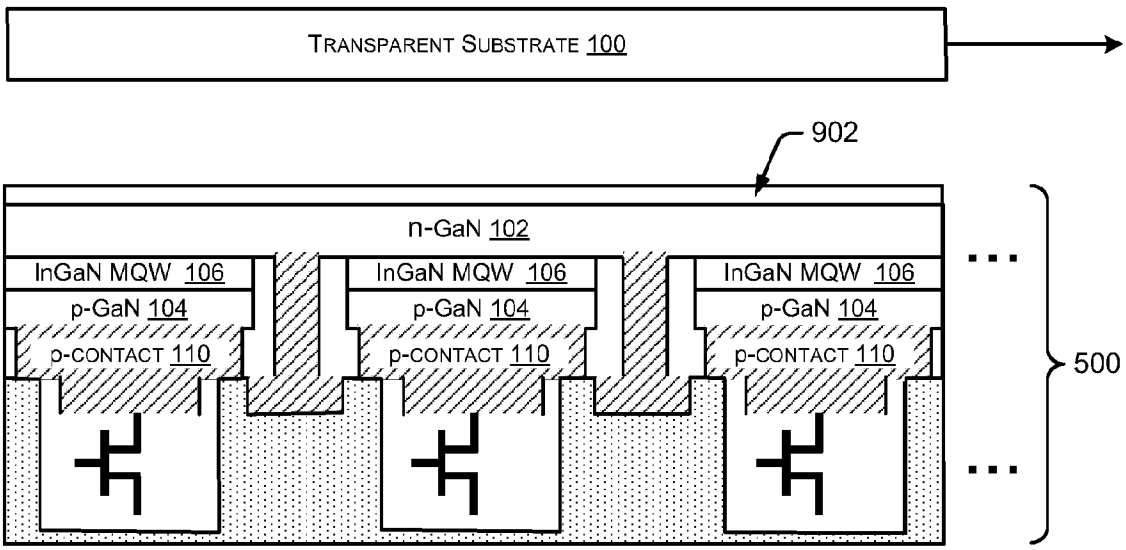
TRANSPARENT SUBSTRATE 100
902
n-GaN 102
InGaN MQW 106
InGaN MQW 106
InGaN MQW 106
p-GaN 104
p-GaN 104
p-GaN 104
p-CONTACT 110
p-CONTACT 110
p-CONTACT 110
500

FIG. 9

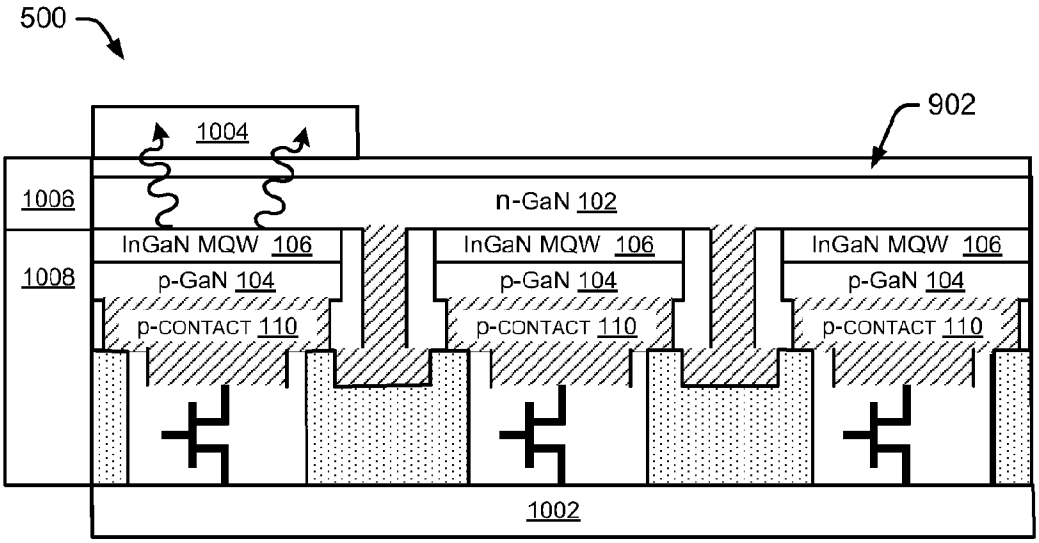
500
902
1004
1006
n-GaN 102
1008
InGaN MQW 106
InGaN MQW 106
InGaN MQW 106
p-GaN 104
p-GaN 104
p-GaN 104
p-CONTACT 110
p-CONTACT 110
p-CONTACT 110
1002

FIG. 10

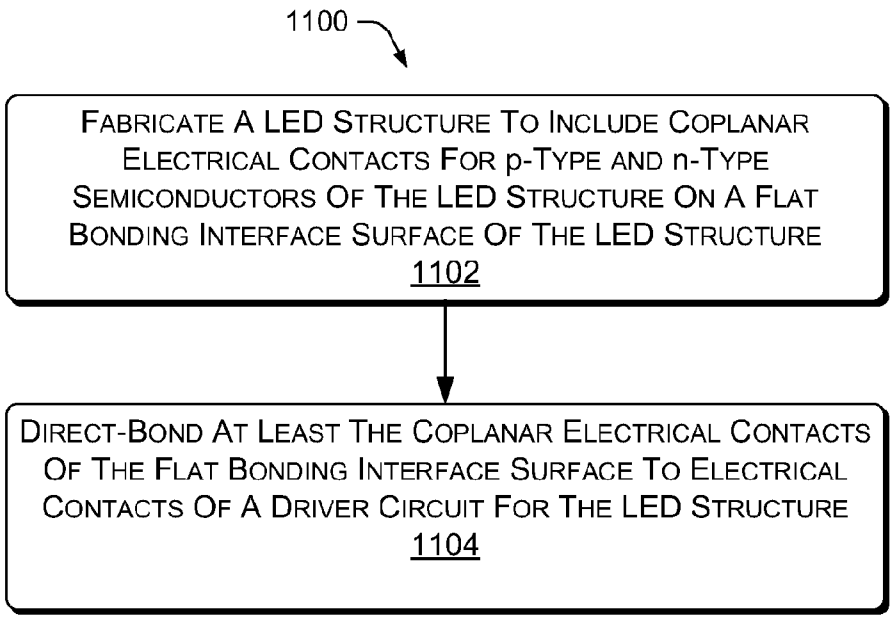
1100
FABRICATE A LED STRUCTURE TO INCLUDE COPLANAR ELECTRICAL CONTACTS FOR p-TYPE AND n-TYPE SEMICONDUCTORS OF THE LED STRUCTURE ON A FLAT BONDING INTERFACE SURFACE OF THE LED STRUCTURE
1102
DIRECT-BOND AT LEAST THE COPLANAR ELECTRICAL CONTACTS OF THE FLAT BONDING INTERFACE SURFACE TO ELECTRICAL CONTACTS OF A DRIVER CIRCUIT FOR THE LED STRUCTURE
1104

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/022199

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/15(2006.01)i, H01L 33/00(2010.01)i, H01L 33/60(2010.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 27/15; H01L 25/16; H01L 21/56; H01L 21/50; H01L 33/10; H01L 33/00; H01L 33/64; H01L 33/38; H01L 33/50; H01L 33/60

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: LED, driver-circuitry, direct-bonded, p-type and n-type GaN, first and second coplanar conductive areas, insulation, plasma-activation

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007-0096130 A1 (STEFANO SCHIAFFINO et al.) 03 May 2007 See paragraphs [0037]-[0078]; claims 1, 22; and figures 2-10.	1-6,8,14-15,25
Y		7,9-13,16-24,26-27
Y	US 2016-0181477 A1 (SEOUL VIOSYS CO., LTD.) 23 June 2016 See paragraphs [0052], [0128], [0133], [0200], [0209]-[0211], [0226]; and figures 1, 19, 21.	7,11-13,16-18,23
Y	US 2016-0141469 A1 (COMMISSARIAT A I`ENERGIE ATOMIQUE ET AUX ENERGIES ALTERNATIVES et al.) 19 May 2016 See paragraph [0077]; and figure 3I.	9-10,20,26-27
Y	US 2010-0317132 A1 (JOHN A. ROGERS et al.) 16 December 2010 See paragraph [0470]; and figure 40.	19-24
A	US 2011-0294242 A1 (LIEN-SHINE LU) 01 December 2011 See paragraphs [0014]-[0020]; and figures 1-8, 14.	1-27

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 June 2018 (29.06.2018)	**29 June 2018 (29.06.2018)**

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Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/022199

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0096130 A1	03/05/2007	CN 101194373 A	04/06/2008
		CN 101194373 B	23/03/2011
		CN 101263614 A	10/09/2008
		CN 101263614 B	19/05/2010
		EP 1894255 A2	05/03/2008
		EP 1894255 B1	11/07/2012
		EP 1927142 A1	04/06/2008
		JP 2006-344971 A	21/12/2006
		JP 2007-081417 A	29/03/2007
		JP 5513707 B2	04/06/2014
		TW 200717862 A	01/05/2007
		TW 200802960 A	01/01/2008
		TW 200845424 A	16/11/2008
		TW I420688 B	21/12/2013
		TW I427815 B	21/02/2014
		US 2006-0281203 A1	14/12/2006
		US 2007-0057271 A1	15/03/2007
		US 2008-0142833 A1	19/06/2008
		US 2010-0207157 A1	19/08/2010
		US 7348212 B2	25/03/2008
		US 7736945 B2	15/06/2010
		US 7754507 B2	13/07/2010
		US 8384118 B2	26/02/2013
		WO 2006-131843 A2	14/12/2006
		WO 2006-131843 A3	07/09/2007
		WO 2007-031893 A1	22/03/2007
		WO 2008-072204 A1	19/06/2008
US 2016-0181477 A1	23/06/2016	KR 10-2016-0025455 A	08/03/2016
		US 9847458 B2	19/12/2017
		WO 2016-032193 A1	03/03/2016
US 2016-0141469 A1	19/05/2016	EP 3024030 A1	25/05/2016
		EP 3024030 B1	05/07/2017
		FR 3028672 A1	20/05/2016
		FR 3028672 B1	20/05/2016
		US 9711694 B2	18/07/2017
US 2010-0317132 A1	16/12/2010	EP 2430652 A1	21/03/2012
		EP 2430652 A4	04/03/2015
		KR 10-1706915 B1	15/02/2017
		KR 10-2017-0018112 A	15/02/2017
		TW 201113940 A	16/04/2011
		TW 201606863 A	16/02/2016
		TW 201711095 A	16/03/2017
		TW I573185 B	01/03/2017
		TW I592996 B	21/07/2017
		US 2015-0132873 A1	14/05/2015
		US 2017-200707 A1	13/07/2017

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/022199

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 8865489 B2	21/10/2014
		US 9647171 B2	09/05/2017
		WO 2010-132552 A1	18/11/2010
US 2011-0294242 A1	01/12/2011	US 2011-0014734 A1	20/01/2011
		US 8211722 B2	03/07/2012