



(51) International Patent Classification:
G06F 17/50 (2006.01)

(21) International Application Number:
PCT/EP2012/069766

(22) International Filing Date:
5 October 2012 (05.10.2012)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: IMEC [BE/BE]; Kapeldreef 75, B-3001 Leuven (BE).

(72) Inventors: CHRISTIE, Phillip; IMEC, IP Department, Kapeldreef 75, B-3001 Leuven (BE). DOBROVOLNY, Petr; IMEC, IP Department, Kapeldreef 75, B-3001 Leuven (BE).

(74) Agents: SARLET, Steven et al.; Holidaystraat 5, B-1831 Diegem (BE).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,

BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

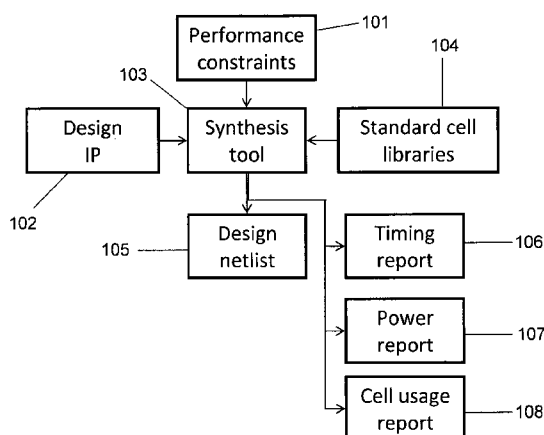
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: METHOD AND SYSTEM FOR CHARACTERIZING INTEGRATED CIRCUIT DESIGN IN TARGET SEMICONDUCTOR MANUFACTURING PROCESS

Fig 1



(57) Abstract: A method for characterizing a given i.c. design in a target semiconductor manufacturing process, comprising: providing a standard cell library for the process; obtaining a timing report for a data path from an existing description of the design, resulting from synthesis of the design in a given manufacturing process, containing: process independent design information comprising a data path structure comprising standard cells and interconnecting nets, and process dependent design information comprising delay and capacitance values of the cells and nets; creating a functionalized timing report for each data path using only process independent design information of the timing report; determining a cumulative delay for each timing report in the process using substitute process dependent design information, comprising: delay and capacitance values for the cells in the data path, calculated from the library, wherein for nets having a fan-out greater than one an off data path termination load capacitance is considered.

**Method and system for characterizing integrated circuit design in target
semiconductor manufacturing process**

Technical field

The present disclosure relates in general to the design of integrated circuits, and more in particular to the characterization of integrated circuit designs in one or more target semiconductor manufacturing processes.

5

Background art

The continuous scaling of semiconductor device features in accordance with Moore's law has been the foundation for the design of ever more powerful and complex semiconductor chips. Scaling of semiconductor devices has the additional benefit that the cost per product is considerably reduced with each technology node since more functionality can be packed in less area. However this is true only when product yield is maintained above a certain threshold, which becomes increasingly difficult with the advent of each semiconductor technology node. To ensure that the design and implementation phase of a semiconductor chip yields a product that meets the yield and performance specifications a large collection of techniques, tools, and design methodologies are at the disposal of the chip designer. Electronic Design Automation (EDA) tools and the availability of design technology information provided by the foundries (i.e. design libraries, technology characterization data, design methodology, etc) have allowed chip designers to prepare a manufacturing-ready chip layout that meets product design specifications. However, as semiconductor device features have reduce in size below approximately 100nm, the so-called deep submicron regime, the designer is required to consider the consequences of selecting a foundry technology node for the design of a chip that is application specific. Nowadays, semiconductor foundries try with each technology node to address all possible application markets. To achieve this objective the semiconductor foundries provide an increasing number of options for each technology node, each optimized to address the needs of a specific application such as low power consumption, high performance, etc. As a result, the chip designer needs to be able to benchmark all available semiconductor technology node options in order to find the one that best meets the product specification. In addition, it is

10

15

20

25

30

important to assess the potential benefits of a technology node on a specific chip prior to the redesigning phase taking place. This is because the complete redesign of a chip requires a considerable investment in time, resources and capital, thus early estimation of return-on-investment (ROI) needs to be determined.

Christie et al., "Rapid Design Flows for Advanced Technology Pathfinding", [P. Christie, A. Nackaerts, A. Kumar, A. S. Terechko, and G. Doornbos, Proc. International Electron Devices Meeting, 2008, pp. 685—688] describes several simplifications to standard design flows to enable short experiment turn-around times (less than a day) while obtaining a reasonable timing accuracy (better than 10%). This approach is illustrated by calculating the variability in performance of a large IP block, implemented using two competing 15nm technologies. Rapid Design Flows (RDF's) are then coupled to a design flow description language, to enable unique experiments which directly link process-level variability to timing variations, without recourse to perturbations of device model parameters. However, the results generated are highly speculative since the timing paths used for determining performance were artificially created and therefore rely on load capacitances calculated by approximate formulas. For the emerging technologies characterized in the paper, this approach is sufficient. But for the characterization of advanced technologies which are already offered by foundries and used by commercial designers, a more accurate method is needed.

Summary of the disclosure

It is an aim of the present disclosure to provide a method and a system for characterizing an integrated circuit design in a target semiconductor manufacturing process, by means of which the characterization can be performed quickly and accurately.

These and other aims are achieved according to the disclosure with the subject-matter of the independent claims.

As used herein, with "known semiconductor manufacturing process" is intended to mean any already known semiconductor device manufacturing process, integrated circuit manufacturing process, variants of so-called technology nodes (e.g. as defined in the International Technology Roadmap for

Semiconductors) and “process corners” thereof, of which the process parameters are known from practical experience.

As used herein, with “target semiconductor manufacturing process” or “candidate semiconductor manufacturing process” is intended to mean any known or to be developed semiconductor device manufacturing process, integrated circuit manufacturing process, variants of so-called technology nodes (e.g. as defined in the International Technology Roadmap for Semiconductors) and process corners thereof, of which the process parameters are known from practical experience or simulation.

As used herein, with “standard cell library” is intended to mean a data collection containing definitions and parameters of standard cells and wire-load models for a semiconductor manufacturing process.

In an aspect, this disclosure provides a method for characterizing the performance of an integrated circuit design in a target semiconductor manufacturing process, the method comprising:

- a) providing a standard cell library for the target semiconductor manufacturing process;
- b) obtaining a timing report for at least one data path of said integrated circuit design, from an existing description of said integrated circuit design, said existing description resulting from synthesis of said integrated circuit design in a given semiconductor manufacturing process, said timing report containing:
 - semiconductor manufacturing process independent design information comprising a data path structure comprising a sequence of standard cells and nets interconnecting said standard cells, and
 - semiconductor manufacturing process dependent design information comprising delay values of said standard cells and capacitance values of said standard cells and said interconnecting nets;
- c) creating a functionalized timing report for each said data path using only the semiconductor manufacturing process independent design information of the timing report;
- d) determining a cumulative delay for each said functionalized timing report in the target semiconductor manufacturing process using substitute semiconductor manufacturing process dependent design information, which comprises

- delay values for the standard cells in the data path, calculated from the standard cell library for the target semiconductor manufacturing process, and

- capacitance values for the standard cells and nets, calculated from the standard cell library for the semiconductor manufacturing process, wherein for
5 nets having a fan-out greater than one an off data path termination load capacitance is considered.

The functionalized timing report can be seen as the essence of the timing report which is taken from the existing timing report, namely the semiconductor manufacturing process independent design information, but functionalized, so
10 that it can take the standard cell library of any target semiconductor manufacturing process as input. By means of these steps, the impact of a large number of semiconductor manufacturing process changes on a given semiconductor chip or integrated circuit can be quickly assessed, thereby avoiding the need for a complete re-design in order to determine the impact. In
15 order to enhance the accuracy for the cumulative delay, measures may be taken to distinguish between interconnecting nets having a fan-out greater than one (where there is an off data path termination load capacitance) and the others, so that the difference in capacitance can be taken into consideration.

The off data path termination load capacitance may be taken into
20 consideration in different ways, a few of which are given below, to enhance the accuracy for the cumulative delay, but this disclosure is not limited thereto.

In embodiments according to the present disclosure, the step of considering the off data path termination load capacitance may mean that for
25 nets having a fan-out greater than one a greater capacitance value is used than for nets having a fan-out of one.

In embodiments according to the present disclosure, the off data path termination load capacitance may comprise, for unspecified cells in the timing report, the sum of an equivalent number of input capacitances of dummy cells, e.g. standard drive-strength inverter cells, defined in said standard cell library for
30 the target semiconductor manufacturing process. This means that the portion of the off data path termination load capacitance due to unspecified standard cell input capacitances in the original timing report may be calculated to be equal to the sum of an equivalent number of input capacitances of the dummy cells.

In embodiments according to the present disclosure, the off data path termination load capacitance may comprise, for unspecified cells in the timing report, an equivalent multiple of an input capacitance of the standard cell which is subsequent to the considered net, the input capacitance being defined in said standard cell library for the target semiconductor manufacturing process. This means that the portion of the off data path termination load capacitance due to unspecified standard cell input capacitances may be calculated to be equal to an equivalent multiple of an input capacitance of the standard cell which is subsequent to the considered net.

The accuracy may be further improved by performing steps b to d of the above method for characterizing the performance of an integrated circuit design in a target semiconductor manufacturing process for a plurality of data paths, for example the N most critical data paths (as regards timing), of the given integrated circuit design. N can be chosen as a trade off between overall calculation time and desired accuracy and can for example be at least 100 and/or at most 1000.

In another aspect, this disclosure provides a system for characterizing a given integrated circuit design in a target semiconductor manufacturing process, the system comprising:

- a storage device containing a standard cell library for the target semiconductor manufacturing process;

- an input device arranged for obtaining a timing report for at least one data path of said integrated circuit design, from an existing description of said integrated circuit design, said existing description resulting from synthesis of said integrated circuit design in a given semiconductor manufacturing process, said timing report containing:

- semiconductor manufacturing process independent design information comprising a data path structure comprising a sequence of standard cells and nets interconnecting said standard cells, and

- semiconductor manufacturing process dependent design information comprising delay values of said standard cells and capacitance values of said standard cells and said interconnecting nets;

- a processing system, communicatively connectable to said input device and said storage device and arranged for creating a functionalized timing report

for each said data path using only the semiconductor manufacturing process independent design information of the timing report;

said processing system being further arranged for determining a cumulative delay for each said functionalized timing report in the target semiconductor manufacturing process using substitute semiconductor manufacturing process dependent design information, which comprises:

- delay values for the standard cells in the data path, calculated from the standard cell library for the target semiconductor manufacturing process, and
- capacitance values for the standard cells and nets, calculated from the standard cell library for the semiconductor manufacturing process, wherein for nets having a fan-out greater than one an off data path termination load capacitance is considered.

Further features and advantages of the system are similar to those of the method described above and will therefore not be elaborated here for reasons of brevity.

In a particular embodiment, the processing system comprises a first processing device, e.g. a mobile terminal such as for example a smartphone or tablet computer or other, and a second processing device which are communicatively connectable to each other, the first processing device being provided with the functionalized timing report and the second processing device storing the standard cell libraries of a plurality of target semiconductor manufacturing processes.

In yet another aspect, this disclosure provides a method for comparing the performance of an integrated circuit manufactured by means of a plurality of candidate semiconductor manufacturing processes, comprising the steps of:

- a) providing a standard cell library for each candidate semiconductor manufacturing process;
- b) providing a functionalized performance report containing semiconductor manufacturing process independent design information and a function to combine this information with semiconductor manufacturing process dependent design information;
- c) determining at least one performance parameter for the functionalized performance report in each candidate semiconductor manufacturing process by applying semiconductor manufacturing process dependent design information,

which is derived from the standard cell library of the respective candidate semiconductor manufacturing process, to the functionalized performance report.

This method provides a solution for quickly comparing candidate semiconductor manufacturing processes as regards a particular integrated circuit, e.g. to quickly determine which of said candidate processes is optimal for a given set of manufacturing constraints.

In embodiments according to this disclosure, the functionalized performance report may comprise:

- a functionalized timing report, e.g. as described above;
- a functionalized power report, e.g. containing dynamic and/or static power consumption values for all the standard cells of the integrated circuit; and/or
- a functionalized area report, e.g. containing area values for all the standard cells of the integrated circuit.

In embodiments according to this disclosure, the performance parameter may be a cumulative delay, a dynamic and/or static power consumption and/or an overall area.

Brief description of the drawings

The disclosure will be further elucidated by means of the following description and the appended figures.

Figure 1 shows a diagram representing parts of the synthesis of a digital integrated circuit design which pertain to this disclosure.

Figure 2 shows an example of a small section of a typical timing report text file for a 40nm Low Power library.

Figure 3 shows an overview of the conversion of a timing report into a functionalized timing report using a "trace extraction tool".

Figure 4 shows the internal modules of the trace extraction tool.

Figure 5 shows the trace function corresponding to the timing report file of Figure 2.

Figure 6 illustrates the construction of functionalized timing reports with multiple paths.

Figure 7 shows the cell usage report.

Figure 8 shows the reformatting of the usage report data into columns

Figure 9 shows a summary of the various possibilities for the use cases.

Detailed description of preferred embodiments

5 The present disclosure will be described with respect to particular
embodiments and with reference to certain drawings but the disclosure is not
limited thereto but only by the claims. The drawings described are only schematic
and are non-limiting. In the drawings, the size of some of the elements may be
exaggerated and not drawn on scale for illustrative purposes. The dimensions
and the relative dimensions do not necessarily correspond to actual reductions to
10 practice of the disclosure.

Furthermore, the terms first, second, third and the like in the description
and in the claims, are used for distinguishing between similar elements and not
necessarily for describing a sequential or chronological order. The terms are
interchangeable under appropriate circumstances and the embodiments of the
15 disclosure can operate in other sequences than described or illustrated herein.

Moreover, the terms top, bottom, over, under and the like in the
description and the claims are used for descriptive purposes and not necessarily
for describing relative positions. The terms so used are interchangeable under
appropriate circumstances and the embodiments of the disclosure described
20 herein can operate in other orientations than described or illustrated herein.

Furthermore, the various embodiments, although referred to as
“preferred” are to be construed as exemplary manners in which the disclosure
may be implemented rather than as limiting the scope of the disclosure.

25 The term “comprising”, used in the claims, should not be interpreted as
being restricted to the elements or steps listed thereafter; it does not exclude
other elements or steps. It needs to be interpreted as specifying the presence of
the stated features, integers, steps or components as referred to, but does not
preclude the presence or addition of one or more other features, integers, steps
or components, or groups thereof. Thus, the scope of the expression “a device
30 comprising A and B” should not be limited to devices consisting only of
components A and B, rather with respect to the present disclosure, the only
enumerated components of the device are A and B, and further the claim should
be interpreted as including equivalents of those components.

Below, preferred embodiments are described for methods and systems for rapidly assessing a given integrated circuit design in one or a plurality of target semiconductor manufacturing processes. The embodiments can be used to rapidly assess a given design in a target semiconductor manufacturing process or for rapidly comparing performance of a given design in a set of candidate semiconductor manufacturing processes.

Overview of the synthesis procedure

Figure 1 shows a diagram representing parts of the synthesis of a digital integrated circuit design which pertain to this disclosure. The design IP 102 is represented by potentially multiple data files written hardware description language such as VHDL and is independent of the process technology used for its final implementation in silicon. The standard logic cell libraries 104 represent data files which may contain timing, power and area information for the logic cells implemented in a specific technology node, node option and process corner (such as the 40nm technology node with a low power, high threshold voltage option and operating a worst case process corner) used for the implementation of the design in silicon.

The synthesis tool 103 implements the design IP 102 in the technology defined by the standard cell libraries 104 by selecting logic cells from the library in order to meet design performance constraints 101 such as clock rate, power and area. The result is the implementation of the design in the form of a technology-dependent netlist 105 which contains the selected cells and the connections (nets) between them. The synthesis tool 103 may also be instructed to provide timing, area and power reports 106-108 which may be used to ensure that the required performance constraints 101 have been met for the specific technology options and process corners defined by the standard cell libraries 104 used in the synthesis procedure.

The timing trace extraction algorithm

An aspect of this disclosure is a method to transform the reports generated as a part of the synthesis from passive, technology-dependent text files into active, technology independent functions, which are referred to as performance reports. Performance reports are active in the sense that they take

standard cell libraries 104 as input arguments and calculate timing, power and area data for that technology. It has been found that the calculations may be extremely fast and can be used to evaluate different technology selections in seconds.

5 We shall first consider the creation of a timing report 106 or timing trace as it is also called herein. The timing report 106 contains a mixture of design information such as pin names, cell names, fan-outs as well as specific numeric technology information in the form of capacitance, transition time, and delay values. An example of a small section of a typical timing report 106 text file for a
10 40nm Low Power library is shown in Figure 2. It indicates that the slowest data path through the circuit (which defines the clock rate of the design) starts with a step input signal (a transition time of zero) at the clock pin (CP) of a D flip-flop (DFQX4). The signal then appears at the output pin of the D flip-flop (Q) with a rise time of 0.036 ns and travels along a net with a fan-out of two and a total
15 capacitance of 0.026 pF and arrives at the input pin (I) an inverter (INVX2) after a delay of 0.17 ns. The signal continues through the inverter to a NOR cell (NR2D4) via one of the seven branches of a net to a Full Adder (FA1X4) and on subsequent cells in the critical timing path of the design until the path is ultimately terminated by another clocked D flip-flop (DFQX2). The setup time for this
20 terminating flip is calculated and this finishes the timing report 106.

Figure 3 shows an overview of the conversion of a timing report 302 into a functionalized timing report using a "trace extraction tool" 304. The tool 304 reads in the timing report 302 text file and the library 305 used to create the report (the reference library 305) is imported into the tool. The output is the
25 functionalized form 307 of the report. The functionalized timing report 307 can be combined with the target library 309 of the target semiconductor manufacturing process to quickly obtain an idea of the timing performance of the given chip design if it were manufactured by means of the target process.

Figure 4 shows the internal modules of the trace extraction tool. Modules
30 401 and 402 perform the read-in of the timing report and reference library, respectively. Module 403 parses through the timing report information and retains information relating to wire-load models, cell names, pin names, net fan-outs and signal transition directions (rising or falling) are stored. In addition, Module 403 also retains load capacitance values for use in the Module 405 for estimating the

missing information in the timing report on the input capacitances of cells terminating high fan-out nets.

Modules 402, 404, and 405 may be used to enhance accuracy. The timing report only specifies cell names which lie directly on the data path. This is not a problem when cells are connected point-to-point by nets with no branches (that is, which have a fan-out of one). When nets have a fan-out greater than one, branches of the direct net split off from the timing path and are terminated by unspecified cell input capacitances. This is not problem for the timing report as only the total load capacitance is required for timing analysis.

The functionalized timing report implements an active timing report by means of which the total load capacitance for each stage in the timing path can be calculated on the basis of the files in the library. Since the library contains wire-load models, the net capacitance for a given fan-out can be calculated. The total load capacitance is the sum of the net capacitance and the input capacitances of the unspecified terminating cells.

Module 405 computes the termination capacitance for cells located on off-path net branches by first calculating the net capacitance from the wire-load model specified in the timing report as a function of its fan-out. This net capacitance and the known capacitance of the cell lying in the timing path are then subtracted from the total capacitance in the timing report to leave the total missing cell termination capacitance. Module 405 then converts this missing termination capacitance into the capacitance associated with an equivalent number of dummy drive-strength 1 inverters from the reference library, using information provided by Module 404. In this way, the numerical value of the total off timing path termination capacitance is converted into an equivalent number of inverter input capacitances which can be re-calculated for each new library given as an input argument to the trace.

Module 405 implements one way to take into consideration that there is an off data path termination load capacitance at the nets having a fan-out greater than one. Other examples are to use a predetermined, greater capacitance value for such nets than for nets having a fan-out of one, or to use an equivalent multiple (i.e. the multiple being chosen in function of the fan-out) of the input capacitance of the standard cell which is immediately subsequent to the considered net.

Finally, Module 406 reconstructs the timing path and inserts low level functions to re-calculate load capacitances and timing data for each stage. The result of this process is shown in Figure 5, which shows the trace function corresponding to the timing report file of Figure 2. We first notice that the function accepts an input argument which is a standard cell library 'lib'. This could be the library of any technology option that we are interested in evaluating. The next stage recalculates the input capacitances of the cells in the timing path using the low-level function 'getcellcap'. This function takes the library and cell names as input arguments, as well as the name of the input pin. The last argument represents a multiplication factor which is not utilized in this section and is set to one.

The second section uses the low-level function 'getintcap' to recalculate net capacitances from the wire-load model contained in the library as a function of the fan-out of the net. We observe that the first three nets specified in this section have fan-outs of 2, 7 and 1, respectively. The third section re-calculates the total load from three components: the known cell loads, the net loads and the capacitances of the equivalent number of dummy inverters calculated by the trace extraction tool. The off path terminating capacitances are calculated using the same 'getcellcap' function from the first section, but this time using the multiplier argument. We observe that the off path terminating capacitance of the first net with fan-out 2 is equivalent to 1.52 IVNX1 input capacitances, while the off-path terminating capacitances of the second net with fan-out 7 are equivalent to 4.45 INVX1 input capacitances. The third net is a direct point-to-point net with no branches (fan-out one) and so the multiplier is set to zero as no additional terminating cells are present.

Section 4 re-assembles the critical path using the data calculated in section 1 through 3 using another low-level function called 'timing'. This function emulates the static timing analysis routines in the synthesis tool and takes the library and cell names as input arguments. The 'timing' also takes the input pin name, the output pin name, the load capacitance and the signal transition time on the input pin. The output of the 'timing' function is the delay through the cell stage and the output transition time. We note that the input transition time of the first cell (DFQX4) is a step input (transition time zero) and that the output transition time is used as the input transition time to the next cell in the path. The end of

section 4 sums all the stage delays and adds the setup time of the terminating flip-flop in order to calculate the total delay through the timing path.

The timing report is not restricted to displaying the slowest timing path in the design. The synthesis tool can be instructed to write out the N slowest paths in the design, N being for example 100 or more up to 1000. Normally, this is not done as it is only the slowest path (termed the critical path) that determines the clock rate of the design. However, when a functionalized timing report is used with a different (target) library than the (reference) library used in its construction, it is possible that the slowest path is different from the slowest path in the reference technology. Therefore, traces are constructed from the N slowest paths obtained from the reference library timing report. The delays through all N paths are computed and the maximum delay selected as the critical path delay. The choice of N is a trade-off between calculation speed and delay path coverage. We have found the N=100 produces satisfactory coverage and calculation times measured in seconds. The construction of functionalized timing reports with multiple paths is illustrated in Figure 6.

Extensions to dynamic power, leakage power and area traces.

As shown in Figure 3, not only a timing report can be functionalized, but also other reports such as an area report 301 and power report 303 which may be obtained from a given chip design implemented in a given semiconductor manufacturing process. The "trace extraction tool" 304 can be configured to turn these into a functionalized area report 306 and a functionalized power report 308. The tool 304 reads in the area report 301 text file, the power report 303 text file and the library 305 used to create the report (the reference library 305) is imported into the tool. The output is the functionalized form 306, 308 of the reports. The functionalized area and power reports can be combined with the target library 309 of the target semiconductor manufacturing process to quickly obtain an idea of the area and power performance of the given chip design if it were manufactured by means of the target process.

The construction of functionalized power and area reports is considerably easier than the construction of functionalized timing reports since that are quantities associated with all the cells in a design and not specific cells chained together in a specific critical path. The total power and area can therefore be

interpreted as corresponding to quantities that are averaged over all the cells in a design. The starting point is the cell usage report shown in Figure 7. The cell usage report has been functionalized in a very straightforward way since no low level functions are required for this procedure. The result is shown in Figure 8
5 which essentially reformats the usage report data into columns. The first column contains cell areas, the second column contains cell leakage and the third column contains the number of instances of each cell. The total design area is calculated by multiplying each cell area in column 1 by its equivalent number in column 3, and summing the results. The total leakage is obtained by multiplying
10 each leakage value in column 2 by its equivalent number in column 3, and summing the results. Finally, the total number of cell is determined by simply summing columns 3.

Use cases

15 The various possibilities for the use cases are summarized in Figure 9. There are four principle variables:

- Report generation 901
- Format of reference and target libraries 902
- Location of extraction tool 903
- 20 • Delivery and format of results 904

Each of these will now be discussed in detail.

Report generation.

The disclosure is based on access to the reports generated as a result of synthesis and timing analysis under defined performance constraints. Depending
25 on the synthesis tool (Cadence, Synopsys, etc.), the resulting report formats may be different but the reports contain broadly similar information. This can be solved by the creation of a suitable file import module.

Format of libraries.

The disclosed implementation uses a library file import module to create a
30 compact binary representation of both the reference and target library text files. These binary files are used to create the functionalized report from a reference library and also when the functionalized report is run with a new target library. The libraries are originally in a text file format. The conversion to binary libraries as inputs is a one-off cost. Alternatively, more sophisticated programming

techniques could be employed to support the import of the libraries in their text format.

Location of extraction tool.

5 The disclosed implementation is in the form of an executable stand-alone trace function which can run on unix or windows machines. The trace function itself is very small in size (less than 1MByte) and so can be easily distributed. The size of the trace is small because it calls functions contained in a much bigger collection of dynamic libraries.

10 Alternatively, it is also possible to write the trace function as a single function which is also very small in size as the complexity of the trace algorithm is very low. It is therefore possible to conceive of the trace being written in java so that it can run as an active component on a web site or in one of the many other high-level languages and deployed as an app on an Apple or android smart phone or tablet. So the location of the trace can be on a client computer or mobile
15 device. The trace can also be located on a server and only accessible by users on the same intranet.

Delivery of results.

The data generated by the trace can for example be stored locally for immediate use by the user, accessed through a web page browser, automatically
20 delivered over the internet, attached in an e-mail, or otherwise delivered.

Claims

1. A method for characterizing a given integrated circuit design in a target semiconductor manufacturing process, the method comprising:

5 a) providing a standard cell library (309) for the target semiconductor manufacturing process;

b) obtaining a timing report (106, 302) for at least one data path of said integrated circuit design, from an existing description of said integrated circuit design, said existing description resulting from synthesis of said integrated circuit design in a given semiconductor manufacturing process, said timing report (106, 10
302) containing:

- semiconductor manufacturing process independent design information comprising a data path structure comprising a sequence of standard cells and nets interconnecting said standard cells, and

15 - semiconductor manufacturing process dependent design information comprising delay values of said standard cells and capacitance values of said standard cells and said interconnecting nets;

c) creating a functionalized timing report (307) for each said data path using only the semiconductor manufacturing process independent design information of the timing report (106, 302);

20 d) determining a cumulative delay for each said functionalized timing report (307) in the target semiconductor manufacturing process using substitute semiconductor manufacturing process dependent design information, which comprises:

25 - delay values for the standard cells in the data path, calculated from the standard cell library (309) for the target semiconductor manufacturing process, and

30 - capacitance values for the standard cells and nets, calculated from the standard cell library (309) for the semiconductor manufacturing process, wherein for nets having a fan-out greater than one an off data path termination load capacitance is considered.

2. Method according to claim 1, wherein the considering of the off data path termination load capacitance means that for nets having a fan-out greater than one a greater capacitance value is used than for nets having a fan-out of one.

3. Method according to claim 1 or 2, wherein the off data path termination load capacitance comprises, for unspecified cells in the timing report (106, 302), the sum of an equivalent number of input capacitances of dummy cells, defined in said standard cell library (309) for the target semiconductor manufacturing process.

4. Method according to claim 3, wherein the dummy cells are standard drive-strength inverter cells.

5. Method according to claim 1 or 2, wherein the off data path termination load capacitance comprises, for unspecified cells in the timing report (106, 302), an equivalent multiple of an input capacitance of the standard cell which is subsequent to the considered net, the input capacitance being defined in said standard cell library (309) for the target semiconductor manufacturing process.

6. Method according to any one of the previous claims, wherein steps b to d are performed for a plurality of data paths of said integrated circuit design.

7. Method according to claim 6, wherein said plurality of data paths comprises the N most critical data paths of said integrated circuit design.

8. Method according to claim 7, wherein N is at least 100.

9. A system for characterizing a given integrated circuit design in a target semiconductor manufacturing process, the system comprising:

a storage device containing a standard cell library (309) for the target semiconductor manufacturing process;

an input device arranged for obtaining a timing report (106, 302) for at least one data path of said integrated circuit design, from an existing description of said integrated circuit design, said existing description resulting from synthesis of said integrated circuit design in a given semiconductor manufacturing process, said timing report (106, 302) containing:

- semiconductor manufacturing process independent design information comprising a data path structure comprising a sequence of standard cells and nets interconnecting said standard cells, and

- semiconductor manufacturing process dependent design information comprising delay values of said standard cells and capacitance values of said standard cells and said interconnecting nets;

a processing system, communicatively connectable to said input device and said storage device and arranged for creating a functionalized timing report

(307) for each said data path using only the semiconductor manufacturing process independent design information of the timing report (106, 302);

said processing system being further arranged for determining a cumulative delay for each said functionalized timing report (307) in the target semiconductor manufacturing process using substitute semiconductor manufacturing process dependent design information, which comprises:

- delay values for the standard cells in the data path, calculated from the standard cell library (309) for the target semiconductor manufacturing process, and

- capacitance values for the standard cells and nets, calculated from the standard cell library (309) for the semiconductor manufacturing process, wherein for nets having a fan-out greater than one an off data path termination load capacitance is considered.

10. System according to claim 9, wherein the processing system is arranged for considering of the off data path termination load capacitance such that for nets having a fan-out greater than one a greater capacitance value is used than for nets having a fan-out of one.

11. System according to claim 9 or 10, wherein the off data path termination load capacitance comprises, for unspecified cells in the timing report (106, 302), the sum of an equivalent number of input capacitances of dummy cells, defined in said standard cell library (309) for the target semiconductor manufacturing process.

12. System according to claim 11, wherein the dummy cells are standard drive-strength inverter cells.

13. System according to claim 9 or 10, wherein the off data path termination load capacitance comprises, for unspecified cells in the timing report (106, 302), an equivalent multiple of an input capacitance of the standard cell which is subsequent to the considered net, the input capacitance being defined in said standard cell library (309) for the target semiconductor manufacturing process.

14. System according to any one of the claims 9-13, wherein the processing system is arranged for creating functionalized timing reports (307) and determining cumulative delays for a plurality of data paths of said integrated circuit design.

15. System according to claim 14, wherein said plurality of data paths comprises the N most critical data paths of said integrated circuit design.

16. System according to claim 15, wherein N is at least 100.

5 17. System according to any one of the claims 9-16, wherein the processing system comprises a first processing device and a second processing device which are communicatively connectable to each other, the first processing device being provided with the functionalized timing report (307) and the second processing device storing the standard cell libraries (309) of a plurality of target semiconductor manufacturing processes.

10 18. System according to claim 17, wherein the first processing device is a mobile terminal.

15 19. Computer program product directly loadable into a memory of a computing device, comprising software code portions for performing the steps of the method of any one of the claims 1-8 when executed on said computing device.

20. Computer readable non-volatile storage medium containing the computer program product according to claim 19.

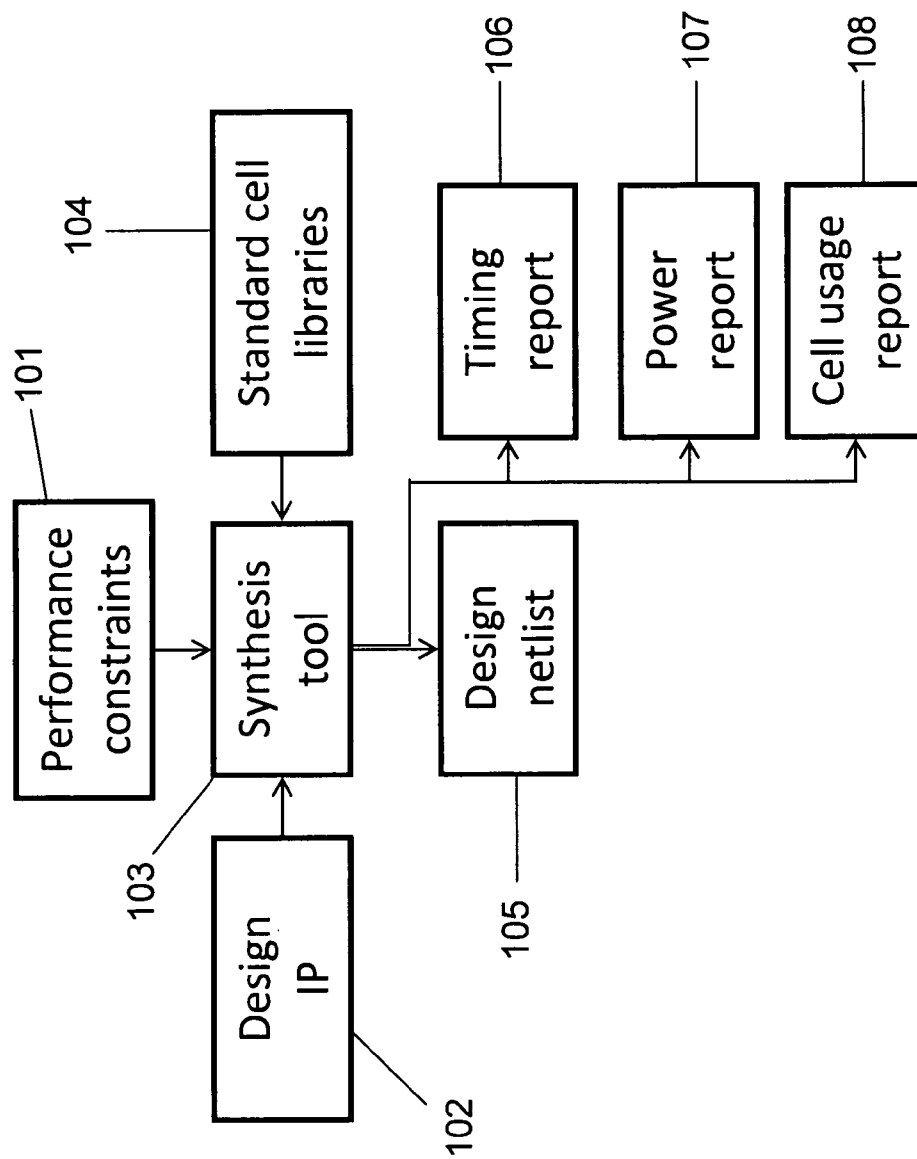
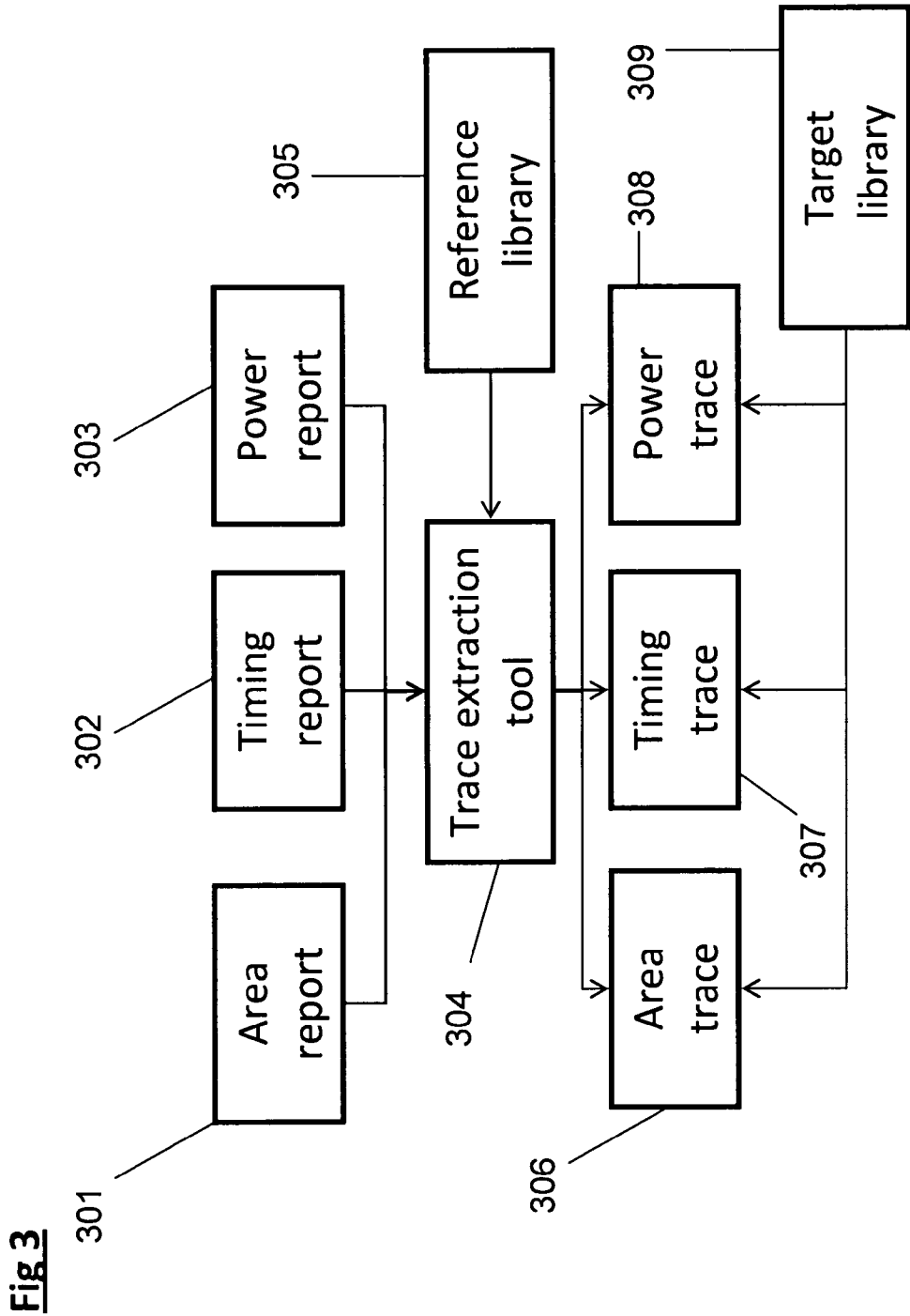
**Fig 1**

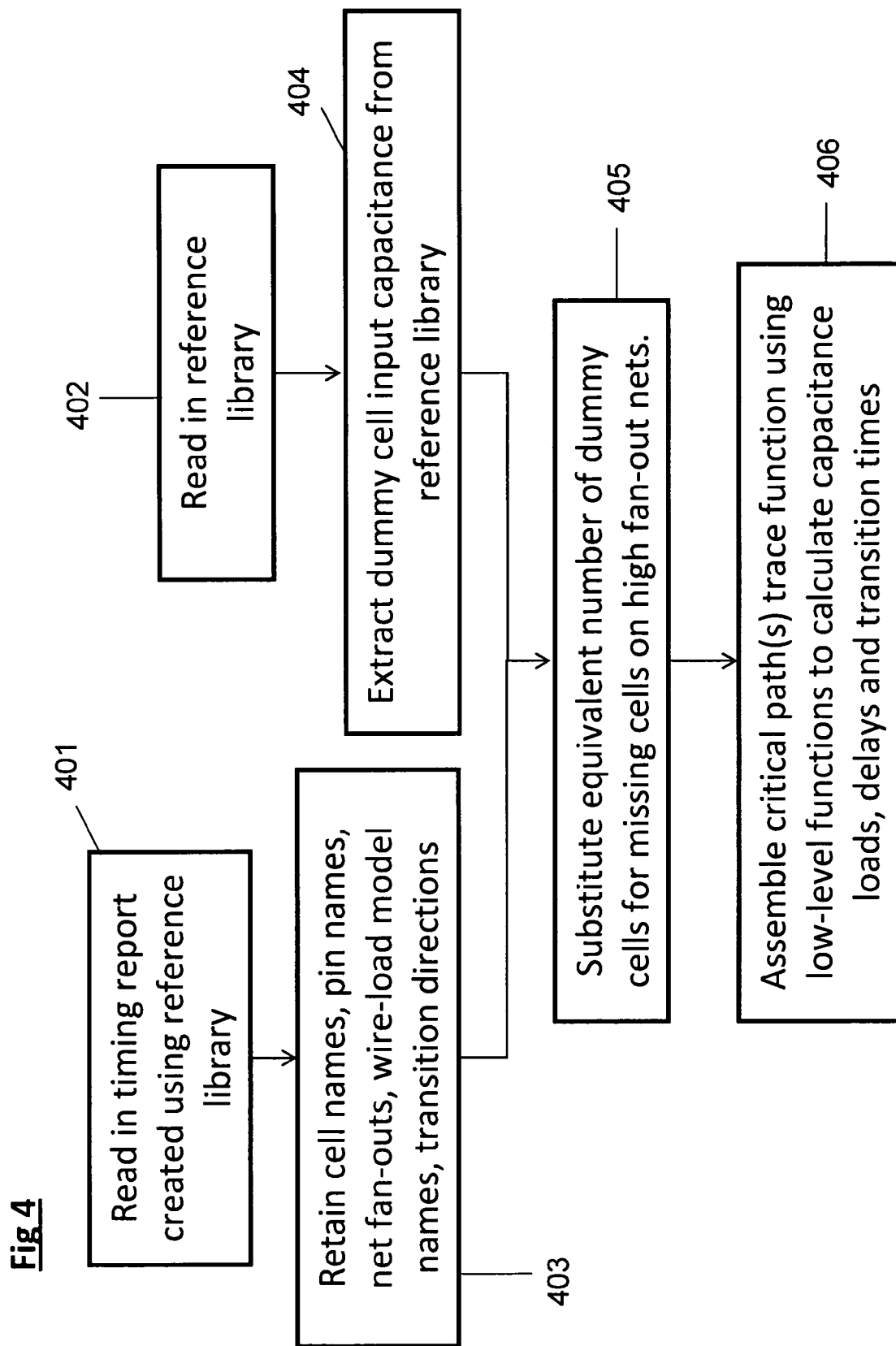
Fig 2

Design	Wire Load Model	Library				
8bit-mult	8K_Aggressive	40LP				
Point	Fanout	Cap	Trans	Derate	Incr	Path
b_reg_reg[4]/CP (DFQX4)			0.00000000		0.00000000	0.00000000 r
b_reg_reg[4]/Q (DFQX4)			0.03609869		0.17114639	0.17114639 r
b_reg[4] (net)	2	0.00262000			0.00000000	0.17114639 r
U6/I (INVX2)			0.03609869		0.00000000	0.17114639 r
U6/ZN (INVX2)			0.04920646		0.04571629	0.21686268 f
mult_x_19_1/n253 (net)	7	0.00716260			0.00000000	0.21686268 f
U63/A1 (NR2X3)			0.04920646		0.00000000	0.21686268 f
U63/ZN (NR2X3)			0.05374572		0.05291045	0.26977313 r
mult_x_19_1/n222 (net)	1	0.00197800			0.00000000	0.26977313 r
U130/B (FA1X4)			0.05374572		0.00000000	0.26977313 r
U130/S (FA1X4)			0.05875276		0.23915631	0.50892943 f
.						
.						
.						
ADDITIONAL STAGES						

N12 (net)	1	0.00068620	0.00000000	1.28159833	r
o_reg[12]/D (DFQX2)		0.03578063	0.00000000	1.28159833	r
data arrival time				1.28159833	
clock clk (rise edge)			1.32625997	1.32625997	
clock network delay (ideal)			0.00000000	1.32625997	
o_reg[12]/CP (DFQX2)			0.00000000	1.32625997	r
library setup time			-0.04464569		
				1.28161430	
data required time				1.28161430	
data required time				1.28161430	
data arrival time				-1.28159833	
slack (MET)				0.00001597	

Fig 2bis





```

function test_trace(lib)

% section 1
ccell(1) = getcellcap(lib, 'INVX2', 'I', 1) ;
ccell(2) = getcellcap(lib, 'NR2X3', 'A1', 1) ;
ccell(3) = getcellcap(lib, 'FA1X4', 'B', 1) ;
.
ADDITIONAL CELL LOAD CAPACITANCES
.
ccell(13) = getcellcap(lib, 'DFQD2', 'D', 1) ;

% section 2
cint(1) = getintcap(lib, '8K_Aggressive', 2) ;
cint(2) = getintcap(lib, '8K_Aggressive', 7) ;
cint(3) = getintcap(lib, '8K_Aggressive', 1) ;
.
.ADDITIONAL NET CAPACITANCES
.
cint(13) = getintcap(lib, 'Aggressive', 1) ;

% section 3
cload(1) = ccell(1) + cint(1) + getcellcap(lib, 'INVX1', 'I', 1.539163) ;
cload(2) = ccell(2) + cint(2) + getcellcap(lib, 'INVX1', 'I', 4.454144) ;
cload(3) = ccell(3) + cint(3) + getcellcap(lib, 'INVX1', 'I', 0.000000) ;
.
ADDITIONAL MISSING CELL LOAD CAPACITANCES
.
cload(13) = ccell(13) + cint(13) + getcellcap(lib, 'INVD1', 'I', 0.000000) ;

% section 4
[delay(1), tran(1)] = timing(lib, 'DFQX4', 'CP', 'Q', cload(1), 0, 'r') ;
[delay(2), tran(2)] = timing(lib, 'INVX2', 'I', 'ZN', cload(2), tran(1), 'f') ;
[delay(3), tran(3)] = timing(lib, 'NR2X3', 'A1', 'ZN', cload(3), tran(2), 'r') ;
.
ADDITIONAL DELAY STAGES
.
setuptime = setup(lib, 'DFQX2', 'CP', 'D', 0.000000, 0.035781, 'r', verbFlag) ;

pathDelay = sum(delay) + setuptime ;

```

Fig 5

```
function test_trace_multiple_paths(lib)

PATH 1
% section 1
% section 2
% section 3
% section 4
pathDelay(1) = sum(delay) + setuptime ;

PATH 2
% section 1
% section 2
% section 3
% section 4
pathDelay(2) = sum(delay) + setuptime ;

ADDITIONAL PATHS

PATH 100
% section 1
% section 2
% section 3
% section 4
pathDelay(100) = sum(delay) + setuptime ;

criticalPathdelay = max(pathDelay)
```

Fig 6

Leaf Cell Report '8bit-mult'.	
NR2XD0	33
XNR2D1	12
FA1D1	12
DFQD4	12
ND2D1	11
NR2XD1	10
DFQD1	10
NR2D3	9
CKND2D1	9
CKND1	9
CKND0	9
IOA21D2	8
INVD1	8
FA1D2	8
OAI21D1	7
NR2XD3	7
XOR2D1	6

Fig 7

Fig 8

function eightbitxPowerTrace (lib)

```

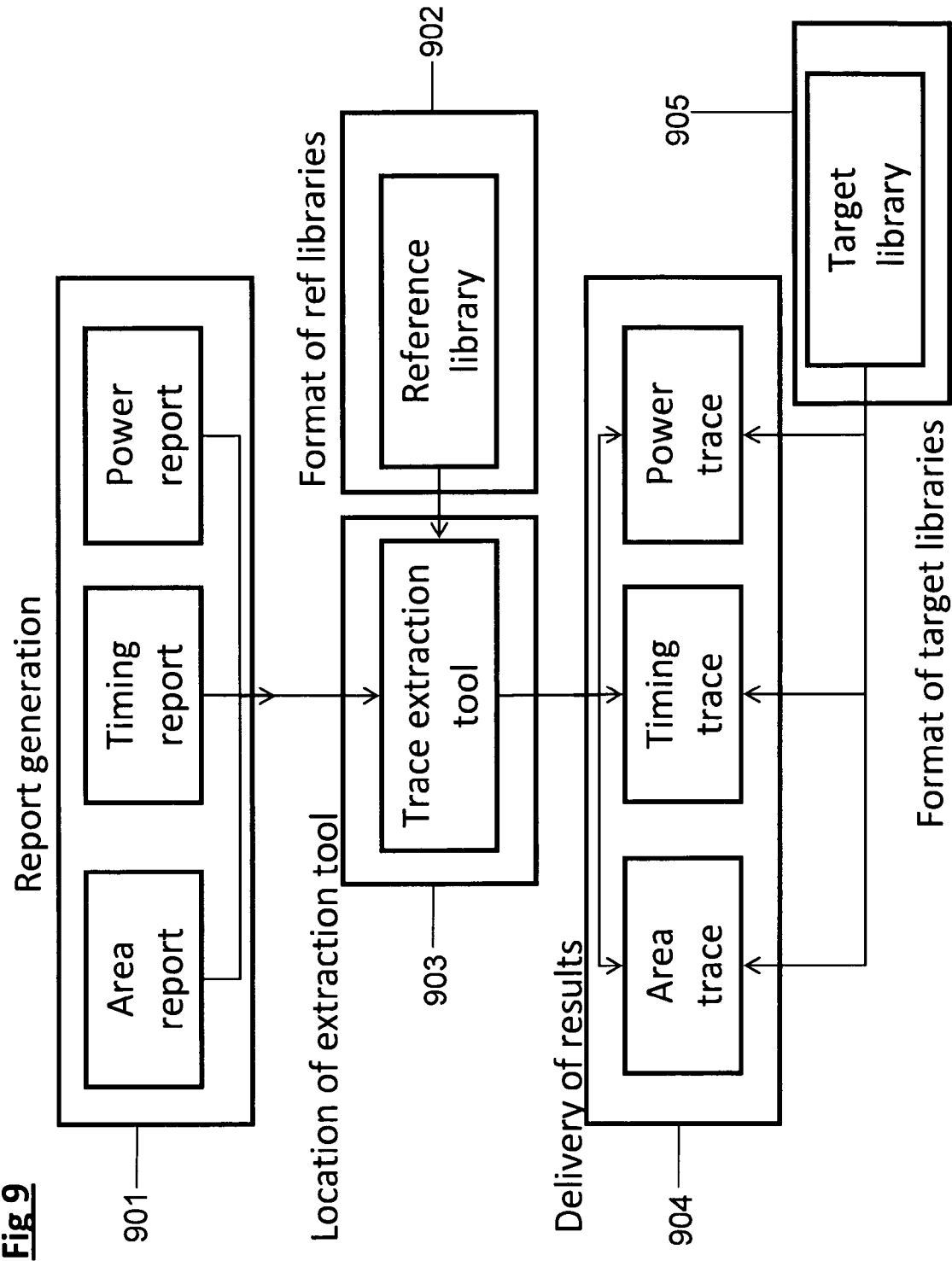
Data (1,1:3) = [lib.NR2XD0.area lib.NR2XD0.leakage_power(1).value 33] ;
Data (2,1:3) = [lib.XNR2D1.area lib.XNR2D1.leakage_power(1).value 12] ;
Data (3,1:3) = [lib.FA1D1.area lib.FA1D1.leakage_power(1).value 12] ;
Data (4,1:3) = [lib.DFQD4.area lib.DFQD4.leakage_power(1).value 12] ;
Data (5,1:3) = [lib.ND2D1.area lib.ND2D1.leakage_power(1).value 11] ;
Data (6,1:3) = [lib.NR2XD1.area lib.NR2XD1.leakage_power(1).value 10] ;
Data (7,1:3) = [lib.DFQD1.area lib.DFQD1.leakage_power(1).value 10] ;
Data (8,1:3) = [lib.NR2D3.area lib.NR2D3.leakage_power(1).value 9] ;
Data (9,1:3) = [lib.CKND2D1.area lib.CKND2D1.leakage_power(1).value 9] ;
Data (10,1:3) = [lib.CKND1.area lib.CKND1.leakage_power(1).value 9] ;
Data (11,1:3) = [lib.CKND0.area lib.CKND0.leakage_power(1).value 9] ;
Data (12,1:3) = [lib.IOA21D2.area lib.IOA21D2.leakage_power(1).value 8] ;
Data (13,1:3) = [lib.INVD1.area lib.INVD1.leakage_power(1).value 8] ;
Data (14,1:3) = [lib.FA1D2.area lib.FA1D2.leakage_power(1).value 8] ;
Data (15,1:3) = [lib.OAI21D1.area lib.OAI21D1.leakage_power(1).value 7] ;
Data (16,1:3) = [lib.NR2XD3.area lib.NR2XD3.leakage_power(1).value 7] ;
Data (17,1:3) = [lib.XOR2D1.area lib.XOR2D1.leakage_power(1).value 6] ;

```

```

Atotal = sum (Data (:,1) .* Data (:,3)) ;
Ptotal = sum (Data (:,2) .* Data (:,3)) ;
Ctotal = sum (Data (:,3)) ;

```



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2012/069766

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F17/50
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ABDOUL RJOUB ET AL: "Graph modeling for Static Timing Analysis at transistor level in nano-scale CMOS circuits", ELECTROTECHNICAL CONFERENCE (MELECON), 2012 16TH IEEE MEDITERRANEAN, IEEE, 25 March 2012 (2012-03-25), pages 80-83, XP032179672, DOI: 10.1109/MELCON.2012.6196385 ISBN: 978-1-4673-0782-6 the whole document ----- -/--	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

15 May 2013

Date of mailing of the international search report

23/05/2013

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Radev, Boyan

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2012/069766

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PULLERITS M ET AL: "Library-free synthesis for area-delay minimization", MICROELECTRONICS, 2008. ICM 2008. INTERNATIONAL CONFERENCE ON, IEEE, PISCATAWAY, NJ, USA, 14 December 2008 (2008-12-14), pages 187-191, XP031615736, ISBN: 978-1-4244-2369-9 the whole document -----	1-20
A	HITCHCOCK R B ET AL: "TIMING ANALYSIS OF COMPUTER HARDWARE", IBM JOURNAL OF RESEARCH AND DEVELOPMENT, INTERNATIONAL BUSINESS MACHINES CORPORATION, NEW YORK, NY, US, vol. 26, no. 1, 1 January 1982 (1982-01-01), pages 100-105, XP000715809, ISSN: 0018-8646 the whole document -----	1-20
A	US 2011/276933 A1 (BANERJI REVANTA [US] ET AL) 10 November 2011 (2011-11-10) the whole document -----	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2012/069766

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011276933	A1	10-11-2011	NONE
