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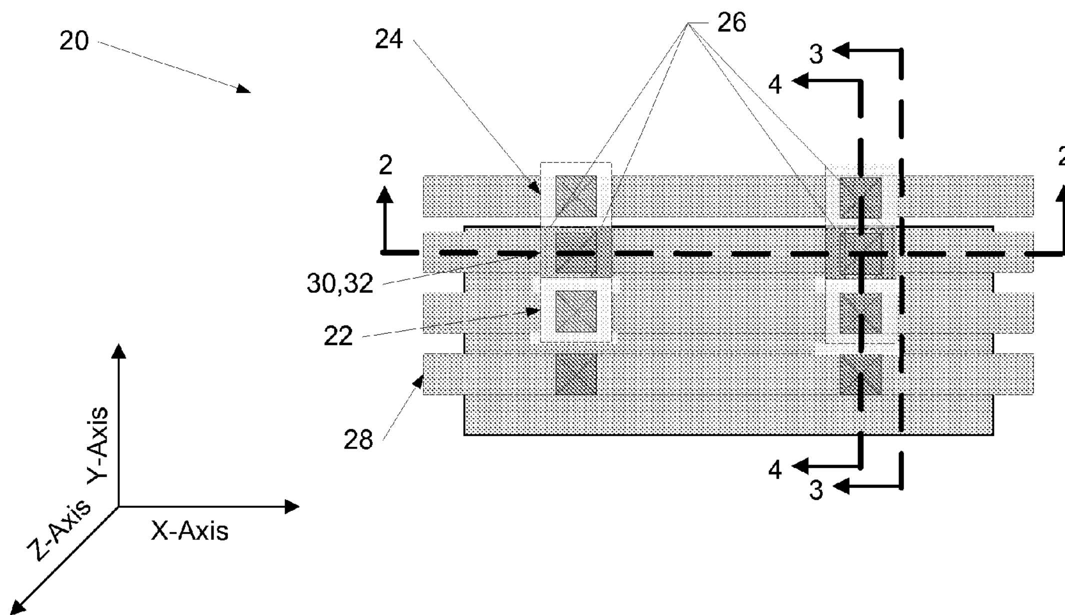
(54) **Title:** DEVICE AND METHOD OF MANUFACTURE FOR A LOW NOISE JUNCTION FIELD EFFECT TRANSISTOR



(57) Abstract: A microelectronic product and the method for manufacturing the product are provided. A source and drain are spaced from one another in a first direction and are connected to opposing ends of a channel to provide a set voltage. First and second gates are spaced from one another in a second direction surrounding a portion of the channel to allow for application and removal of a gate voltage. Application of the gate voltage repels majority carriers in the channel to reduce the current that conducts between the source and drain.

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DEVICE AND METHOD OF MANUFACTURE FOR A LOW NOISE JUNCTION FIELD EFFECT TRANSISTOR

BACKGROUND OF THE INVENTION

1). Field of the Invention

[0001] Embodiments of this invention relate to a junction field effect transistor (JFET) that provides greater control over current flow through the channel.

2). Discussion of Related Art

[0002] Semiconductor devices can be manufactured in the form of an integrated circuit or single device on a semiconductor substrate. A transistor is a type of semiconductor device that can be used for switching, amplification, signal modulation, and many other functions.

[0003] A type of transistor, called the field effect transistor (FET), relies on the application of a voltage to a gate in order to control the conductivity or current flow of a "channel."

[0004] The channel region of any FET can be doped with either n-type implants or p-type implants, creating an n-type device or p-type device. Various types of FETs use different types of insulation between the channel and the gate.

[0005] Perhaps the most common FET is a metal oxide semiconductor field effect transistor (MOSFET) that uses an insulator between the channel and the gate, such as SiO_2 (oxide).

[0006] Another type of FET, known as a JFET, utilizes a p-n junction as the gate. A conventional three-terminal JFET allows current to flow from a source to a drain while controlling the current flow with two gates.

[0007] Without a gate voltage, the charge carriers flow in the channel region between the source and drain terminals and are "normally on" unless a gate voltage is applied. When the gate voltage is applied, a depletion region is created by pushing mobile carriers away from the channel and "pinching off" the channel.

[0008] Gate voltages can be varied to cause the JFET to act as a switch or to modulate the flow of current by affecting the cross-sectional area of the channel and the channel resistance. The type of JFET application will determine whether the JFET is most desirable as a switch or modulator.

[0009] In one example, JFETs can be useful in designing radio transceivers using direct

conversion. Essentially, a radio frequency signal and local oscillator signal are fed into a mixer at the same carrier frequency. The signals are subtracted from one another, resulting in a low-frequency base-band output signal.

[0010] One of the problems with direct conversion is that the mixer must operate at very high frequencies while providing some gain, which introduces noise that makes signal processing difficult.

[0011] Mixer transistors should ideally be small in order to support frequencies in excess of 6GHz. However, the area of the device is inversely proportional to the flicker noise created. At lower frequencies, the dominant flicker noise source in a MOSFET transistor is due to the interaction of the mobile charges with the silicon-oxide interface and the dopant ions in the channel.

[0012] In contrast, JFETs mitigate flicker noise, because the conduction occurs via the p-n junction, in the bulk, rather than near the surface of the oxide interface. However, a problem still exists with manufacturing JFETs with standard complementary metal oxide semi-conductor (CMOS) procedures. Manufacturing an effective JFET with standard CMOS procedures would have traditionally required carefully tailored implants to achieve the correct channel depth, which further requires additional masking, which increases the cost of the product. Many JFETs use a buried gate within the substrate material to act as another means to control the channel flow. If a buried gate is not used, the resulting JFET would inefficiently require up to several hundred volts to "pinch off" the channel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The invention is described by way of examples with reference to the accompanying drawings, wherein:

[0014] Figure 1 is a top view of a substrate containing multiple junction field effect transistors, according to one embodiment of the invention;

[0015] Figure 2 is a cross-sectional front view taken on 2–2 of Figure 1;

[0016] Figure 3 is a cross-sectional side view taken on 3–3 of Figure 1;

[0017] Figure 4 is a cross-sectional side view on lines 4–4 of Figure 1;

[0018] Figure 5 is a cross-sectional front view similar to Figure 2, illustrating a stage in a manufacturing process wherein an insulator material is applied to a substrate;

[0019] Figure 6 is a view similar to Figure 5, illustrating a stage in a manufacturing process wherein a conformal layer is applied to a substrate;

[0020] Figure 7 is a view similar to Figure 6, illustrating a stage in a manufacturing process wherein the conformal layer is etched;

[0021] Figure 8 is a view similar to Figure 7, illustrating a stage in a manufacturing process wherein implants are inserted into the substrate;

5 **[0022]** Figure 9 is a view similar to Figure 8, illustrating a stage in a manufacturing process wherein the device has been annealed;

[0023] Figure 10 is a top view of a substrate containing a junction field effect transistor according to another embodiment of the invention;

[0024] Figure 11 is a cross-sectional side view on 11–11 of Figure 10; and

10 **[0025]** Figure 12 is a cross-sectional front view on 12–12 of Figure 10.

DETAILED DESCRIPTION OF THE INVENTION

[0026] Figures 1 to 4 of the accompanying drawings illustrate a JFET 20, according to one embodiment of the invention, including a source 22, a drain 24, a channel 26, and first
15 and second gates 30 and 32.

[0027] The fabrication of the junction field effect transistor is first described with respect to Figures 5 to 9, whereafter its functioning is described.

[0028] Figure 5 shows a p-substrate 36 of a wafer. The substrate material can be gallium-arsenide, silicon, germanium, silicon carbide, or other known semiconductor
20 substrate materials. The substrate material is then p-doped to form a p-substrate 36 which will later act as a second gate 32 and third gate 34.

[0029] A thin epitaxial layer of insulator material 38, such as oxide, is grown on top of the p-substrate 36 and an electrode material 40 is applied on top of the insulator material 38. An n-type dopant is then implanted into unmasked portions of the p-substrate 36,
25 resulting in n-type regions 42. The n-type dopant can be phosphorous, arsenic, antimony, or any other known doping agent that can produce an abundance of mobile electrons in the material to which it is applied.

[0030] As shown in Figure 6, after the n-type regions 42 have been created, an oxide conformal layer 44 is applied over the insulator material 38, electrode material 40, and n-
30 type regions 42. Conformal layer 44 material can be chosen according to the type of etching process used.

[0031] In Figure 7, the conformal layer 44 is anisotropically etched back by the etching process, forming spacers 46 extending over a portion of the n-type region 42. The etching

process can be plasma etching or any known anisotropic etching process.

[0032] As shown in Figure 8, P-implants 48 are then implanted next to the spacers 46 by any known method of p-type doping with a p-type doping agent, such as boron. The spacers 46, resulting from the anisotropic etching process, are positioned so that the P-implants 48 are prevented from completely covering the n-type doped regions 42. Therefore, as shown in Figure 8, small N-tip implant channels 50 are created under the spacers 46 after P-implants 48 are inserted. Also shown in Figure 8, the N-tip channels 50 are located directly under the spacers 46 and do not yet extend under the electrode material 40. The P-implants 48 are spaced away from the electrode material 40 by the N-tip channels 50.

[0033] As shown in Figure 9, the device assembly is then annealed, causing the activation and diffusion of the P-implants 48 and N-tip channels 50. The high-temperature annealing process causes the N-tip channels 50 and P-implants 48 to diffuse both vertically and horizontally, which results in a final N-tip channel 50 location being underneath the electrode material 40. The P-implants 48 also diffuse to a position where a P-implant 48 edge is aligned with an edge of the electrode material 40. In the final position, the P-implant 48 is no longer spaced away from the electrode material 40 by the N-tip channel 50. The p-substrate 36 continues to surround the N-tip channel 50 on sides that do not face the P-implant 48 or oxide interface 38.

[0034] After diffusion, the P-implant 48 effectively acts as a first gate 30, and portions of the p-substrate 36 act as a second gate 32 and a third gate 34. Furthermore, the electrode material 40 effectively acts as a fourth gate 52. Activation of the doped regions 48 and 50 also occurs in the annealing process by repairing any lattice damage that may have occurred during the implantation process. Furthermore, the N-tip channel 50 becomes an activated N-tip channel 26.

[0035] Referring again to Figures 2, 3, and 4, a second insulator material is then created in the z-direction, forming a second insulator layer 54 surrounding the fourth gate 52. A contact material 56, which can be tungsten or any known contact material, is applied on top of the fourth gate 52 surrounded by a third insulator layer 60 created on top of the second insulator layer 54. A final conductor layer 62 is applied from a metallizing process to the top of the contact 56 and third insulator layer 60. The final conductor layer 62 is copper or any other acceptable conducting material.

[0036] As shown in Figure 1, the source 22 and the drain 24 are generally spaced apart

from one another in the y-direction and are N+ doped. The substrate 36 extends primarily in the x- and y- directions. A P+ depletor electrode 28 is spaced from the source 22 and drain 24 in the y-direction connected to apply a gate voltage to the first gate 30, second gate 32, third gate 34, and fourth gate 52.

5 **[0037]** Referring to Figure 4, the N+ doped source 22 and drain 24 regions are disposed on opposing sides of the N-tip channel 26. The source 22 and drain 24 are arranged in contact with the N-tip channel 26. The arrangement allows current to flow between the source 22 and drain 24 via contact with the N-tip channel 26.

[0038] As shown in Figure 3, the source 22 and drain 24 can have a voltage applied 10 through a contact material 58, which can be selected from any known contact material such as tungsten.

[0039] As shown in Figure 2, the fourth gate 52 is positioned above the N-tip channel 26 and the first gate 30 is positioned to the side of the N-tip channel 26, while the p-substrate 36 surrounds the N-tip channel 26 acting as a second gate 32 and third gate 34. The first 15 gate 30 and second gate 32 are spaced apart in the x-direction.

[0040] As further shown in Figures 1 and 2, four N-tip channels 26 extend in the y-direction and are spaced apart from one another in the x-direction. It should be noted that the device can be created with one or more N-tip channels 26, depending upon the application and current flow demands.

20 **[0041]** Figure 2 shows a total of three first gates 30, four N-tip channels 26, and two fourth gates 52. Referring to Figure 2, two N-tip channels 26 are located under a fourth gate 52 while being spaced apart by the p-substrate 36. Two N-tip channels 26 and a portion of p-substrate 36 are located between two first gates 30.

[0042] In use, referring to Figures 1 to 4, a set voltage is applied through the contact 25 material 58 to the source 22 and drain 24, causing a current to flow through the N-tip channel 26. The N-tip channel 26 is surrounded by a first gate 30 and a p-substrate material 36 which acts as a second gate 32 and third gate 34. The fourth gate 52 is also disposed above the N-tip channel 26 in the z-direction.

[0043] Referring to Figure 1, when a negative gate voltage is then applied through the 30 P+ depletor 28, the first gate 30, second gate 32, third gate 34, and fourth gate 52 create a reverse bias region within the N-tip channel 26, causing the N-tip channel 26 to be "pinched off" and completely deplete with no conduction. The gates create a negative bias region by repelling or pushing holes away in the N-tip channel 26, therefore stopping

the flow of electrons. The majority carriers in this embodiment are holes, but the majority carriers can also be electrons in an electron-based device.

[0044] The first gate 30 and fourth gate 52 are doped P+ in order to more easily make a contact through the material. When the gate voltage is applied to the first gate 30, it also causes the p-substrate 36 material to act as a second 32 and third 34 gate. Surrounding the N-tip channel 26 with gates allows for even more effective restriction of the current flow through the N-tip channel 26. When the gate voltage is removed, the current will resume flow between the source 22 and drain 24.

[0045] The typical metal oxide semiconductor field effect transistor having an N+ source and drain (NMOS) creates a channel just under an oxide layer when a positive gate voltage is applied. The typical NMOS device has higher flicker noise or 1/f (1/frequency) noise because the electrons are trapped along the silicon-oxide interface when flowing between the source and drain.

[0046] The evolution of the JFET allowed for lower 1/f flicker noise than the NMOS because there is no oxide interface to trap electrons, since conduction occurs via the bulk rather than the surface of the substrate. However, common JFET arrangements require carefully tailored buried implants to achieve the correct channel depth and control, which requires additional masking and manufacturing. Increased manufacturing steps result in increased cost and complexity of the product. If a buried gate was not used in a typical JFET, the resulting JFET would ineffectively require several hundred volts to turn off a deep channel.

[0047] A main advantage of the embodiment in Figures 1 to 4 is that it uses existing standard complementary metal-oxide semiconductor manufacturing processes while reducing 1/f noise by relying on N-tip channels 26 without a buried gate. Even though there is an oxide or insulator layer 38 near the N-tip channel 26, the 1/f noise in the embodiment in Figures 1 to 4 is significantly reduced.

[0048] The JFET 20 of Figure 1 is thus a microelectronic product that has a substrate 36 extending primarily in x- and y-directions, a channel 26 formed on the substrate36, a source and drain 22 and 24 spaced from one another in the y-direction and connected to opposing sides of the channel 26 to provide a set voltage over the channel 26, and first and second gate portions 30 and 32 spaced from one another in the x-direction and located on opposing sides of the channel 26 to allow for application and removal of a gate voltage over the gate portions, application of the gate voltage repelling majority carriers in the x-

direction to reduce current that conducts between the source and the drain 22 and 24.

[0049] The substrate 36 includes part of a wafer and JFET 20 further has a p-doped layer on the wafer, the channel 26 being an n-doped channel on the p-doped layer, and a p+ doped implant next to the channel 26, the first 30 and second 32 gate portions being the p+ doped implant and a portion of the p-doped layer respectively. The p-doped layer forms a third gate 34 portion below the channel 26.

[0050] The JFET 20 also has an electrode in the form of the gate 52 above the p-doped layer, the channel 26 being a tip implant below the electrode.

[0051] As should be evident from the description of Figures 1 to 9, a method of making a junction field effect transistor is described. Specifically, the channel 26, the source 22, the drain 24, and the first and second gate portions 30 and 32 are formed on a substrate 24 extending primarily in x- and y-directions. The source and the drain 22 and 24 are spaced from one another in the y-direction and connected to opposing sides of the channel 26 to provide a set voltage over the channel 26. The first and second gate portions 30 and 32 are spaced from one another in the x-direction and located on opposing sides of the channel 26, such that application and removal of a gate voltage over the gate portions respectively reduces and increases current that conducts between the source 22 and the drain 24.

[0052] It should also be evident that a method of controlling current flow is described. A set voltage is applied over the source 22 and the drain 24 connected over the channel 26 formed on the substrate 24 extending in x- and y-directions. A gate voltage is alternately applied and removed over the first and second gate portions 30 and 32 spaced from one another in the x-direction, application of the gate voltage repelling majority carriers in the x-direction to reduce current flowing through the channel 26.

[0053] The JFET 20 formed by the structure in Figures 1 to 9 consists of a long channel 26 of semiconductor material. This material is doped so that it contains an abundance of positive charge carriers (p-type), or of negative charge carriers (n-type). There is a contact at each end; these are the source and drain 22 and 24. The third control terminal, the gate, surrounds the channel 26, and is doped opposite to the doping-type of the channel 26.

[0054] With no gate voltage, current flows easily when a voltage is applied between the source 22 and drain 24. The current flow is modulated by applying a voltage between gate and source terminals. The polarity of the gate voltage is such that it puts the p-n junction between the gate and channel in reverse bias, increasing the width of the depletion region

in the junction. As the current-carrying channel shrinks with increasing gate voltage, the current from source to drain also shrinks. In this way, the gate controls the conductance of the channel 26, just like in a MOSFET. Unlike most MOSFETs, JFETs are always depletion-mode devices — they're "on" unless a gate voltage is applied.

5 **[0055]** The JFET gate presents a small current load which is the reverse leakage of the gate-to-channel junction. The MOSFET has the advantage of extremely low gate current (measured in picoamps) because of the insulating oxide between the gate and channel. However, compared to the base current of a bipolar junction transistor the JFET gate current is much lower, and the JFET has higher transconductance than the MOSFET.
10 Therefore JFETs are used to advantage in some low-noise, high input-impedance op-amps and sometimes used in switching applications.

[0056] Current in N-JFET due to a small voltage V_{DS} is given by:

$$I_{DS} = (2a)WQD_D\mu\frac{V_{DS}}{L}$$ where

$2a$ = channel thickness

15 W = width

L = length

Q = electronic charge = 1.6×10^{-19} C

μ = electron mobility

[0057] In saturation region,

$$I_{DS} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

20

[0058] In linear region,

$$I_D = \frac{(2a)WQN_D\mu_D}{L}\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{1/2}\right]V_{DS}$$

[0059] A second embodiment shown in Figures 10 to 12 illustrates another alternate embodiment having a source 64, a drain 66, a n-well channel 72, and first gate 68 and
25 second gate 70. As shown in Figure 10, the source 64 and drain 66 are spaced in the y-direction, while the first gate 68 and second gate 70 are generally spaced in the x-direction from one another within a p-substrate 74. The n-well channel 72 connects the source 64 and drain 66 to allow current to flow between them when a voltage is applied through contact material 78.

30 **[0060]** As shown in Figure 12, the first gate 68 and second gate 70 can have a voltage

applied to them through gate contact material 80. As shown in Figure 11, the n-well channel 72 has a source end 72a and a drain end 72b.

[0061] A third gate 76 extends in primarily x- and y-directions and is located on top of first gate 68 and second gate 70, and the n-well channel 72. The third gate 76 can be chosen from any known effective conductor or gate material such as polysilicon.

[0062] As shown in Figures 11 and 12, the n-well channel 72 extends under the first gate 68 and second gate 70 to connect the source 64 and drain 66. Referring to Figure 12 specifically, the first gate 68 and second gate 70 are aligned in the same plane above the n-well channel 72.

[0063] Referring specifically to Figure 11, the source end 72a of the n-well channel 72 is in full contact with the source 64 N+ region; however, the drain end 72b of the n-well channel 72 is only slightly touching the drain 66 N+ region. Moreover, referring to Figure 10, the first gate 68 and second gate 70 are offset slightly in the y-direction toward the drain 66.

[0064] The n-well channel can have an impurity concentration of about $1{\times}10^{18}$ cm^{-3}, and source and drain concentrations can be about $1{\times}10^{20}$ cm^{-3}.

[0065] The first gate 68 and second gate 70 and the source 64 and drain 66 can be manufactured to a depth of about .3 μm from the top of the p-substrate 36. The n-well 72 can be manufactured to a depth of about 1.7 μm.

[0066] In use, a set voltage is applied between the source 64 and drain 66 through contact material 78 in order to allow a current to flow between the source 64 and drain 66 via the n-well channel 72. However, when a negative gate voltage is applied through gate contact material 80 to the first gate 68 and second gate 70, a reverse bias region is created by pushing holes away in the n-well channel 72 and the n-well channel ends 72a and 72b. As shown in Figure 12, the reverse bias region will pinch off the n-well channel 72 in the z-direction. Also shown in Figure 12, a negative voltage on the third gate 76 will invert the n-well channel 72, thereby causing further depletion. Typically, pinching the current flow in the z-direction alone may still be ineffective in preventing bulk current leakage that occurs at the bottom of the n-well channel 72.

[0067] However, referring to Figure 11, the n-well channel 72 is only slightly touching the drain 66 N+ region at the drain end 72b. Moreover, the first gate 68 and second gate 70 are laterally disposed on either side of the n-well channel drain end 72b, and offset in the y-direction toward the drain 66. When a gate voltage is applied to all the gates 68, 70,

and 76, a gate voltage not only pinches in the z-direction but also in the x- and y-directions as well. The pinching at the n-well channel drain end 72b causes the drain 66 to be isolated and ceases all current flow.

[0068] The combination of providing a small drain 66 contact area with the n-well drain end 72b and specifically placing first gate 68 and second gate 70 near the n-well drain end 72b results in drain isolation. Therefore, bulk leakage through the bottom of the n-well channel 72 is not a concern, since the drain 66 is pinched off from the source 64. In this arrangement, a large amount of voltage is not needed to pinch off the n-well channel 72. The n-well channel 72 is sufficiently thin so that it can be pinched off with just a few volts.

[0069] As mentioned before, NMOS arrangements have a higher 1/f noise because of the flow of electrons along an oxide-silicon interface. Also, JFET arrangements without a buried gate may require several hundred volts to deplete a deep channel.

[0070] The main advantage of the embodiment of Figures 10-12 is that the device is able to eliminate any 1/f noise resulting from an oxide-silicon interface, while shutting off current flow without the use of a buried gate and without the use of several hundred volts. Furthermore, the unique location of the first gate 68, second gate 70, and n-well channel 72 enables the device to deplete a deep channel without the use of a buried gate, while also eliminating bulk leakage that might occur through the bottom of the n-well channel by isolating the drain 66.

[0071] While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative and not restrictive of the current invention, and that this invention is not restricted to the specific constructions and arrangements shown and described since modifications may occur to those ordinarily skilled in the art.

CLAIMS

What is claimed:

1. A microelectronic product comprising:
5 a substrate extending primarily in x- and y-directions;
a channel formed on the substrate;
a source and drain spaced from one another in the y-direction and connected to opposing sides of the channel to provide a set voltage over the channel; and
first and second gate portions spaced from one another in the x-direction and located
10 on opposing sides of the channel to allow for application and removal of a gate voltage over the gate portions, application of the gate voltage repelling majority carriers in the x-direction to reduce current that conducts between the source and the drain.

2. A microelectronic product as claimed in claim 1, further comprising a p-doped layer
15 on the substrate, the channel being an n-doped channel on the p-doped layer, and a p+ doped implant next to the channel, the first and second gate portions being the p+ doped implant and a portion of the p-doped layer respectively.

3. A microelectronic product as claimed in claim 2, further comprising an electrode
20 above the p-doped layer, the channel being a tip implant below the electrode.

4. A microelectronic product as claimed in claim 2, wherein the p-doped layer forms a third gate portion below the channel.

25 5. A microelectronic product as claimed in claim 1, further comprising an n-well, the channel being an upper portion of the n-well, wherein current leakage below the channel between the source and the drain is prevented due to the first and second gate portions repelling majority carriers in the n-well below the channel.

30 6. A microelectronic product as claimed in claim 5, further comprising a third gate position above the channel and repelling majority carriers in a z-direction.

7. A microelectronic product as claimed in claim 1, wherein the source and the drain

are n+ regions.

8. A microelectronic product as claimed in claim 7, wherein the channel is n-doped.

5 9. A microelectronic product as claimed in claim 8, wherein the first and second gates are p+ regions.

10. A method of making a junction field effect transistor, comprising:

forming a channel, a source, a drain, and first and second gate portions on a substrate 10 extending primarily in x- and y-directions, the source and the drain being spaced from one another in the y-direction and connected to opposing sides of the channel to provide a set voltage over the channel, and the first and second gate portions being spaced from one another in the x-direction and located on opposing sides of the channel, such that application and removal of a gate voltage over the gate portions respectively reducing and 15 increasing current that conducts between the source and the drain.

11. The method of making a junction field effect transistor as claimed in claim 10, further comprising forming a p-doped layer on the substrate, the channel being an n-doped channel on the p-doped layer, and a p+ doped implant next to the channel, the first and 20 second gate portions being the p+ doped implant and a portion of the p-doped layer respectively.

12. The method of making a junction field effect transistor as claimed in claim 10, further comprising forming an n-well, the channel being an upper portion of the n-well, 25 wherein current leakage below the channel between the source and the drain is prevented due to the first and second gate portions repelling majority carriers in the n-well below the channel.

13. A method of controlling current flow, comprising:

30 applying a set voltage over a source and a drain connected over a channel formed on a substrate extending in x- and y-directions; and

alternately applying and removing a gate voltage over first and second gate portions spaced from one another in the x-direction, application of the gate voltage repelling

majority carriers in the x-direction to reduce current flowing through the channel.

14. The method of controlling current flow as claimed in claim 13, further comprising applying the gate voltage to a gate portion between the substrate and the channel to repel
5 majority carriers in a z-direction.

15. The method of controlling current flow as claimed in claim 14, further comprising applying the gate voltage to a gate portion on a side of the channel opposing the substrate to repel majority carriers in a z-direction.

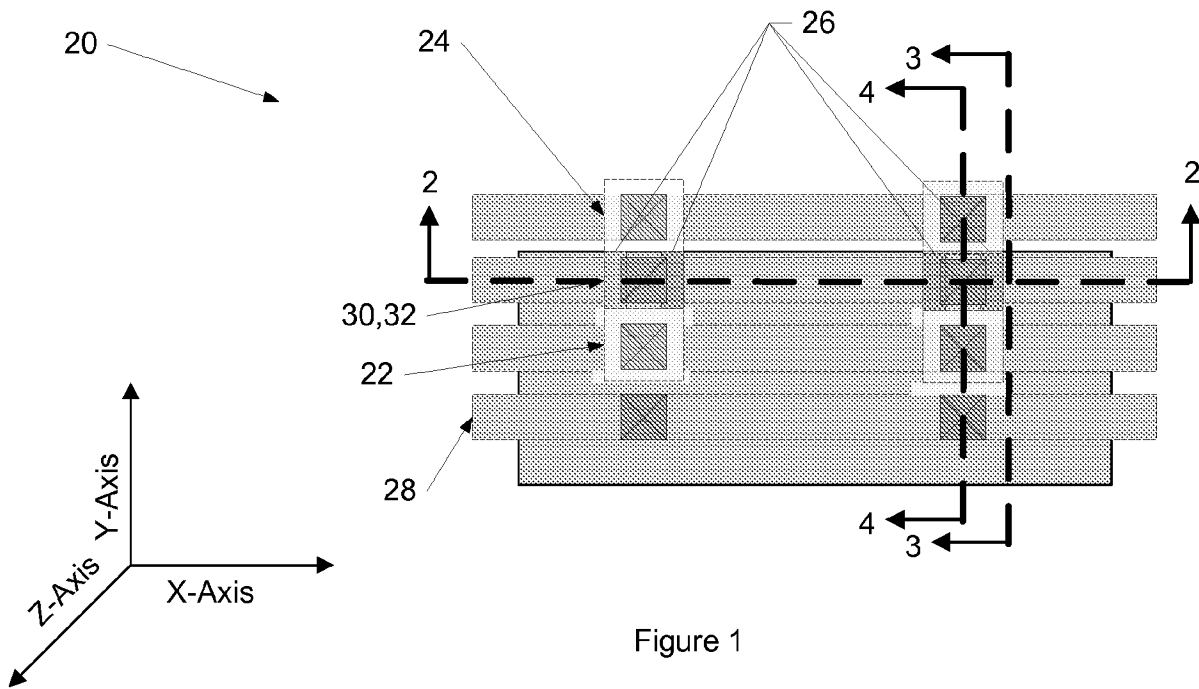


Figure 1

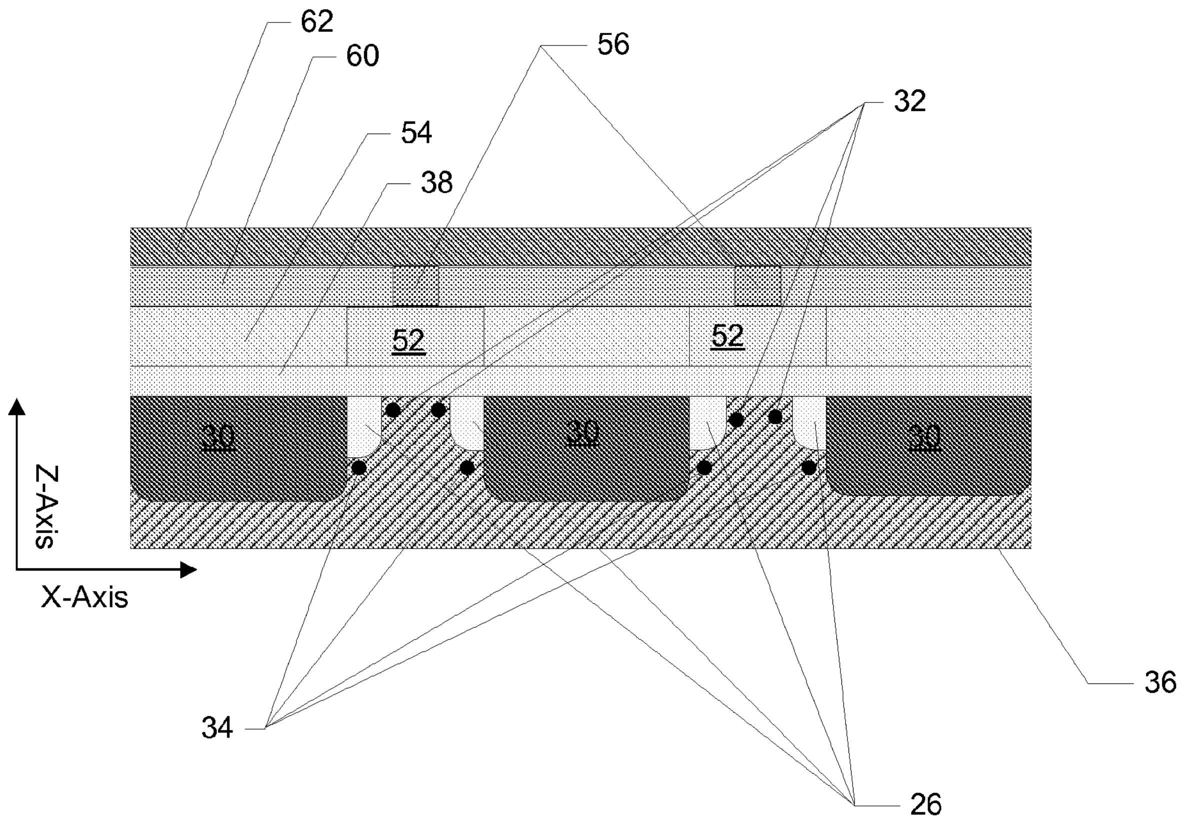


Figure 2

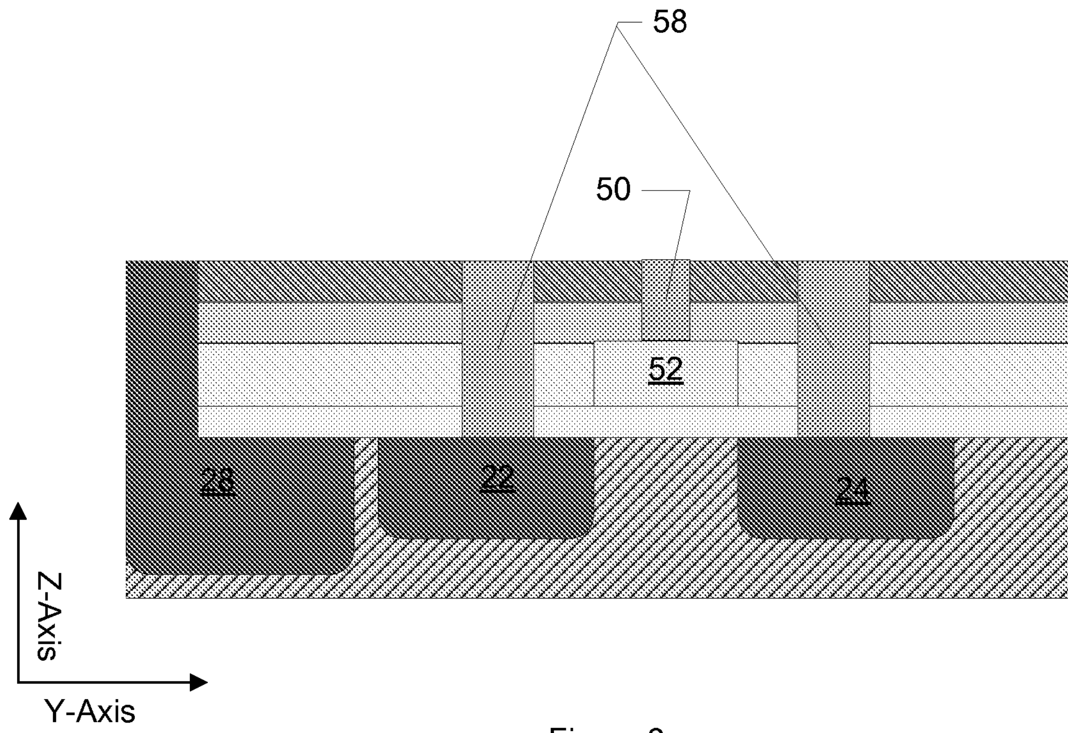


Figure 3

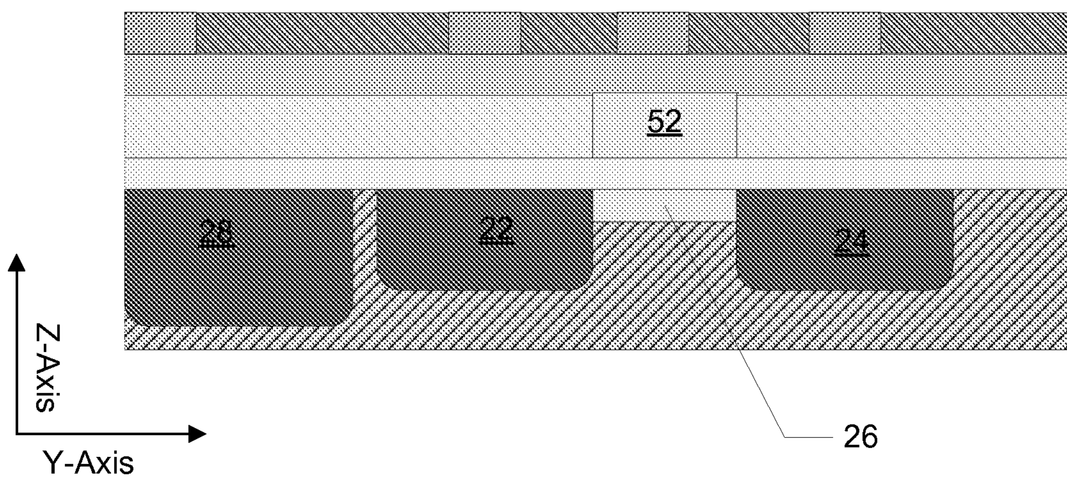
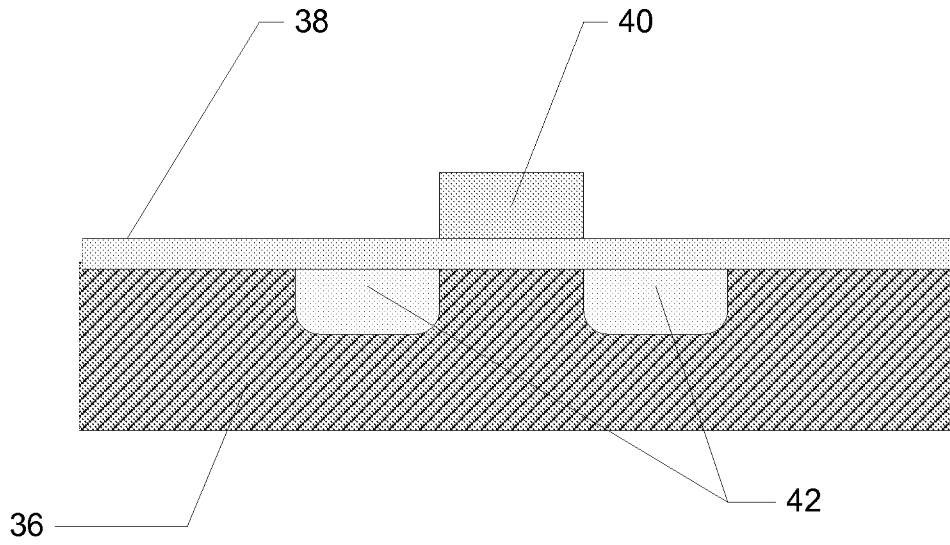


Figure 4



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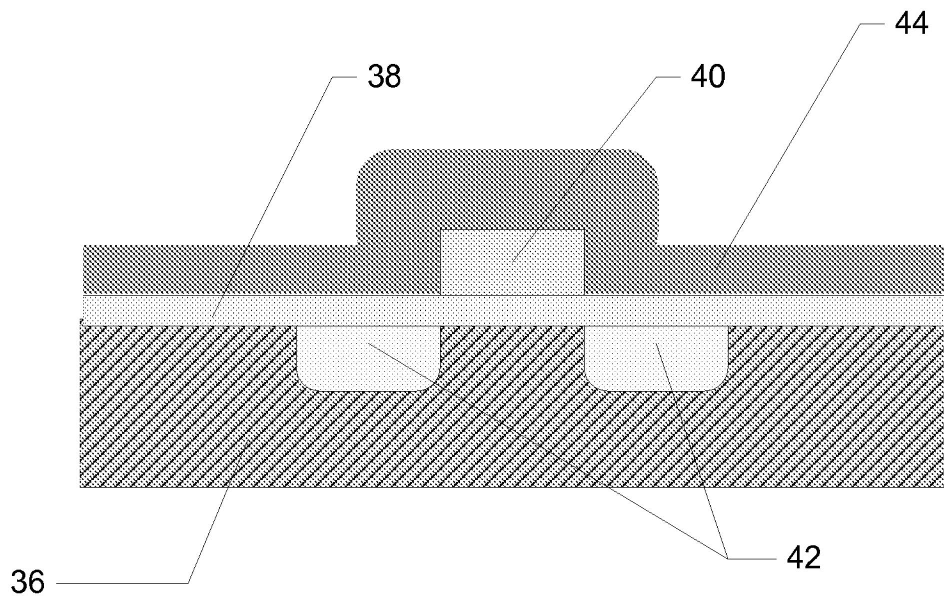
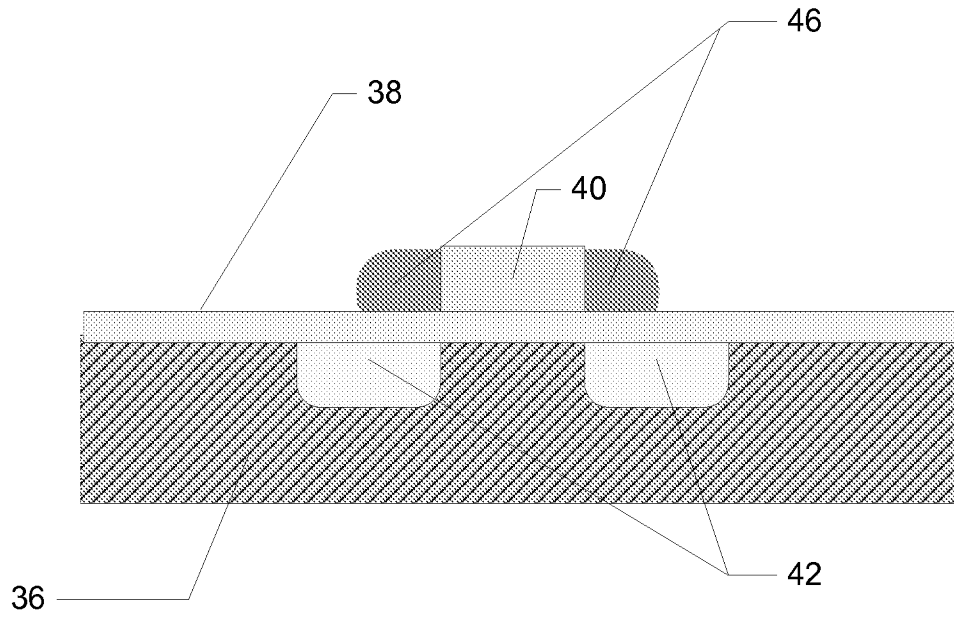


Figure 6



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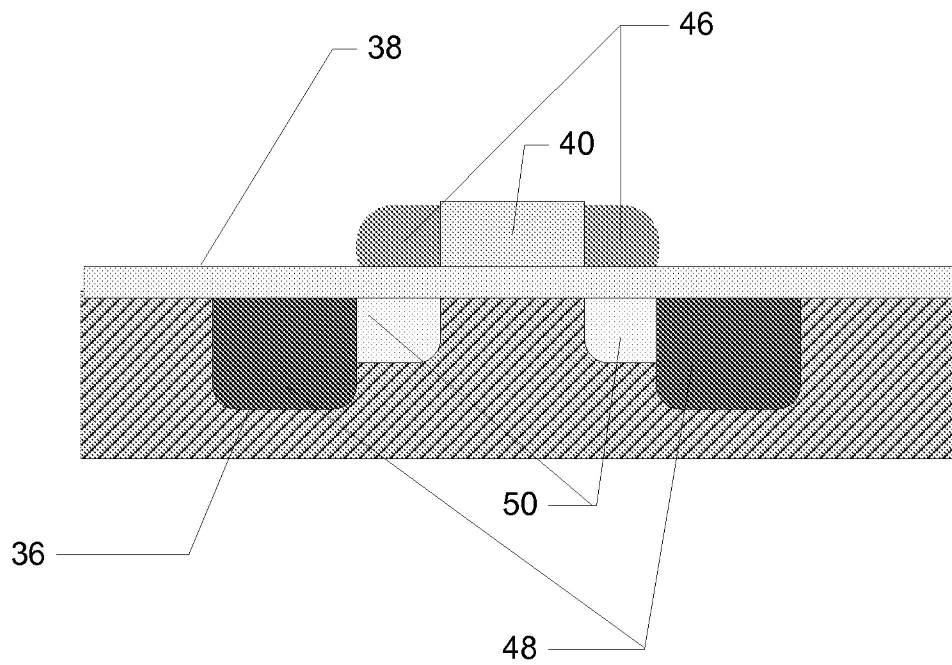

Figure 8

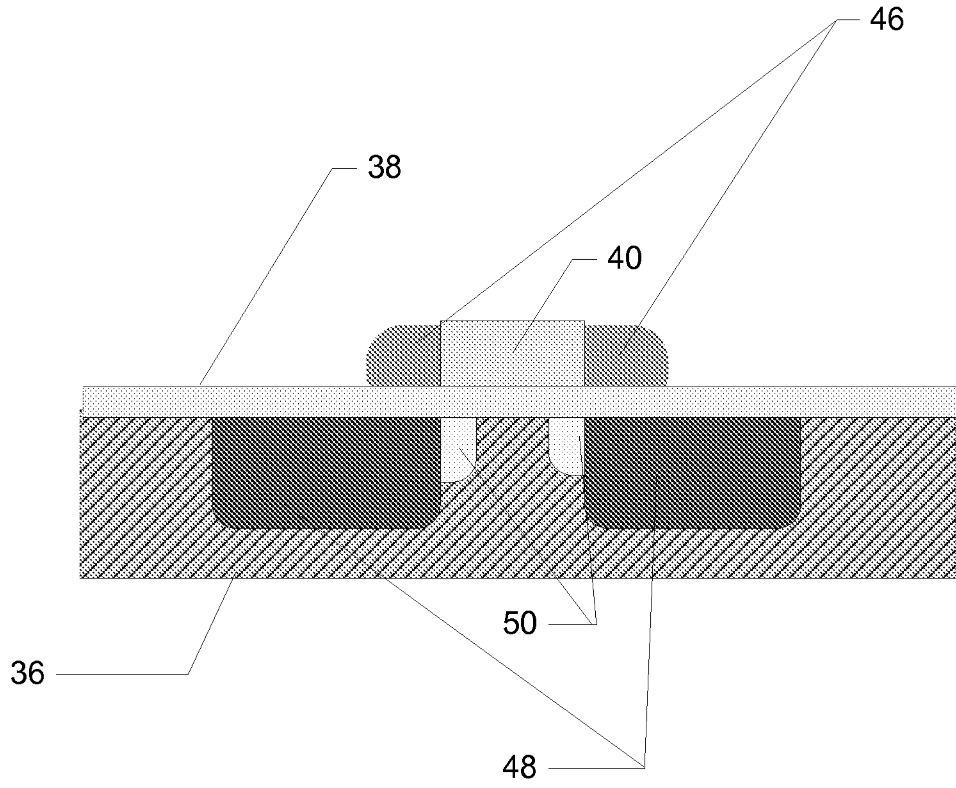

Figure 9

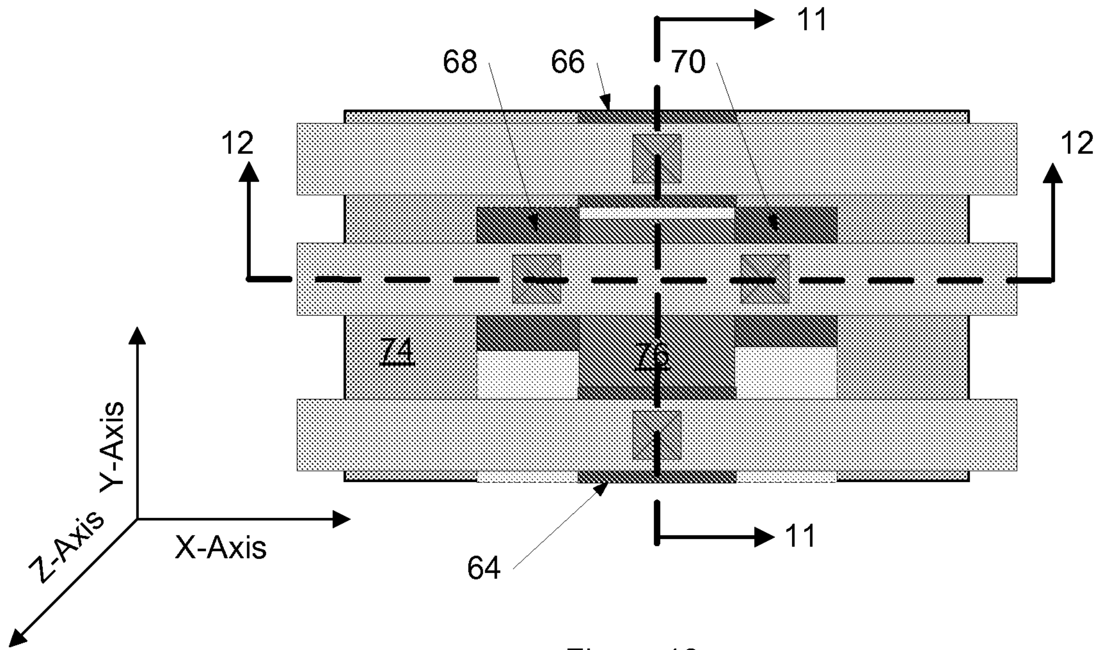

Figure 10

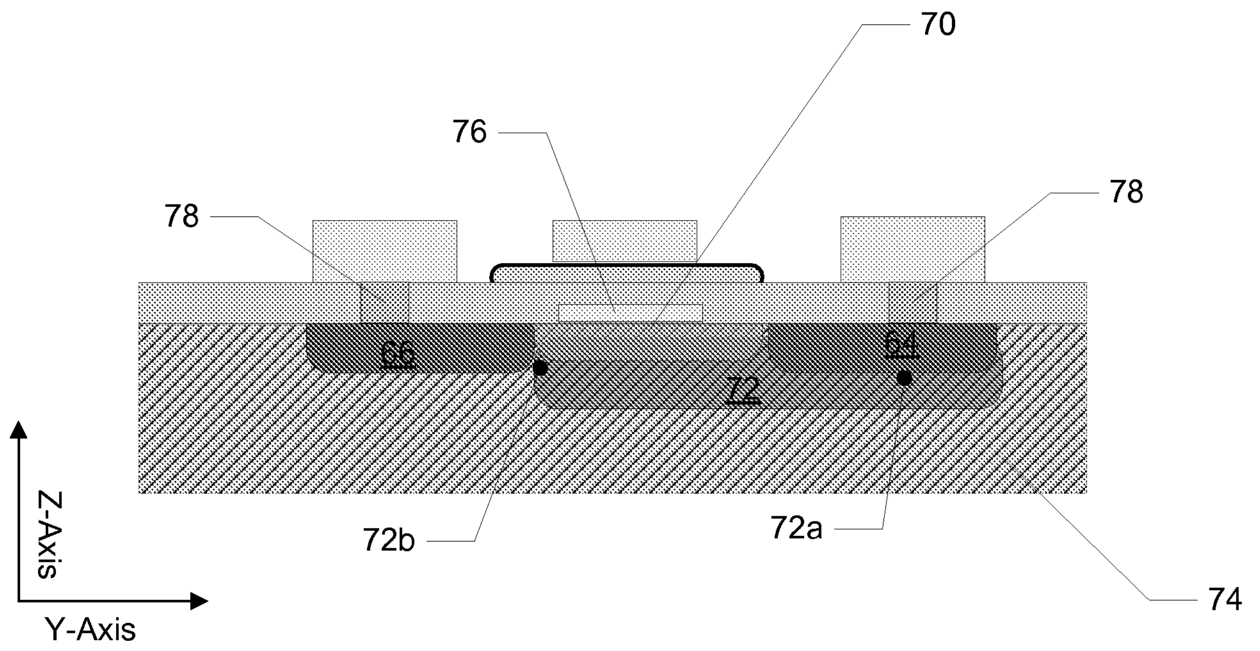

Figure 11

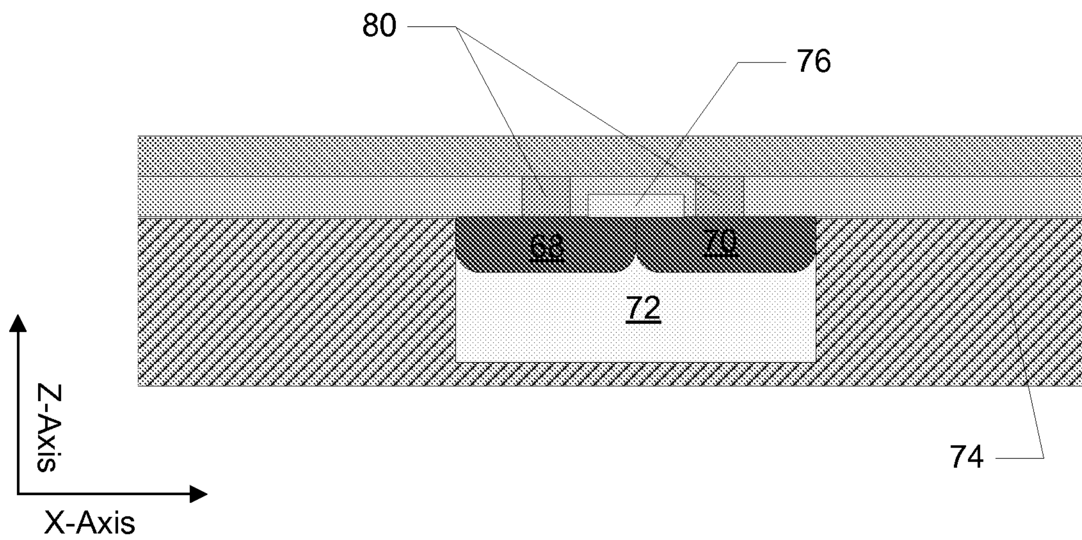

Figure 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2007/078438

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/335(2006.01)i, H01L 29/78(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 8 : H01L21/22, H01L21/335, H01L21/336, H01L21/337, H01L21/338

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Utility models and applications for Utility models since 1975
Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKIPASS(KIPONET internal) "JFET"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US04373253 A (National Semiconductor Corp.) 15 February 1983 See the abstract, figure 12	1-15
A	US06624030 B2 (Advanced Power Devices, Inc.) 23 September 2003 See the abstract, figure 4	1-15
A	JP18196789 A (Nikon Corp.) 27 July 2006 See the abstract, figure 2	1-12
A	JP10256273 A (Toshiba Corp.) 25 September 1998 See the abstract, figures 1,9	1-12

☐ Further documents are listed in the continuation of Box C.   ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 JANUARY 2008 (07.01.2008)	**07 JANUARY 2008 (07.01.2008)**

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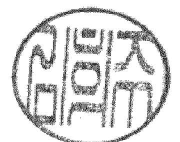
KIM, Hee Ju



Telephone No. 82-42-481-5800

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2007/078438

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
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JP18196789	A	27.07.2006	NONE	
JP10256273	A	25.09.1998	NONE	