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(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) Inventors: KHIRE, Vaibhav S.; 4673 NW 126th PL, Portland, Oregon 97229 (US). GANESAN, Krishna Prakash; 11371 NW Odeon Ln, Portland, Oregon 97229 (US). LYTLE, Wayne M.; 53110 NW Strassel Road, Banks, Oregon 97106 (US). SATTIRAJU, Seshu V.; 15744 NW Wismer Dr, Portland, Oregon 97229 (US).

(74) Agents: PARKER, Wesley E. et al.; 1211 SW 5th Avenue, Suite 1600, Portland, Oregon 97204 (US).

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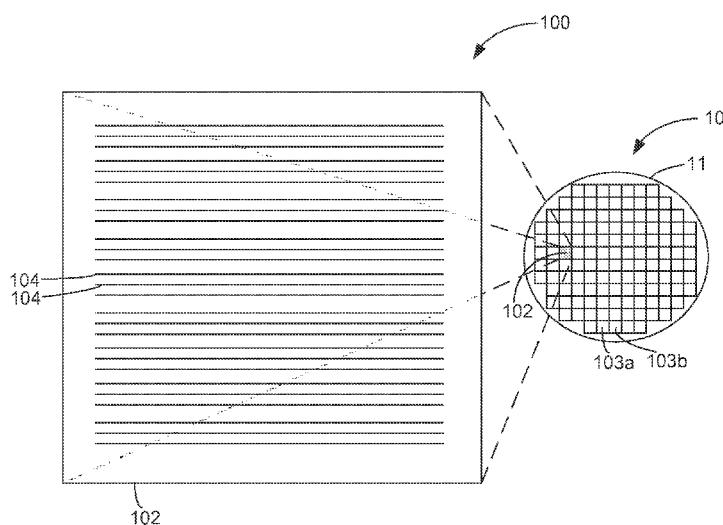


FIG. 1

(57) Abstract: Embodiments of the present disclosure describe techniques to prevent film cracking in thermally cured dielectric film, and associated configurations. A dielectric film may be formed on a patterned metal layer and a substrate on which the patterned metal layer is disposed. A photo-patterned dielectric resist film may be formed on the dielectric film, while providing an opening in the dielectric resist film over the metal layer. A first curing process may be performed to remove a solvent from the dielectric resist film. An exposed portion of the dielectric film, that is disposed in the opening, may then be removed. A second curing process may be performed after the exposed portion of the dielectric film is removed, to polymerize the dielectric resist film. Other embodiments may be described and/or claimed.

TECHNIQUES TO PREVENT FILM CRACKING IN THERMALLY CURED DIELECTRIC FILM, AND ASSOCIATED CONFIGURATIONS

Field

5 Embodiments of the present disclosure generally relate to the field of integrated circuits, and more particularly, to techniques to prevent film cracking in thermally cured dielectric film, and associated configurations.

Background

10 In integrated circuit devices, a patterned dielectric stack may be formed on a semiconductor substrate by spinning a dielectric resist on a dielectric film, thermally curing the dielectric resist, and then etching away the dielectric film from openings in the spun dielectric resist. However, the etching of the dielectric film can result in damage to the cured dielectric resist.

Brief Description of the Drawings

15 Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example and not by way of limitation in the figures of the accompanying drawings.

20 **FIG. 1** schematically illustrates a top view of an example die in wafer form and in singulated form, in accordance with some embodiments.

FIG. 2 schematically illustrates a cross-section side view of an integrated circuit (IC) assembly, in accordance with some embodiments.

25 **FIG. 3** is a flow diagram that illustrates a method for forming an IC structure including a patterned dielectric stack, in accordance with some embodiments.

FIGS. 4A-E schematically illustrate a cross-section side view of an IC structure during various stages of the method of **FIG. 3**, in accordance with some embodiments.

30 **FIG. 5** schematically illustrates an example system that may include a transistor electrode assembly as described herein, in accordance with some embodiments.

Detailed Description

Embodiments of the present disclosure describe techniques to prevent film cracking in thermally cured dielectric film, and associated configurations. A dielectric film may be formed on a patterned metal layer and a substrate on which the patterned metal layer is disposed. A photo-patterned dielectric resist film may be formed on the dielectric film, while providing an opening in the dielectric resist film over the metal layer. A first curing process may be performed to remove a solvent from the dielectric resist film. An exposed portion of the dielectric film, that is disposed in the opening, may then be removed. A second curing process may be performed after the exposed portion of the dielectric film is removed, to polymerize the dielectric resist film.

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, wherein like numerals designate like parts throughout, and in which is shown by way of illustration embodiments in which the subject matter of the present disclosure may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense, and the scope of embodiments is defined by the appended claims and their equivalents.

For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C).

The description may use perspective-based descriptions such as top/bottom, side, over/under, and the like. Such descriptions are merely used to facilitate the discussion and are not intended to restrict the application of embodiments described herein to any particular orientation.

The description may use the phrases "in an embodiment," or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous.

The term “coupled with,” along with its derivatives, may be used herein. “Coupled” may mean one or more of the following. “Coupled” may mean that two or more elements are in direct physical or electrical contact. However, “coupled” may also mean that two or more elements indirectly contact each other, but yet still cooperate or interact with each other, and may mean that one or more other elements are coupled or connected between the elements that are said to be coupled with each other. The term “directly coupled” may mean that two or more elements are in direct contact.

In various embodiments, the phrase “a first feature formed, deposited, or otherwise disposed on a second feature” may mean that the first feature is formed, deposited, or disposed over the second feature, and at least a part of the first feature may be in direct contact (e.g., direct physical and/or electrical contact) or indirect contact (e.g., having one or more other features between the first feature and the second feature) with at least a part of the second feature.

As used herein, the term “circuitry” may refer to, be part of, or include an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group) and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable components that provide the described functionality.

FIG. 1 schematically illustrates a top view of an example die 102 in wafer form 10 and in singulated form 100, in accordance with some embodiments. In some embodiments, the die 102 may be one of a plurality of dies (e.g., dies 102, 103a, 103b) of a wafer 11 composed of semiconductor material such as, for example, silicon or other suitable material. The plurality of dies may be formed on a surface of the wafer 11. Each of the dies may be a repeating unit of a semiconductor product that includes one or more integrated circuit (IC) structures (e.g., IC structure 400 of FIG. 4F) as described herein. For example, the die 102 may include circuitry having transistor structures 104 such as, for example, one or more channel bodies (e.g., fin structures, nanowires, planar bodies, etc.) that provide a channel pathway for mobile charge carriers of one or more transistor devices or source/drain regions. Electrical interconnect structures such as, for example, transistor electrode assemblies (e.g., terminal contacts) may be formed

on and coupled with the one or more transistor structures 104 to route electrical energy to or from the transistor structures 104. For example, terminal contacts may be electrically coupled with a channel body to provide a gate electrode for delivery of a threshold voltage and/or a source/drain current to provide mobile charge carriers for operation of a transistor device. Although the transistor structures 104 are depicted in rows that traverse a substantial portion of the die 102 in FIG. 1 for the sake of simplicity, it is to be understood that the transistor structures 104 may be configured in any of a wide variety of other suitable arrangements on the die 102 in other embodiments, including, for example, vertical and horizontal features having much smaller dimensions than depicted.

After a fabrication process of the semiconductor product embodied in the dies is complete, the wafer 11 may undergo a singulation process in which each of the dies (e.g., die 102) is separated from one another to provide discrete “chips” of the semiconductor product. The wafer 11 may be any of a variety of sizes. In some embodiments, the wafer 11 has a diameter ranging from about 25.4 mm to about 450 mm. The wafer 11 may include other sizes and/or other shapes in other embodiments. According to various embodiments, the transistor structures 104 may be disposed on a semiconductor substrate in wafer form 10 or singulated form 100. The transistor structures 104 described herein may be incorporated in a die 102 for logic or memory, or combinations thereof. In some embodiments, the transistor structures 104 may be part of a system-on-chip (SoC) assembly.

FIG. 2 schematically illustrates a cross-section side view of an IC assembly 200, in accordance with some embodiments. In some embodiments, the IC assembly 200 may include one or more dies (hereinafter “die 102”) electrically and/or physically coupled with a package substrate 121. In some embodiments, the package substrate 121 may be electrically coupled with a circuit board 122, as can be seen. In some embodiments, an integrated circuit (IC) assembly 200 may include one or more of the die 102, package substrate 121 and/or circuit board 122, according to various embodiments. Embodiments described herein for an IC structure may be implemented in any suitable IC device according to various embodiments.

The die 102 may represent a discrete product made from a semiconductor material (e.g., silicon) using semiconductor fabrication techniques

such as thin film deposition, lithography, etching and the like used in connection with forming CMOS devices. In some embodiments, the die 102 may be, include, or be a part of a processor, memory, SoC or ASIC. In some embodiments, an electrically insulative material such as, for example, molding compound or underfill material (not shown) may encapsulate at least a portion of the die 102 and/or die-level interconnect structures 106.

The die 102 can be attached to the package substrate 121 according to a wide variety of suitable configurations including, for example, being directly coupled with the package substrate 121 in a flip-chip configuration, as depicted. In the flip-chip configuration, an active side, S1, of the die 102 including circuitry is attached to a surface of the package substrate 121 using die-level interconnect structures 106 such as bumps, pillars, or other suitable structures that may also electrically couple the die 102 with the package substrate 121. The active side S1 of the die 102 may include active devices such as, for example, transistor devices. An inactive side, S2, may be disposed opposite to the active side S1, as can be seen.

The die 102 may generally include a semiconductor substrate 102a, one or more device layers (hereinafter "device layer 102b") and one or more interconnect layers (hereinafter "interconnect layer 102c"). The semiconductor substrate 102a may be substantially composed of a bulk semiconductor material such as, for example silicon, in some embodiments. The device layer 102b may represent a region where active devices such as transistor devices are formed on the semiconductor substrate. The device layer 102b may include, for example, transistor structures such as channel bodies and/or source/drain regions of transistor devices. The interconnect layer 102c may include interconnect structures (e.g., electrode terminals) that are configured to route electrical signals to or from the active devices in the device layer 102b. For example, the interconnect layer 102c may include horizontal lines (e.g., trenches) and/or vertical plugs (e.g., vias) or other suitable features to provide electrical routing and/or contacts.

In some embodiments, the die-level interconnect structures 106 may be electrically coupled with the interconnect layer 102c and configured to route electrical signals between the die 102 and other electrical devices. The electrical

signals may include, for example, input/output (I/O) signals and/or power/ground signals that are used in connection with operation of the die 102.

In some embodiments, the package substrate 121 is an epoxy-based laminate substrate having a core and/or build-up layers such as, for example, an Ajinomoto Build-up Film (ABF) substrate. The package substrate 121 may include other suitable types of substrates in other embodiments including, for example, substrates formed from glass, ceramic, or semiconductor materials.

The package substrate 121 may include electrical routing features configured to route electrical signals to or from the die 102. The electrical routing features may include, for example, pads or traces (not shown) disposed on one or more surfaces of the package substrate 121 and/or internal routing features (not shown) such as, for example, trenches, vias or other interconnect structures to route electrical signals through the package substrate 121. For example, in some embodiments, the package substrate 121 may include electrical routing features such as pads (not shown) configured to receive the respective die-level interconnect structures 106 of the die 102.

The circuit board 122 may be a printed circuit board (PCB) composed of an electrically insulative material such as an epoxy laminate. For example, the circuit board 122 may include electrically insulating layers composed of materials such as, for example, polytetrafluoroethylene, phenolic cotton paper materials such as Flame Retardant 4 (FR-4), FR-1, cotton paper and epoxy materials such as CEM-1 or CEM-3, or woven glass materials that are laminated together using an epoxy resin prepreg material. Interconnect structures (not shown) such as traces, trenches, or vias may be formed through the electrically insulating layers to route the electrical signals of the die 102 through the circuit board 122. The circuit board 122 may be composed of other suitable materials in other embodiments. In some embodiments, the circuit board 122 is a motherboard (e.g., motherboard 502 of FIG. 5).

Package-level interconnects such as, for example, solder balls 112 may be coupled to one or more pads (hereinafter "pads 110") on the package substrate 121 and/or on the circuit board 122 to form corresponding solder joints that are configured to further route the electrical signals between the package substrate 121 and the circuit board 122. The pads 110 may be composed of any

suitable electrically conductive material such as metal including, for example, nickel (Ni), palladium (Pd), gold (Au), silver (Ag), copper (Cu), and combinations thereof. Other suitable techniques to physically and/or electrically couple the package substrate 121 with the circuit board 122 may be used in other

5 embodiments.

The IC assembly 200 may include a wide variety of other suitable configurations in other embodiments including, for example, suitable combinations of flip-chip and/or wire-bonding configurations, interposers, multi-chip package configurations including system-in-package (SiP) and/or package-on-package (PoP) configurations. Other suitable techniques to route electrical signals between the die 102 and other components of the IC assembly 200 may be used in some embodiments.

FIG. 3 is a flow chart to illustrate a method 300 for forming an IC structure in accordance with various embodiments. **FIGS. 4A, 4B, 4C, 4D, 4E,** and **4F** schematically illustrate a cross-sectional side view of an IC structure 400 at various stages of the method 300, in accordance with various embodiments. Accordingly, the method 300 will be described below with reference to **FIGS. 4A-4E**. Similar fabrication principles to those described herein may be used to form IC structures with other configurations than that shown in **FIGS. 4A-4E**. In some embodiments, the IC structure 400 may correspond to an electrode terminal (e.g., a contact of a gate, source, or drain) of a transistor. Alternatively, the IC structure 400 may correspond to an interconnect structure (e.g., a trench or via).

At 302, the method 300 may include forming a metal layer on a portion of a substrate. For example, **FIG. 4A** illustrates the IC structure 400 including a metal layer 402 formed on a portion of a substrate 404. In some embodiments, the metal layer 402 may be in direct contact with the substrate 404, as shown in **FIG. 4A**. In other embodiments, one or more other material layers may be disposed between the metal layer 402 and the substrate 404.

The metal layer may be formed on the portion of the substrate by any suitable deposition technique, including a conformal and/or selective deposition process. For example, the metal layer may be formed by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), electroless, electroplating, or suitable combinations of these deposition techniques.

The metal layer may include any suitable metal. For example, in some embodiments, the metal layer may include copper (Cu), gold (Au), tungsten (W), titanium (Ti), tantalum (Ta), platinum (Pt), nickel (Ni), cobalt (Co), rhodium (Rh), ruthenium (Ru), palladium (Pd), hafnium (Hf), zirconium (Zr), or aluminum (Al), or combinations thereof. In some embodiments, the metal layer may include a metal nitride such as, for example, titanium nitride (TiN), tungsten nitride (WN), or tantalum nitride (Ta₃N₅), or combinations thereof. In some embodiments, the metal may include a metal silicide such as, for example, titanium silicide (TiSi₂), tungsten silicide (WSi₂), tantalum silicide (TaSi₂), cobalt silicide (CoSi₂), platinum silicide (PtSi₂), nickel silicide (NiSi₂), or combinations thereof. In some embodiments, the metal layer may include a metal silicon nitride such as, for example, titanium silicon nitride (TiSiN), or tantalum silicon nitride (TaSiN), or combinations thereof. In some embodiments, the metal layer may include a metal carbide such as, for example, titanium carbide (TiC), zirconium carbide (ZrC), tantalum carbide (TaC), hafnium carbide (HfC), or aluminum carbide (AlC), or combinations thereof. In some embodiments, the metal layer may include a metal carbon nitride such as, for example, tantalum carbon nitride (TaCN), titanium carbon nitride (TiCN), or combinations thereof. In some embodiments, the metal layer may include a conductive metal oxide (e.g., ruthenium oxide).

At 304, the method 300 may further include forming a dielectric film on the metal layer and the substrate. For example, FIG. 4B illustrates the IC structure 400 with a dielectric film 406 formed on the metal layer 402 and the substrate 404. The dielectric film 406 may be unpatterned (e.g., deposited on an entire surface of the IC structure 400). The dielectric film 406 may be in direct contact with top and sidewall surfaces of the metal layer 402. Additionally, the dielectric film 406 may be disposed on the substrate 404 adjacent to the metal layer 402. The dielectric film 406 may be in direct contact with the substrate 404, as shown in FIG. 4B, or one or more other material layers may be disposed between the dielectric film 406 and the substrate 404. The dielectric film 406 may act as an adhesion film between the metal layer 402 and a dielectric resist film that is formed on the dielectric film 406, as further discussed below.

The dielectric film may be formed by any suitable deposition process, such as CVD, ALD, or PVD. Additionally, the dielectric film may include

any suitable dielectric material or combination of dielectric materials, including one or more high-K or low-K materials.

For example, the dielectric film may include silicon oxide (SiO_2), silicon oxynitride (SiO_xN_y), silicon nitride (Si_xN_y), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), hafnium aluminum oxide (HfAl_xO_y), hafnium silicon oxide (HfSi_xO_y), zirconium oxide (ZrO_2), zirconium silicon oxide (ZrSi_xO_y), lanthanum oxide (La_2O_3), yttrium oxide (Y_2O_3), lanthanum aluminum oxide (LaAl_xO_y), tantalum oxide (Ta_2O_5), titanium oxide (TiO_2), barium strontium titanium oxide ($\text{BaSrTi}_x\text{O}_y$), barium titanium oxide (BaTi_xO_y), strontium titanium oxide (SrTi_xO_y), lead scandium tantalum oxide ($\text{PbSc}_x\text{Ta}_y\text{O}_z$), or lead zinc niobate ($\text{PbZn}_x\text{Nb}_y\text{O}_z$), carbon doped oxide (CDO), organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass, or combinations thereof, where x, y, and z represent suitable quantities of the respective elements. In some embodiments, an annealing process may be carried out on the dielectric layer to improve its quality when a high-k material is used. Other materials may be used in other embodiments for the dielectric layer.

At 306, the method 300 may further include forming a photo-patterned resist film (e.g., a dielectric resist film) on the dielectric film, leaving an opening (e.g., a gap or recess) in the resist film over the metal layer. For example, FIG. 4C illustrates the IC structure 400 with a photo-patterned dielectric resist film 408 (hereinafter "resist film 408") formed on the dielectric film 406, and providing an opening 410 in the resist film 408 above the metal layer 402. In some embodiments, a width of the opening 410 may be substantially the same as a width of the metal layer 402. In other embodiments, the width of the opening 410 may be shorter or longer than the width of the metal layer 402. As discussed above, the dielectric film 406 may act as an adhesion film between the metal layer 402 and the resist film 408.

The resist film may be formed on the dielectric film by any suitable process, such as a spin-on process (e.g., spin-on glass (SOG)). In some embodiments, the resist film may be formed on the IC structure by the spin-on process, and then a portion of the resist film may be removed to form the opening. As formed on the dielectric film, the resist film may include one or more resist materials and one or more solvents. The one or more resist materials may

include any suitable material that will resist etching when an exposed portion of the dielectric film is etched away (e.g., by dry etch), and/or that is polymerized by thermal curing, as further discussed below.

5 The one or more solvents may facilitate application of the resist film, e.g., by the spinning process. The one or more solvents may include any suitable solvent, such as an organic solvent, e.g., ethanol, toluene, acetone, etc.

At 308, the method 300 may include performing a first curing process on the resist film. The first curing process may remove the one or more solvents from the resist film. However, the first curing process may not
10 polymerize the resist film. The resist film may be referred to as a semi-cured resist film after the first curing process has been performed. FIG. 4D illustrates the IC structure 400 after the first curing process has been performed to remove the one or more solvents from the resist film 408.

The first curing process may include applying first curing conditions
15 to the resist film (e.g., subjecting the resist film to a first temperature for a first time period). In some embodiments, the first temperature may be about 125 degrees Celsius to about 175 degrees Celsius. Additionally, or alternatively, the first time period may be about 15 minutes to about 45 minutes.

At 310, the method 300 may include removing the dielectric layer
20 from the opening in the resist layer (e.g., from the top surface of the metal layer). For example, FIG. 4E illustrates the IC structure 400 with the dielectric layer 406 removed from the top surface of the metal layer 402 in the opening 410. The dielectric layer may be removed from opening by any suitable process, such as a dry etch process.

25 At 312, the method 300 may include performing a second curing process on the resist film. The second curing process may polymerize the resist film. The resist film may be referred to as a fully cured resist film after the first curing process has been performed. During polymerization, molecules of the one or more resist materials may bond to one another to form polymer chains. The
30 polymerization may harden the resist film. FIG. 4F illustrates the IC structure 400 after the second curing process has been performed to polymerize the resist film 408.

The second curing process may include applying second curing conditions to the resist film (e.g., subjecting the resist film to a second temperature

for a second time period). In some embodiments, the second temperature of the second curing process may be greater than the first temperature of the first curing process. Additionally, or alternatively, the second time period may be longer than the first time period.

5 For example, in some embodiments, the second temperature may be about 225 degrees Celsius to about 275 degrees Celsius. Additionally, or alternatively, the second time period may be about 60 minutes to about 120 minutes.

10 In various embodiments, separating the curing of the resist film into the first curing process and the second curing process, and removing the dielectric layer from the opening in the resist film in between the first curing process and the second curing process, may prevent or reduce cracking in the resist film. In prior fabrication techniques, the resist film is fully cured in a single curing process prior to etching away the dielectric. The etch conditions may
15 cause damage to the cured resist film, such as one or more cracks at the edge of the opening in the resist film. The cracks can deteriorate in subsequent (e.g., downstream) processing and may provide a path for chemical attack, ultimately resulting in failure of reliability and electrical properties of the die. These problems may be averted using the techniques described herein.

20 The removal of the one or more solvents in the resist layer, as effected by the first curing process, may be necessary for the removal of the dielectric film from the opening in the resist layer (e.g., by dry etch) to be effective. If the one or more solvents were present during the etch process, the resist film would not be physically well defined, and the one or more solvents may evaporate
25 in an uncontrolled manner during the etch process, thereby causing the resist film to become deformed, some of the uncured resist material to flow into the openings over the dielectric material resulting in unformed openings, lack of control during the etch process resulting in different areas of the wafer getting different etch processing and hence different film thicknesses, and/or incomplete polymerization
30 or unintended reaction in the resist film during the subsequent polymerization that is performed to harden the resist film. Additionally, evaporation of the one or more solvents in the etch chamber may cause damage to the etch chamber.

Furthermore, when the dielectric layer is removed from the opening (e.g., by dry etch) with a semi-cured resist film, the processing may not crack the

resist film since the resist film is still relatively soft (e.g., compared with the fully cured resist film). The second curing process may polymerize the resist film and thereby harden the resist film.

In various embodiments, after the resist layer is fully cured, further processing may be performed on the IC structure. For example, one or more additional material layers may be formed on the metal layer (e.g., in the opening in the resist layer). In some embodiments, one or more additional metal layers may be formed in the opening on the metal layer. For example, another metal layer with a different composition may be formed on the metal layer. In some embodiments, the metal layer and the other metal layer may form the electrode terminal of the transistor.

Various operations are described as multiple discrete operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. Embodiments of the present disclosure may be implemented into a system using any suitable hardware and/or software to configure as desired.

FIG. 5 schematically illustrates an example system (e.g., computing device 500) that may include an IC structure (e.g., IC structure 400 of FIGS. 4A-4F, and/or an IC structure formed using method 300) as described herein, in accordance with some embodiments. Components of the computing device 500 may be housed in an enclosure (e.g., housing 508). The motherboard 502 may include a number of components, including but not limited to a processor 504 and at least one communication chip 506. The processor 504 may be physically and electrically coupled to the motherboard 502. In some implementations, the at least one communication chip 506 may also be physically and electrically coupled to the motherboard 502. In further implementations, the communication chip 506 may be part of the processor 504.

Depending on its applications, computing device 500 may include other components that may or may not be physically and electrically coupled to the motherboard 502. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an

audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, a Geiger counter, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

5 The communication chip 506 may enable wireless communications for the transfer of data to and from the computing device 500. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The
10 term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 506 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-
15 2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., LTE-Advanced project, ultra mobile broadband (UMB) project (also referred to as “3GPP2”), etc.). IEEE 802.16 compatible broadband wireless access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for
20 Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 506 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile
Telecommunications System (UMTS), High Speed Packet Access (HSPA),
25 Evolved HSPA (E-HSPA), or LTE network. The communication chip 606 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 606 may operate in accordance with Code Division Multiple Access (CDMA), Time
30 Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 506 may operate in accordance with other wireless protocols in other embodiments.

The computing device 500 may include a plurality of communication chips 506. For instance, a first communication chip 506 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 506 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, and others.

The processor 504 of the computing device 500 may include a die (e.g., die 102 of FIGS. 1-2) having an IC structure (e.g., IC structure 400 of FIGS. 4A-4F, and/or an IC structure formed using method 300) as described herein. For example, the die 102 of FIGS. 1-2 may be mounted in a package assembly that is mounted on a circuit board such as the motherboard 502. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 506 may also include a die (e.g., die 102 of FIGS. 1-2) having an IC structure (e.g., IC structure 400 of FIGS. 4A-4F, and/or an IC structure formed using method 300) as described herein. In further implementations, another component (e.g., memory device or other integrated circuit device) housed within the computing device 500 may contain a die (e.g., die 102 of FIGS. 1-2) having an IC structure (e.g., IC structure 400 of FIGS. 4A-4F, and/or an IC structure formed using method 300) as described herein.

In various implementations, the computing device 500 may be a mobile computing device, a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 500 may be any other electronic device that processes data.

Some non-limiting Examples of various embodiments are provided below.

Example 1 is a method for fabricating an integrated circuit (IC) structure, comprising: providing a semiconductor substrate having a metal layer disposed on a portion of the semiconductor substrate and a dielectric film disposed on the metal layer and the semiconductor substrate; forming a photo-

patterned dielectric resist film on the dielectric film and providing an opening in the dielectric resist film over the metal layer; performing a first curing process on the dielectric resist film to remove a solvent from the dielectric resist film; removing, after performing the first curing process, a portion of the dielectric film that is disposed in the opening; and performing, after the removing, a second curing process on the dielectric resist film to polymerize the dielectric resist film.

Example 2 is the method of Example 1, further comprising forming the dielectric film on the metal layer and the semiconductor substrate in an unpatterned manner.

Example 3 is the method of Example 2, further comprising forming the metal layer on the portion of the semiconductor substrate.

Example 4 is the method of Example 1, wherein the first curing process includes subjecting the dielectric resist film to a first curing temperature, and wherein the second curing process includes subjecting the dielectric resist film to a second curing temperature that is higher than the first curing temperature.

Example 5 is the method of Example 4, wherein the first curing temperature is about 125 degrees Celsius to about 175 degrees Celsius, and the second curing temperature is about 225 degrees Celsius to about 275 degrees Celsius.

Example 6 is the method of Example 4, wherein the first curing process further includes subjecting the dielectric resist film to the first curing temperature for a first time period, wherein the second curing process further includes subjecting the dielectric resist film to the second curing temperature for a second time period, and wherein the second time period is longer than the first time period.

Example 7 is the method of any one of Examples 1 to 6, wherein the IC structure forms a transistor.

Example 8 is the method of any one of Examples 1 to 6, wherein the metal layer is a first metal layer, and wherein the method further comprises, after performing the second curing process, forming a second metal layer in the opening on the first metal layer.

Example 9 is the method of Example 8, wherein the second metal layer includes a different metal than a metal of the first metal layer.

Example 10 is the method of any one of Examples 1 to 6, wherein the forming the dielectric resist film on the dielectric film includes spinning the dielectric resist film on the dielectric film.

5 Example 11 is the method of any one of Examples 1 to 6, wherein the portion of the dielectric film that is disposed in the opening is removed by dry etch in an etch chamber.

Example 12 is the method of Example 11, wherein the first curing process is not performed in the etch chamber.

10 Example 13 is a method for fabricating an integrated circuit (IC) structure, comprising: providing a semiconductor substrate having a metal layer disposed on a portion of the semiconductor substrate and a dielectric film disposed on the metal layer and the semiconductor substrate; spinning a photo-patterned dielectric resist film on the dielectric film and providing an opening in the dielectric resist film over the metal layer, the spun dielectric resist film including a
15 resist material and a solvent; subjecting the dielectric resist film to a first curing temperature as part of a first curing process; removing, after the first curing process, a portion of the dielectric film that is disposed on the metal layer in the opening; and subjecting, after the removing, the dielectric resist film to a second curing temperature as part of a second curing process, wherein the second curing
20 temperature is higher than the first curing temperature.

Example 14 is the method of Example 13, further comprising forming the dielectric film on the metal layer and the semiconductor substrate in an unpatterned manner.

25 Example 15 is the method of Example 13, wherein the first curing temperature is about 125 degrees Celsius to about 175 degrees Celsius, and the second curing temperature is about 225 degrees Celsius to about 275 degrees Celsius.

30 Example 16 is the method of Example 13, wherein the first curing process further includes subjecting the dielectric resist film to the first curing temperature for a first time period, wherein the second curing process further includes subjecting the dielectric resist film to the second curing temperature for a second time period, and wherein the second time period is different than the first time period.

Example 17 is the method of Example 13, wherein the IC structure forms a transistor.

Example 18 is the method of Example 13, wherein the metal layer is a first metal layer, and wherein the method further comprises, after performing the
5 second curing process, forming a second metal layer in the opening on the first metal layer, wherein the second metal layer includes a different metal than a metal of the first metal layer.

Example 19 is the method of Example 13, wherein the portion of the dielectric film that is disposed in the opening is removed by dry etch in an etch
10 chamber, and wherein the first and second curing processes are not performed in the etch chamber.

Example 20 is the method of any one of Examples 13 to 20, wherein the first curing process removes the solvent from the dielectric resist film and the second curing process polymerizes the dielectric resist film.

15 Various embodiments may include any suitable combination of the above-described embodiments including alternative (or) embodiments of embodiments that are described in conjunctive form (and) above (e.g., the “and” may be “and/or”). Furthermore, some embodiments may include one or more articles of manufacture (e.g., non-transitory computer-readable media) having
20 instructions, stored thereon, that when executed result in actions of any of the above-described embodiments. Moreover, some embodiments may include apparatuses or systems having any suitable means for carrying out the various operations of the above-described embodiments.

The above description of illustrated implementations, including what
25 is described in the Abstract, is not intended to be exhaustive or to limit the embodiments of the present disclosure to the precise forms disclosed. While specific implementations and examples are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the present disclosure, as those skilled in the relevant art will recognize.

30 These modifications may be made to embodiments of the present disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit various embodiments of the present disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope is to be determined entirely by the following

claims, which are to be construed in accordance with established doctrines of claim interpretation.

Claims

What is claimed is:

1. A method for fabricating an integrated circuit (IC) structure, comprising:
providing a semiconductor substrate having a metal layer disposed on a
5 portion of the semiconductor substrate and a dielectric film disposed on the metal
layer and the semiconductor substrate;
forming a photo-patterned dielectric resist film on the dielectric film and
providing an opening in the dielectric resist film over the metal layer;
performing a first curing process on the dielectric resist film to remove a
10 solvent from the dielectric resist film;
removing, after performing the first curing process, a portion of the
dielectric film that is disposed in the opening; and
performing, after the removing, a second curing process on the dielectric
resist film to polymerize the dielectric resist film.
- 15 2. The method of claim 1, further comprising forming the dielectric film on the
metal layer and the semiconductor substrate in an unpatterned manner.
3. The method of claim 2, further comprising forming the metal layer on the
portion of the semiconductor substrate.
4. The method of claim 1, wherein the first curing process includes subjecting
20 the dielectric resist film to a first curing temperature, and wherein the second
curing process includes subjecting the dielectric resist film to a second curing
temperature that is higher than the first curing temperature.
5. The method of claim 4, wherein the first curing temperature is about 125
degrees Celsius to about 175 degrees Celsius, and the second curing
25 temperature is about 225 degrees Celsius to about 275 degrees Celsius.
6. The method of claim 4, wherein the first curing process further includes
subjecting the dielectric resist film to the first curing temperature for a first time
period, wherein the second curing process further includes subjecting the
dielectric resist film to the second curing temperature for a second time period,
30 and wherein the second time period is longer than the first time period.
7. The method of any one of claims 1 to 6, wherein the IC structure forms a
transistor.

8. The method of any one of claims 1 to 6, wherein the metal layer is a first metal layer, and wherein the method further comprises, after performing the second curing process, forming a second metal layer in the opening on the first metal layer.
- 5 9. The method of claim 8, wherein the second metal layer includes a different metal than a metal of the first metal layer.
10. The method of any one of claims 1 to 6, wherein the forming the dielectric resist film on the dielectric film includes spinning the dielectric resist film on the dielectric film.
- 10 11. The method of any one of claims 1 to 6, wherein the portion of the dielectric film that is disposed in the opening is removed by dry etch in an etch chamber.
12. The method of claim 11, wherein the first curing process is not performed in the etch chamber.
13. A method for fabricating an integrated circuit (IC) structure, comprising:
- 15 providing a semiconductor substrate having a metal layer disposed on a portion of the semiconductor substrate and a dielectric film disposed on the metal layer and the semiconductor substrate;
- spinning a photo-patterned dielectric resist film on the dielectric film and providing an opening in the dielectric resist film over the metal layer, the spun
- 20 dielectric resist film including a resist material and a solvent;
- subjecting the dielectric resist film to a first curing temperature as part of a first curing process;
- removing, after the first curing process, a portion of the dielectric film that is disposed on the metal layer in the opening; and
- 25 subjecting, after the removing, the dielectric resist film to a second curing temperature as part of a second curing process, wherein the second curing temperature is higher than the first curing temperature.
14. The method of claim 13, further comprising forming the dielectric film on the metal layer and the semiconductor substrate in an unpatterned manner.

15. The method of claim 13, wherein the first curing temperature is about 125 degrees Celsius to about 175 degrees Celsius, and the second curing temperature is about 225 degrees Celsius to about 275 degrees Celsius.

5 16. The method of claim 13, wherein the first curing process further includes subjecting the dielectric resist film to the first curing temperature for a first time period, wherein the second curing process further includes subjecting the dielectric resist film to the second curing temperature for a second time period, and wherein the second time period is different than the first time period.

17. The method of claim 13, wherein the IC structure forms a transistor.

10 18. The method of claim 13, wherein the metal layer is a first metal layer, and wherein the method further comprises, after performing the second curing process, forming a second metal layer in the opening on the first metal layer, wherein the second metal layer includes a different metal than a metal of the first metal layer.

15 19. The method of claim 13, wherein the portion of the dielectric film that is disposed in the opening is removed by dry etch in an etch chamber, and wherein the first and second curing processes are not performed in the etch chamber.

20 20. The method of any one of claims 13 to 20, wherein the first curing process removes the solvent from the dielectric resist film and the second curing process polymerizes the dielectric resist film.

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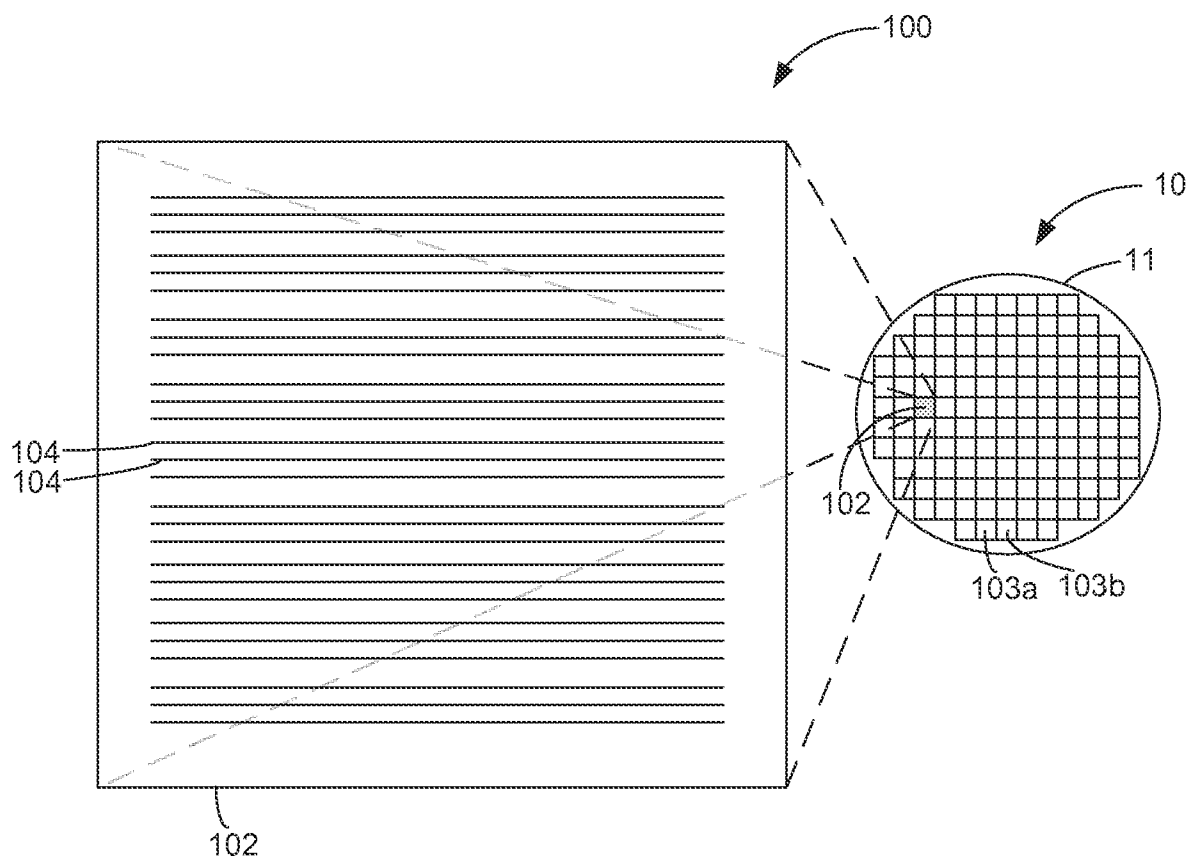


FIG. 1

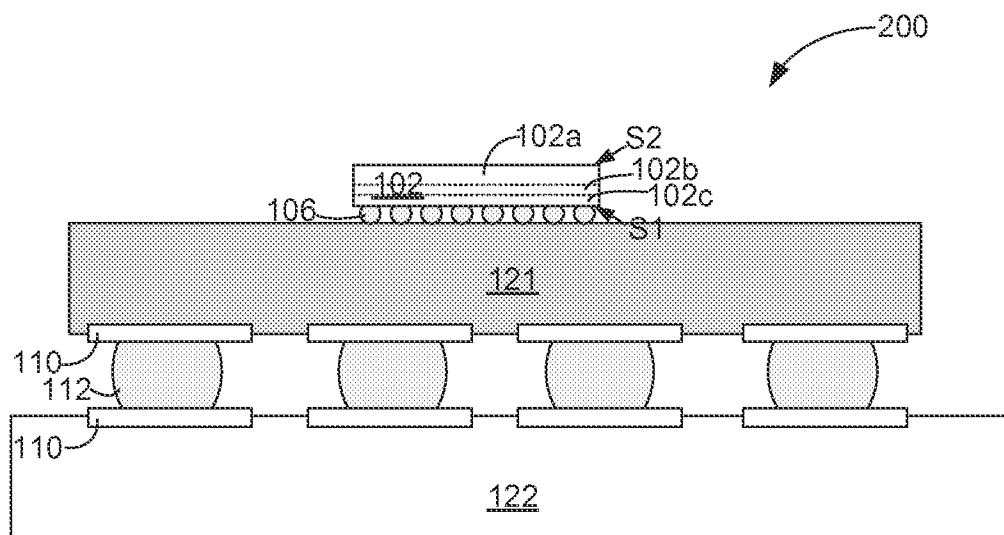


FIG. 2

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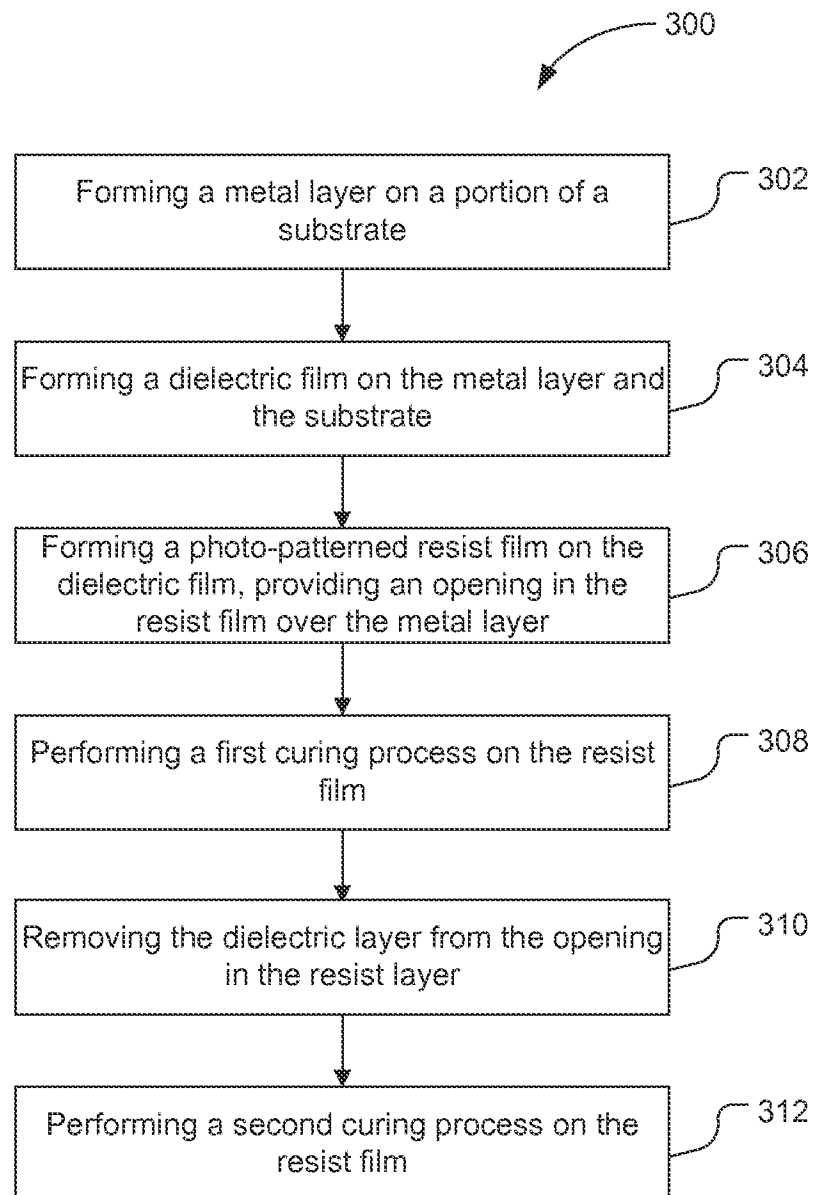


FIG. 3

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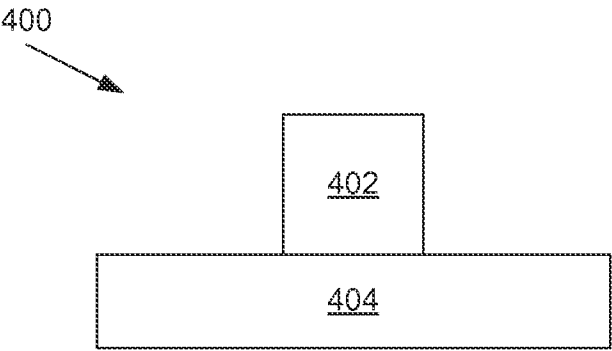


FIG. 4A

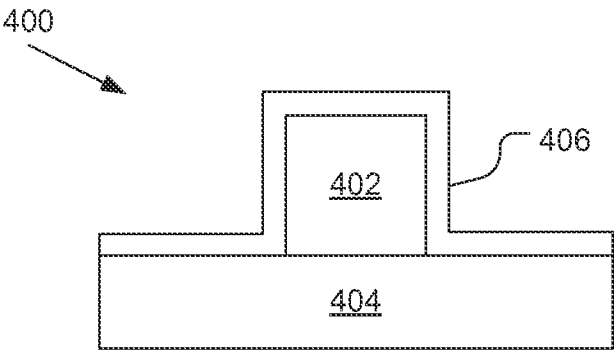


FIG. 4B

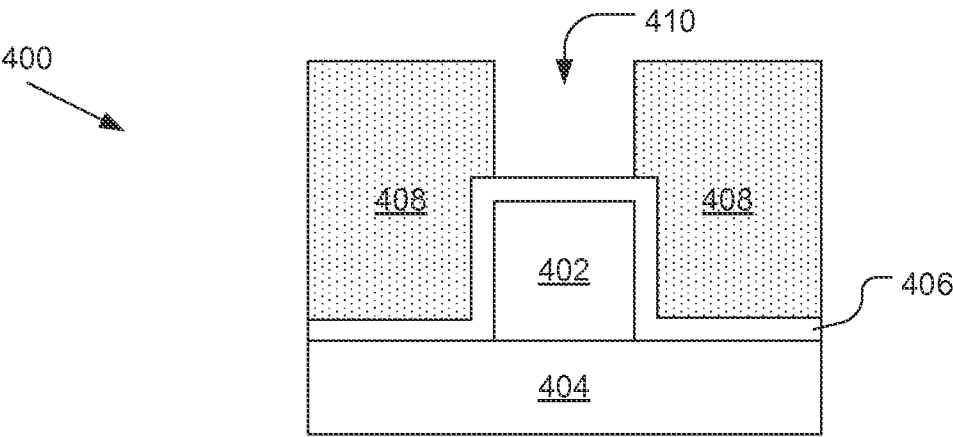


FIG. 4C

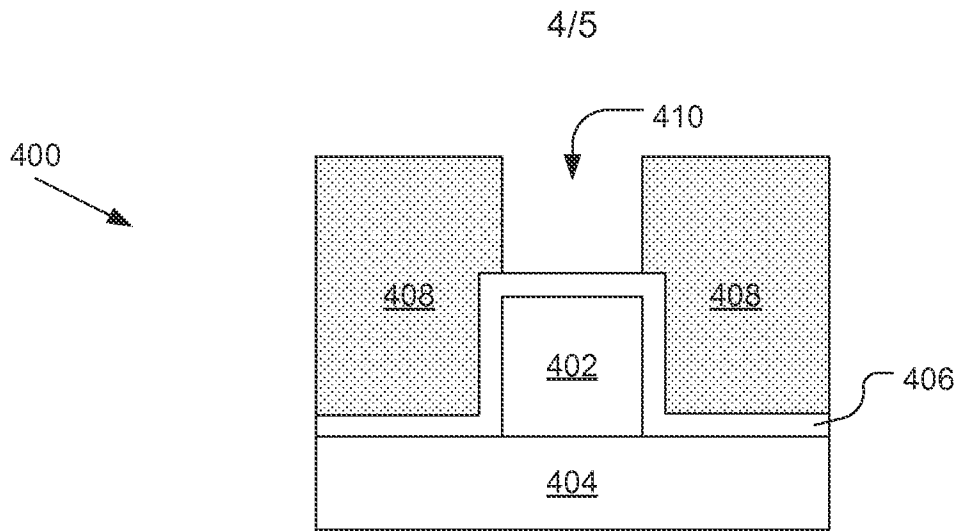


FIG. 4D

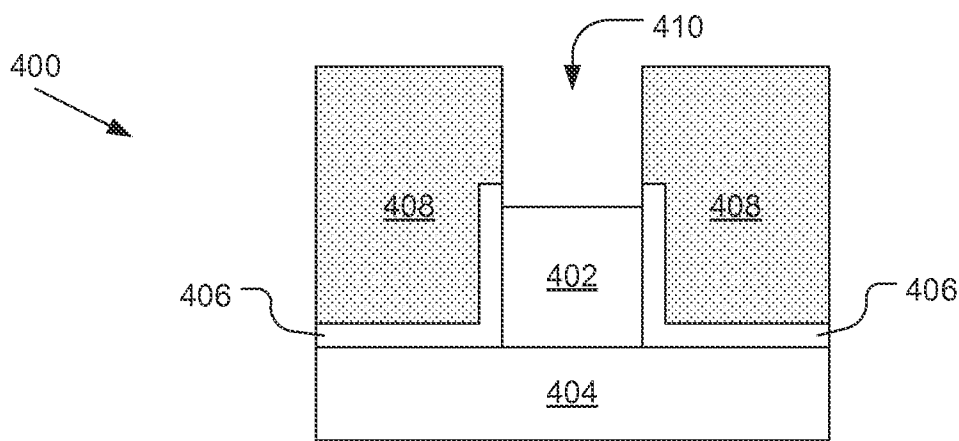


FIG. 4E

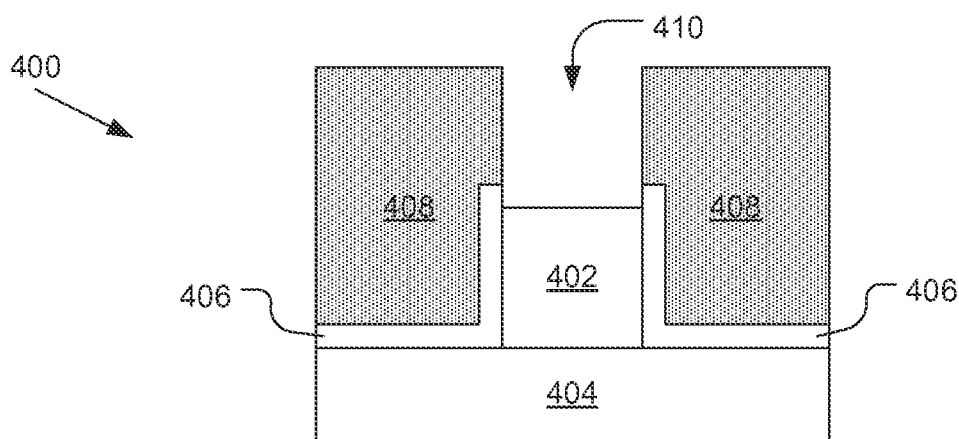


FIG. 4F

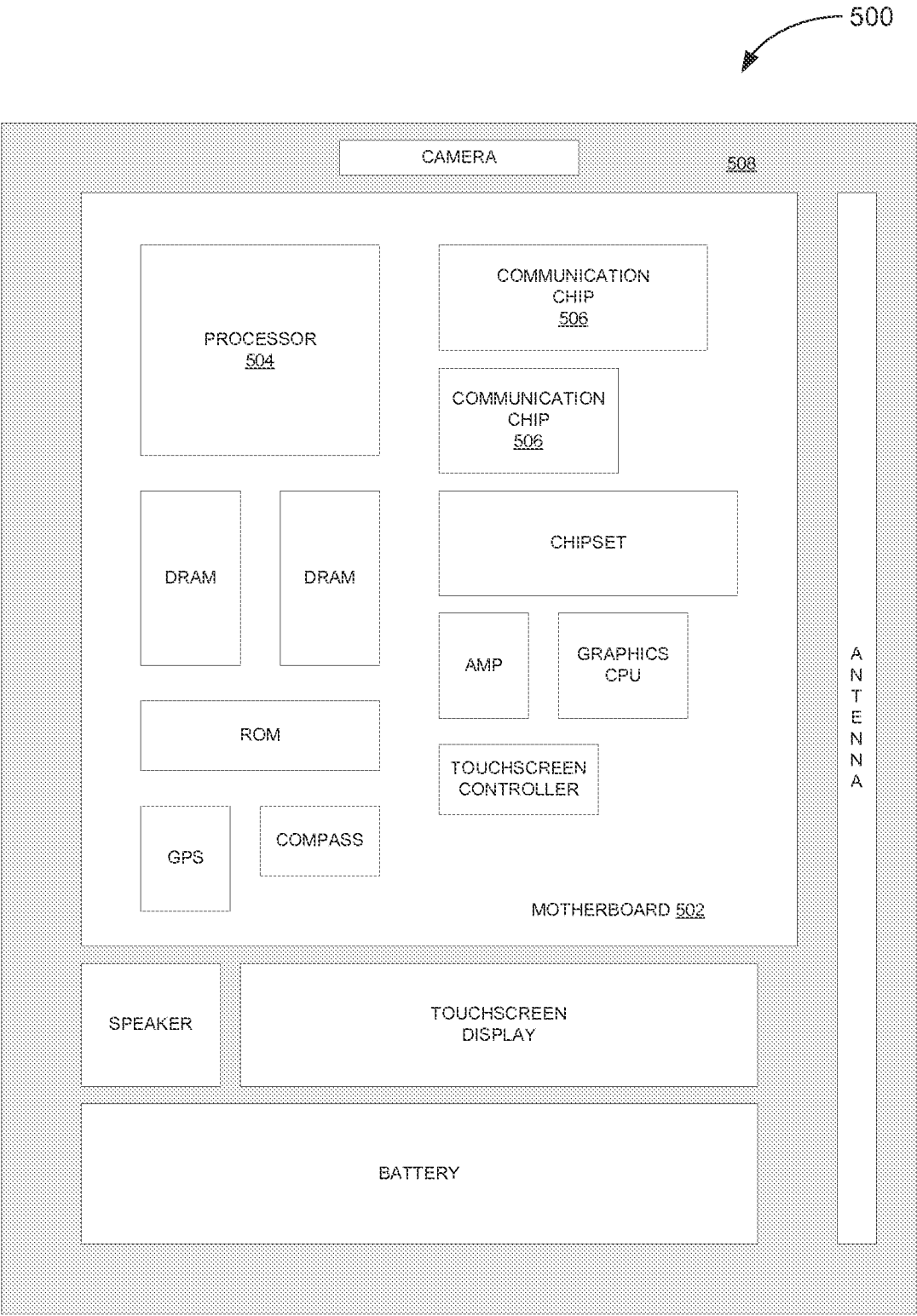


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/048324**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/027(2006.01)i, H01L 21/28(2006.01)i, H01L 21/31(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/027; H01L 23/52; H01L 23/535; H01L 21/768; H01L 21/4763; G03F 7/004; H01L 21/02; B32B 9/04; H01L 29/24; H01L 21/28; H01L 21/31

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: integrated circuit, dielectric layer, resist, curing, polymerizing

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007-0281471 A1 (DROR HURWITZ et al.) 06 December 2007 See abstract, paragraphs [0238]-[0247], claims 1-4 and figure 6.	1-20
A	US 2009-0072401 A1 (JOHN C. ARNOLD et al.) 19 March 2009 See paragraphs [0101]-[0114], claim 7 and figures 2A-2F.	1-20
A	US 2012-0032336 A1 (QINGHUANG LIN) 09 February 2012 See paragraphs [0129]-[0137], claims 1, 13, 16 and figures 5, 6.	1-20
A	US 2012-0119202 A1 (DOUGLAS A. KESZLER et al.) 17 May 2012 See paragraphs [0119]-[0122], claims 25-28 and figure 10.	1-20
A	US 2015-0200133 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 16 July 2015 See paragraphs [0008]-[0015], claim 1 and figure 1A. (** NOTE: As claim 20 refers to itself, this International Search Report has been established on the assumption that claim 20 refers to any one of claims 13-19.)	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

30 May 2016 (30.05.2016)

Date of mailing of the international search report

30 May 2016 (30.05.2016)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

CHOI, Sang Won

Telephone No. +82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/048324

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