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(54) **Title**: SYSTEM AND METHOD FOR FORMING A BURIED LOWER ELECTRODE IN CONJUNCTION WITH AN ENCAPSULATED MEMS DEVICE

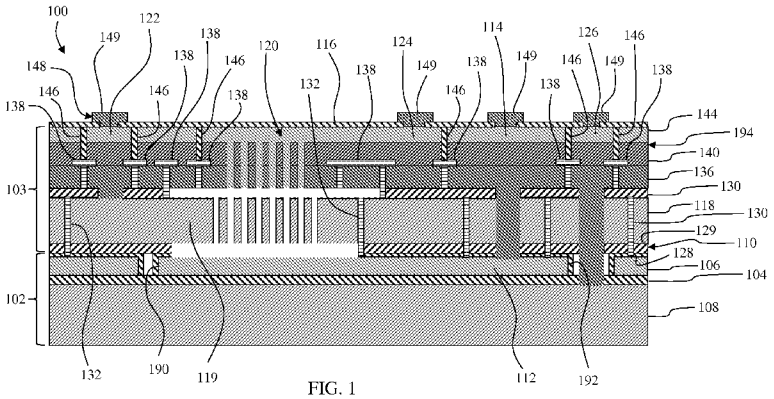

FIG. 1

(57) **Abstract**: A system and method for forming a sensor device with a buried first electrode includes providing a first silicon portion with an electrode layer and a second silicon portion with a device layer. The first silicon portion and the second silicon portion are adjoined along a common oxide layer formed on the electrode layer of the first silicon portion and the device layer of the second silicon portion. The resulting multi-silicon stack includes a buried lower electrode that is further defined by a buried oxide layer, a highly-doped ion implanted region, or a combination thereof. The multi-silicon stack has a plurality of silicon layers and silicon dioxide layers with electrically isolated regions in each layer allowing for both the lower electrode and an upper electrode. The multi-silicon stack further includes a spacer that enables the lower electrode to be accessible from a topside of the sensor device.

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SYSTEM AND METHOD FOR FORMING A BURIED LOWER ELECTRODE IN CONJUNCTION WITH AN ENCAPSULATED MEMS DEVICE

This application claims the benefit of U.S. Provisional Application No. 61/691,662, filed August 21, 2012.

Field of the Invention

[0001] The present disclosure relates to capacitive micro electrical mechanical system (MEMS) devices.

Background

[0002] For many capacitive MEMS devices, the use of electrodes above and below the device structure is either required for the basic operation of the device or greatly enhances the performance of the device. One or more of the electrodes are typically formed by deposition of a conductive film, electrical isolation of a conductive layer, or by simply adding a spacer layer between two conductive materials.

[0003] The electrode configuration of such a capacitive MEMS device allows for closed-loop operation in which the device is held fixed in place by electrostatic forces or for differential sensing of an open-loop measurement of the device. Many encapsulation methods used to produce capacitive MEMS devices, however, either do not allow for an arbitrary placement of one or both of the upper and lower electrodes or do not allow for any such out-of-plane electrodes.

Summary

[0004] In accordance with one embodiment, a method of forming a MEMS device includes defining a first electrode in a silicon on insulator (SOI) wafer, forming a second electrode in a first layer located above an upper surface of the SOI wafer, forming a third electrode in a second layer located above an upper surface of the first layer, forming a first contact above the second layer in electrical communication with the first electrode through the second layer and the first layer, forming a second contact above the second layer in electrical communication with the second electrode through the second layer, and defining a third contact above the second layer in electrical communication with the third.

[0005] In another embodiment, a MEMS device includes a first electrode in a silicon on insulator (SOI) wafer, a second electrode in a first layer located above an upper surface of the SOI wafer, a third electrode in a second layer located above an upper surface of the first layer, a first contact above the second layer in electrical communication with the first electrode through the second layer and the first layer, a second contact above the second layer in electrical communication with the second electrode through the second layer, and a third contact above the second layer in electrical communication with the third electrode.

Brief Description of the Drawings

[0006] FIG. 1 depicts a side cross-sectional view of a sensor device incorporating a plurality of electrodes electrically connected to a top side of the sensor device via respective corresponding contacts;

[0007] FIG. 2 depicts a process for forming the sensor device of FIG. 1;

[0008] FIG. 3 depicts a side cross-sectional view of a silicon on insulator (SOI) wafer provided in accordance with the process of FIG. 2;

[0009] FIG. 4 depicts a side cross-sectional view of a second SOI wafer provided in accordance with the process of FIG. 2;

[0010] FIG. 5 depicts a side cross-sectional view of the SOI wafer and the second SOI wafer bonded together along respective oxide layers with a first electrode buried therebetween;

[0011] FIG. 6 depicts a side cross-sectional view of the wafer configuration of FIG. 5 with a first layer of the second SOI wafer having trenches etched and refilled with dielectric material;

[0012] FIG. 7 depicts a side cross-sectional view of the wafer configuration of FIG. 6 showing the first layer after being patterned and covered with an oxide layer and after having the oxide layer patterned to form portions of the contacts;

[0013] FIG. 8 depicts a side cross-sectional view of the wafer configuration of FIG. 7 after a trenching operation with an additional photomask exposes the first electrode and a substrate layer of the SOI wafer;

[0014] FIG. 9 depicts a side cross-sectional view of the wafer configuration of FIG. 8 with a first epitaxial portion of a second layer having trenches etched and refilled with dielectric material;

[0015] FIG. 10 depicts a side cross-sectional view of the wafer configuration of FIG. 9 with the first epitaxial portion and a second epitaxial portion of the second layer having trenches etched to expose buried oxide layers;

[0016] FIG. 11 depicts a side cross-sectional view of another embodiment of the sensor device of FIG. 1 with the first electrode further defined by a first highly-doped ion implanted region in the silicon layer;

[0017] FIG. 12 depicts a side cross-sectional view of a sensor device incorporating a first electrode defined by a highly-doped ion implanted region in a silicon layer of silicon wafer; and

[0018] FIG. 13 depicts a side cross-sectional view of a sensor device incorporating a first electrode defined by stacking a first highly-doped ion implanted region and a second highly-doped ion implanted region in a silicon layer of a silicon wafer.

Description

[0019] For the purpose of promoting an understanding of the principles of the disclosure, reference will now be made to the embodiments illustrated in the drawings and described in the following written specification. It is understood that no limitation to the scope of the disclosure is thereby intended. It is further understood that the disclosure includes any alterations and modifications to the illustrated embodiments and includes further applications of the principles of the disclosure as would normally occur to one skilled in the art to which this disclosure pertains.

[0020] In many of these embodiments, a MEMS sensor may be used to sense a physical condition such as acceleration, pressure, or temperature, and to provide an electrical signal representative of the sensed physical condition. The embodiments may be implemented in or associated with a variety of applications such as automotives, home appliances, laptops, handheld or portable computers, mobile telephones, smart phones, wireless devices, tablets, personal data assistants (PDAs), MP3 players, camera, GPS receivers or navigation systems, electronic reading displays, projectors, cockpit controls, game consoles, earpieces, headsets, hearing aids, wearable display devices, security systems, and etc.

[0021] FIG. 1 depicts a sensor device 100 that includes a first silicon portion 102 and a second silicon portion 103 that is adjacent to the first silicon portion 102. A first buried oxide layer 104 is positioned within the first silicon portion 102 to separate the first silicon portion 102 into a silicon layer 106 and a substrate layer 108. A first oxide layer 110 is positioned between the silicon layer 106 and the second silicon portion 103 to define a first electrode 112.

[0022] The positioning of the first buried oxide layer 104 and the first oxide layer 110 electrically isolates the first electrode 112 from the first silicon portion 102 and enables electrical isolation of the first electrode 112 from portions of the second silicon portion 103. A vertical electrical interconnect or first contact 114 is used to provide electrically isolated access to the first electrode 112 from a topside 116 of the sensor 100.

[0023] The second silicon portion 103 includes a first layer 118 with a second electrode 119 defined therein and a second layer 194 with a third electrode 120 defined therein. In the embodiment shown, the first layer 118 includes a functional device that

has a deformable portion configured to move or deform relative to the electrodes in response to an applied force. A second contact 122, a third contact 124, and a fourth contact 126 are incorporated within the second silicon portion 103 to provide electrically isolated access to the second electrode 119, the third electrode 120, and the substrate layer 108, respectively, from the topside 116 of the sensor 100.

[0024] A process 150 for forming a substrate configuration that is used in a sensor, such as the sensor device 100, is discussed with reference to FIG. 2. Initially, a first silicon portion 102 is provided for further processing (block 152). In one embodiment, the first silicon portion 102 is a wafer that is processed to form a silicon layer 106 and a substrate layer 108 that are electrically isolated from one another. In this embodiment, a first buried oxide layer 104 is formed on a surface of the first silicon portion 102 (block 154). The first buried oxide layer 104 can be a top layer of silicon dioxide that is grown by the technique of thermal oxidation, in which the first silicon portion 102 is exposed to oxygen and/or steam.

[0025] A layer of silicon is deposited on the first buried oxide layer 104 of the first silicon portion 102 to form a silicon layer 106, which is then patterned to define a first electrode 112 (block 156). The silicon layer 106 is deposited by chemical vapor deposition (CVD) or, more particularly, low pressure chemical vapor deposition (LPCVD), it can also be deposited via epitaxial layer growth or using a silicon wafer-bond with a back-grind process. In one embodiment, the silicon layer 106 is deposited to a thickness of approximately 0.1 to 3 μm. The patterning of the silicon layer 106 forms a first first electrode trench 190 and a second first electrode trench 192 that bound the first

electrode 112. The silicon layer 106 can be patterned by any process that enables the transfer of a pattern into a material.

[0026] A first portion 128 of a first oxide layer 110 is formed on the deposited and patterned silicon layer 106 to provide appropriate electrical isolation of the first electrode 112 in accordance with the principles of the disclosure (block 158). The first portion 128 of the first oxide layer 110 can be grown by thermal oxidation or deposited by a known deposition process. Optionally, the first portion 128 of the first oxide layer 110 can be smoothed using a polishing process, such as chemical mechanical polishing/planarization (CMP).

[0027] In one embodiment, the first silicon portion 102 is a silicon-on-insulator (SOI) wafer, which is provided with a silicon layer 106 and a substrate layer 108 already separated by a buried oxide layer. In this embodiment, the silicon layer 106 is patterned and the first portion 128 of the first oxide layer 110 is formed on the silicon layer 106 to provide appropriate electrical isolation of the first electrode 112.

[0028] Additionally, a second silicon portion 103 is provided for further processing (block 160). The second silicon portion 103 can be provided as a blank wafer or as a SOI wafer. In at least one embodiment, the second silicon portion 103 has a first layer 118 with a thickness of approximately 10 to 40 μm. The second silicon portion 103 is processed by forming a second portion 129 of the first oxide layer 110 on the first layer 118 and patterning the second portion 129 of the first oxide layer 110 (block 162). Similar to the buried oxide layer 104 and the first portion 128 of the first oxide layer 110, the second portion 129 of the first oxide layer 110 can be a silicon dioxide layer grown by thermal oxidation.

[0029] A multi-silicon stack is formed by wafer bonding the first and second silicon portions 102, 103 to one another at the first and second portions 128, 129 of the first oxide layer 110 (block 164). Prior to wafer bonding, the first and second silicon portions 102, 103 are positioned relative to one another such that at least some of the patterning of the first silicon portion 102 aligns with the patterning of the second silicon portion 103 when the first and second portions 128, 129 of the first oxide layer 110 are adjacent. This positioning enables the formation of a first contact 114 and a fourth contact 126, which connect the first electrode 112 and the substrate layer 108, respectively, to a topside 116 of the sensor 100. The wafer bonding of the first and second silicon portions 102, 103 can be accomplished by any wafer bonding technique. The surface of the second silicon portion 103 opposite the bonded region can be back-ground to produce a desired thickness of the first layer 118 or of the sensor device 100.

[0030] In at least one embodiment, starting from the processed first silicon portion 102 at block 158, a polysilicon layer can be grown from the first silicon portion 102 to achieve the same substrate configuration produced at block 164. This embodiment, however, does not allow for a top layer of the final substrate configuration to be of single crystal silicon.

[0031] First trenches 132 are etched into the first layer 118 and the first and second portions 128, 129 of the first oxide layer 110. The first trenches 132 are then refilled with a dielectric material, such as silicon nitride, to provide electrical isolation between selected portions of the first layer 118 (block 166), and to provide a lateral etch-stop during the oxide release etching. The trenches can be etched and refilled by any desired process. In some embodiments, the trenches are etched and refilled using methods

generally described in U.S. Patent Application Nos. 13/232,005 and 13/767,594, the entire contents of which are herein incorporated by reference.

[0032] At block 168, the first layer 118 is patterned, a second oxide layer 130 is formed on the patterned first layer 118, and the second oxide layer 130 is patterned (block 168). The patterning of the first layer 118 and the forming of the second oxide layer 130 are conformal in one embodiment. In another embodiment, the patterning of the first layer 118 and the forming of the second oxide layer 130 are non-conformal. The patterning of the second oxide layer 130 is used in the formation of the first contact 114, the fourth contact 126, and a second contact 122, which connect the first electrode 112, the substrate layer 108, and the first layer 118, respectively, to the topside 116 of the sensor 100. After the second oxide layer 130 is patterned (block 168), selected portions of the first layer 118 are etched with an additional photomask to form second trenches 134 (FIG. 8) that extend into the first electrode 112 and the substrate layer 108 (block 170).

[0033] A first epitaxial portion 136 of the second layer 194 is formed that covers the exposed first layer 118 and the second oxide layer 130 and fills the second trenches 134 formed at block 170 (block 172). In one embodiment, the first epitaxial portion 136 is polished by using the CMP process. Also at block 172, third trenches 138 are etched into the first epitaxial portion 136 and, in some cases, into the second oxide layer 130. The third trenches 138 are subsequently refilled with a dielectric material, such as silicon nitride, which is then patterned.

[0034] A second epitaxial portion 140 of the second layer 194 is formed over both the first epitaxial portion 136 and the patterned dielectric material adjacent to the first epitaxial portion 136 (block 174). The second epitaxial portion 140 is smoothed

using a polishing process, such as CMP. Vent holes 142 are etched into the first and second epitaxial portions 136, 140 to expose the second oxide layer 130 (block 176). Selected portions of the first and second oxide layers 110, 130 are then release etched at block 176 using a vapor phase hydrofluoric acid (HF) process.

[0035] A third epitaxial portion 144 of the second layer 194 is formed over the second epitaxial portion 140 to seal the resulting substrate configuration (block 178). The third epitaxial portion 144 is smoothed using a polishing process, such as CMP. Fourth trenches 146 are etched into the second and third epitaxial portions 140, 144 and intersect with selected third trenches 138, which have been previously refilled with dielectric material (block 180). The fourth trenches 146 are refilled with dielectric material, such as silicon nitride, and then patterned. A metal layer 148 is deposited over both the patterned dielectric material adjacent to the third epitaxial portion 144 and the exposed portions of the third epitaxial portion 144 (block 182). The metal layer 148 is then patterned to form electrically isolated metal contacts 149 operatively associated with the second contact 122, the third contact 124, the first contact 114, and the fourth contact 126.

[0036] As shown in FIG. 1, the third electrode 120 is electrically isolated from other conductive elements encapsulated within the sensor 100, and the third contact 124 provides access to the third electrode 120 from the topside 116 of the sensor 100. Moreover, the substrate layer 108, the first electrode, and the first layer 118 are electrically isolated from the third electrode 120 and from one another and are accessible from the topside 116 of the sensor via the fourth contact 126, the first contact 114, and the second contact, respectively

[0037] The process 150 is further illustrated by reference to FIG. 1 and FIGS. 3-10. Referring initially to FIG. 3, a first silicon portion 102 is provided and processed according to blocks 152-158 to define a first electrode 112. Referring to FIG. 4, a second silicon portion 103 is provided and processed according blocks 160-162.

[0038] FIG. 5 depicts the first and second silicon portions 102, 103 after being wafer bonded to one another to encapsulate the first electrode 112 (block 164). FIG. 6 depicts the multi-silicon stack after first trenches 132 have been etched into the first layer 118 and then refilled with a dielectric material (block 166). FIG. 7 depicts the multi-silicon stack after the first layer 118 is patterned, a second oxide layer 130 is formed on the patterned first layer 118, and the second oxide layer 130 is patterned (block 168).

[0039] FIG. 8 depicts the multi-silicon stack after selected portions of first layer 118 are etched with an additional photomask to form second trenches 134. The second trenches 134 are formed with enough depth to extend into the first electrode 112 and the substrate layer 108 (block 170). FIG. 9 depicts the first epitaxial portion 136 of the second layer 194 of silicon that is formed on both the exposed first layer 118 and the second oxide layer 130 and that fills the second trenches 134 (block 172). Third trenches 138 are etched into the first epitaxial portion 136 and then refilled with a dielectric material, which is subsequently patterned.

[0040] FIG. 10 depicts the second epitaxial portion 140 of the second layer 194 that is formed over both the first epitaxial portion 136 and the patterned dielectric material adjacent to the first epitaxial portion 136 (block 174). FIG. 10 also depicts the vent holes 142 that are etched into the first and second epitaxial portions 136, 140 to

expose the second oxide layer 130 (block 176). As shown in FIG. 10, the vent holes 142 are used to release etch selected portions of the first and second oxide layers 110, 130.

[0041] FIG. 1 depicts the third epitaxial portion 144 of the second layer 194 that is formed over the second epitaxial portion 140 to seal the resulting substrate configuration. FIG. 1 also depicts the fourth trenches 146 that are etched into the second and third epitaxial portions 140, 144 after the fourth trenches 146 have been refilled with dielectric material and patterned.

[0042] The process 150 results in the sensor device 100 as illustrated in FIG. 1. The sensor device 100 has a plurality of electrically isolated vertical interconnects or contacts that provide wafer topside access to electrical elements buried within the configuration, such as the first electrode 112, the substrate layer 108, and the first layer 118. As shown in FIG. 1, the third electrode 120 is electrically isolated from other conductive elements encapsulated within the sensor 100, and the third contact 124 provides access to the third electrode 120 from the topside 116 of the sensor 100. Moreover, the substrate layer 108, the first electrode, and the first layer 118 are electrically isolated from the third electrode 120 and from one another and are accessible from the topside 116 of the sensor via the fourth contact 126, the first contact 114, and the second contact, respectively.

[0043] FIGS. 11-13 illustrate other embodiments of a first electrode encapsulated within a sensor in accordance with principles of the disclosure. FIG. 11 depicts a sensor 200 that includes a first electrode 202 defined after implementing a doping process. The substrate configuration of this embodiment is similar to the substrate configuration of the sensor 100 of FIG. 1 except that a doping process is used to define the first electrode 202

during the processing of the first silicon portion 102. In this embodiment, only a single doping is needed to define the first electrode 202 because the substrate layer 108 of the first silicon portion 102 is electrically isolated from the first electrode 202 via the first buried oxide layer 104.

[0044] FIG. 12 depicts a sensor 210 that includes a first electrode 212 defined after applying different doping processes to the first silicon portion 102 and the first electrode 212. In this embodiment, an buried oxide layer is not provided in the first silicon portion 102. As such, different doping of the first electrode 212 and the first silicon portion 102 provides electrical isolation between the first electrode 212 and the first silicon portion 102. In at least one embodiment, the first silicon portion 102 is P+ doped, although other doping can be used if desired. The first electrode 212 is an N+ region of the first silicon portion 102.

[0045] FIG. 13 depicts a sensor 220 that includes a first electrode 222 defined by implementing a stacked doping process. The substrate configuration of this embodiment is similar to the substrate configuration of FIG. 12 except that the first silicon portion 102 is P-type doped, a first region 224 of the first silicon portion 102 is N- doped, and a second region of the first silicon portion 102, which defines the first electrode 222, is P+ doped. The stacked doping of this substrate configuration provides electrical isolation between the first electrode 222 and the first silicon portion 102.

[0046] While the disclosure has been illustrated and described in detail in the drawings and foregoing description, the same should be considered as illustrative and not restrictive in character. It is understood that only the preferred embodiments have been

presented and that all changes, modifications and further applications that come within the spirit of the disclosure are desired to be protected.

Claims

Claim 1. A method of forming a MEMS device comprising:

defining a first electrode in a silicon on insulator (SOI) wafer;

forming a second electrode in a first layer, the first layer located above an upper surface of the SOI wafer;

forming a third electrode in a second layer, the second layer located above an upper surface of the first layer;

forming a first contact above the second layer in electrical communication with the first electrode through the second layer and the first layer;

forming a second contact above the second layer in electrical communication with the second electrode through the second layer; and

defining a third contact above the second layer in electrical communication with the third electrode.

Claim 2. The method of claim 1, wherein the first layer is provided on a second SOI wafer, the method further comprising:

providing a first portion of a first oxide layer over the first electrode;

providing a second portion of the first oxide layer over the first layer; and

connecting the SOI wafer and the second SOI wafer at the respective first and second portions of the first oxide layer to electrically isolate the first electrode and the second electrode.

Claim 3. The method of claim 1, wherein the first electrode is defined in a silicon layer of the SOI wafer, the method further comprising:

doping a first region of the silicon layer with a first dopant type to form a first doped region, the first doped region defining the first electrode.

Claim 4. The method of claim 1, wherein the first electrode is defined in a silicon layer of a silicon wafer that is not an SOI wafer, the method further comprising:

doping a first region of the silicon layer with a first dopant type to form a first doped region, the first doped region defining the first electrode; and

doping a second region of the silicon layer with a second dopant type to form a second doped region, the first doped region being a N+ type doped region and the second doped region being a P+ type doped region, the first doped region and the second doped region defining the first electrode.

Claim 5. The method of claim 1, wherein the first electrode is defined in a silicon layer of a silicon wafer that is not an SOI wafer, the method further comprising:

doping a first region of the silicon layer with a first dopant type to form a first doped region, the first doped region defining the first electrode;

doping a second region of the silicon layer with a second dopant type to form a second doped region; and

doping a third region of the silicon layer with a third dopant type to form a third doped region, the third doped region positioned between the first doped region and the second doped region, the first doped region being a P+ type doped region, the second doped region being a P type doped region, and the third doped region being a N- well type doped region, the first doped region, the second doped region, and the third doped region defining the first electrode.

Claim 6. The method of claim 1, wherein the SOI wafer includes a buried oxide layer, the method further comprising:

providing a first oxide layer on an upper surface of the first electrode;

forming a functional device within the first layer;

providing a second oxide layer on an upper surface of the first layer;

patterning a first portion of the first oxide layer and the second oxide layer to form a first portion of the first contact;

patterning a second portion of the first oxide layer and the second oxide layer and a portion of the buried oxide layer to form a first portion of a fourth contact, the fourth contact in electrical communication with a substrate layer located below the buried oxide layer;

etching first trenches in the first layer and the first oxide layer; and

filling the etched first trenches with a dielectric material to electrically isolate the first portion of the first contact and the first portion of the fourth contact within the first layer.

Claim 7. The method of claim 6, further comprising:

etching second trenches in the first layer within the first portion of the first contact and within the first portion of the fourth contact;

forming a first epitaxial portion of the second layer on the second oxide layer and within the second trenches;

etching third trenches through the first epitaxial portion of the second layer to form a second portion of the first contact, a second portion of the fourth contact, and a first portion of the second contact; and

filling the etched third trenches with the dielectric material to electrical isolate the second portion of the first contact, the second portion of the fourth contact, and the first portion of the second contact within the second layer.

Claim 8. The method of claim 7, further comprising:

forming a second epitaxial portion of the second layer on the first epitaxial portion;

releasing the functional device through vent holes formed in the second epitaxial portion and the first epitaxial portion; and

forming a third epitaxial portion of the second layer on the second epitaxial portion.

Claim 9. The method of claim 8, further comprising:

etching fourth trenches in the third epitaxial portion and the second epitaxial portion and stopping at selected ones of the etched and filled third trenches, the etched fourth trenches forming a third portion of the first contact, a third portion of the fourth contact, a second portion of the second contact, and a first portion of the third contact; and

filling the etched fourth trenches with the dielectric material to electrically isolate the third portion of the first contact, the third portion of the fourth contact, the second portion of the second contact, and the first portion of the third contact within the second layer.

Claim 10. The method of claim 9, further comprising:

forming a passive layer on the third epitaxial portion of the second layer;

patterning portions of the passive layer to expose portions of the third epitaxial portion corresponding to the third portion of the first contact, the third portion of the fourth contact, the second portion of the second contact, and the first portion of the third contact;

forming a metal layer on the patterned passive layer; and

patterning the metal layer to electrically isolate the first contact, the second contact, the third contact, and the fourth contact above the second layer.

Claim 11. The method of claim 8, wherein the first epitaxial portion, the second epitaxial portion, and the third epitaxial portion are deposited by an epitaxial deposition process.

Claim 12. The method of claim 6, wherein the dielectric material includes at least one of silicon dioxide, silicon nitride, and ALD alumina.

Claim 13. A MEMS device, comprising:

a first electrode in a silicon on insulator (SOI) wafer;

a second electrode in a first layer located above an upper surface of the SOI wafer;

a third electrode in a second layer located above an upper surface of the first layer;

a first contact above the second layer in electrical communication with the first electrode through the second layer and the first layer;

a second contact above the second layer in electrical communication with the second electrode through the second layer; and

a third contact above the second layer in electrical communication with the third electrode.

Claim 14. The device of claim 13, wherein the first electrode is defined in a first doped region of the SOI wafer, the first doped region including a first dopant type.

Claim 15. The device of claim 13, wherein the first electrode is defined in a silicon layer of a silicon wafer that is not an SOI wafer, the silicon layer including:

a doped first region of a first dopant type; and

a doped second region of a second dopant type, the first doped region being a N+ type doped region and the second doped region being a P+ type doped region, the first doped region and the second doped region defining the first electrode.

Claim 16. The device of claim 13, wherein the first electrode is defined in a silicon layer of a silicon wafer that is not an SOI wafer, the silicon layer including:

a doped first region of a first dopant type;

a doped second region of a second dopant type; and

a doped third region of a third dopant type, the third doped region positioned between the first doped region and the second doped region, the first doped region being a P+ type doped region, the second doped region being a P type doped region, and the third doped region being a N- well type doped region, the first doped region, the second doped region, and the third doped region defining the first electrode.

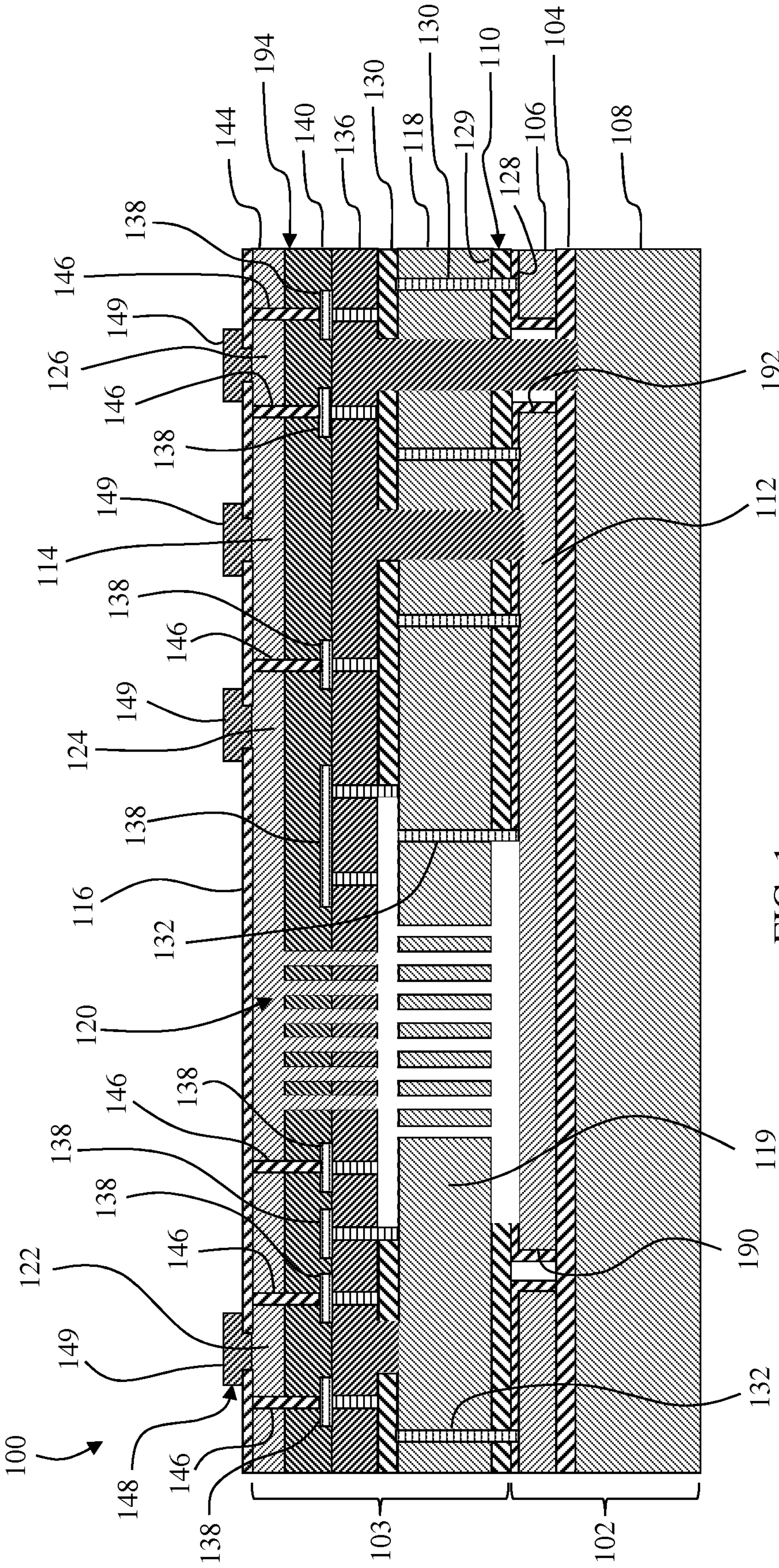
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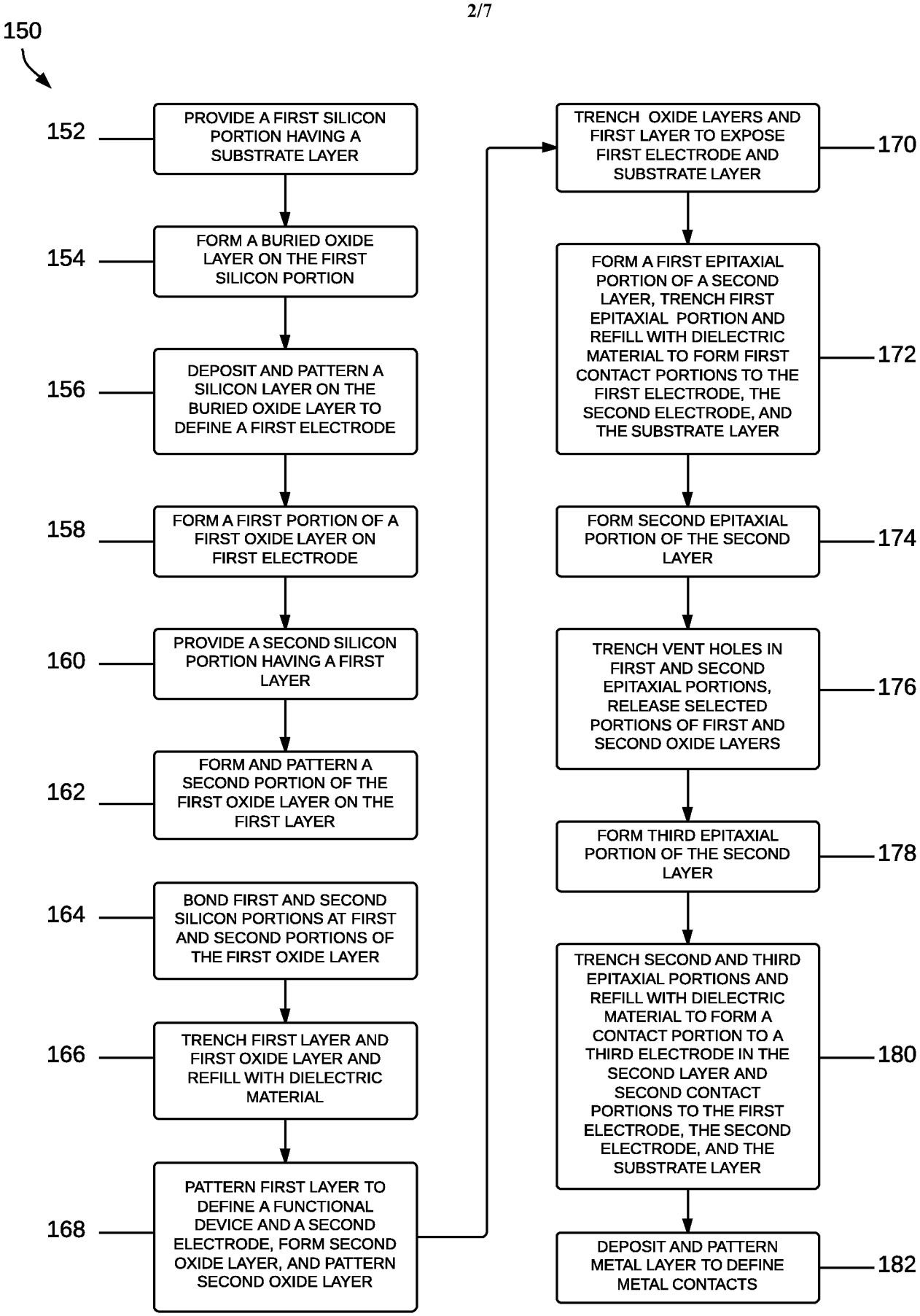
FIG. 1


150
152
PROVIDE A FIRST SILICON PORTION HAVING A SUBSTRATE LAYER
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FORM A BURIED OXIDE LAYER ON THE FIRST SILICON PORTION
156
DEPOSIT AND PATTERN A SILICON LAYER ON THE BURIED OXIDE LAYER TO DEFINE A FIRST ELECTRODE
158
FORM A FIRST PORTION OF A FIRST OXIDE LAYER ON FIRST ELECTRODE
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PROVIDE A SECOND SILICON PORTION HAVING A FIRST LAYER
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BOND FIRST AND SECOND SILICON PORTIONS AT FIRST AND SECOND PORTIONS OF THE FIRST OXIDE LAYER
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TRENCH FIRST LAYER AND FIRST OXIDE LAYER AND REFILL WITH DIELECTRIC MATERIAL
168
PATTERN FIRST LAYER TO DEFINE A FUNCTIONAL DEVICE AND A SECOND ELECTRODE, FORM SECOND OXIDE LAYER, AND PATTERN SECOND OXIDE LAYER
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TRENCH OXIDE LAYERS AND FIRST LAYER TO EXPOSE FIRST ELECTRODE AND SUBSTRATE LAYER
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FORM A FIRST EPITAXIAL PORTION OF A SECOND LAYER, TRENCH FIRST EPITAXIAL PORTION AND REFILL WITH DIELECTRIC MATERIAL TO FORM FIRST CONTACT PORTIONS TO THE FIRST ELECTRODE, THE SECOND ELECTRODE, AND THE SUBSTRATE LAYER
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FORM SECOND EPITAXIAL PORTION OF THE SECOND LAYER
176
TRENCH VENT HOLES IN FIRST AND SECOND EPITAXIAL PORTIONS, RELEASE SELECTED PORTIONS OF FIRST AND SECOND OXIDE LAYERS
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182
DEPOSIT AND PATTERN METAL LAYER TO DEFINE METAL CONTACTS

FIG. 2

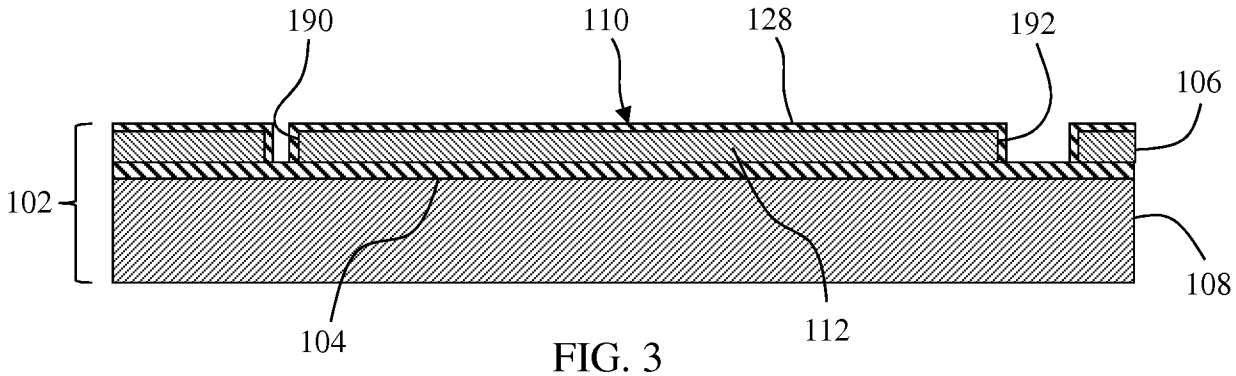

FIG. 3

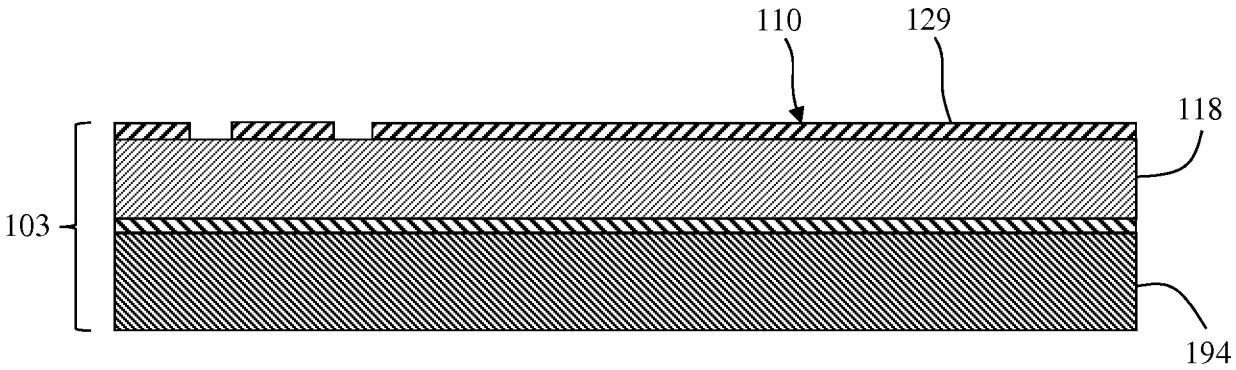

FIG. 4

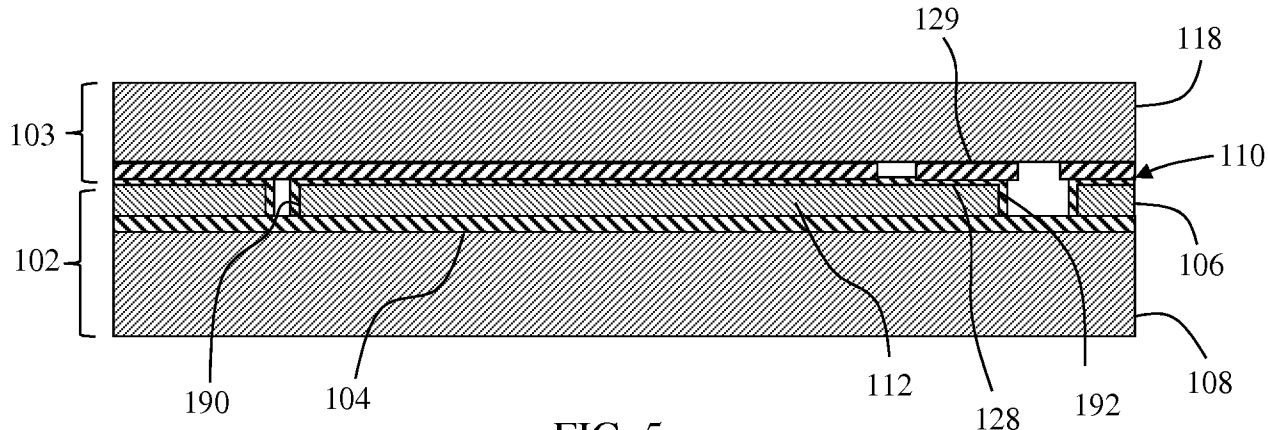

FIG. 5

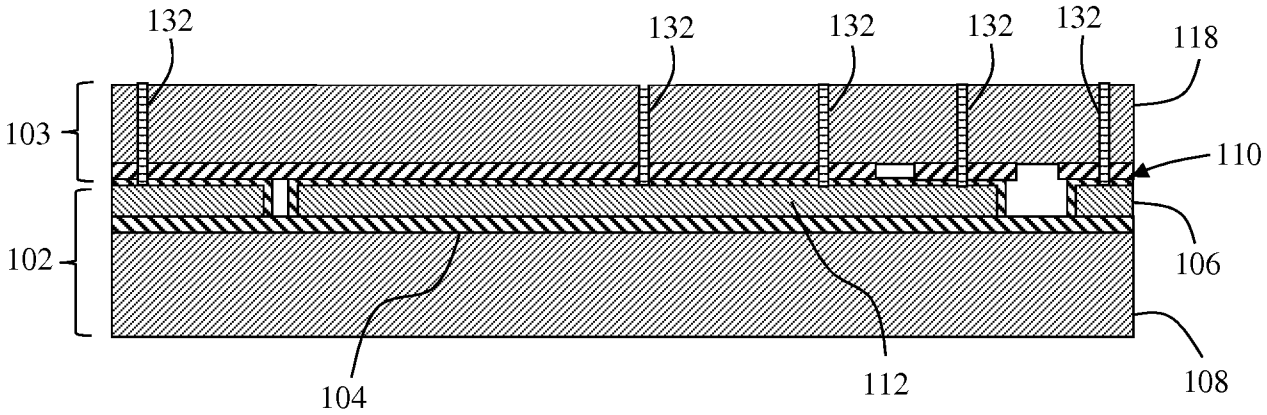

FIG. 6

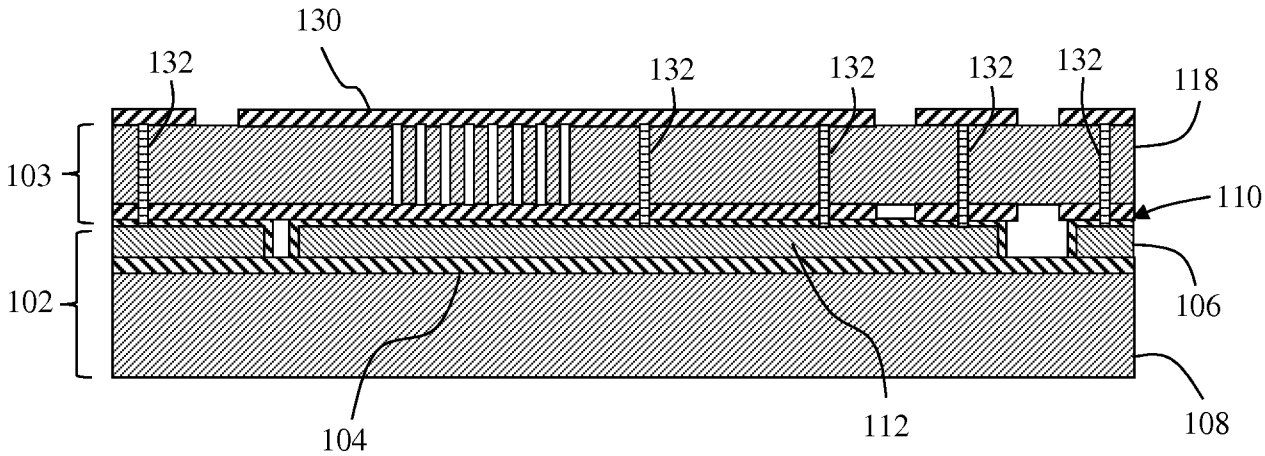

FIG. 7

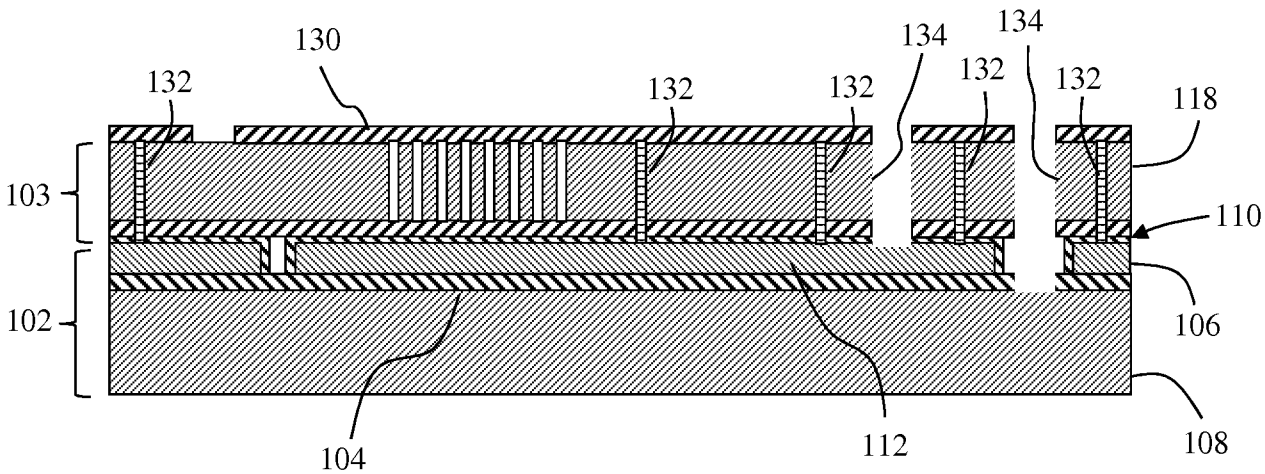

FIG. 8

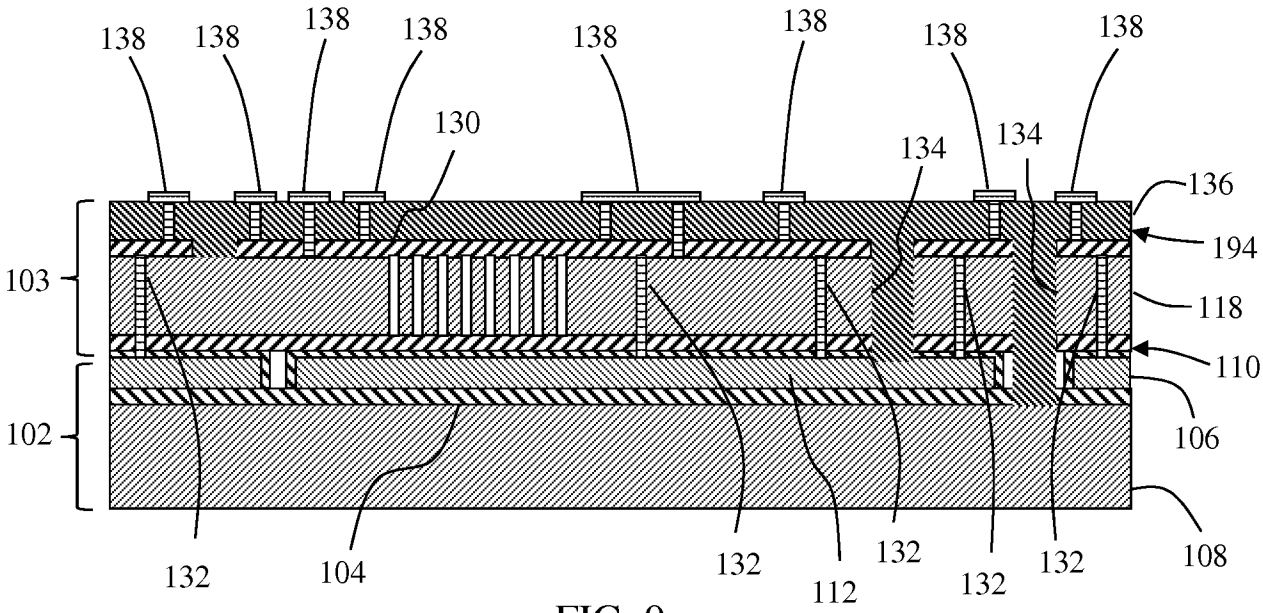
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FIG. 9

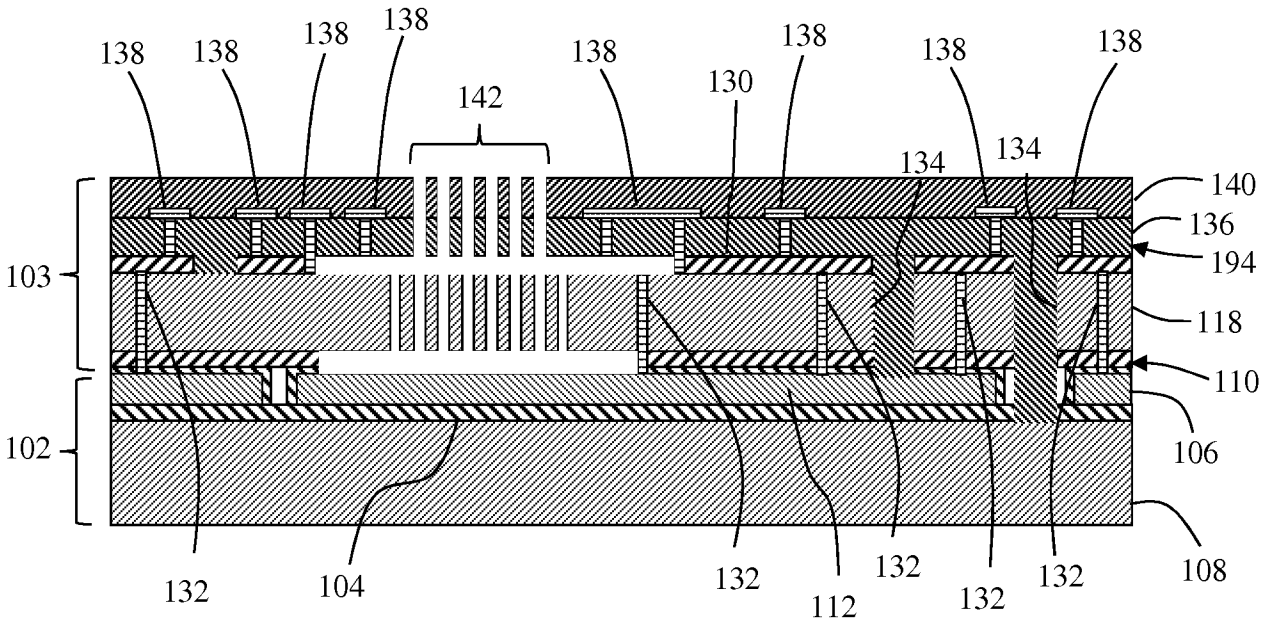
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FIG. 10

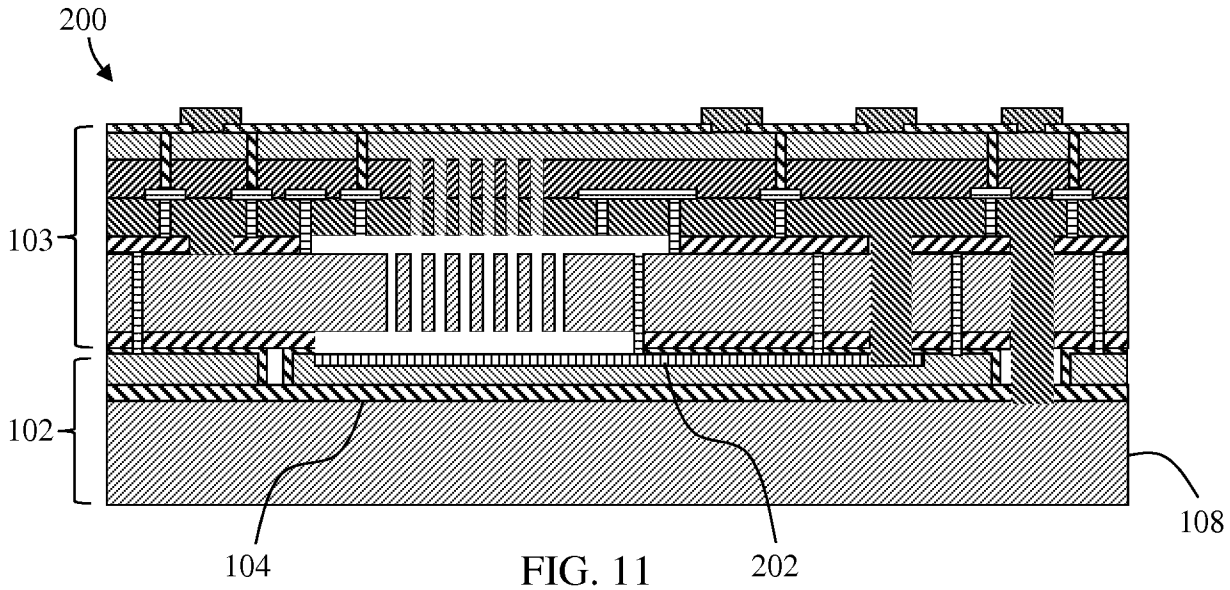

FIG. 11

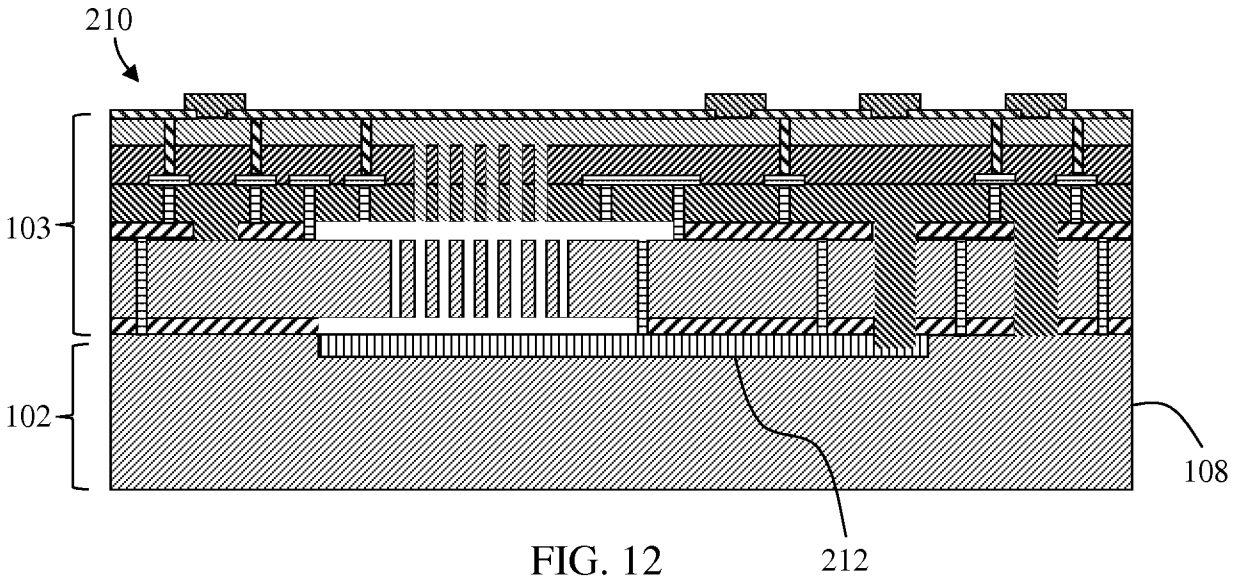

FIG. 12

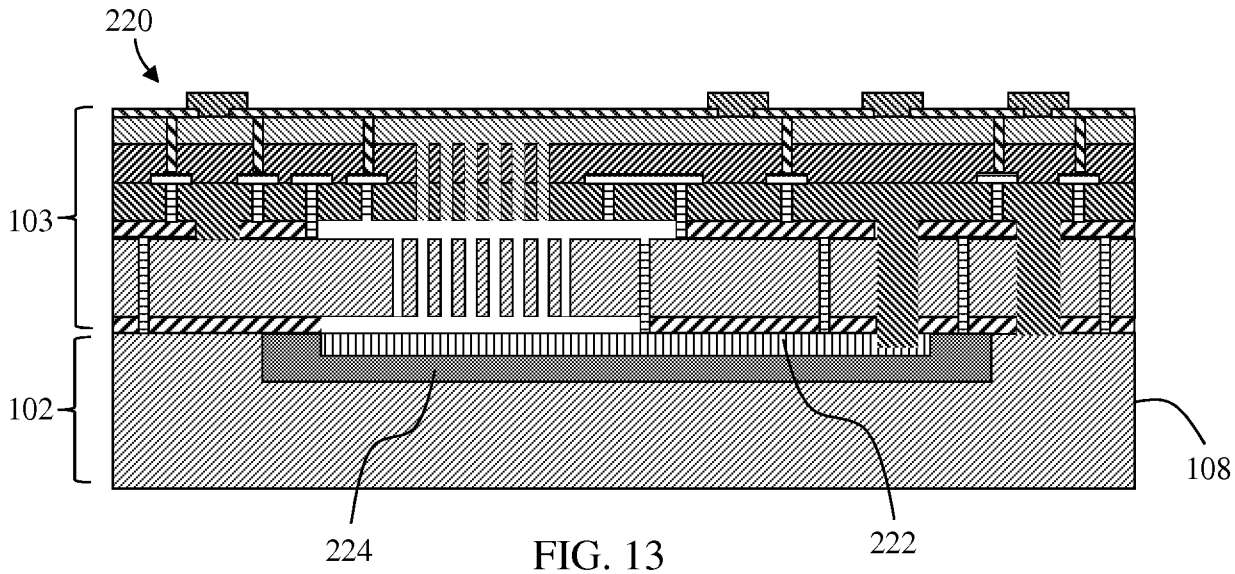

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/055668

A. CLASSIFICATION OF SUBJECT MATTER
INV. B81B7/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
B81C B81B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 10 2010 062555 A1 (BOSCH GMBH ROBERT [DE]) 14 June 2012 (2012-06-14) figure 1 -----	1-16

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 November 2013	29/11/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	McGinley, Colm

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2013/055668

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 102010062555 A1	14-06-2012	NONE	