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(54) COMPLEMENTARY CONDUCTIVITY FET MIXER CIRCUITS

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

This invention relates generally to mixer circuits and more particularly to such circuits employing field effect transistors (FET's).

FET's, such as those of the metal oxide semiconductor (MOS) type, are widely used in mixer circuits. One form of transistor which is particularly popular is the dual-gate, N-channel, depletion-mode, MOS/FET device. It is usually operated in the cascode mode; that is, one of the gate electrodes of the transistor to which the signal at one frequency is applied serves as an input to a common source amplifier and the other gate electrode to which the signal at a second frequency is applied serves as an input to a common gate stage. Such circuit configurations tend to be complex in the sense that a fair number of peripheral elements, such as resistors, are required. Other mixer circuits employ individual FET's of the same conductivity type and these too require a substantial number of peripheral components. A typical mixer circuit of the latter type is shown in the RCA Solid State 1975 DataBook Series SSD-202C, page 83, FIGURE 32.

According to the present invention there is provided a mixer circuit comprising, in combination: two terminals between which an operating voltage may be applied;

two field effect transistors of complementary conductivity types, each having an input electrode, an output electrode, a conduction path between these electrodes, and a control electrode, said two paths being connected to one another at their output electrodes, and said two paths being connected in series between said terminals;

means for quiescently biasing both control electrodes to quiescently operate both transistors in the linear region of their operating range;

means for applying a signal at a frequency f_1 between the control and input electrodes of said first transistor;

means for applying a signal at a frequency f_2 between the control and input electrodes of said second transistor; and

a circuit output terminal connected to said output electrodes.

An embodiment of the present application employs two complementary symmetry field-effect transistors such as those of the MOS type. These circuits employ common-source amplifiers to process both of the frequencies to be mixed, even though the two amplifiers are series connected as viewed by the DC power supply. Operation in the common source mode permits optimum gain to be obtained from both stages of the mixer and, in addition, the circuits are relatively simple and therefore relatively inexpensive.

In the drawing:

FIGURE 1 is a schematic circuit diagram of a single-ended mixer embodying the invention;

FIGURE 2 shows a portion of the circuit of FIGURE 1 in modified form;

FIGURE 3 is a schematic circuit diagram of a push-pull mixer embodying the invention; and

FIGURE 4 is a circuit diagram of a balanced mixer embodying the invention.

Referring first to FIGURE 1, two transistors P_A and N_A of complementary conductivity types have their conduction paths connected in series between a terminal 10 for an operating voltage +V and a terminal 12 at a reference voltage level, shown here as ground. These transistors may be of the MOS enhancement type and together may be

referred to as a complementary field-effect transistor (FET) amplifier. A first input signal E_{IN1}, which may be at a carrier frequency f_1, is supplied to the primary winding 14 of transformer 16. The secondary winding 18 of this transformer forms with tunable capacitor 20 a parallel-resonant circuit tuned to frequency f_1. This circuit is connected at one terminal to the gate electrode 21 of N-type transistor N_A and at its other terminal through a decoupling capacitor 22 to ground. The second input signal E_{IN2}, which may be at a modulating frequency f_2 is applied to the primary winding 24 of a transformer 26. Its secondary winding 28 and variable capacitor 30 together form a parallel resonant circuit tuned to frequency f_2. This circuit is connected at one terminal to the gate electrode 32 of P-type transistor P_A and at its other terminal is connected to ground through decoupling capacitor 34.

The common drain electrode connection 36 of the transistors P_A and N_A is connected through biasing resistor 38 to circuit node 40. This node connects via a first direct current path including resistor 42 to the gate electrode 32 of transistor P_A and via a second direct current path including resistor 44 to the gate electrode 21 of the second transistor N_A. Normally, the resistors 42 and 44 are of the same value and of much lower resistance than resistor 38. For example, biasing resistor 38 may have a value of 22 megohms and resistors 42 and 44 may each have a resistance of 100 K ohms. (The same is true of the biasing and decoupling resistors of the FIGURE 3 and 4 circuits.) The source electrodes of transistors P_A and N_A are held at AC ground by direct connection in the case of N_A and by capacitor 45 in the case of P_A.

The output circuit of the mixer may be a series tuned circuit which includes coil 46 and variable capacitor 48. This circuit is tuned to a desired output signal which may be at the upper (f_1+f_2) or the lower (f_1-f_2) sideband frequency.

In operation, the biasing resistor 38 (together with resistors 42 and 44, respectively) bias the complementary FET amplifier at or close to the center of its linear operating range. In other words, the biasing is such that transistors N_A and P_A both quiescently conduct. The two signals to be mixed are applied to the primary windings 14 and 24, respectively, and cause conduction through the respective transistors N_A and P_A to vary in accordance with the relative amplitudes of these signals. With respect to these AC signals, each amplifier operates in the common-source mode and therefor permits optimum gain to be obtained from its transistor. If the circuit is perfectly symmetrical, as should be the case when the circuit is fabricated in integrated form, resistors 42 and 44 may be of the same value.

The output signal appears at the common drain connection 36 and it includes, among other components, the two sideband frequencies of interest, namely f_1+f_2 and f_1-f_2. The series resonant circuit is tuned to the one of these frequencies for supplying the signal at this frequency to the following stage. In one particular advantageous configuration for integrated circuit implementation, the subsequent stage is a second complementary FET amplifier, as shown. It is advantageous because no additional quiescent bias circuit is needed, as the mixer stage P_A, N_A itself automatically provides the correct bias level via the DC path through coil 46. In similar fashion, if there are following complementary FET amplifier stages they too can make use of this same source of quiescent bias. It is possible to have a number of such stages receive bias from the same source because they have very high input impedance and do not draw any significant amount of DC current. In a preferred embodiment, the following stages such as P_B, N_B are integrated onto the same substrate as transistors P_A and N_A.

The RC networks 42, 34 and 44, 22 serve as bias decoupling networks. A bypass capacitor such as 22 does not have zero ohms reactance at frequency f_1. Consequently, a small increment of the input voltage signal f_1 is developed across capacitor 22. A resistor such as 44 attenuates some of this incremental signal at frequency f_1 which would otherwise pass to tuned circuit 28, 30 and possibly introduce undesired effects. The network 34, 42 performs a similar function for signals at frequency f_2, and both networks attenuate feedback signal from terminal 36.

A number of alternative forms of the circuit of FIGURE 1 are possible. For example, a parallel resonant circuit such as shown in FIGURE 2 may be substituted for the series resonant circuit of FIGURE 1. The capacitor 52 serves to isolate the output lead from ground with respect to DC but provides a low impedance path to the various AC frequency components which are present. Capacitor 52 may instead be inserted between the ground connection and the circuit 54, the choice being dependent on the characteristics of the following circuit. As a third alternative, an appropriate Pi-network may be substituted for the parallel tuned circuit 54.

FIG. 3 illustrates a push-pull embodiment of the invention. It employs two complementary FET amplifiers P_1, N_1 and P_2, N_2, respectively. These, like the amplifier of FIG. 1 are biased by resistor 60 to operate at the center of the linear region of their operating range. The resistor preferably is connected at one end to the center tap of coil 82 and at its other end to decoupling networks 88, 91 and 84, 86. The resistor 84 is connected at its other end to the center tap of coil 74 and resistor 88 to the center tap of coil 64.

The first input signal E_{IN1} is applied to primary winding 62. The secondary winding 64 serves as the inductance of tuned circuit 66 which includes also variable capacitor 68. This tuned circuit is connected between the gate electrodes of N-type MOS transistors N_1 and N_2. In similar fashion, the second input signal E_{IN1} is applied to the primary winding 70. Tuned circuit 72 comprises secondary winding 74 and variable capacitor 76. This parallel tuned circuit is connected at the two terminals thereof to the gate electrodes of P-type transistors P_1 and P_2, respectively.

FIGURE 3 also includes parallel tuned circuit 78 which is connected between the common drain electrode connections of the two amplifiers. The output signal is available at the terminals of a winding 80 which is coupled to the inductor 82 of tuned circuit 78. The circuit also includes a first RC decoupling circuit 84, 86 and a second such circuit 88, 91.

The operation of the circuit should be clear from the description of FIGURE 1. The first input signal at frequency f_1 is coupled to tuned circuit 66 whose resonant frequency is f_1. This circuit supplies input signals to the N-type transistors N_1 and N_2, 180° out of phase. Similarly, tuned circuit 72, which is tuned to the second input frequency f_2, supplies 180° out-of-phase signals to the gate electrodes of transistors P_1 and P_2, respectively. The output parallel resonant circuit 78 is tuned to the sideband frequency of interest. For example, it may be tuned to f_1+f_2 or f_1-f_2. This output signal is sensed by coil 80 and is available at its output terminals.

Operation in the push-pull mode increases the amplitude of the output signal by a factor of two over that obtainable with the circuit of FIGURE 1, assuming the transistors employed have the same transconductance (g_m) in both circuits. Another important advantage of this circuit is that the amplitude of the even harmonics which are generated is greatly reduced. The circuit is also useful in reducing the amount of "leak through" between the two signals of frequencies f_1 and f_2. If the mixer is to be used, for example, in a super-hetrodyne receiver and f_2 is the local oscillator frequency, it is desirable to minimize the portion of this signal which may leak through to the f_1 port and possibly be radiated through the front end of the receiver. Such radiation is undesirable because it can act as a source of interference to other equipments. However, there is a remanent route of coupling, namely the drain-gate capacitance of the N-type transistors, by which a portion of the signal at f_2 may be coupled to the f_1 port. The signal at node 90 is 180° out of phase with the signal at node 92 and therefore any of such signals which pass through these coupling paths appear out-of-phase at the opposite terminals of parallel tuned circuit 66. They can cause a small increment of f_2 current flow through winding 62, which is undesirable. The even-ordered harmonics of f_2 are of much lower amplitude that f_2 and therefore the feedthrough, if any, is correspondingly lower than that of f_2 and is usually not significant.

The balance mixer of FIGURE 4 reduces the f_2 feedthrough even further. This circuit differs from the FIGURE 3 circuit in that the parallel-tuned circuit 72 is connected at one terminal to radio-frequency ground through by-pass capacitor 86, and is connected at its other terminal to the gate electrodes of both transistor P_1 and P_2. Thus, the f_2 signals applied to these gate electrodes are in-phase and nodes 90 and 92 therefore receive f_2 components of the same amplitude. Any feedthrough via the drain-gate capacitance of transistors N_1 and N_2 of this f_2 component will therefore be at the same potential at both terminals of tuned circuit 66, and will have no effect. It is assumed here that transistor P_1 has characteristics similar to transistor P_2 and also that transistor N_1 has characteristics similar to those of transistor N_2. This assumption is a reasonable one in the case of monolithic integrated circuits.

WHAT WE CLAIM IS:

1. A mixer circuit comprising, in combination:

two terminals between which an operating voltage may be applied;

two field effect transistors of complementary conductivity types, each having an input electrode, an output electrode, a conduction path between these electrodes, and a control electrode, said two paths being connected to one another at their output electrodes, and said two paths being connected in series between said terminals;

means for quiescently biasing both control electrodes to quiescently operate both transistors in the linear region of their operating range;

means for applying a signal at a frequency f_1 between the control and input electrodes of said first transistor;

means for applying a signal at a frequency f_2 between the control and input electrodes of said second transistor; and

a circuit output terminal connected to said output electrodes.

2. A mixer circuit as set forth in claim 1, further including a resonant circuit tuned to one of the frequencies (f_1+f_2) and (f_1-f_2) connected between said output terminal and another circuit point.

3. A mixer circuit as set forth in claim 2, wherein said resonant circuit comprises a parallel resonant circuit said other circuit point comprising a point at a reference potential.

4. A mixer circuit as set forth in claim 2, wherein said resonant circuit comprises a

series resonant circuit, said other circuit point comprising a point at a reference potential and further including a point on said series resonant circuit to which the control electrode of another field effect transistor may be connected.

5. A mixer circuit as set forth in claim 1, wherein said means for applying a signal at frequency f_1, comprises a parallel resonant circuit tuned to frequency f_1, and wherein said means for applying a signal at frequency f_2 comprises a parallel resonant circuit tuned to frequency f_2.

6. A mixer circuit substantially as hereinbefore described with reference to any of FIGURES 1, 3 or 4 or Figure 1 as modified by Figure 2 of the accompanying drawing.

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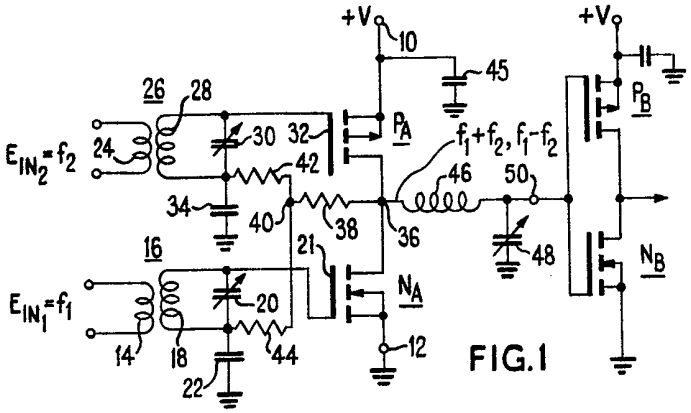

FIG.1

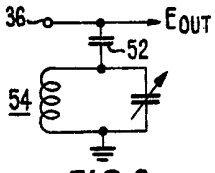

FIG.2

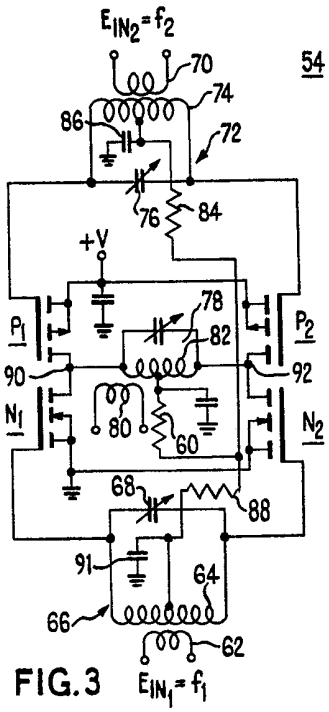

FIG.3

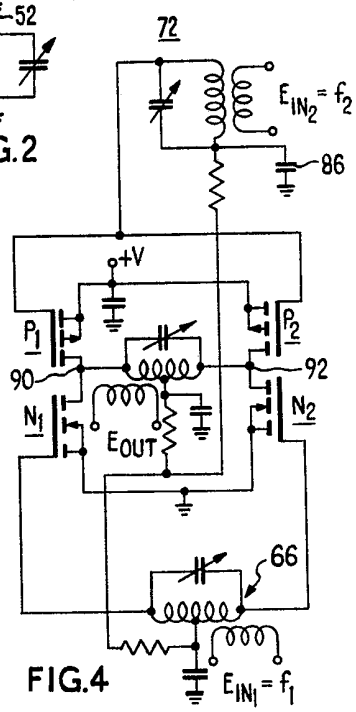

FIG.4