(19) World Intellectual Property Organization

International Bureau





(43) International Publication Date 26 February 2009 (26.02.2009)

(10) International Publication Number WO 2009/026171 A2

(51) International Patent Classification: *H01L 23/12* (2006.01)

(21) International Application Number:

PCT/US2008/073365

(22) International Filing Date: 15 August 2008 (15.08.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

60/965,184 17 August 2007 (17.08.2007) US

(71) Applicant (for all designated States except US): VERTI-CAL CIRCUITS, INC. [US/US]; 10 Victor Square, Scotts Valley, CA 95066 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): CASKEY, Terrence [US/US]; 236 John Street, Santa Cruz, CA 95606 (US). ANDREWS, Lawrence, Douglas [US/US]; 22545 Old Santa Cruz Hwy., Los Gatos, CA 95033 (US). MCEL-REA, Simon, J.s. [GB/US]; 621 Acorn Court, Scotts Valley, CA 95066 (US). MCGRATH, Scott [US/US]; 13 Terrace View Court, Scotts Valley, CA 95066 (US). ROBINSON, Marc [US/US]; 1235 Valley Quail Circle, San Jose, CA 95120 (US). SCOTT, Mark [US/US]; 16061 Mays Avenue, Monte Sereno, CA 95030 (US). DU, Yong [CN/US]; 10190 N. Foothill Boulevard, Apt. F23,

Cupertino, CA 95014 (US). **JONES, Roydn** [US/US]; 1815 B Speyer Lane, Redondo Beach, CA 90278 (US). **TRAN, Thanh, Van** [US/US]; 9478 Daines Drive, Temple City, CA 91780 (US).

- (74) Agent: KENNEDY, Bill; Haynes Beffel & Wolfeld Llp, P.o. Box 366, Half Moon Bay, CA 94019 (US).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

 without international search report and to be republished upon receipt of that report

(54) Title: STACKED DIE VERTICAL INTERCONNECT FORMED BY TRANSFER OF INTERCONNECT MATERIAL

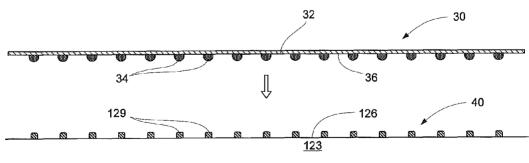


Fig. 4A

(57) Abstract: Apparatus for making electrical interconnection of semiconductor die includes a transfer carrier having an electrically conductive material arranged in a pattern on a transfer surface. A transfer process for electrical interconnect includes steps of aligning the transfer apparatus with an edge of a die to be interconnected; and moving the transfer apparatus toward the die edge (or moving the die edge toward the transfer apparatus, or moving both the transfer carrier and the die edge in relation to one another) to bring the patterned conductive material on the transfer surface and interconnect terminals on the die into contact. In some embodiments the carrier is left in place in a functioning interconnected device; in other embodiments the transfer carrier and the die edge are separated to leave at least a portion of the conductive material in contact with the interconnect terminals.





STACKED DIE VERTICAL INTERCONNECT FORMED BY TRANSFER OF INTERCONNECT MATERIAL

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority from T. Caskey *et al.*, U.S Provisional Application No. 60/965,184, titled "Stacked die interconnect formed by transfer of interconnect material", which was filed August 17, 2007, and which is hereby incorporated by reference herein.

5

10

15

20

25

30

35

BACKGROUND

[0002] This invention relates to electrical interconnection of integrated circuit chips and, particularly, to interconnection of assemblies including one or more integrated circuit chips.

[0003] Interconnection of stacked die with the substrate presents a number of challenges.

[0004] Some die as provided have die pads along one or more of the die margins, and these may be referred to as peripheral pad die. Other die as provided have die pads arranged in one or two rows near the center of the die, and these may be referred to as center pad die. The die may be "rerouted" to provide a suitable arrangement of interconnect pads at or near one or more of the margins of the die.

SUMMARY

[0005] In various general aspects the invention features methods for electrical interconnection of a stack of die, or of a die or a stack of die with underlying circuitry such as a substrate, and assemblies made by the methods.

[0006] In one general aspect the invention features a method for electrical interconnection by a transfer process using transfer apparatus. The transfer apparatus includes a transfer carrier having an electrically conductive material arranged in a pattern on a transfer surface, and the transfer process includes steps of aligning the transfer apparatus with an edge of a die to be interconnected; moving the transfer apparatus toward the die edge (or moving the die edge toward the transfer apparatus, or moving both the transfer carrier and the die edge in relation to one another) to bring the patterned conductive material on the transfer surface and interconnect terminals on the die into contact; and moving the transfer carrier away from the die edge (or moving the die edge away from the transfer carrier, or moving both the transfer carrier and the die edge in relation to one another), leaving at least a portion of the conductive material in contact with the interconnect terminals. The expressions "moving the carrier toward the die edge" and "moving the carrier away from the die edge" are employed herein to include any of moving the carrier, or moving the die edge, or moving both the carrier and the die edge. [0007] The electrically conductive material can be arranged on the transfer surface in any of a variety of ways such as, for example: by directed dispense, continuously or in pulses (e.g., spotwise) from a needle or nozzle; by printing, using an array of nozzles, for example, or by

- 2 -

using a mask or screen or stencil. Methods for pulsed dispense of interconnect material are disclosed, for example, in T. Caskey *et al.* U.S. Application No. 12/124,097, titled "Electrical interconnect formed by pulsed dispense", which was filed May 20, 2008, and which is hereby incorporated herein by reference.

5

10

15

20

25

30

35

[0008] The carrier may have any of a variety of forms. For example, the carrier may be a sheet or film; the carrier may be stiff or flexible; the transfer surface may be smooth or rough, textured (for example having raised ridges or bumps) or planar; the carrier may be continuous or discontinuous (that is, it may be perforated in any of a variety of configurations); the carrier may have the form of an open meshwork or web or screen. In some embodiments the transfer carrier is a single strand or wire or fiber or thread.

[0009] In some embodiments the transfer surface is of a material that holds the conductive material in a prescribed pattern during the transfer, and in some embodiments releases an amount of the material following contact of the material with the interconnect terminals on the die, sufficient to provide the desired electrical interconnection.

[0010] In some embodiments the transfer surface is configured so that -- whatever the material characteristics of the transfer surface -- it holds the conductive material in a prescribed pattern during the transfer, and in some embodiments releases at least a sufficient amount of the material following contact of the material with the interconnect terminals on the die. In some such embodiments the transfer surface is constructed or textured so that the contact of the patterned conductive material on the surface is small; this may be accomplished, for example, in a transfer carrier in the form of an open meshwork or web or screen, for example; or in a carrier transfer surface having raised ridges or bumps, for example, on which the electrically conductive material is carried.

[0011] In another general aspect the invention features a method for electrical interconnection by a process using a carrier having an electrically conductive material arranged in a pattern on a carrier surface, and the process includes steps of aligning the carrier with an edge of a die to be interconnected; moving the carrier toward the die edge (or moving the die edge toward the carrier, or moving both the carrier and the die edge in relation to one another) to bring the patterned conductive material on the carrier surface and interconnect terminals on the die into contact. The expression "moving the carrier toward the die edge" is employed herein to include any of moving the carrier, or moving the die edge, or moving both the carrier and the die edge in relation to one another.

[0012] In some embodiments the carrier is left in place in the interconnection; in other embodiments the carrier is subsequently moved away from the die edge (or the die edge is moved away from the carrier, or both the carrier and the die edge are moved in relation to one another), leaving at least a portion of the conductive material in contact with the interconnect terminals. The expression "moving the carrier away from the die edge" is employed herein to

include any of moving the carrier, or moving the die edge, or moving both the carrier and the die edge in relation to one another.

[0013] In embodiments in which the carrier is left in place, the carrier may be made of an electrically insulative material, to avoid electrical shorts between elements of the patterned conductive material.

5

10

15

25

30

[0014] Or, where the carrier is left in place, it may be configured so that the carrier does not span between elements of the patterned conductive material; for example, the carrier may be a matrix or array of wires or threads or the like that coincide with the patterned elements of electrically conductive material. In such embodiments the carrier may be made of a material that is either electrically insulative or more or less electrically conductive.

[0015] In another general aspect the invention features transfer apparatus for electrical interconnection, the apparatus including a transfer carrier having an electrically conductive material arranged in a pattern on a transfer surface.

[0016] In some embodiments the apparatus includes automated means for manipulating the transfer carrier.

[0017] In another general aspect the invention features a stacked integrated chip assembly electrically interconnected according to the methods.

[0018] In another general aspect the invention features a die electrically interconnected to underlying circuitry according to the methods.

20 **[0019]** In another general aspect the invention features a stacked integrated chip assembly electrically interconnected according to the methods and electrically interconnected to underlying circuitry.

[0020] The interconnected die and assemblies according to the invention can be used for building computers, telecommunications equipment, and consumer and industrial electronics devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] FIG. 1 is a diagrammatic sketch in a perspective view showing a four-die stack.

[0022] FIG. 2 is a diagrammatic sketch in a perspective view showing a four-die stack situated in relation to a substrate.

[0023] FIG. **3** is a diagrammatic sketch in elevational view showing interconnect material arrayed on a release form according to an embodiment of the invention.

[0024] FIGs. **4A** through **4C** are diagrammatic sketches in plan view showing stages in a process for transferring interconnect material from a release form onto a die stack, and forming stacked die interconnection, according to an embodiment of the invention.

[0025] FIGs. 5A through 5C are diagrammatic sketches in sectional view showing stages in a process for transferring interconnect material from a release form onto a die stack, and forming stacked die interconnection, according to an embodiment of the invention.

-4-

[0026] FIGs. 6A and 6B are diagrammatic sketches in sectional view as in FIG. 5C, showing stages in mounting a four-die stack assembly onto a substrate according to an embodiment of the invention.

5

10

15

20

25

30

35

[0027] FIGs. 7A and 7B are diagrammatic sketches in plan view, showing stages in mounting a stacked die assembly onto a substrate according to an embodiment of the invention.

DETAILED DESCRIPTION

[0028] The invention will now be described in further detail by reference to the drawings, which illustrate alternative embodiments of the invention. The drawings are diagrammatic, showing features of the invention and their relation to other features and structures, and are not made to scale. For improved clarity of presentation, in the FIGs. illustrating embodiments of the invention, elements corresponding to elements shown in other drawings are not all particularly renumbered, although they are all readily identifiable in all the FIGs. Also for clarity of presentation certain features are not shown in the FIGs., where not necessary for an understanding of the invention.

[0029] Turning now to FIG. 1, there is shown in a perspective view a stack 10 of four semiconductor die 12, 14, 16, 18, in a die stack assembly, in which the die have off-die interconnect terminals. The die stack assembly may be mounted on underlying circuitry, such as on another die, or such as on a substrate, as indicated generally at 20 in FIG. 2. Each die has two larger generally parallel, generally rectangular (for example square) sides, and four edges. One larger side may be referred to as the front side, and the other may be referred to as the back side. The circuitry of the die is situated at or near the die surface at the front side, and so the front side may be referred to as the active side of the die. In the view presented in FIGs. 1 and 2 the die are shown with the respective active sides facing away from the substrate 20, so that the front side 124 of die 12 is visible. Also visible in the view shown in FIGs. 1 and 2 are edges 122, 126 of die 12, edges 142, 146 of die 14, edges 162, 166 of die 16, and edges 182, 186 of die 18. Margins of the die are adjacent the edges; for example, margins 127 and 123 are adjacent the edges 126 and 122 on the back side of die 12, and margins 125 and 121 are adjacent the edges 126 and 122 on the front side of die 12. The die in the example shown in FIGs. 1 and 2 have "off-die" interconnects; other interconnect configurations are contemplated. In an off-die configuration as shown in FIGs. 1 and 2, where interconnect terminals are employed, interconnect terminals 129 are bonded to interconnect pads 128 in or near the margin 125 at the active side 124 of die 12, interconnect terminals 149 can be optionally bonded to interconnect pads in or near the margin at the active side of

10

15

20

25

30

35

die 14, interconnect terminals 169 can be bonded to interconnect pads in or near the margin at the active side of die 16, and interconnect terminals 189 can be bonded to interconnect pads in or near the margin at the active side of die 18. The interconnect terminals, if provided, can project outward beyond the die edge as in the embodiments shown in the FIGs.

[0030] A substrate 20, shown in FIG. 2, has a die attach side 224, on which bond pads 228 are situated. A number of substrates 20 may be provided in a row or array, as suggested by the broken lines X; at some stage in the process, the substrates are separated, for example by sawing or punching. Each substrate has edges, of which edge 226 and 222 are visible in the view shown in FIG. 1; and margins of the substrate are adjacent the substrate edges; for example margins 227 and 221 are adjacent the edges 226 and 222 on the die attach side 224 of the substrate 20, and margins 225 and 223 are adjacent the edges 226 and 222 on the obverse side of the substrate 20.

[0031] In the assembly shown by way of example in FIG. 2, the bond pads 228 are arranged in two rows, one generally parallel to the margin 227 and one generally parallel to the opposite margin. The locations of the bond pads correspond to the locations of the interconnect terminals on the die, when the die is mounted onto the substrate. Accordingly, the interconnect pads on the die in the examples illustrated in these examples are arranged along two opposite margins. Other arrangements of bond pads are contemplated, according to the arrangements of pads on the particular die. In other embodiments the interconnect pads on the die may be situated along one die margin, or along three or all four margins; and the bond pads on the substrate in such embodiments are arranged correspondingly. Bond pads on the substrate may be arranged in two or more rows of pads along any one or more boundaries of the die footprint; and the bond pads may be interdigitated. In some embodiments, certain of the pads on a given die may not be electrically connected to other die in the stack; for example, "chip select" or "chip enable" pins on a given die may be electrically connected to underlying circuitry (on the substrate, for example), but not to other die. In such embodiments the terminals from such pads may be fanned out horizontally on the die, and on a given die one or more (or, optionally, none) of the pads at the ends of the fanned-out traces may be connected by way of pedestals in an optional second row along an edge of the die.

[0032] In a conventional approach, interconnection may be accomplished by applying an electrically conductive material such as a conductive epoxy using a capillary dispenser. For example, die may be stacked as shown for example in FIG. 1, and mounted in a fixture. The conductive material may then be applied through a capillary dispenser as the dispenser is moved over the die edges at a face of the stack.

[0033] The invention provides for electrical interconnection of die in a die stack, as in FIG. 1, and of a die stack to a substrate, as in FIG. 2, in one general aspect, by using a transfer process. An embodiment of a transfer apparatus according to the invention is shown by way

10

15

20

25

30

35

of example in FIG. 3, and an embodiment of a transfer process for electrically interconnecting a stack of four die according to the invention is shown by way of example in FIGs. 4A through 4C (die in plan view) and FIGs. 5A through 5C (die in sectional view).

[0034] Referring now to FIG. 3, there is shown in a face-on view a part of a transfer apparatus 30 including a transfer carrier 32 having a transfer surface 36 on which an electrically conductive material is arranged in a pattern 34. The transfer carrier may be configured to be manipulable using automated equipment (not shown in the FIG.). The transfer carrier may be a more or less stiff or flexible block or sheet or film. In some embodiments the transfer surface may be smooth or rough, textured (for example having raised ridges or bumps) or planar. In some embodiments the transfer carrier may be continuous or discontinuous (that is, it may be perforated any of a variety of configurations), and it may have the form of an open meshwork or web or screen. In some embodiments the transfer carrier is an array or matrix of threads or wires or the like, or a single thread or wire or the like.

[0035] The electrically conductive material may be, for example, an electrically conductive polymer. In the illustrated example the conductive material is arranged as a series of linear beads, each bead intended to contact an interconnect terminal on a die, or a set of corresponding interconnect terminals on stacked die. The material of the transfer carrier, at least at the transfer surface of the carrier, retains the patterned arrangement of the electrically conductive material during manipulation of the device, and releases the electrically conductive material following the application of the material to interconnect terminals at the die edge, as described below with reference to FIGs. 4A through 4C and 5A through 5C. Accordingly, the material of the transfer carrier at the transfer surface is selected according to the characteristics of the electrically conductive material.

[0036] The transfer process includes steps of aligning the transfer apparatus with an edge of a die to be interconnected (FIGs. 4A, 5A, for example); moving the transfer apparatus toward the die edge (or moving the die edge toward the transfer apparatus, or moving both the transfer carrier and the die edge in relation to one another) to bring the patterned conductive material on the transfer surface into contact with interconnect terminals on the die (FIG. 4B, 5B, for example); and moving the transfer carrier away from the die edge (or moving the die edge away from the transfer carrier, or moving both the transfer carrier and the die edge in relation to one another), leaving the conductive material in contact with the interconnect terminals (FIG. 4C, 5C, for example). FIG. 4A shows a transfer carrier 32 aligned face-to-face with edge 126 of a die 40. In this view, the backside 123 of the die faces the viewer, and the active side of the die faces away. Accordingly, in this view only the portions 129 projecting beyond the margin of the die can be seen, the remainder being obscured by the die. The transfer surface 36 of the transfer carrier 32 faces the die edge 126, so that while the die

-7-

appears in a plan view, the transfer carrier appears in a sectional view. To effect contact of the patterned conductive material with the respective interconnect terminals, the die edge and the transfer carrier are moved toward one another (as indicated by the arrow in FIG. 4A, 5A) until the interconnect terminals 129 press against and into the patterned conductive material 314, as shown in FIG. 4B, 5B. In a following step the transfer carrier 32 and the die 50 are moved away from one another (as indicated by the arrow in FIG. 4C, 5C), leaving the conductive material 324 in place at the die edge 126.

5

10

15

20

25

30

35

[0037] The process is carried out at all the die edges having interconnect terminals to be interconnected, either simultaneously (using a suitable fixture) or serially (one or two edges being processed at one time).

[0038] Suitable electrically conductive polymers include, polymers filled with conductive material in particle form such as, for example, metal-filled polymers, including, for example metal filled epoxy, metal filled thermosetting polymers, metal filled thermoplastic polymers, or an electrically conductive ink. The conductive particles may range widely in size and shape; they may be for example nanoparticles or larger particles. In some embodiments the conductive material can be a partially-curable polymer; a partial cure may be performed at an earlier stage in the process (for example, following application of the conductive material to the transfer surface), and a final cure or post-cure may be performed at a later stage (for example, following removal of the transfer carrier from the die edge) to increase the robustness of the interconnection. In some embodiments the interconnect material provides a mechanical strength (for example, helping to hold the die together in the stack) as well as a reliable electrical interconnection. In some embodiments, a cure step can reduce the adhesion of the conductive polymer to the transfer surface, and such a cure step can be performed following contact with the interconnect terminals, to facilitate separation of the transfer carrier from the formed interconnects. Or, a suitable solvent may be employed to facilitate separation of the transfer carrier from the conductive material.

[0039] The conductive material may be applied onto the transfer surface of the transfer carrier by directed dispense, for example from a needle, or continuously or spotwise from a nozzle, for example; or by printing, using an "ink jet" approach, for example; or by use of a mask or screen, as in screen printing or stencil printing, for example. The pattern of the conductive material on the transfer surface is designed to mirror the interconnect scheme on the die to be interconnected, and the carrier is aligned with the die edge with sufficient precision to ensure good registration of the patterned conductive material with the interconnect terminals. As may be appreciated, patterns other than the illustrated series of straight beads may be suitable for a particular die stack.

10

15

20

25

30

35

-8-

[0040] It is not necessary that all the interconnect material be left on the die after the transfer carrier is withdrawn; it is necessary only that a sufficient amount of the material remain to effect the desired interconnection.

[0041] The transfer carrier may be disposable, or it may be reusable. In some embodiments, the transfer carrier is not removed following the step of contacting the conductive material with the interconnect terminals; instead, it is left in place as part of the assembly, and may be left in place as part of a final functional device. In embodiments where the transfer carrier is left in place in a functioning device, the transfer carrier may be made of an electrically insulative material, to avoid electrical shorts between elements of the patterned conductive material. Or, where the transfer carrier is left in place, it may be configured so that the carrier does not span between elements of the patterned conductive material; for example, the carrier may be a matrix or array of wires or threads or the like that coincide with the patterned elements of electrically material. In such embodiments the transfer carrier may be made of a material that is either electrically insulative or more or less electrically conductive.

[0042] The transfer method may be employed to interconnect die having any of a range of die edge configurations having various interconnect terminal configurations, and the interconnect terminals need not be off-die interconnects, as in the examples shown in the FIGs. The interconnect terminals may be more or less flush with the die edges, for example. Or, where a single die is to be connected, or where the die in a stack are separated from one another sufficiently to allow incursion of a small amount of the conductive material into the gap between adjacent die at the die margin, the interconnect terminals may be on or in the active surface of the die at or near the die margin. Interconnect terminal configurations include, for example, an "off-die" interconnect terminal; a bump or glob on the die pad, which may extend (or not) beyond the die edge; a terminal constituting an extension of the die pad to near the die edge, or extending on the die surface over the die edge, and in such examples the die edge may be chamfered. These are disclosed, for example, in S.J.S. McElrea *et al.* U.S. Application No. 12/124,077, titled "Electrically interconnected stacked die assemblies", which was filed May 20, 2008, and which is hereby incorporated herein by reference.

[0043] Die assemblies made according to embodiments of the invention, such as four-die assemblies 50, as shown for example in FIG. 5C, or others, can be mounted on and electrically connected with a substrate as shown for example in FIGs. 6A and 6B, showing an embodiment in which the die are mounted with the active side facing away from the substrate, or for example in FIGs. 7A and 7B, showing an embodiment in which the die are mounted with the active side facing toward the substrate.

[0044] FIG. 6A shows a substrate <u>20</u> having bond pads <u>228</u> exposed at a die attach side for interconnection. The four-die assembly <u>50</u> is oriented in this embodiment with the back side of a die in the assembly facing toward the die attach side of the substrate. In the embodiment

10

15

20

25

30

35

shown in FIGs. 6A, 6B, the four-die assembly 50 is affixed to the substrate using a die attach adhesive 84, which may be applied to the substrate, as illustrated for example in FIG. 6A, or to the surface of the die assembly. In some embodiments the electrical connection is secured by depositing a spot 82 of a conductive material on the bond pad. The electrically conductive material may be a curable material such as a conductive epoxy, for example. The ends 54 of the conductive elements on the die assembly are pressed against the spots, and then the assembly is treated to cure or reflow the spots, to complete the interconnection, as shown for example at 83 in FIG. 6B. In some embodiments the adhesive 84 is omitted, and the assembly 50 is secured to the substrate 20 by the cured conductive epoxy spots only. [0045] FIG. 7A also shows a substrate 20 having bond pads 228 exposed at a die attach side for interconnection. The four-die assembly 50 is oriented in this embodiment with the front (active) side of a die in the assembly facing toward the die attach side of the substrate. The four-die assembly 50 can optionally be affixed to the substrate using, for example a die attach adhesive, and a spacer may optionally be situated between the die front side and the adhesive. The adhesive, where used, may be applied to the substrate, or it may be applied to the die surface. Where a spacer is employed it may be applied to the die surface, or it may be applied to an adhesive on the substrate. Or, an adhesive/spacer may be employed, including for example an adhesive containing glass or polymer spheres (for example) dimensioned to provide a suitable standoff between the die surface and the die attach surface of the substrate, or including for example a thermoset adhesive that maintains a sufficient thickness during processing and cure. In some embodiments the electrical connection is secured by depositing a spot 82 of a conductive material on the bond pad. The electrically conductive material may be a curable material such as a conductive epoxy, for example. The ends 54 of the conductive elements on the die assembly are pressed against the spots, and then the assembly is treated to cure or reflow the spots, to complete the interconnection, as shown for example at 83 in FIG. 7B. In the example shown in these FIGs., no adhesive is employed between the assembly and the substrate, and the assembly 50 is secured to the substrate 20

[0046] Alternatively, an assembly may be oriented with the front side of a die in the assembly facing toward the die attach side of the substrate, as shown in FIG. **7A**, but not affixed to the substrate using an adhesive. In such embodiments, the assembly may be secured to the substrate by the electrically conductive material joining the interconnects with the bond pads. The narrow space between the die and the substrate can later be underfilled.

by the cured conductive epoxy spots 83 only.

[0047] FIG. 8A shows in plan view an example of a substrate <u>20</u>, generally similar to the substrate <u>20</u> shown in sectional view in FIG. 7A, which is taken at 7A - 7A in FIG. 8A. FIG. 8B shows in plan view an example of an interconnected stacked die assembly 50 mounted on a

- 10 -

substrate, generally similar to the assembly shown in sectional view in FIG. **7B**, which is taken at **7B** - **7B** in FIG. **8B**.

[0048] In the stacks of die shown by way of example in the drawings, the edges of the die having terminals to be interconnected are aligned substantially vertically in the stack; that is, the stack presents for interconnection a substantially planar face that is roughly perpendicular to the front sides of the die. The transfer method and apparatus may be employed to interconnect die that are not vertically aligned in the stack. The interconnect edges of the die in the stack may be offset, for example; they may present a tiered or stepped interconnect surface, or they may be staggered so that interconnect edges of alternating die in the stack are presented for interconnection. Various stacking configurations are illustrated, for example in S.J.S. McElrea *et al.* U.S. Application No. 12/124,077 (referenced above).

[0049] Other embodiments are within the claims.

10

5

CLAIMS

We claim:

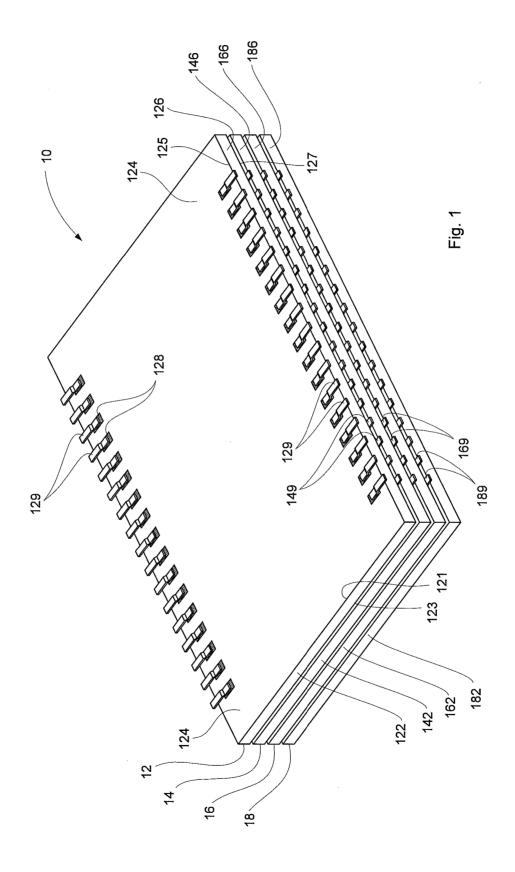
- 1. A method for electrical interconnection, comprising providing a carrier having an electrically conductive material arranged in a pattern on a carrier surface, aligning the carrier with an edge of a die to be interconnected; and moving the carrier toward the die edge to bring the patterned conductive material on the carrier surface and interconnect terminals on the die into contact.
- 2. The method of claim 1 wherein the carrier is left in place in the interconnection.
- 3. The method of claim 1 further comprising, following bringing the conductive material and the interconnect terminal into contact, moving the carrier away from the die edge, leaving at least a portion of the conductive material in contact with the interconnect terminals.
- 4. The method of claim 2 wherein the carrier surface comprises an electrically insulative material.
- 5. The method of claim 2 wherein the carrier is configured so that the carrier does not span between elements of the patterned conductive material.
- 6. The method of claim 1 wherein the carrier comprises a matrix of filaments.
- 7. The method of claim 1 wherein the carrier surface comprises an electrically insulative material.
- 8. The method of claim 1 wherein the interconnect material comprises an electrically conductive polymer.
- 9. A method for making integrated circuit chip assemblies, comprising: stacking a plurality of die to form a die stack, each die having at east one interconnect edge having interconnect terminals to be interconnected with interconnect terminals on an interconnect edge of at least one other die in the stack, the stack presenting the interconnect edges at an interconnect face; providing a carrier having an electrically conductive material arranged in a pattern on a carrier surface, aligning the carrier with the interconnect face; and moving the carrier toward

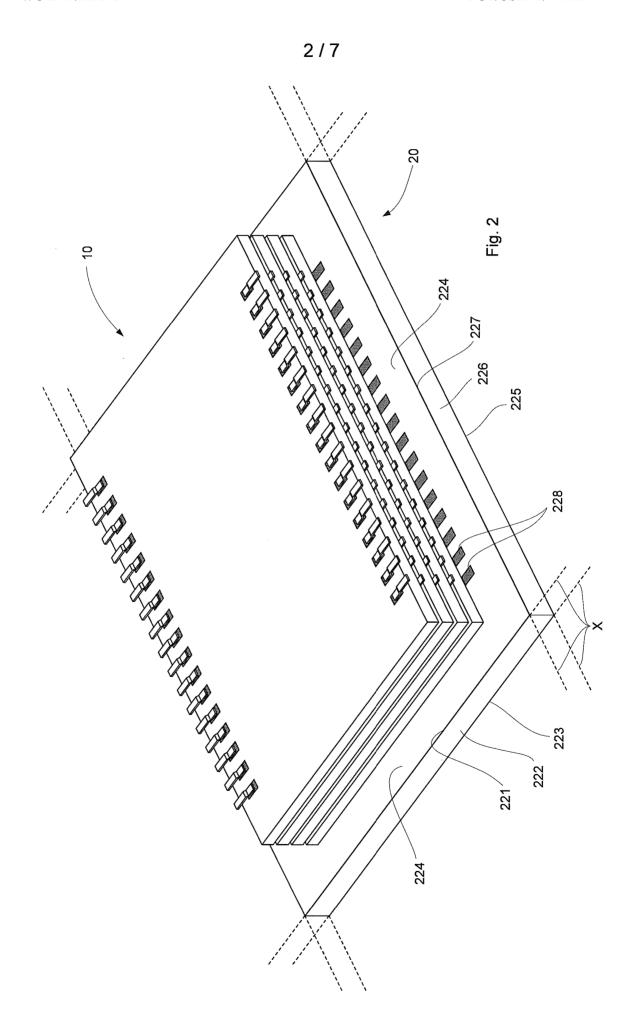
- 12 -

the interconnect face to bring the patterned conductive material on the carrier surface and interconnect terminals on the die into contact.

- 10. The method of claim 9 wherein the carrier is left in place in the interconnection.
- 11. The method of claim 9 further comprising, following bringing the conductive material and the interconnect terminal into contact, moving the carrier away from the die edge, leaving at least a portion of the conductive material in contact with the interconnect terminals.
- 12. The method of claim 10 wherein the carrier surface comprises an electrically insulative material.
- 13. The method of claim 10 wherein the carrier is configured so that the carrier does not span between elements of the patterned conductive material.
- 14. The method of claim 9 wherein the carrier comprises a matrix of filaments.
- 15. The method of claim 9 wherein the carrier surface comprises an electrically insulative material.
- 16. Transfer apparatus for electrical interconnection of a die having an edge to be interconnected, comprising a carrier having an electrically conductive material arranged in a pattern on a carrier surface.
- 17. Transfer apparatus for making an integrated circuit chip assembly, the assembly comprising a plurality of die in a die stack, each die having at east one interconnect edge having interconnect terminals to be interconnected with interconnect terminals on an interconnect edge of at least one other die in the stack, the stack presenting the interconnect edges at an interconnect face, the apparatus comprising a carrier having an electrically conductive material arranged in a pattern on a carrier surface.

1/7







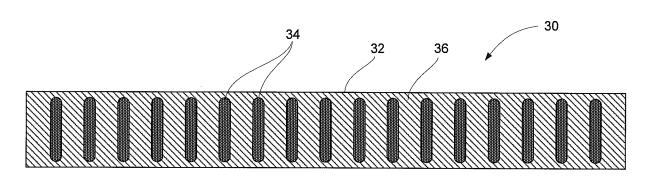


Fig. 3

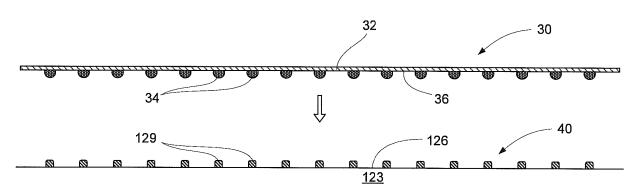
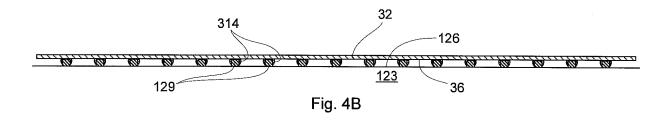


Fig. 4A



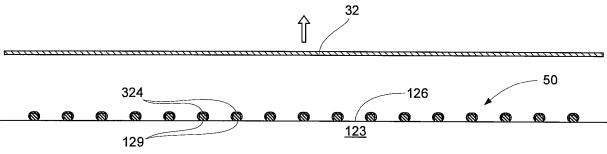
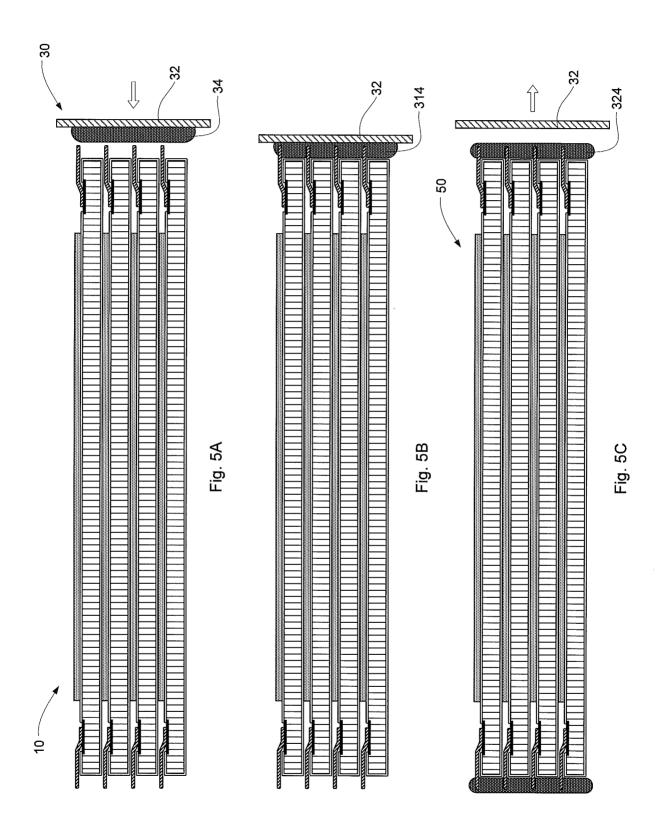
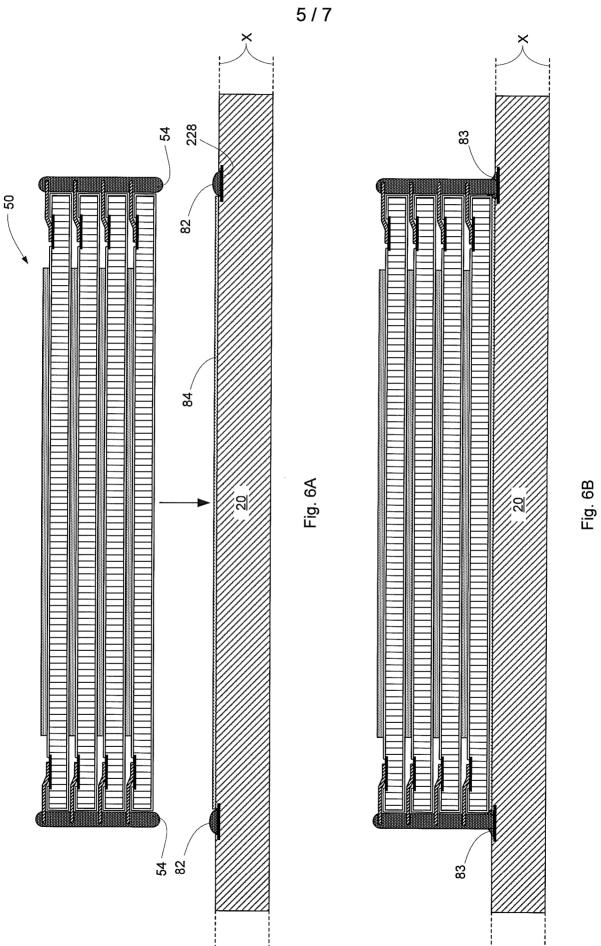


Fig. 4C





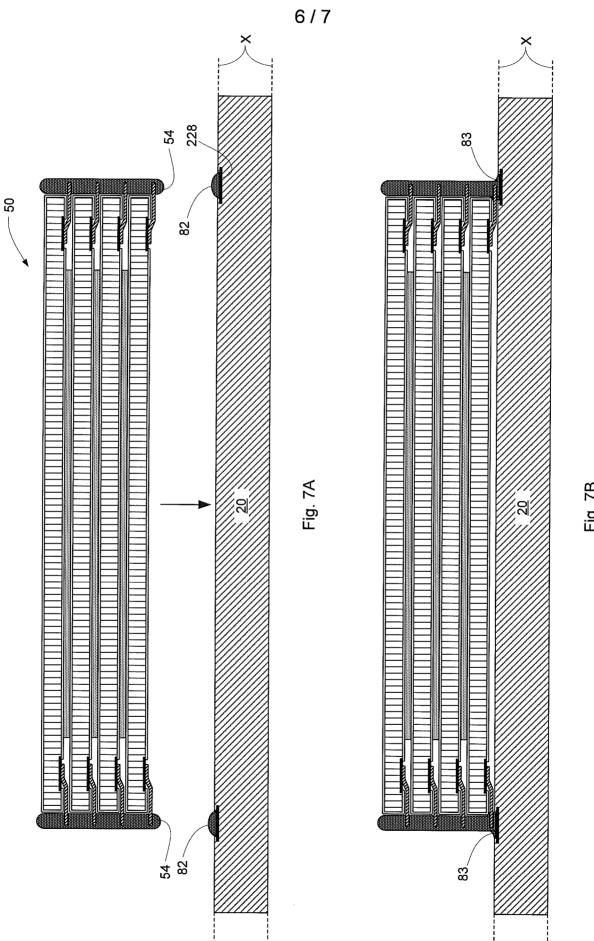


FIG. /B

