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(54) Title: POWER AMPLIFIER HAVING STAGGERED CASCODE LAYOUT FOR ENHANCED THERMAL RUGGEDNESS

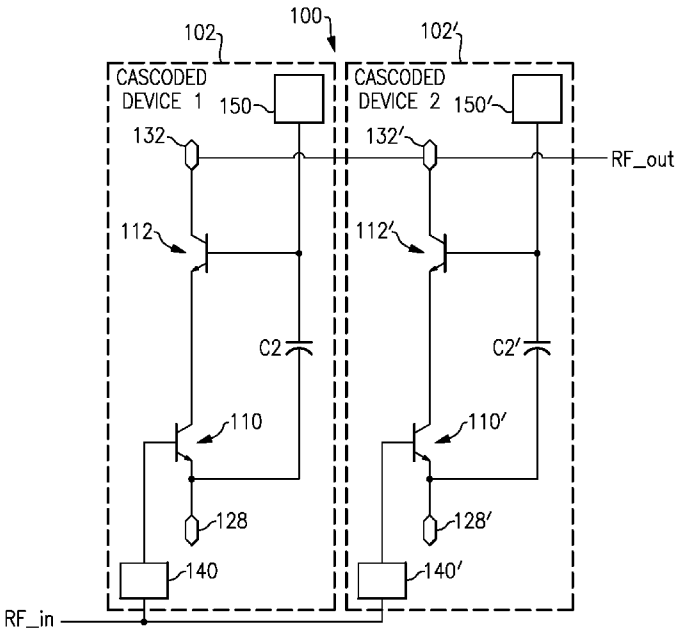

FIG.5

(57) Abstract: Power amplifier having staggered cascode layout for enhanced thermal ruggedness. In some embodiments, a radio-frequency (RF) amplifier such as a power amplifier (PA) can be configured to receive and amplify an RF signal. The PA can include an array of cascoded devices connected electrically parallel between an input node and an output node. Each cascoded device can include a common emitter transistor and a common base transistor arranged in a cascode configuration. The array can be configured such that the common base transistors are positioned in a staggered orientation relative to each other.

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POWER AMPLIFIER HAVING STAGGERED CASCODE LAYOUT FOR ENHANCED THERMAL RUGGEDNESS

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims priority to U.S. Provisional Application No. 62/116,509 filed February 15, 2015, entitled POWER AMPLIFIER HAVING STAGGERED CASCODE LAYOUT FOR ENHANCED THERMAL RUGGEDNESS, and U.S. Provisional Application No. 62/116,508 filed February 15, 2015, entitled CASCODE AMPLIFIER SEGMENTATION FOR ENHANCED THERMAL RUGGEDNESS, the disclosure of each of which is hereby expressly incorporated by reference herein in its entirety.

BACKGROUND

Field

[0002] The present disclosure relates to power amplifiers for radio-frequency (RF) applications.

Description of the Related Art

[0003] In many radio-frequency (RF) applications, an RF signal to be transmitted is typically amplified by a power amplifier. Such a power amplifier can generate heat and/or be affected by heat.

SUMMARY

[0004] According to a number of implementations, the present disclosure relates to a radio-frequency (RF) amplifier that includes an input node and an output node configured to receive an RF signal and provide an amplified RF signal, respectively. The RF amplifier further includes an array of cascoded devices implemented between the input node and the output node to generate the amplified RF signal. Each cascoded device includes a common emitter transistor and a common base transistor arranged in a cascode configuration. The array is configured such that the common base transistors are positioned in a staggered orientation relative to each other.

base transistors can provide an increase in a nearest pair spacing, when compared to a non-staggered orientation. The common base transistor can be configured to handle more power than the common emitter transistor. The increased spacing can result in a smaller rise in temperature due to the operation of the RF amplifier, when compared to the non-staggered orientation. The rise in temperature resulting from the staggered orientation can be less than half of the rise in temperature resulting from the non-staggered orientation.

[0006] In some embodiments, the cascoded devices can be electrically connected in parallel such that each of the input node and the output node is a respective common node for the cascoded devices.

[0007] In some embodiments, the array of cascoded devices can include a plurality of cascoded devices arranged in the staggered orientation in a first row. The plurality of cascoded devices in the first row can be electrically connected in parallel. The plurality of cascoded devices in the first row can be coupled to a common input and a common output.

[0008] In some embodiments, the array of cascoded devices can further include a plurality of cascoded devices arranged in the staggered orientation in a second row. The staggered arrangement of cascoded devices in the first row and the staggered arrangement of cascoded devices in the second row can be offset to avoid direct row-to-row adjacent pair of common base transistors. The plurality of cascoded devices in each row can be coupled to a common input and a common output.

[0009] In some embodiments, each cascoded device can be configured such that a base of the common emitter transistor is coupled to the input node, a collector of the common emitter transistor is coupled to an emitter of the common base transistor, and a collector of the common base transistor is coupled to the output node. A base of the common base transistor can be coupled to an emitter of the common emitter transistor through a bypass capacitance.

[0010] In some embodiments, the RF amplifier can be a power amplifier (PA). In some embodiments, the PA can be configured to operate with a high-voltage supply.

[0011] In some teachings, the present disclosure relates to a semiconductor die that includes a substrate, and a power amplifier (PA)

frequency (RF) signal. The PA includes an array of cascoded devices implemented between an input node and an output node. Each cascoded device includes a common emitter transistor and a common base transistor arranged in a cascode configuration. The array is configured such that the common base transistors are positioned in a staggered orientation relative to each other.

[0012] In a number of implementations, the present disclosure relates to a radio-frequency (RF) module that includes a packaging substrate configured to receive a plurality of components, and a power amplification system implemented on the packaging substrate. The power amplification system includes a power amplifier (PA) configured to receive and amplify a radio-frequency (RF) signal. The PA includes an input node and an output node configured to facilitate the amplification of the RF signal. The PA further includes an array of cascoded devices implemented between the input node and the output node. Each cascoded device includes a common emitter transistor and a common base transistor arranged in a cascode configuration. The array is configured such that the common base transistors are positioned in a staggered orientation relative to each other.

[0013] In some embodiments, the RF module can be a power amplifier module. In some embodiments, the RF module can be a front-end module.

[0014] In accordance with a number of implementations, the present disclosure relates to a wireless device that includes a transceiver configured to generate a radio-frequency (RF) signal, and a front-end module (FEM) in communication with the transceiver. The FEM includes a packaging substrate configured to receive a plurality of components, and a PA configured to amplify the RF signal. The PA includes an input node and an output node configured to facilitate the amplification of the RF signal. The PA further includes an array of cascoded devices implemented between the input node and the output node. Each cascoded device includes a common emitter transistor and a common base transistor arranged in a cascode configuration. The array is configured such that the common base transistors are positioned in a staggered orientation relative to each other. The wireless device further includes an antenna in communication with the FEM. The antenna is configured to transmit the amplified RF signal.

a cellular phone.

[0016] For purposes of summarizing the disclosure, certain aspects, advantages and novel features of the inventions have been described herein. It is to be understood that not necessarily all such advantages may be achieved in accordance with any particular embodiment of the invention. Thus, the invention may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other advantages as may be taught or suggested herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Figure 1 shows a wireless system or architecture that includes an amplification system.

[0018] Figure 2 shows that the amplification system of Figure 1 can include a radio-frequency (RF) amplifier assembly having one or more power amplifiers (PAs).

[0019] Figures 3A-3E show examples of how the PA of Figure 2 can be configured.

[0020] Figure 4 shows that in some embodiments, the amplification system of Figure 2 can be implemented as a high-voltage (HV) power amplification system.

[0021] Figure 5 shows an example of an array of cascoded devices, where each cascoded device includes an RF transistor and a cascode transistor.

[0022] Figure 6 depicts an example of a physical layout of an array, where the orientations of two cascoded devices are the same.

[0023] Figure 7 depicts an example physical layout of an array, where one cascoded device has an inverted orientation relative to an adjacent cascoded device, so as to form a staggered configuration.

[0024] Figure 8 shows that an array can include more than two cascoded devices.

[0025] Figure 9 shows that an array can include more than one row of cascoded devices so as to yield a two-dimensional arrangement.

[0026] Figure 10 shows an example layout that is similar to the block diagram representation of Figure 6.

based on the non-staggered configuration of Figure 6.

[0028] Figure 12 shows another view of the two-dimensional array of Figure 11.

[0029] Figure 13 shows temperature profiles at an example spacing between cascode transistors in the two-dimensional array of Figure 12.

[0030] Figure 14 shows an example layout that is similar to the block diagram representation of Figure 7.

[0031] Figure 15 shows an example of a two-dimensional array that is based on the staggered configuration of Figure 7.

[0032] Figure 16 shows another view of the two-dimensional array of Figure 15.

[0033] Figure 17 shows temperature profiles at an example spacing between cascode transistors in the two-dimensional array of Figure 16.

[0034] Figure 18 shows a comparison of areas associated with non-staggered and staggered arrays.

[0035] Figure 19 shows that in some embodiments, some or all of a PA array having one or more features as described herein can be implemented in a module.

[0036] Figure 20 depicts an example wireless device having one or more advantageous features described herein.

DETAILED DESCRIPTION OF SOME EMBODIMENTS

[0037] The headings provided herein, if any, are for convenience only and do not necessarily affect the scope or meaning of the claimed invention.

[0038] Referring to Figure 1, one or more features of the present disclosure generally relate to a wireless system or architecture 50 having an amplification system 52. In some embodiments, the amplification system 52 can be implemented as one or more devices, and such device(s) can be utilized in the wireless system/architecture 50. In some embodiments, the wireless system/architecture 50 can be implemented in, for example, a portable wireless device. Examples of such a wireless device are described herein.

typically includes a radio-frequency (RF) amplifier assembly 54 having one or more power amplifiers (PAs). In the example of Figure 2, three PAs 60a-60c are depicted as forming the RF amplifier assembly 54. It will be understood that other numbers of PA(s) can also be implemented. It will also be understood that one or more features of the present disclosure can also be implemented in RF amplifier assemblies having other types of RF amplifiers.

[0040] In some embodiments, the RF amplifier assembly 54 can be implemented on one or more semiconductor die, and such die can be included in a packaged module such as a power amplifier module (PAM) or a front-end module (FEM). Such a packaged module is typically mounted on a circuit board associated with, for example, a portable wireless device.

[0041] The PAs (e.g., 60a-60c) in the amplification system 52 are typically biased by a bias system 56. Further, supply voltages for the PAs are typically provided by a supply system 58. In some embodiments, either or both of the bias system 56 and the supply system 58 can be included in the foregoing packaged module having the RF amplifier assembly 54.

[0042] In some embodiments, the amplification system 52 can include a matching network 62. Such a matching network can be configured to provide input matching and/or output matching functionalities for the RF amplifier assembly 54.

[0043] For the purpose of description, it will be understood that each PA (60) of Figure 2 can be implemented in a number of ways. Figures 3A-3E show non-limiting examples of how such a PA can be configured. Figure 3A shows an example PA having an amplifying transistor 64, where an input RF signal (RF_in) is provided to a base of the transistor 64, and an amplified RF signal (RF_out) is output through a collector of the transistor 64.

[0044] Figure 3B shows an example PA having a plurality of amplifying transistors (e.g., 64a, 64b) arranged in stages. An input RF signal (RF_in) is provided to a base of the first transistor 64a, and an amplified RF signal from the first transistor 64a is output through its collector. The amplified RF signal from the first transistor 64a is provided to a base of the second transistor 64b, and an amplified RF signal from the second transistor 64b is output through its collector to thereby yield an output RF signal (RF_out) of the PA.

of Figure 3B can be depicted as two or more stages as shown in Figure 3C. The first stage 64a can be configured as, for example, a driver stage; and the second stage 64b can be configured as, for example, an output stage.

[0046] Figure 3D shows that in some embodiments, a PA can be configured as a Doherty PA. Such a Doherty PA can include amplifying transistors 64a, 64b configured to provide carrier amplification and peaking amplification of an input RF signal (RF_in) to yield an amplified output RF signal (RF_out). The input RF signal can be split into the carrier portion and the peaking portion by a splitter. The amplified carrier and peaking signals can be combined to yield the output RF signal by a combiner.

[0047] Figure 3E shows that in some embodiments, a PA can be implemented in a cascode configuration. An input RF signal (RF_in) can be provided to a base of the first amplifying transistor 64a operated as a common emitter device. The output of the first amplifying transistor 64a can be provided through its collector and be provided to an emitter of the second amplifying transistor 64b operated as a common base device. The output of the second amplifying transistor 64b can be provided through its collector so as to yield an amplified output RF signal (RF_out) of the PA.

[0048] In the various examples of Figures 3A-3E, the amplifying transistors are described as bipolar junction transistors (BJTs) such as heterojunction bipolar transistors (HBTs). It will be understood that one or more features of the present disclosure can also be implemented in or with other types of transistors such as field-effect transistors (FETs).

[0049] Figure 4 shows that in some embodiments, the amplification system 52 of Figure 2 can be implemented as a high-voltage (HV) power amplification system 70. Such a system can include an HV power amplifier assembly 54 configured to include HV amplification operation of some or all of the PAs (e.g., 60a-60c). As described herein, such PAs can be biased by a bias system 56. In some embodiments, the foregoing HV amplification operation can be facilitated by an HV supply system 58. In some embodiments, an interface system 72 can be implemented to provide interface functionalities between the HV power amplifier assembly 54 and either or both of the bias system 56 and the HV supply system 58.

arrays, such as power amplifier (PA) arrays, typically requires sufficient spacing of adjacent elements for ruggedness and device reliability. Such spacing typically requires larger die size which in turn results in higher cost implementations.

[0051] Described herein are examples related to reduction of die temperatures without necessarily requiring an increase in die size. Such an advantageous feature can be achieved by selected placement of high thermal dissipation devices within a given array. In the context of a cascode PA array, it is noted that such an array typically includes lower temperature RF devices (also referred to herein as common emitter (CE) devices) and higher temperature cascode devices (also referred to herein as common base (CB) devices). Thus, a stagger arrangement of the RF and cascode transistors can be implemented such that one high temperature device is not directly adjacent to another high temperature device.

[0052] Figure 5 shows an example of an array 100 of cascoded devices, where each cascoded device 102 includes an RF transistor 110 (also referred to herein as a CE device) and a cascode transistor 112 (also referred to herein as a CB device). Among others, examples of how such an array can be implemented are described in U.S. Provisional Application No. 62/116,508 filed February 15, 2015, entitled CASCODE AMPLIFIER SEGMENTATION FOR ENHANCED THERMAL RUGGEDNESS, the disclosure of which is hereby expressly incorporated by reference herein in its entirety.

[0053] In the example of Figure 5, the array 100 is shown to include two cascoded devices 102, 102'. It will be understood that more than two cascoded devices can be arranged in a similar manner.

[0054] Referring to Figure 5, each of the cascoded device (102 or 102') is shown to include a common emitter (CE) device (110 or 110') (also referred to herein as an RF transistor) coupled to a common base (CB) device (112 or 112') (also referred to herein as a cascode transistor). The emitter of the RF transistor (110 or 110') is shown to be coupled to the base of the cascode transistor (112 or 112') through a cascode bypass capacitance (C2 or C2'). The emitter of the RF transistor (110 or 110') can be coupled to ground (128 or 128').

include its own bias circuits for the RF transistor and the cascode transistor. More particularly, the RF transistor 110 of the first cascoded device 102 is shown to have a input bias circuit 140 coupled to its base, and the cascode transistor 112 is shown to have a cascode bias circuit 150 coupled to its base. Similarly, the RF transistor 110' of the second cascoded device 102' is shown to have an input bias circuit 140' coupled to its base, and the cascode transistor 112' is shown to have a cascode bias circuit 150' coupled to its base.

[0056] In the example of Figure 5, at least some portions of the input bias circuits 140, 140' can be coupled to facilitate, for example, a common RF input (RF_in). Similarly, the collectors 132, 132' of the cascode transistors 112, 112' can be coupled to yield a common RF output (RF_out), and to receive a common supply voltage.

[0057] In some embodiments, the array of cascoded devices of Figure 5 can be implemented so as to yield isolated connections between the parallel elements. For example, the array can be built with a plurality of CE (110)/CB (112) pairs, instead of building a separate CE array and a separate CB array.

[0058] Figure 6 depicts an example of a physical layout of an array 100, where the orientations of two cascoded devices are the same. Accordingly, the cascode transistors 112 of the two adjacent cascoded devices are shown to be directly adjacent to each other. The example physical layout of Figure 6 can represent the example of Figure 5, if the two cascoded devices 102, 102' are physically laid out as shown in the circuit representation.

[0059] Figure 7 depicts an example physical layout of an array 100, where one cascoded device has an inverted orientation relative to an adjacent cascoded device, so as to form a staggered configuration. Accordingly, the cascode transistor 112 of one cascoded device (e.g., upper portion of the cascoded device on the left) is at a diagonal orientation relative to the cascode transistor 112 of the adjacent cascoded device (e.g., lower portion of the cascoded device on the right). It is noted that the distance between such diagonally arranged cascode transistors 112 is greater than the distance between the directly adjacent cascode transistors 112 of Figure 6, if all other dimensions remain generally the same.

cascoded devices. Such cascoded devices can be arranged as a continuation of the staggered configuration of the example of Figure 7. Accordingly, it is noted that each cascode transistor 112 is at a diagonal arrangement relative to another cascode transistor 112 of an adjacent cascoded device.

[0061] In the foregoing example of Figure 8, one row of cascoded devices are shown. Figure 9 shows that an array 100 can include more than one row of cascoded devices so as to yield a two-dimensional arrangement. In such a two-dimensional arrangement, a given row (e.g., such as the row of Figure 8) can have an offset arrangement with an adjacent row, such that between such two rows, there is no direct row-to-row adjacent pair of cascode transistors 112.

[0062] Figure 10 shows an example layout that is similar to the block diagram representation of Figure 6. Figures 11 and 12 show an example of a two-dimensional array that is based on the non-staggered configuration of Figure 6. Figure 14 shows an example layout that is similar to the block diagram representation of Figure 7, in which the cascode transistors are in a staggered configuration. Figures 15 and 16 show an example of a two-dimensional array that is based on the staggered configuration of Figure 7. In the examples shown, various values such as dimensions are shown. It will be understood that such values are examples, and that other values can be utilized.

[0063] For the purpose of comparing the foregoing non-staggered and staggered configurations, it will be understood that dimensions associated with a given cascoded device (whether in non-staggered or staggered arrangement) generally remain the same. For example, each RF transistor has an area of approximately 40 μm^2, each cascode transistor has a much larger area of approximately 160 μm^2, and the center-to-center spacing between two directly adjacent cascode transistors is approximately 55 μm.

[0064] As stated above, two cascode transistors are spaced at approximately 55 μm when in a direct adjacent configuration (e.g., see Figure 10). When in a diagonal configuration resulting from a staggered configuration, center-to-center spacing between the cascode transistors of two adjacent cascode devices is approximately 100 μm (e.g., see Figure 14) which is almost twice the 55 μm separation.

(having the staggered and row-offset configuration) is expected to have better thermal dissipation property than the two-dimensional array of Figures 11 and 12 (having the direct adjacent configuration within a given row). Figures 13 (direct adjacent configuration) and 17 (staggered and row-offset configuration) show that such is indeed true. Compared to about 4 degree C rise in temperature (Figure 13) due to the 55 μm spacing of the direct adjacent configuration, the staggered and row-offset configuration yields a temperature rise that is less than 2 degree C (Figure 17) due to the 100 μm spacing.

[0066] Referring to Figures 11 (direct adjacent configuration) and 15 (staggered and row-offset configuration), one can see that the latter configuration can yield narrower but taller dimensions compared to the former configuration. In some embodiments, such narrower dimension can be allowed due to the stagger configuration in which two cascoded devices can be brought closer together without the cascode transistors becoming too close. In some embodiments, such taller dimension can facilitate RF signal input and biasing connections associated with the row-offset configuration.

[0067] Figure 18 shows a comparison of areas of the two foregoing example arrays, as well as an array of common emitters. One can see that the staggered cascode array on the left has an overall area that is similar to the area of the non-staggered array in the center.

[0068] For the purpose of description, it will be understood that an array can include a plurality of units (e.g., cascoded devices) arranged in one or more rows and/or columns. Thus, an array can include a plurality of units arranged in a single row, such as in the examples of Figures 7, 8 and 14. An array can also include a plurality of units arranged in a plurality of rows, such as in the examples of Figures 9, 15 and 16.

[0069] It will also be understood that in an array of cascoded devices, each cascoded device can have a separate input and a separate output for an RF signal, a common input and a common output for each of a plurality of groups of cascoded devices, a common input and a common output for all of the cascoded devices in the array, or any combination thereof. For example, in the example of Figure 15, each row of three cascoded devices can be arranged in an electrically parallel manner, sharing a common input and a common output for an

cascoded devices can provide three separate amplification paths.

[0070] In some embodiments, an array of cascoded devices having one or more features as described herein can be implemented on a semiconductor die. For example, the array of cascoded devices of Figures 15 and 16 can be implemented on a single semiconductor die.

[0071] Figure 19 shows that in some embodiments, one or more features associated with a cascode architecture as described herein (e.g., array 100 in Figures 7-9 and 14-16) can be implemented in a module. Such a module can be, for example, a front-end module (FEM). In the example of Figure 19, a module 300 can include a packaging substrate 302, and a number of components can be mounted on such a packaging substrate. For example, an FE-PMIC component 304, a power amplifier assembly 306, a match component 308, and a duplexer assembly 310 can be mounted and/or implemented on and/or within the packaging substrate 302. Other components such as a number of SMT devices 314 and an antenna switch module (ASM) 312 can also be mounted on the packaging substrate 302. Although all of the various components are depicted as being laid out on the packaging substrate 302, it will be understood that some component(s) can be implemented over other component(s).

[0072] In some implementations, a device and/or a circuit having one or more features described herein can be included in an RF device such as a wireless device. Such a device and/or a circuit can be implemented directly in the wireless device, in a modular form as described herein, or in some combination thereof. In some embodiments, such a wireless device can include, for example, a cellular phone, a smart-phone, a hand-held wireless device with or without phone functionality, a wireless tablet, etc.

[0073] Figure 20 depicts an example wireless device 400 having one or more advantageous features described herein. In the context of a module having one or more features as described herein, such a module can be generally depicted by a dashed box 300, and can be implemented as, for example, a front-end module (FEM). Such a module can include an array 100 of cascoded devices as described herein.

their respective RF signals from a transceiver 410 that can be configured and operated in known manners to generate RF signals to be amplified and transmitted, and to process received signals. The transceiver 410 is shown to interact with a baseband sub-system 408 that is configured to provide conversion between data and/or voice signals suitable for a user and RF signals suitable for the transceiver 410. The transceiver 410 can also be in communication with a power management component 406 that is configured to manage power for the operation of the wireless device 400. Such power management can also control operations of the baseband sub-system 408 and the module 300.

[0075] The baseband sub-system 408 is shown to be connected to a user interface 402 to facilitate various input and output of voice and/or data provided to and received from the user. The baseband sub-system 408 can also be connected to a memory 404 that is configured to store data and/or instructions to facilitate the operation of the wireless device, and/or to provide storage of information for the user.

[0076] In the example wireless device 400, outputs of the PAs 420 are shown to be matched (via respective match circuits 422) and routed to their respective duplexers 420. Such amplified and filtered signals can be routed to an antenna 416 through an antenna switch 414 for transmission. In some embodiments, the duplexers 420 can allow transmit and receive operations to be performed simultaneously using a common antenna (e.g., 416). In Figure 20, received signals are shown to be routed to "Rx" paths that can include, for example, a low-noise amplifier (LNA).

[0077] A number of other wireless device configurations can utilize one or more features described herein. For example, a wireless device does not need to be a multi-band device. In another example, a wireless device can include additional antennas such as diversity antenna, and additional connectivity features such as Wi-Fi, Bluetooth, and GPS.

[0078] Unless the context clearly requires otherwise, throughout the description and the claims, the words “comprise,” “comprising,” and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of “including, but not limited to.” The word

either directly connected, or connected by way of one or more intermediate elements. Additionally, the words “herein,” “above,” “below,” and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Description using the singular or plural number may also include the plural or singular number respectively. The word “or” in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0079] The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

[0080] The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

[0081] While some embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are

spirit of the disclosure.

1. A radio-frequency (RF) amplifier comprising:

an input node and an output node configured to receive an RF signal and provide an amplified RF signal, respectively; and

an array of cascoded devices implemented between the input node and the output node to generate the amplified RF signal, each cascoded device including a common emitter transistor and a common base transistor arranged in a cascode configuration, the array configured such that the common base transistors are positioned in a staggered orientation relative to each other.

2. The RF amplifier of claim 1 wherein the staggered orientation of the common base transistors provide an increase in a nearest pair spacing, when compared to a non-staggered orientation.

3. The RF amplifier of claim 2 wherein the common base transistor is configured to handle more power than the common emitter transistor.

4. The RF amplifier of claim 3 wherein the increased spacing results in a smaller rise in temperature due to the operation of the RF amplifier, when compared to the non-staggered orientation.

5. The RF amplifier of claim 4 wherein the rise in temperature resulting from the staggered orientation is less than half of the rise in temperature resulting from the non-staggered orientation.

6. The RF amplifier of claim 1 wherein the cascoded devices are electrically connected in parallel such that each of the input node and the output node is a respective common node for the cascoded devices.

includes a plurality of cascoded devices arranged in the staggered orientation in a first row.

8. The RF amplifier of claim 7 wherein the plurality of cascoded devices in the first row are electrically connected in parallel.

9. The RF amplifier of claim 8 wherein the plurality of cascoded devices in the first row are coupled to a common input and a common output.

10. The RF amplifier of claim 7 wherein the array of cascoded devices further includes a plurality of cascoded devices arranged in the staggered orientation in a second row.

11. The RF amplifier of claim 10 wherein the staggered arrangement of cascoded devices in the first row and the staggered arrangement of cascoded devices in the second row are offset to avoid direct row-to-row adjacent pair of common base transistors.

12. The RF amplifier of claim 11 wherein the plurality of cascoded devices in each row are coupled to a common input and a common output.

13. The RF amplifier of claim 1 wherein each cascoded device is configured such that a base of the common emitter transistor is coupled to the input node, a collector of the common emitter transistor is coupled to an emitter of the common base transistor, and a collector of the common base transistor is coupled to the output node.

14. The RF amplifier of claim 13 wherein a base of the common base transistor is coupled to an emitter of the common emitter transistor through a bypass capacitance.

15. The RF amplifier of claim 1 wherein the RF amplifier is a power amplifier (PA).

16. The RF amplifier of claim 15 wherein the PA is configured to operate with a high-voltage supply.

17. A semiconductor die comprising:

a substrate; and

a power amplifier (PA) implemented on the substrate and configured to receive and amplify a radio-frequency (RF) signal, the PA including an array of cascoded devices implemented between an input node and an output node, each cascoded device including a common emitter transistor and a common base transistor arranged in a cascode configuration, the array configured such that the common base transistors are positioned in a staggered orientation relative to each other.

18. A radio-frequency (RF) module comprising:

a packaging substrate configured to receive a plurality of components; and

a power amplification system implemented on the packaging substrate, the power amplification system including a power amplifier (PA) configured to receive and amplify a radio-frequency (RF) signal, the PA including an input node and an output node configured to facilitate the amplification of the RF signal, the PA further including an array of cascoded devices implemented between the input node and the output node, each cascoded device including a common emitter transistor and a common base transistor arranged in a cascode configuration, the array configured such that the common base transistors are positioned in a staggered orientation relative to each other.

19. The RF module of claim 18 wherein the RF module is a power amplifier module.

20. The RF module of claim 18 wherein the RF module is a front-end module.

a transceiver configured to generate a radio-frequency (RF) signal;

a front-end module (FEM) in communication with the transceiver, the FEM including a packaging substrate configured to receive a plurality of components, the FEM further including a PA configured to amplify the RF signal, the PA including an input node and an output node configured to facilitate the amplification of the RF signal, the PA further including an array of cascoded devices implemented between the input node and the output node, each cascoded device including a common emitter transistor and a common base transistor arranged in a cascode configuration, the array configured such that the common base transistors are positioned in a staggered orientation relative to each other; and

an antenna in communication with the FEM, the antenna configured to transmit the amplified RF signal.

22. The wireless device of claim 21 wherein the wireless device is a cellular phone.

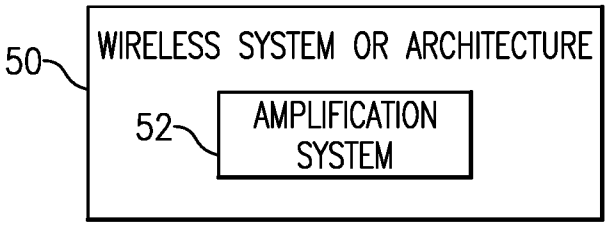


FIG.1

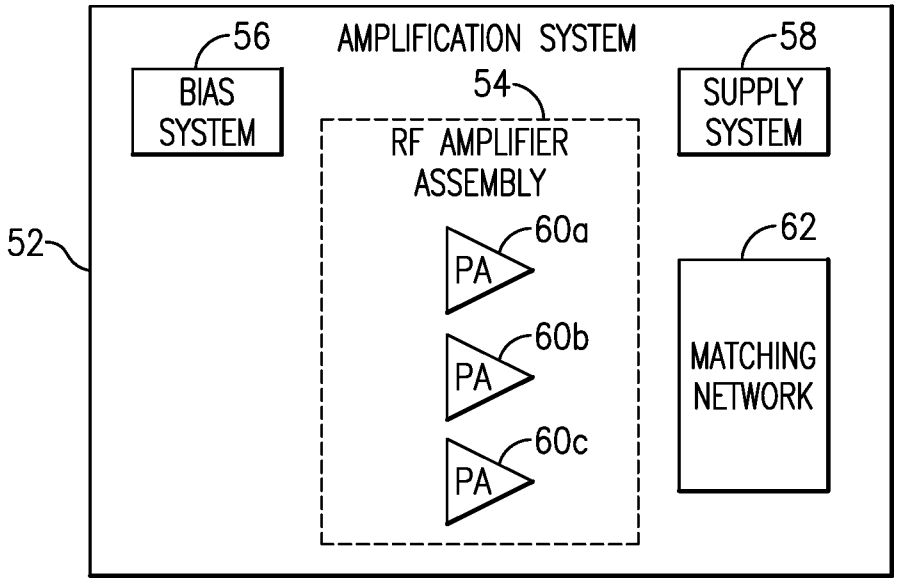


FIG.2

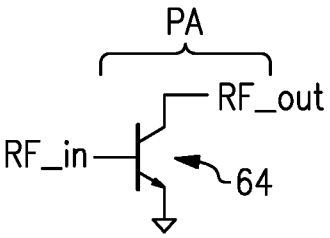


FIG.3A

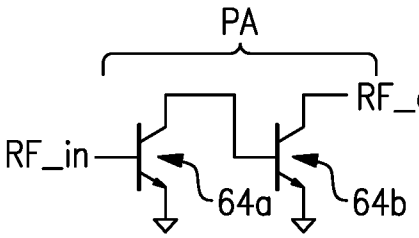


FIG.3B

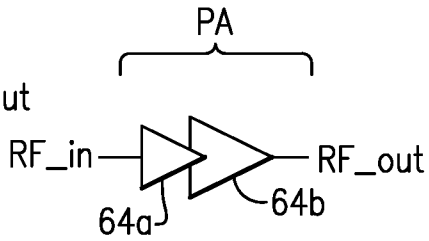


FIG.3C

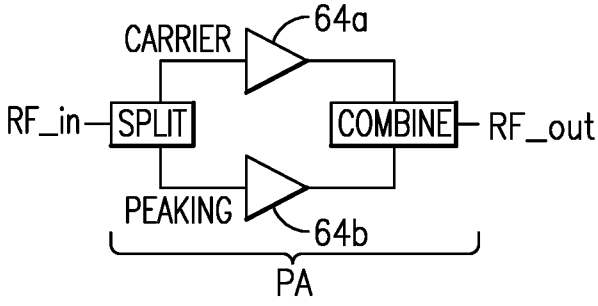


FIG.3D

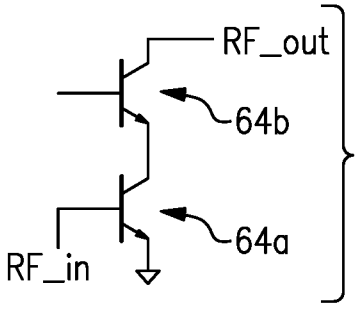


FIG.3E

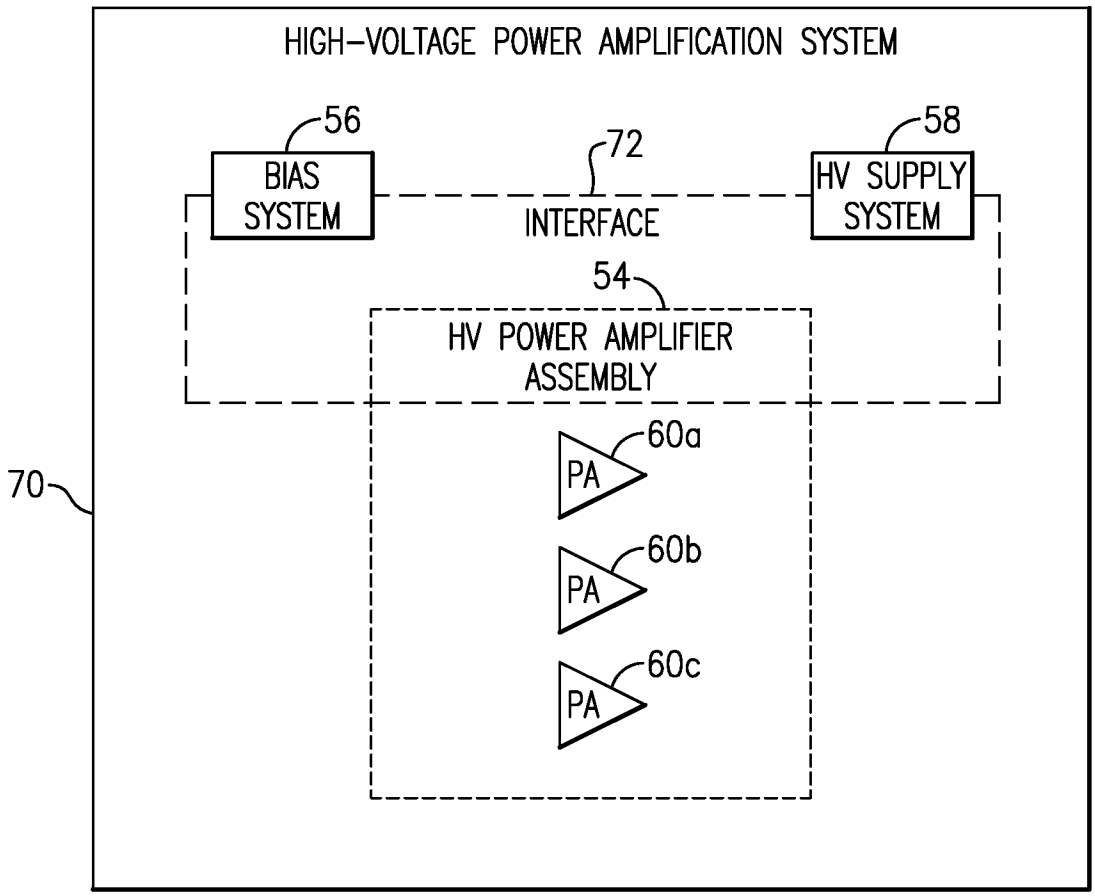

HIGH-VOLTAGE POWER AMPLIFICATION SYSTEM
56
BIAS SYSTEM
72
INTERFACE
58
HV SUPPLY SYSTEM
54
HV POWER AMPLIFIER ASSEMBLY
60a
PA
60b
PA
60c
PA
70

FIG.4

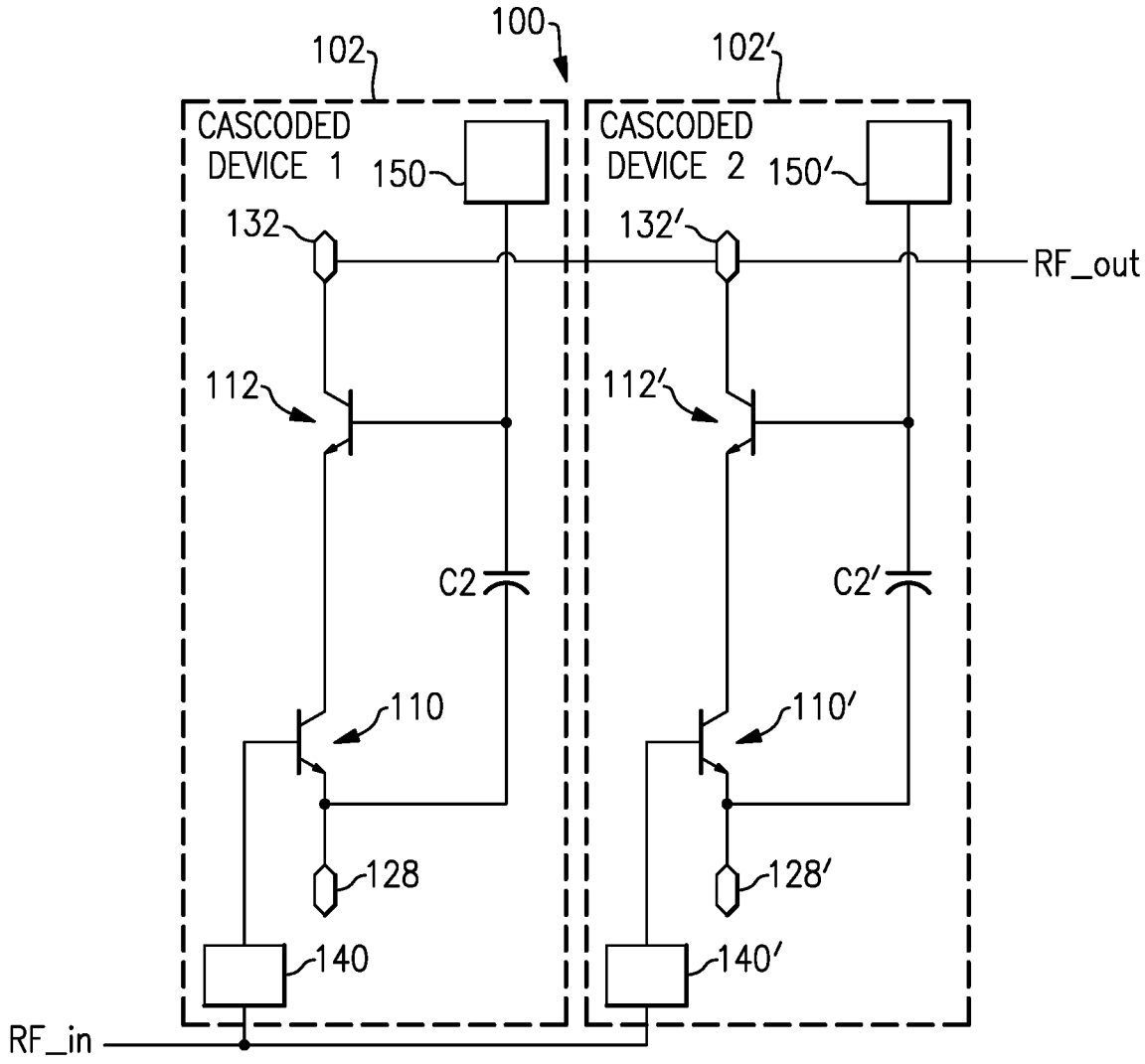

100
102
102′
CASCODED DEVICE 1
CASCODED DEVICE 2
150
150′
132
132′
RF_out
112
112′
C2
C2′
110
110′
128
128′
140
140′
RF_in

FIG.5

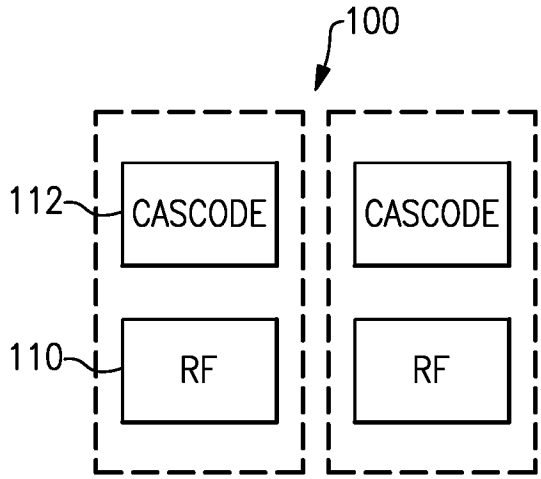


FIG.6

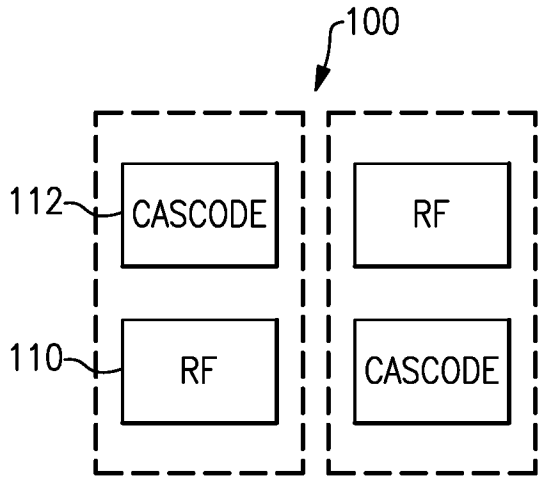


FIG.7

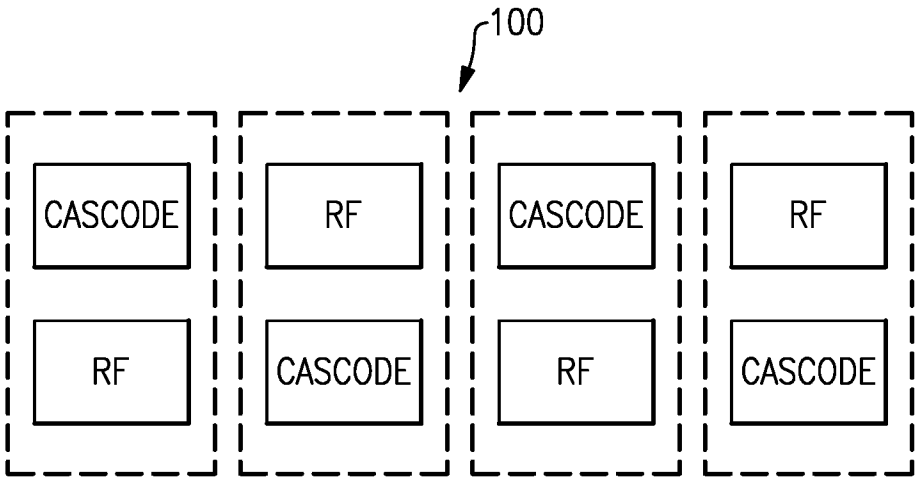


FIG.8

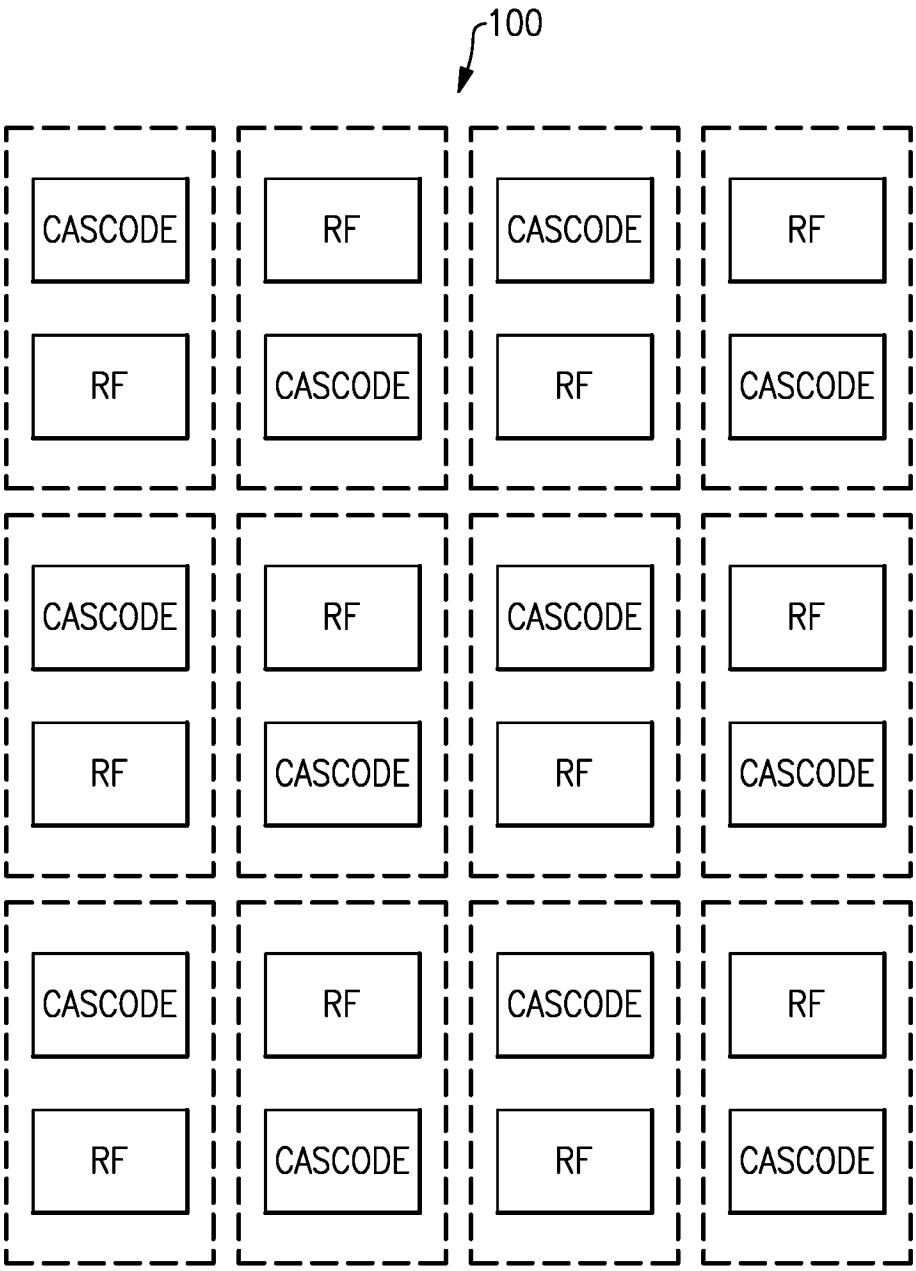

100
CASCODE
RF
CASCODE
RF
CASCODE
RF
CASCODE
RF
CASCODE
RF
CASCODE
RF
CASCODE
RF
CASCODE
RF
CASCODE
RF
CASCODE
RF
CASCODE
RF
CASCODE
RF
CASCODE

FIG.9

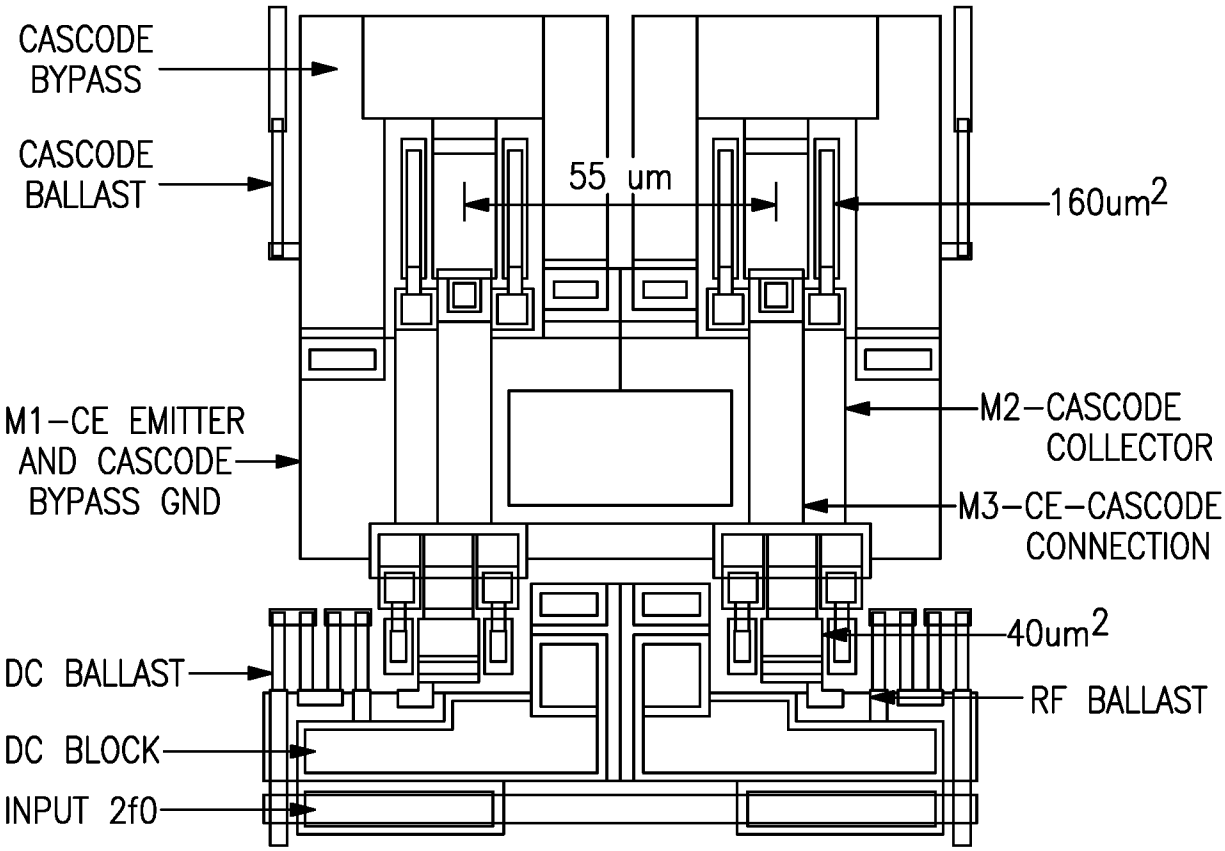

CASCODE BYPASS
CASCODE BALLAST
55 um
160um2
M1–CE EMITTER AND CASCODE BYPASS GND
M2–CASCODE COLLECTOR
M3–CE–CASCODE CONNECTION
40um2
DC BALLAST
RF BALLAST
DC BLOCK
INPUT 2f0

FIG.10

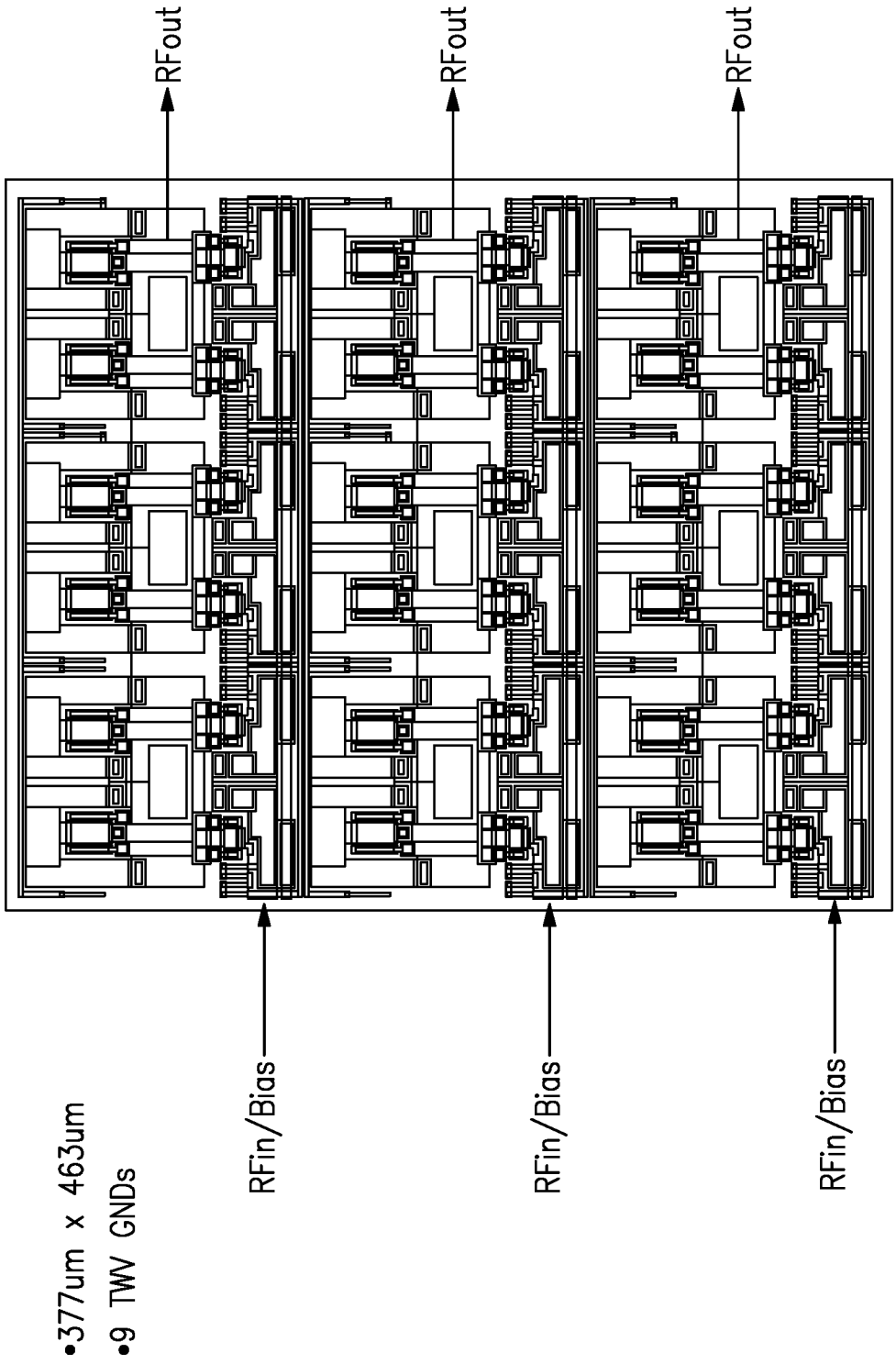

RFout
RFout
RFout
RFin/Bias
RFin/Bias
RFin/Bias
•377um x 463um
•9 TWV GNDs

FIG.11

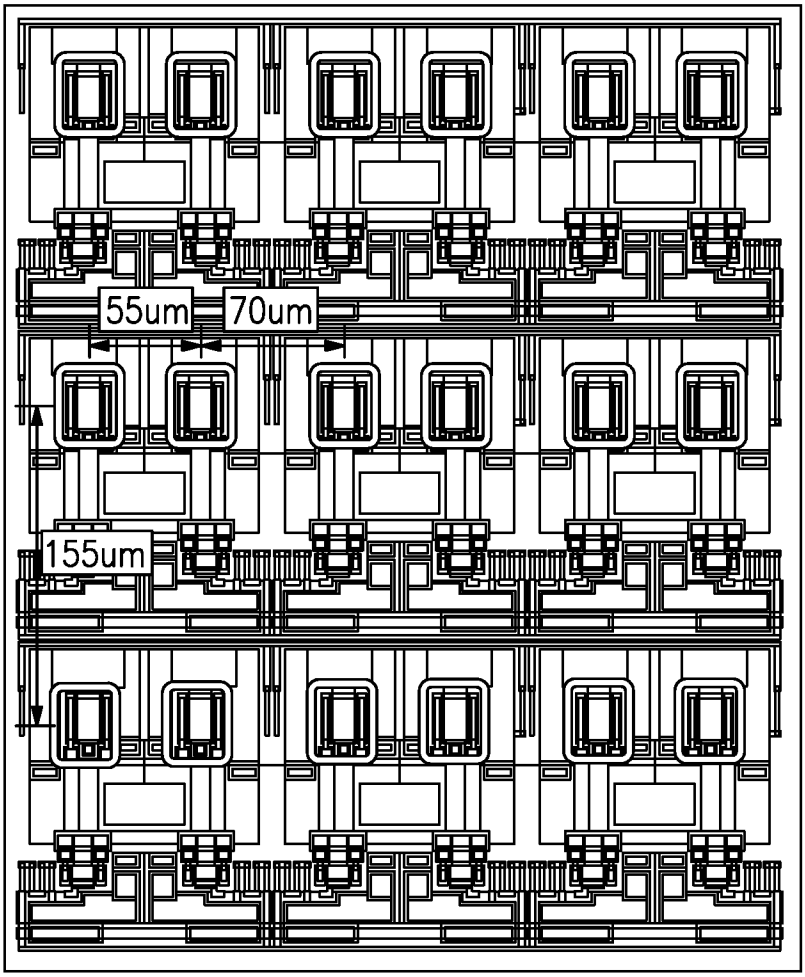

55um
70um
155um

FIG.12

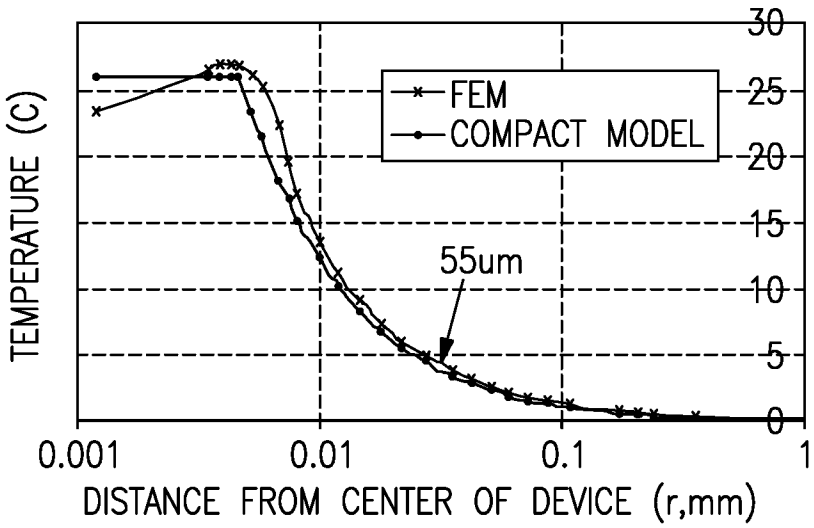

TEMPERATURE (C)
30
25
20
15
10
5
0
FEM
COMPACT MODEL
55um
0.001
0.01
0.1
1
DISTANCE FROM CENTER OF DEVICE (r,mm)

FIG.13

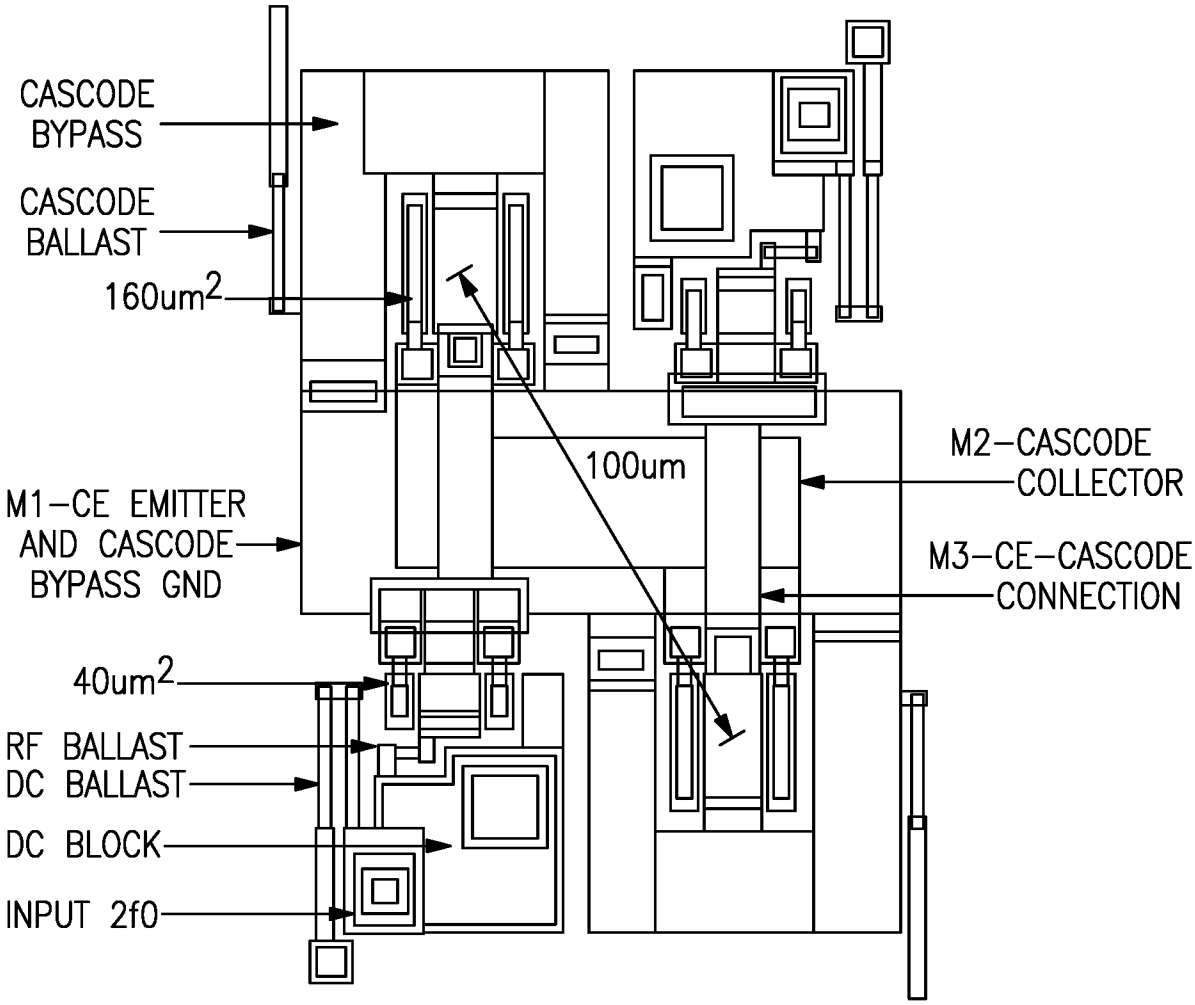

CASCODE BYPASS
CASCODE BALLAST
160um2
100um
M2–CASCODE COLLECTOR
M1–CE EMITTER AND CASCODE BYPASS GND
M3–CE–CASCODE CONNECTION
40um2
RF BALLAST
DC BALLAST
DC BLOCK
INPUT 2f0

FIG.14

- 327um X 533um
- 9 TWV GNDs

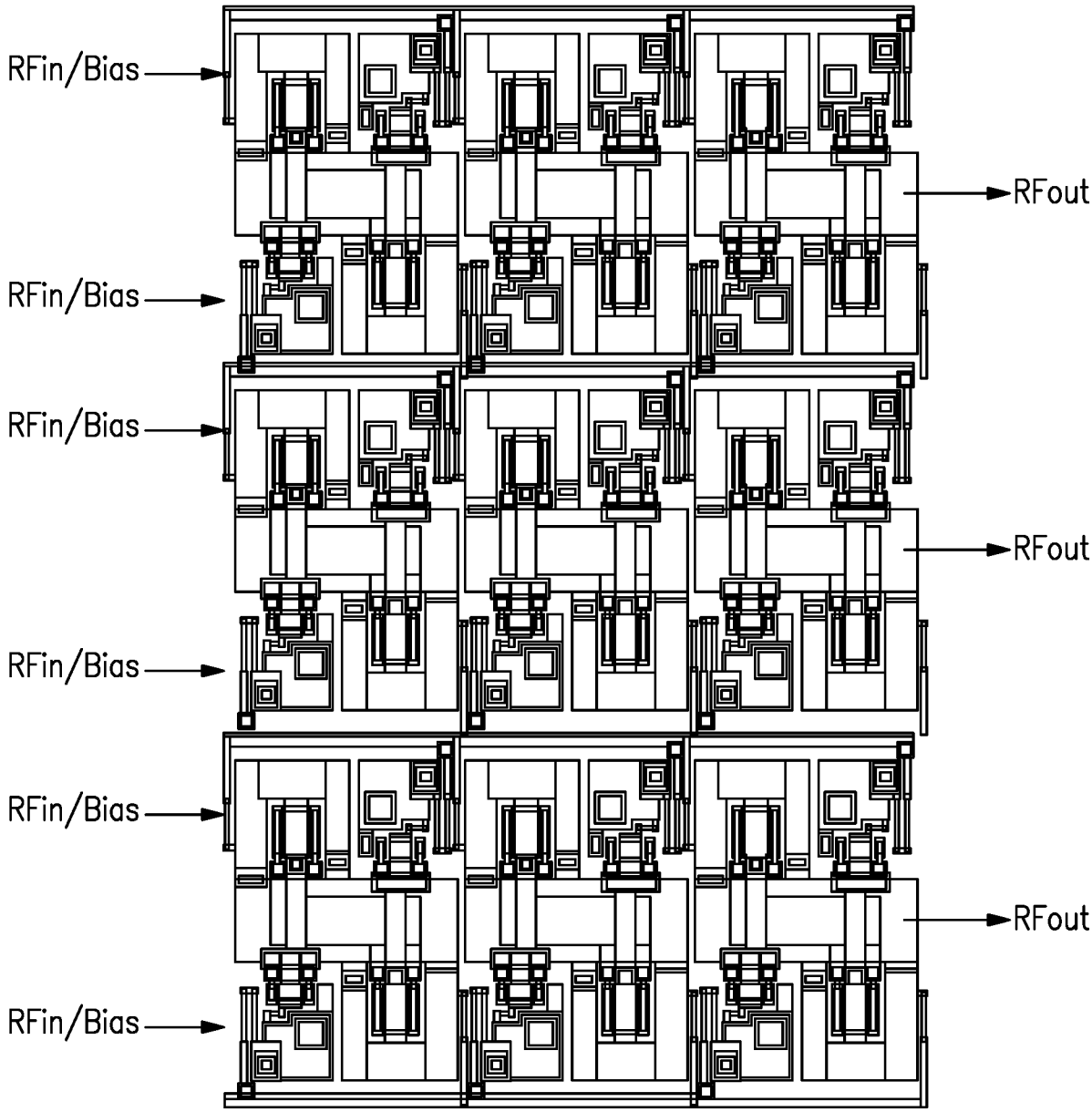


FIG.15

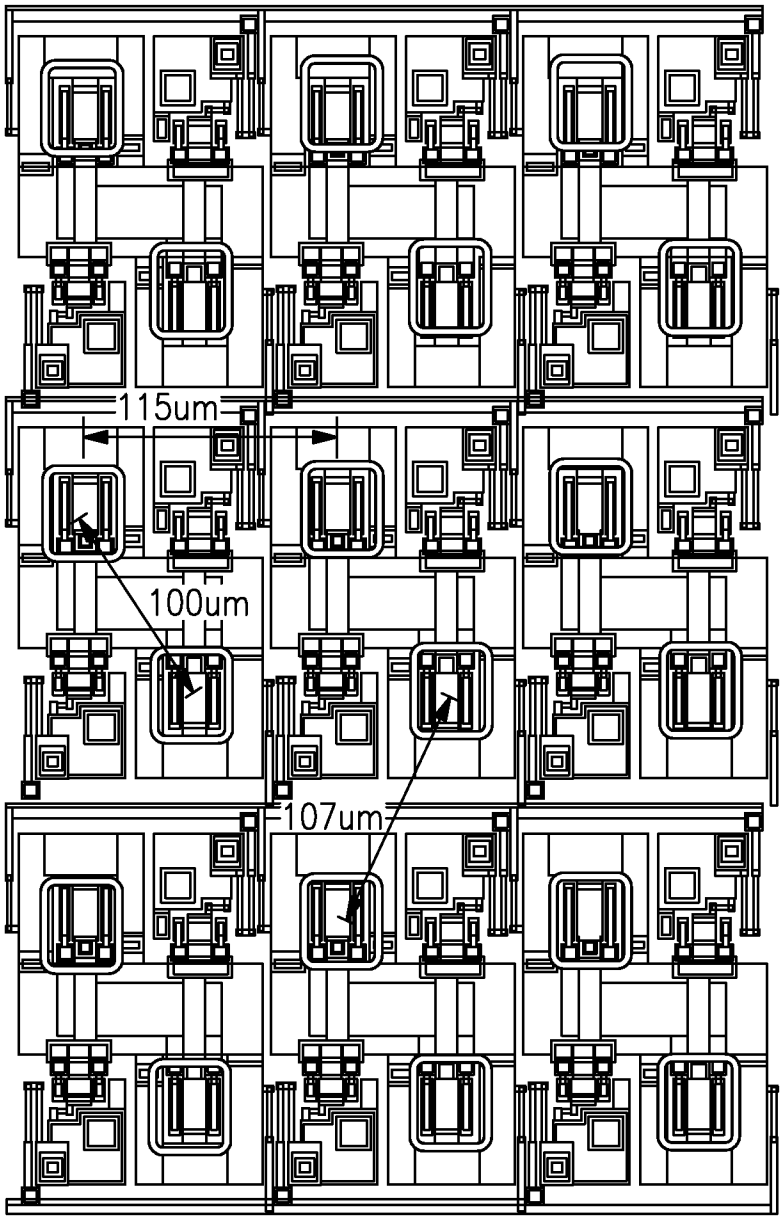

115um
100um
107um

FIG.16

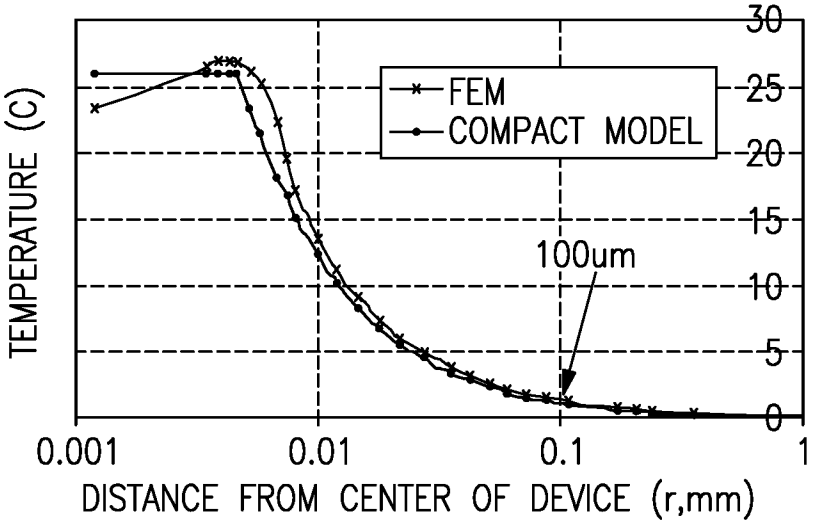
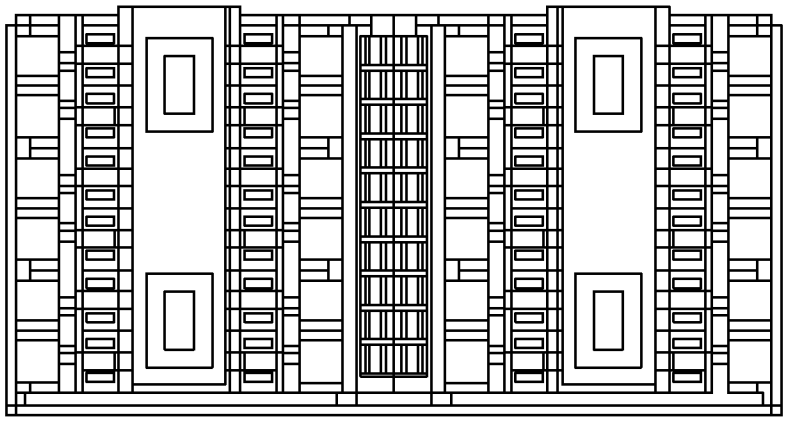
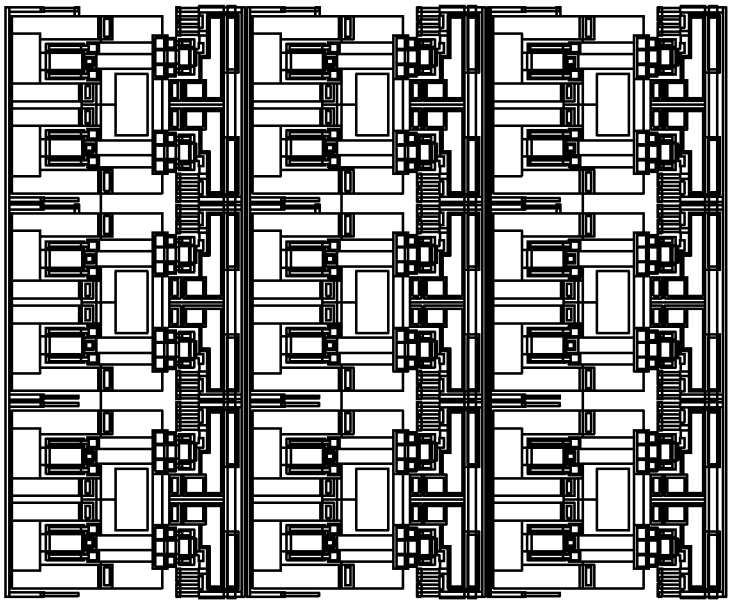

TEMPERATURE (C)
30
25
20
15
10
5
0
FEM
COMPACT MODEL
100um
0.001
0.01
0.1
1
DISTANCE FROM CENTER OF DEVICE (r,mm)

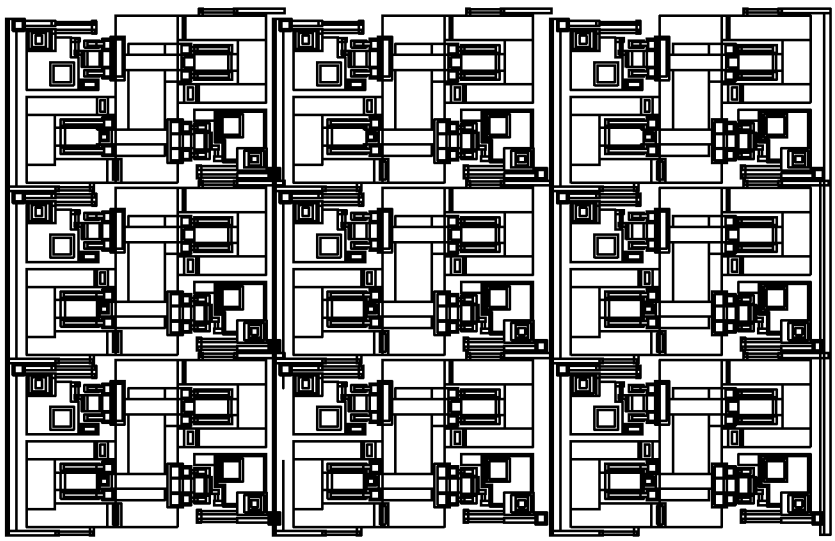
FIG.17



3V COMMON EMITTER
0.13mm2



PARALLEL CASCODE
0.1745mm2



STAGGERED CASCODE
0.1743mm2

FIG.18

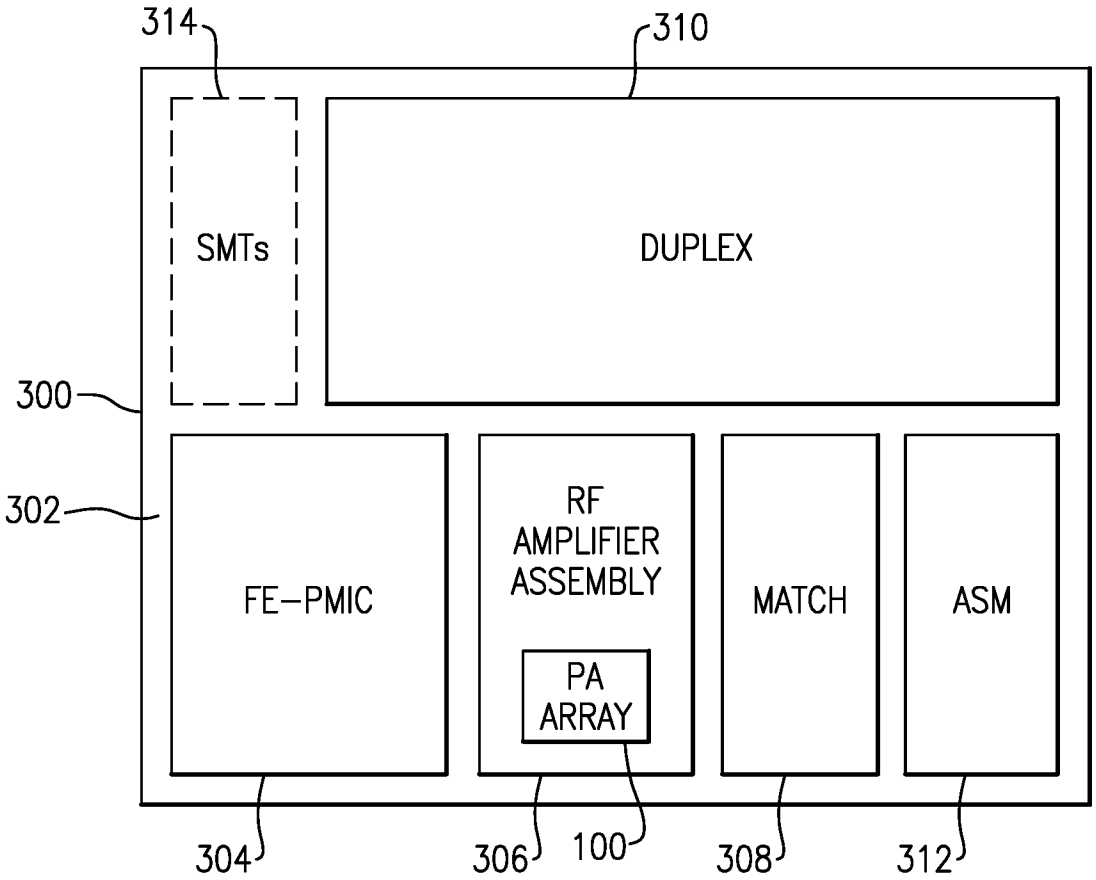

314
310
SMTs
DUPLEX
300
302
FE–PMIC
RF
AMPLIFIER
ASSEMBLY
PA
ARRAY
MATCH
ASM
304
306
100
308
312

FIG.19

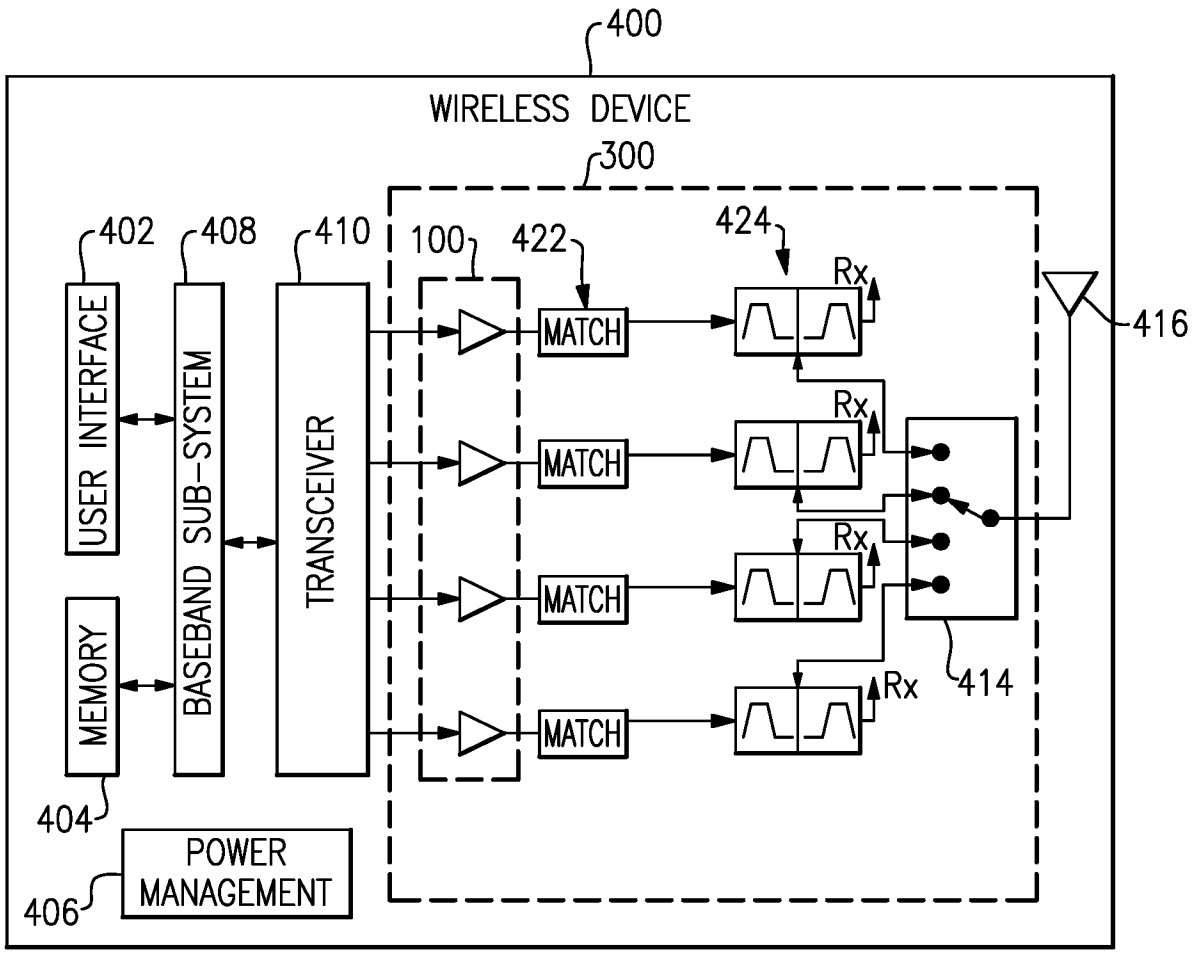

400
WIRELESS DEVICE
300
402
408
410
100
422
424
Rx
416
USER INTERFACE
BASEBAND SUB-SYSTEM
TRANSCEIVER
MATCH
MATCH
MATCH
MATCH
Rx
Rx
Rx
414
MEMORY
404
POWER MANAGEMENT
406

FIG.20

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/017917

A. CLASSIFICATION OF SUBJECT MATTER

H03F 1/02(2006.01)i, H03F 1/22(2006.01)i, H03F 3/68(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F 1/02; H03F 3/21; H03F 3/68; H03F 3/04; H03F 3/14; H01L 27/12; H03F 1/22

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: power amplifier, staggered cascode layout, common emitter transistor, common base transistor, array of cascoded device

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5066926 A (RAVI RAMACHANDRAN et al.) 19 November 1991 See column 2, lines 49-51, column 3, lines 14-18, claims 1-2, and figure 3.	1-22
Y	US 2003-0164738 A1 (KANG WU et al.) 04 September 2003 See paragraph [0012], claim 1, and figure 5.	1-22
A	US 2013-0130630 A1 (SKYWORKS SOLUTIONS, INC.) 23 May 2013 See claims 1, 19, and figures 8A-10.	1-22
A	JP 2014-222836 A (MITSUBISHI ELECTRIC CORP.) 27 November 2014 See abstract, paragraph [0005], and figures 1-4.	1-22
A	US 7429894 B2 (WOO JIN CHANG et al.) 30 September 2008 See abstract, claim 1, and figure 1.	1-22

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 June 2016 (17.06.2016)	**17 June 2016 (17.06.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
KIM, Sung Gon
Telephone No. +82-42-481-8746

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/017917

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5066926 A	19/11/1991	None	
US 2003-0164738 A1	04/09/2003	US 6844783 B2	18/01/2005
US 2013-0130630 A1	23/05/2013	CN 103999227 A	20/08/2014
		KR 10-2014-0089589 A	15/07/2014
		TW 201330227 A	16/07/2013
		TW 201330270 A	16/07/2013
		US 2013-0115895 A1	09/05/2013
		US 9064746 B2	23/06/2015
		US 9159743 B2	13/10/2015
		WO 2013-070971 A2	16/05/2013
		WO 2013-070971 A3	04/07/2013
JP 2014-222836 A	27/11/2014	None	
US 7429894 B2	30/09/2008	KR 10-0768060 B1	18/10/2007
		US 2007-0132514 A1	14/06/2007