(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 November 2013 (07.11.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/163789 A1

(51) International Patent Classification:
G06K 9/36 (2006.01)

(21) International Application Number:
PCT/CN2012/074954

(22) International Filing Date:
30 April 2012 (30.04.2012)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

WO 2013/163789 A1

(54) Title: HARDWARE-BASED IMAGE DATA BINARIZATION IN AN INDICIA READING TERMINAL

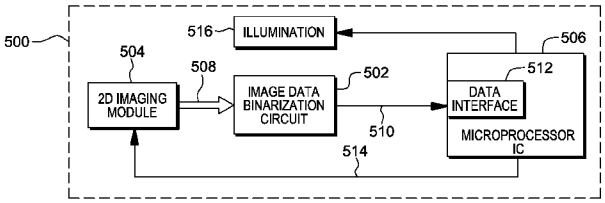

FIG. 5

(57) Abstract: Honeywell Docket No. H003278 Attorney Docket No. 4283.909 PATENT Page 26 of 26 ABSTRACT An indicia reading terminal is provided having an image data binarization circuit configured to receive image data, binarize at least a portion of the received image data into a binarized signal representative of dark and light portions of a target, and output the binarized signal to a microprocessor integrated circuit. The microprocessor integrated circuit need not include a dedicated cameral interface, which facilitates minimizing component costs for the indicia reading terminal, while maintaining acceptable scan performance.

HARDWARE-BASED IMAGE DATA BINARIZATION IN AN INDICIA READING TERMINAL

BACKGROUND

[0001] In barcode scanners and other types of indicia reading terminals, complex hardware components can hinder cost-cutting efforts. For imaging based barcode scanners, for instance, there are limitations on the selection of a processor and memory sizes of memory for use in the barcode scanner. For linear charge-coupled device (CCD) based solutions, the charge-coupled device itself and lens assembly are relatively costly components. For two-dimensional imaging based solutions, the processor has a dedicated camera interface and large memory size for image processing, both of which tend to increase cost. What is needed is a solution that facilitates attainting a lower component-cost while maintaining acceptable performance of the scanner.

BRIEF SUMMARY

[0002] The shortcomings of the prior art are overcome and additional advantages are provided through the provision of an indicia reading terminal that includes, for instance, an image sensor integrated circuit, the image sensor integrated circuit including a two-dimensional image sensor array including a plurality of selectively-addressable pixels for capturing an image of a target, wherein the target comprises at least one bar and at least one space of a barcode, analog-to-digital conversion circuitry configured to convert analog pixel values of the selectively-addressable pixels into digital image data, an image data binarization circuit configured to receive the image data from the analog-to-digital conversion circuitry, binarize at least a portion of the received image data into a binarized signal representative of the at least one bar and at least one space of the barcode, and output the binarized signal, and a microprocessor integrated circuit, the microprocessor integrated circuit including a central processing unit (CPU) and a data interface, the data interface configured to receive the binarized signal from the image data binarization

circuit, and the CPU configured to decode encoded information encoded in the barcode utilizing the binarized signal.

[0003] Additional features and advantages are realized through the concepts of the present invention. Other embodiments and aspects of the invention are described in detail herein and are considered a part of the claimed invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] One or more aspects of the present invention are particularly pointed out and distinctly claimed as examples in the claims at the conclusion of the specification. The foregoing and other objects, features, and advantages of the invention are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[0005] FIG. 1 depicts a block diagram of one embodiment of an indicia reading terminal in accordance with one or more aspects of the present invention;

[0006] FIG. 2 depicts an exploded assembly perspective view of an imaging module;

[0007] FIG. 3 depicts a perspective view of an imaging module;

[0008] FIG. 4 is a schematic physical form view of an indicia reading terminal in one embodiment of the present invention;

[0009] FIG. 5 depicts a block diagram of another embodiment of an indicia reading terminal in accordance with one or more aspects of the present invention;

[0010] FIG. 6 depicts one example of a windowed frame, a portion of which can be binarized by an image data binarization circuit, in accordance with one or more aspects of the present invention; and

[0011] FIG. 7 depicts one example of a binarized signal from an image data binarization circuit, in accordance with one or more aspects of the present invention.

DETAILED DESCRIPTION

[0012] In accordance with aspects of the present invention, an image data binarization circuit of an indicia reading terminal receives image data and produces a binarized signal, based on the received image data, that is representative of at least a portion of a target, such as a barcode. The binarized signal can be provided to a processor without requiring that the processor have a dedicated cameral interface, such as an interface specially designed and dedicated to receiving image data. Advantageously, the use of relatively low-cost components is thereby enabled and facilitates minimizing component costs for the system (indicia reading terminal, also referred to herein as a "scanner"), while maintaining acceptable scan performance.

[0013] In one example, as described in further detail below with reference to FIG. 5, a low cost two-dimensional camera module is used, where no additional imaging lens and lens assembly are required. Additionally, a low cost illumination component (such as a light-emitting diode) can be used for near field illumination not requiring a long depth-of-field. The binarization circuit converts parallel or serial image data into a binarized signal that indicates dark and light spaces of a target, such as the bar and space of a barcode, to a data interface of a processor. In one particular embodiment, the data interface is a general-purpose I/O pin of the processor for counting the width of level '1' and '0' (high states and low states) of the binarized signal.

[0014] FIG. 1 depicts one embodiment of a block diagram of an indicia reading terminal to incorporate one or more aspects of the present. Indicia reading terminal 100 can include an image sensor 101 comprising a multiple pixel image sensor array 102 having pixels arranged in rows and columns of pixels, along with associated column circuitry 103 and row circuitry 104. Associated with image sensor 101 can be amplifier circuitry 105 (amplifier), and an analog-to-digital converter 106 which converts image information in the form of analog signals read out of image sensor array 102 into image information in the form of digital signals. Image sensor 101 can also have an associated timing and control circuit 107 for use in controlling *e.g.,* the exposure period of image

sensor 101, and gain applied to amplifier 105. The noted circuit components 101, 105, 106, and 107 can be packaged into a common image sensor integrated circuit 108. Image sensor integrated circuit 108 can, in some embodiments, incorporate fewer than the noted number of components or additional components as would be appreciated by those having ordinary skill in the art. For instance, analog-to-digital converter 106 may, in one example, reside separate from image sensor integrated circuit 108. In one example, image sensor integrated circuit 108 can be provided *e.g.,* by an MT9V022 (752x480 pixel array), an MT9V023 (752x480 pixel array), or an MT9M114 (1296x976 pixel array) image sensor integrated circuit available from Micron Technology, Inc. In another example, image sensor integrated circuit 108 can be provided *e.g.,* by a CM8237-A030SF-E (640x480) camera module (which also includes a lens component) available from Truly Semiconductors Ltd. In one example, image sensor array 102 can be a monochrome sensor array, a color image sensor array, or a hybrid monochrome and color image sensor array having a first subset of monochrome pixels without color filter elements and a second subset of color pixels having color sensitive filter elements. In one example, image sensor integrated circuit 108 can incorporate a Bayer pattern filter, so that defined at image sensor array 102 are red pixels at red pixel positions, green pixels at green pixel positions, and blue pixels at blue pixel positions. In the example of an image sensor array incorporating a Bayer pattern filter, frames that are provided can include red pixel values at red pixel positions, green pixel values at green pixel positions, and blue pixel values at blue pixel positions. Further in an embodiment incorporating a Bayer pattern image sensor array, CPU 115, described in further detail below, can, prior to subjecting a frame to further processing, interpolate pixel values at frame pixel positions intermediate of green pixel positions utilizing green pixel values for development of a monochrome frame of image data. Alternatively, CPU 115 can, prior to subjecting a frame for further processing, interpolate pixel values intermediate of red pixel positions utilizing red pixel values for development of a monochrome frame of image data. CPU 115 can, alternatively, prior to subjecting a frame for further processing, interpolate pixel values intermediate of blue pixel positions utilizing blue pixel values.

[0015] An imaging subsystem of terminal 100 can include image sensor 101 and, optionally, a lens assembly 109 for focusing an image onto image sensor array 102 of image sensor 101. As noted above, lens assembly 109 is optional, and, in cases where cost minimization is of paramount importance, can be omitted.

[0016] In the course of operation of terminal 100, image signals can be read out of image sensor 101, and optionally converted and stored into, for instance, a system memory such as RAM 111. A memory 110 of terminal 100 can include RAM 111, a nonvolatile memory such as EPROM 112 and a storage memory device 113 such as may be provided by a flash memory or a hard drive memory. Terminal 100 includes a microprocessor integrated circuit 114 that includes CPU 115 which can be adapted to read out image data stored in memory 110 and subject such image data to various image processing algorithms.

[0017] Terminal 100 can also include an image data binarization circuit 116 for binarizing image data read out from image sensor integrated circuit 108 and providing a binarized signal to microprocessor integrated circuit 114 for, e.g., further processing and/or storage in RAM 111, as is explained in further detail below. Image data binarization circuit 116 receives image data by way of bus 159 and provides a binarized signal to microprocessor integrated circuit 114 by way of signal line 160.

[0018] Referring to further aspects of terminal 100, imaging lens assembly 109, if present, can be adapted for focusing an image of decodable indicia 15 located within a field of view 16 on a substrate, T, onto image sensor array 102. A size in target space of a field of view 16 of terminal 100 can be varied in a number of alternative ways. A size in target space of a field of view 16 can be varied, e.g., by changing a terminal-to-target distance, changing an imaging lens assembly setting, and/or changing a number of pixels of image sensor array 102 that are subject to read out. Imaging light rays can be transmitted about imaging axis 25. Lens assembly 109 can be adapted to be capable of multiple focal lengths and multiple planes of optimum focus (best focus distances), if desired.

[0019] Terminal 100 can include an illumination subsystem 117 of varying complexity for illumination of target, T, and projection of an illumination pattern 118. Illumination pattern 118, in the embodiment shown, can be projected to be proximate to, but larger than, an area defined by field of view 16, and/or can also be projected in an area smaller than an area defined by a field of view 16. Illumination subsystem 117 can include a light source bank 119, comprising one or more light sources. A physical form view of an example of an illumination subsystem is shown in FIGS. 2 and 3. As shown in FIGS. 2 and 3, an imaging module 120 can be provided having a circuit board 121 carrying image sensor 101 and optional lens assembly 109 disposed in support 122 disposed on circuit board 121. In the embodiment of FIGS. 2 and 3, illumination subsystem 117 has a light source bank 119 provided by single light source 123. In another embodiment, light source bank 119 can be provided by more than one light source. In one particular embodiment, illumination subsystem 117 comprises a light-emitting diode.

[0020] Referring back to FIG. 1, terminal 100 can optionally include an aiming subsystem 124 for projecting an aiming pattern (not shown). Aiming subsystem 124, which can comprise a light source bank, can be coupled to aiming light source bank power input unit 125 for providing electrical power to a light source bank of aiming subsystem 124. Power input unit 125 can be coupled to system bus 126 via interface 127 for communication with other components of terminal 100, such as microprocessor integrated circuit 114 and/or CPU 115 thereof.

[0021] In one embodiment, illumination subsystem 117 can include, in addition to light source bank 119, an illumination lens assembly 128, as is shown in the embodiment of FIG. 1. In addition to, or in place of, illumination lens assembly 128, illumination subsystem 117 can include alternative light shaping optics, *e.g.* one or more diffusers, mirrors and prisms.

[0022] In use, terminal 100 can be oriented by an operator with respect to a target, T, (*e.g.*, a piece of paper, a package, another type of substrate) bearing decodable indicia 15

in such manner that illumination pattern 118 is projected on decodable indicia 15. In the example of FIG. 1, decodable indicia 15 are provided by a 1D bar code symbol. Decodable indicia 15 could also be provided by a 2D bar code symbol or optical character recognition (OCR) characters.

[0023] Referring to further aspects of terminal 100, lens assembly 109, if present, can be controlled with use of electrical power input unit 129 which provides energy for changing a plane of optimum focus of lens assembly 109. In one embodiment, an electrical power input unit 129 can operate as a controlled voltage source, and in another embodiment, as a controlled current source. Electrical power input unit 129 can apply signals for changing optical characteristics of lens assembly 109, *e.g.,* for changing a focal length and/or a best focus distance of (a plane of optimum focus of) lens assembly 109. Light source bank electrical power input unit 130 can provide energy to light source bank 119. In one embodiment, electrical power input unit 130 can operate as a controlled voltage source. In another embodiment, electrical power input unit 130 can operate as a controlled current source. In another embodiment electrical power input unit 130 can operate as a combined controlled voltage and controlled current source. Electrical power input unit 130 can change a level of electrical power provided to (energization level of) light source bank 119, *e.g.*, for changing a level of illumination output by light source bank 119 of illumination subsystem 117 for generating illumination pattern 118.

[0024] In another aspect, terminal 100 can include power supply 131 that supplies power to a power grid 132 to which electrical components of terminal 100 can be connected. Power supply 131 can be coupled to various power sources, *e.g.,* a battery 133, a serial interface 134 (*e.g.,* USB, RS232), and/or AC/DC transformer 135.

[0025] Further regarding power input unit 130, power input unit 130 can include a charging capacitor that is continually charged by power supply 131. Power input unit 130 can be configured to output energy within a range of energization levels. An average energization level of illumination subsystem 117 during exposure periods with the first

illumination and exposure control configuration active can be higher than an average energization level of illumination and exposure control configuration active.

[0026] Terminal 100 can also optionally include a number of peripheral devices including trigger 136 which may be used to make active a trigger signal for activating frame readout and/or certain decoding processes. Terminal 100 can be adapted so that activation of trigger 136 activates a trigger signal and initiates a decode attempt. Specifically, terminal 100 can be operative so that, in response to activation of a trigger signal, a succession of frames can be captured by way of read out image information from image sensor array 102 (typically, though not always, in the form of analog signals) and then storage of the image information after binarization and conversion into memory 110 (which can buffer one or more of the succession of frames at a given time). Microprocessor integrated circuit 114 can be operative to subject one or more of the succession of frames to a decode attempt, for instance by CPU 115 of microprocessor integrated circuit 114.

[0027] In attempting to decode a bar code symbol, *e.g.*, a one dimensional bar code symbol, microprocessor integrated circuit 114 can process image data of a frame corresponding to a line of pixel positions (*e.g.*, a row, a column, or a diagonal set of pixel positions) to determine a spatial pattern of dark and light cells and can convert each light and dark cell pattern determined into a character or character string via table lookup. In one particular embodiment, CPU 115 of microprocessor integrated circuit 114 performs such processing of image data. Where a decodable indicia representation is a 2D bar code symbology, a decode attempt can include locating a finder pattern using a feature detection algorithm, locating matrix lines intersecting the finder pattern according to a predetermined relationship with the finder pattern, determining a pattern of dark and light cells along the matrix lines, and converting each light pattern into a character or character string via table lookup.

[0028] Terminal 100 can include various interface circuits for coupling various of the peripheral devices to system address/data bus (system bus) 126, for communication with

microprocessor integrated circuit 114, which is also coupled to system bus 126. Terminal 100 can include interface circuit 137 for coupling image sensor timing and control circuit 107 to system bus 126, interface circuit 138 for coupling electrical power input unit 129 to system bus 126, interface circuit 139 for coupling illumination light source bank power input unit 130 to system bus 126, and interface circuit 140 for coupling trigger 136 to system bus 126. Terminal 100 can also include a display 141 coupled to system bus 126 and in communication with microprocessor integrated circuit 114 (for instance CPU 115 thereof), via interface 142, as well as pointer mechanism 143 in communication with microprocessor integrated circuit 114 (for instance CPU 115 thereof) via interface 144 connected to system bus 126. Terminal 100 can additionally include keyboard 145 coupled to system bus 126 via interface 146. Terminal 100 can also include range detector unit 147 coupled to system bus 126 via interface 148. In one embodiment, range detector unit 147 can be an acoustic range detector unit.

[0029] Terminal 100 can additionally include an accelerometer 149 which can be coupled to system bus 126 for communication across bus 126 with microprocessor integrated circuit 114, and/or CPU 115 thereof, via interface 150. Terminal 100 can monitor an output of accelerometer 149 for determining a measure of motion of terminal 100. Terminal 100 can also compare pixel values of successive frames for determining a measure of motion of terminal 100 (with an increase in motion the pixel values of corresponding pixel positions of successive frames can be expected to increase).

[0030] Various interface circuits of terminal 100 can share circuit components. For example, a common microcontroller can be established for providing control inputs to both image sensor timing and control circuit 107 and to power input unit 130. A common microcontroller providing control inputs to circuit 107 and to power input unit 130 can be provided to coordinate timing between image sensor array controls and illumination subsystem controls.

[0031] A succession of frames of image data that can be captured and subject to the described processing can be full frames (including pixel values corresponding to each

pixel of image sensor array 102 or a maximum number of pixels read out from image sensor array 102 during operation of terminal 100). A succession of frames of image data that can be captured and subject to the described processing can also be "windowed frames" comprising pixel values corresponding to less than a full frame of pixels of image sensor array 102. A succession of frames of image data that can be captured and subject to the described processing can also comprise a combination of full frames and windowed frames. A full frame can be read out for capture by selectively addressing pixels of image sensor 101 having image sensor array 102 corresponding to the full frame. A windowed frame can be read out for capture by selectively addressing pixels of image sensor 101 having image sensor array 102 corresponding to the windowed frame. In one embodiment, a number of pixels subject to addressing and read out determine a picture size of a frame. Accordingly, a full frame can be regarded as having a first relatively larger picture size and a windowed frame can be regarded as having a relatively smaller picture size relative to a picture size of a full frame. A picture size of a windowed frame can vary depending on the number of pixels subject to addressing and readout for capture of a windowed frame.

[0032] Terminal 100 can capture frames of image data at a rate known as a frame rate. A typical frame rate is 60 frames per second (FPS) which translates to a frame time (frame period) of 16.6 ms. Another typical frame rate is 30 frames per second (FPS) which translates to a frame time (frame period) of 33.3 ms per frame. A frame rate of terminal 100 can be increased (and frame time decreased) by decreasing a frame picture size.

[0033] Further aspects of terminal 100 in one embodiment are described with reference to Fig. 4. Trigger 136, display 141, pointer mechanism 143, and keyboard 145 can be disposed on a common side of a hand held housing 151 as shown in FIG. 4. Display 141 and pointer mechanism 143 in combination can be regarded as a user interface of terminal 100. Display 141 in one embodiment can incorporate a touch panel for navigation and virtual actuator selection in which case a user interface of terminal 100

can be provided by display 141. A user interface of terminal 100 can also be provided by configuring terminal 100 to be operative to be reprogrammed by decoding of programming bar code symbols. Terminal 100 can be operative so that user-selectable modes of operation are selectable with use of displayed actuators 152, 153,..., 157, or with use of programming bar code symbols. A hand held housing 151 for terminal 100 can, in another embodiment, be devoid of a display and/or keyboard and can be in a gun style form factor. Additionally, imaging module 120, including image sensor array 102 and imaging lens assembly 109 can be incorporated in hand held housing 151.

[0034] In accordance with aspects of the present invention, hardware-based image data binarization is provided in an indicia reading terminal. This is facilitated by provision of an image data binarization circuit (e.g. 116 of FIG. 1) and is explained in further detail below with reference to FIG. 5, which depicts a block diagram of one embodiment of an indicia reading terminal in accordance with one or more aspects of the present invention. Whereas the indicia reading terminal of FIG. 1 depicts a terminal having many optional components, the block diagram of FIG. 5 presents a more simplistic embodiment omitting many of the optional components described in connection with FIG. 1. The indicia reading terminal depicted in, and described with reference to, FIG. 5 depicts one example of an indicia reading terminal in accordance with one or more aspects of the present invention when cost-minimization is of paramount importance.

[0035] Referring to FIG. 5, indicia reading terminal 500 includes image data binarization circuit 502 disposed between two-dimensional imaging module 504 and microprocessor integrated circuit 506. In one example, imaging module 504 includes an image sensor integrated circuit (e.g. FIG. 1, 108) including a lens, and analog-to-digital conversion circuitry (e.g. FIG. 1, 106) which provides image data to image data binarization circuit 500. (In one particular embodiment, imaging module 504 comprises a CM8237-A030SF-E camera module reference above). Image signals (such as analog signal pixel values) are supplied to analog-to-digital conversion circuitry which converts

the analog signal pixel values to digital image data for output via bus 508 to image data binarization circuit 502. Image data binarization circuit is configured to receive image data from the analog-to-digital conversion circuitry via bus 508, binarize at least a portion of the received image data into a binarized signal, and output the binarized signal by way of signal line 510 to data interface 512 of microprocessor integrated circuit 506. In addition, microprocessor integrated circuit 506 is capable of providing sensor configuration to imaging module 504 via sensor configuration line 514.

[0036] In operation, image module 504 generates, in one example, a two-dimensional image of decodable indicia of a target, as explained above. Illumination component 516 provides illumination of the target and, in one embodiment, comprises a light-emitting diode. Imaging module 504 is configured to sense projected light and output image data, which may optionally be windowed (as described above) so that image frame rate can be adjusted (i.e. increased) without requiring a change in pixel clock speed. Generally, the smaller the picture (window) size, the less data that is required to be processed (e.g. read-out, stored, processed, etc.). When less data is being processed, pixel data can be read-out (e.g. from the image sensor array) at a faster pixel clock speed. Conversely, when images of larger picture size are obtained, comparatively more data is required to be processed, and a slower pixel clock speed can be used to read-out pixel data.

[0037] The image data output by the imaging module and received by image data binarization circuit 502 can be in parallel format or in serial format. In this regard, bus 508 could be a bus that includes multiple signal lines to carry the parallel data (or serial data on one of the multiple lines), or could comprise a single signal line, if only serial image data is output by imaging module 504.

[0038] Image data binarization circuit 502 receives the digitized image data and binarizes at least a portion thereof (such as the image data corresponding to a sequence of linearly-arranged spots, for instance pixels, of the image) into a binarized signal representative of at least a portion of the target, such as the decodable indicia portion thereof. In binarizing the image data, the binarization circuit 502 can select a subset of

the received image data, such as one or more lines thereof, and therefore has the ability to window the received image data received from imaging module 504. FIG. 6 depicts one example of a windowed frame. In FIG. 6, frame 602 includes n rows of linearly-arranged pixels. Window 604 of frame 602 encompasses, in this example, five rows (r_1, ..., r_5) of the n rows of linearly-arranged pixels. In other examples, binarization circuit may window only a single row of image data traversing a one-dimensional barcode, or may not window the image data at all.

[0039] Binarization circuit 502 binarizes the image data by generating and outputting a sequence of high and low states of the binarized signal based on a comparison of values of the image data (forming, for instance, a linear arrangement of pixels) with one or more threshold values representative of a maximum image data value indicative of a dark spot (e.g. bar) of the target. The values of image data can be determined in different ways. In one embodiment, where only a single row of image data is examined for binarization, the values of image data include pixel signal values of the row of pixels, and each pixel signal value (such as an intensity signal) of the row of pixels is compared against a threshold value. A high state is output if the pixel signal value is below the threshold and a low state is output if the pixel signal value is above the threshold (or vice-versa). In another example, an average of a consecutive plurality of pixel signal values of a row of pixels is selected as the image data value and compared to the threshold, and a next consecutive plurality of pixel signal values of a row of pixels is selected as the next image data value for comparison to the threshold.

[0040] When multiple rows of image data are examined for binarization, the image data value being compared to the threshold can be an average of a plurality of pixel signal values from pixels of the multiple rows of the pixel array. As an example, if four rows are being examined, the binarization circuit can, when generating the high or low state for a spot within the multiple rows, determine an average pixel signal value of pixels surrounding that spot. The average value can be compared to the threshold, and a high or low state output for that spot. Examination of multiple rows for discerning an accurate

intensity measurement may be useful in cases where blurring has occurred (such as is sometimes the case at the extreme edges of a frame).

[0041] Alternatively or additionally, the appropriate image data value for comparison to the threshold can be determined using various other techniques for more accurately approximating the intensity of a particular spot of an image, as would be appreciated by those having ordinary skill in the art.

[0042] Binarization into a sequence of high or low states is especially applicable to barcodes and other targets, which include a sequence of dark spots (bars) and light spots (spaces) of varying widths. Information is encoded by the varying widths of the bars and spaces, as is appreciated by those having ordinary skill in the art. The comparison of the image data values to the threshold is an effort to determine whether the portion of the image (to which the image data value corresponds, such as a pixel thereof) is representative of a dark spot or a light spot of a target. For instance, when the image data value indicates a signal intensity above the threshold, then it can be concluded that the image data value correlates to a space, or lighter portion, of the imaged target barcode, and when the image data value indicates a signal intensity below the threshold, then it can be concluded that the image data value correlates to a bar, or darker portion, of the imaged target barcode.

[0043] As will be appreciated by those having ordinary skill in the art, the threshold(s) can be predefined or based on portions of the image data itself. Global thresholding, in which a threshold is used for all comparisons to image data values of the image data being binarized, or local/dynamic thresholding, in which multiple thresholds are computed, with a unique threshold being computed for each image data value (corresponding to a spot area/pixel), based on image data values surrounding the spot area/pixel, can be used to define the threshold, as is appreciated by those having ordinary skill in the art. In this manner, the thresholds being used for comparison may include many different thresholds vary across the image (e.g. of the barcode).

[0044] The image data binarization circuit can be achieved by, for instance, one or more complex programmable logic device(s) (CPLD) or field-programmable gate array(s) (FPGA), as examples.

[0045] FIG. 7 depicts one example of a binarized signal from binarization circuit 502. The binarized signal 700 includes high states 704a, 704b, 704c, and 704d, and low states 702a, 702b, 702c, and 702d. A high state can correspond to a binary '1' and a low state can correspond to a binary '0'. In one embodiment, a high state represents a bar (or relatively dark portion of the image) and a low state represents a space (or relatively light portion of the image). In another embodiment, a high state represents a space (or relatively light portion of the image) and a low state represents a bar (or relatively dark portion of the image).

[0046] Additionally, it can be seen that the binarized signal transitions between high and low states. As an example, binarized signal 700 transitions from low state 702a to high state 704a at transition 706a (time t_0) and from high state 704a to low state 702b at transition 706b (time t_1). The time between transitions (i.e. width of the peaks (high states) and valleys (low states) of the binarized signal) is indicative of a width of the dark or light spot (e.g. bar or space of a barcode), as the case may be. As the binarization circuit outputs a binarized signal representing the binarization of image data values from a linear portion of an image of a target's decodable indicia, e.g. a barcode, a wider peak or valley corresponds to a wider bar or space.

[0047] High or low state width, can be determined based on an amount of time (measured by, for instance, detecting a number of clock cycles of the microprocessor integrated circuit) between state transitions of binarized signal 700. For instance, as binarized signal 700 is captured by the data interface (e.g. FIG. 5, 512) of the microprocessor integrated circuit, the width of each high or low state can be determined. As an example, it is determined that high state 704b has a width of one clock cycle (time t_2 to time t_3), while high state 704c has a width of two clock cycles (time t_4 to time t_5).

This indicates that the bar (or space) represented by high state 704b is twice as wide as that represented by high state 704c.

[0048] Thus, a binarized signal generated from, e.g., linearly-arranged image data values spanning a barcode, can be observed on the data interface of a processor in order to accurately sense the bars/spaces of the barcode. Data interface 512 (FIG. 5) is, in one example, a general purpose data interface of a microprocessor integrated circuit 506 (or processor thereof), for instance a general-purpose I/O (GPIO) of the microprocessor integrated circuit 506 (or processor thereof). In one example, the GPIO comprises a data input pin of the microprocessor integrated circuit 506 or processor. The microprocessor integrated circuit 506 can capture the binarized signal for decoding the information encoded in the target.

[0049] In one example, the image data received by the image data binarization circuit comprises monochrome image data (such as grayscale) and the image data binarization circuit binarizes the image data based on whether the image data values exceed a threshold intensity value. For instance, if a pixel intensity value exceeds the threshold, a high state (corresponding to white) is output for at least one clock cycle. In other examples, a low state corresponds to white, and is output when the pixel intensity value exceeds the threshold.

[0050] In another example, the image data received by the image data binarization circuit comprises color image data. In one example, the binarization circuit receives color image data in YUV or YCbCr format and binarizes the color image data based on the Y component (luminescence signal) thereof, and optionally discards or ignores the UV or CbCr component. The Y component, in this case, comprises the intensity that is compared to the threshold for high/low state output determination.

[0051] In yet another example, the binarization circuit receives color image data in raw RGB format and binarizes the color image data based on the intensity at least one

additive color of the RGB data, such as red, blue, or green component, as is appreciated by those having ordinary skill in the art.

[0052] Described above, and in accordance with aspects of the present invention, an indicia reading terminal is provided which includes an image data binarization circuit that produces a binarized signal based on received image data and representative of, for instance, a barcode. The binarized signal is provided to a data interface, such as a GPIO of a processor, and therefore does not require that the processor include a dedicated cameral interface for receiving the image data. Advantageously, relatively low-cost components can be used, thus facilitating minimizing component costs for the system without sacrificing acceptable scan performance. In some embodiments, the target comprises a barcode and the binarized signal is representative of bars and spaces thereof. In other embodiments, the target comprises one or more characters to be optically recognized and the binarized signal represents dark and light areas of the characters to facilitate optical character recognition.

[0053] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprise" (and any form of comprise, such as "comprises" and "comprising"), "have" (and any form of have, such as "has" and "having"), "include" (and any form of include, such as "includes" and "including"), and "contain" (and any form contain, such as "contains" and "containing") are open-ended linking verbs. As a result, a method or device that "comprises", "has", "includes" or "contains" one or more steps or elements possesses those one or more steps or elements, but is not limited to possessing only those one or more steps or elements. Likewise, a step of a method or an element of a device that "comprises", "has", "includes" or "contains" one or more features possesses those one or more features, but is not limited to possessing only those one or more features.

Furthermore, a device or structure that is configured in a certain way is configured in at least that way, but may also be configured in ways that are not listed.

[0054] The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The embodiment was chosen and described in order to best explain the principles of the invention and the practical application, and to enable others of ordinary skill in the art to understand the invention for various embodiment with various modifications as are suited to the particular use contemplated.

[0055] A small sample of systems that are described herein are as follows:

A1. An indicia reading terminal comprising: an image sensor integrated circuit, the image sensor integrated circuit including a two-dimensional image sensor array comprising a plurality of selectively-addressable pixels for capturing an image of a target, wherein the target comprises at least one bar and at least one space of a barcode; analog-to-digital conversion circuitry configured to convert analog pixel values of the selectively-addressable pixels into digital image data; an image data binarization circuit configured to receive the image data from the analog-to-digital conversion circuitry, binarize at least a portion of the received image data into a binarized signal representative of the at least one bar and at least one space of the barcode, and output the binarized signal; and a microprocessor integrated circuit, the microprocessor integrated circuit comprising a central processing unit (CPU) and a data interface, the data interface configured to receive the binarized signal from the image data binarization circuit, and the CPU configured to decode encoded information encoded in the barcode utilizing the binarized signal.

A2. The indicia reading terminal of A1, wherein the binarized signal comprises one or more high states and one or more low states, wherein a high state of the

one or more high states represents one of: a bar of the at least one bar of the barcode or a space of the at least one space of the barcode, and wherein a low state of the one or more low states represents the other of the bar of the at least one bar of the barcode or a space of the at least one space of the barcode.

A3. The indicia reading terminal of A2, wherein the high state represents the bar of the at least one bar of the barcode, and the CPU is further configured to determine a width of the bar by determining a width of the high state representative of the bar, wherein the width of the high state is defined by a first transition and a second transition of the binarized signal, the first transition comprising a transition from a first low state of the one or more low states to the high state, and the second transition comprising a transition from the high state to a second low state of the one or more low states.

A4. The indicia reading terminal of A3, wherein determining the width of the high state comprises counting a number of consecutive CPU clocks for which the high state is received by the data interface of the microprocessor integrated circuit.

A5. The indicia reading terminal of A1, wherein the data interface of the microprocessor integrated circuit comprises a general purpose input/output pin.

A6. The indicia reading terminal of A1, wherein binarizing the portion of the received image data into the binarized signal comprises comparing a value of the image data with a threshold value, the threshold value representative of a maximum image data value indicative of a bar of the barcode.

A7. The indicia reading terminal of A6, wherein the image data binarization circuit is configured to output one of a high state of the binarized signal or a low state of the binarized signal responsive to the value being below the threshold, and to output the other of the high state of the binarized signal or the low state of the binarized signal, responsive to the value being above the threshold.

A8. The indicia reading terminal of A6, wherein the value of the image data comprises an average of a plurality of pixel values from pixels of at least one row of the pixel array.

A9. The indicia reading terminal of A6, wherein the threshold is predefined.

A10. The indicia reading terminal of A6, wherein the threshold is selected based, as least in part, on image data values of the portion of the received image data being binarized.

A11. The indicia reading terminal of A10, wherein the threshold is selected by local thresholding.

A12. The indicia reading terminal of A10, wherein the threshold is selected by global thresholding.

A13. The indicia reading terminal of A1, wherein the image data binarization circuit comprises at least one of a complex programmable logic device or a field-programmable gate array.

A14. The indicia reading terminal of A1, wherein the image data binarization circuit is further configured to window the received image data.

A15. The indicia reading terminal of A14, wherein windowing selects a subset of the image data, the subset of image data comprising image data from a linear arrangement of pixels of the image sensor array.

A16. The indicia reading terminal of A15, wherein the subset of image data corresponds to a one-dimensional representation of the barcode.

A17. The indicia reading terminal of A1, wherein the received image data comprises monochrome image data

A18. The indicia reading terminal of A1, wherein the received image data comprises color image data.

A19. The indicia reading terminal of A18, wherein the color image data comprises at least one of YUV or YCbCr format image data comprising a luminance signal thereof, and wherein the portion of the YUV or YCbCr format image data binarized by the image data binarization circuit comprises the luminance signal thereof.

A20. The indicia reading terminal of A18, wherein the color image data comprises raw RGB format image data comprising at least one additive color intensity thereof, and wherein the portion of the RGB format image data binarized by the image data binarization circuit comprises the at least one additive color intensity thereof.

CLAIMS

What is claimed is:

1. An indicia reading terminal comprising:

an image sensor integrated circuit, the image sensor integrated circuit including a two-dimensional image sensor array comprising a plurality of selectively-addressable pixels for capturing an image of a target, wherein the target comprises at least one bar and at least one space of a barcode;

analog-to-digital conversion circuitry configured to convert analog pixel values of the selectively-addressable pixels into digital image data;

an image data binarization circuit configured to receive the image data from the analog-to-digital conversion circuitry, binarize at least a portion of the received image data into a binarized signal representative of the at least one bar and at least one space of the barcode, and output the binarized signal; and

a microprocessor integrated circuit, the microprocessor integrated circuit comprising a central processing unit (CPU) and a data interface, the data interface configured to receive the binarized signal from the image data binarization circuit, and the CPU configured to decode encoded information encoded in the barcode utilizing the binarized signal.

2. The indicia reading terminal of claim 1, wherein the binarized signal comprises one or more high states and one or more low states, wherein a high state of the one or more high states represents one of: a bar of the at least one bar of the barcode or a space of the at least one space of the barcode, and wherein a low state of the one or more low states represents the other of the bar of the at least one bar of the barcode or a space of the at least one space of the barcode.

3. The indicia reading terminal of claim 2, wherein the high state represents the bar of the at least one bar of the barcode, and the CPU is further configured to determine a width of the bar by determining a width of the high state representative of the bar, wherein the width of the high state is defined by a first transition and a second transition of the binarized signal, the first transition comprising a transition from a first low state of the one or more low states to the high state, and the second transition comprising a transition from the high state to a second low state of the one or more low states.

4. The indicia reading terminal of claim 3, wherein determining the width of the high state comprises counting a number of consecutive CPU clocks for which the high state is received by the data interface of the microprocessor integrated circuit.

5. The indicia reading terminal of claim 1, wherein the data interface of the microprocessor integrated circuit comprises a general purpose input/output pin.

6. The indicia reading terminal of claim 1, wherein binarizing the portion of the received image data into the binarized signal comprises comparing a value of the image data with a threshold value, the threshold value representative of a maximum image data value indicative of a bar of the barcode.

7. The indicia reading terminal of claim 6, wherein the image data binarization circuit is configured to output one of a high state of the binarized signal or a low state of the binarized signal responsive to the value being below the threshold, and to output the other of the high state of the binarized signal or the low state of the binarized signal, responsive to the value being above the threshold.

8. The indicia reading terminal of claim 6, wherein the value of the image data comprises an average of a plurality of pixel values from pixels of at least one row of the pixel array.

9. The indicia reading terminal of claim 6, wherein the threshold is predefined.

10. The indicia reading terminal of claim 6, wherein the threshold is selected based, as least in part, on image data values of the portion of the received image data being binarized.

11. The indicia reading terminal of claim 10, wherein the threshold is selected by local thresholding.

12. The indicia reading terminal of claim 10, wherein the threshold is selected by global thresholding.

13. The indicia reading terminal of claim 1, wherein the image data binarization circuit comprises at least one of a complex programmable logic device or a field-programmable gate array.

14. The indicia reading terminal of claim 1, wherein the image data binarization circuit is further configured to window the received image data.

15. The indicia reading terminal of claim 14, wherein windowing selects a subset of the image data, the subset of image data comprising image data from a linear arrangement of pixels of the image sensor array.

16. The indicia reading terminal of claim 15, wherein the subset of image data corresponds to a one-dimensional representation of the barcode.

17. The indicia reading terminal of claim 1, wherein the received image data comprises monochrome image data

18. The indicia reading terminal of claim 1, wherein the received image data comprises color image data.

19. The indicia reading terminal of claim 18, wherein the color image data comprises at least one of YUV or YCbCr format image data comprising a luminance signal thereof, and wherein the portion of the YUV or YCbCr format image data binarized by the image data binarization circuit comprises the luminance signal thereof.

20. The indicia reading terminal of claim 18, wherein the color image data comprises raw RGB format image data comprising at least one additive color intensity thereof, and wherein the portion of the RGB format image data binarized by the image data binarization circuit comprises the at least one additive color intensity thereof.

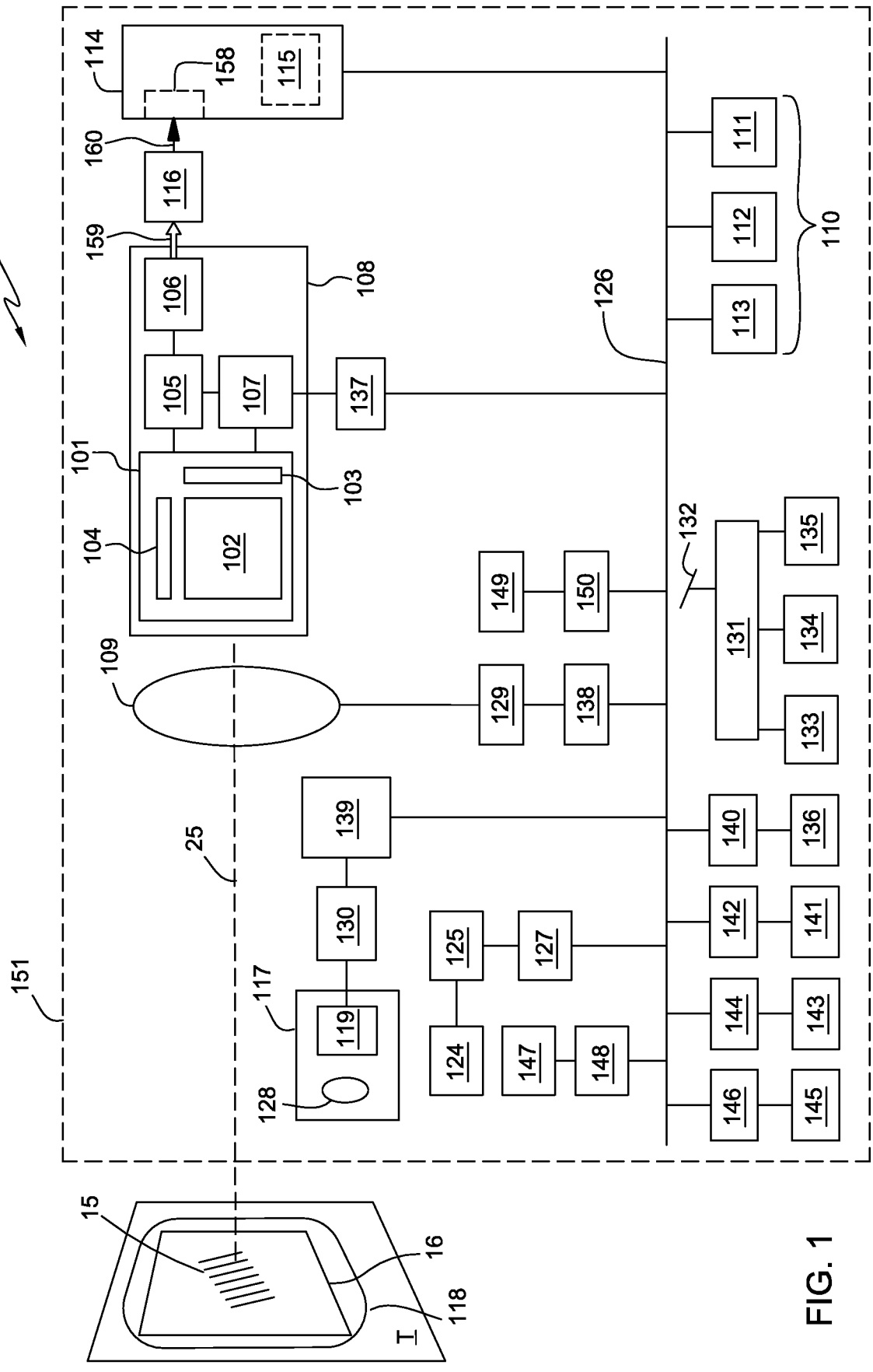
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FIG. 1

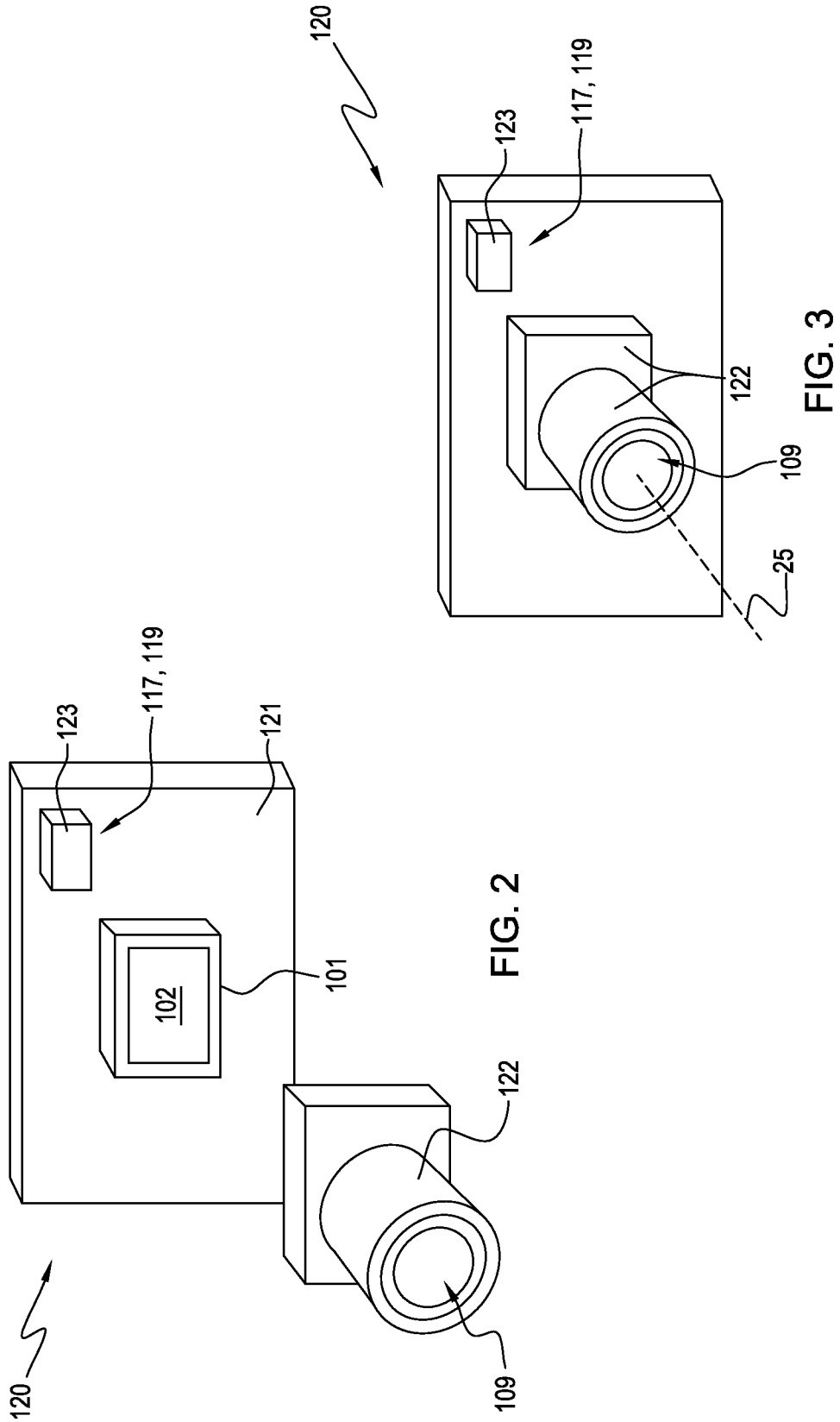
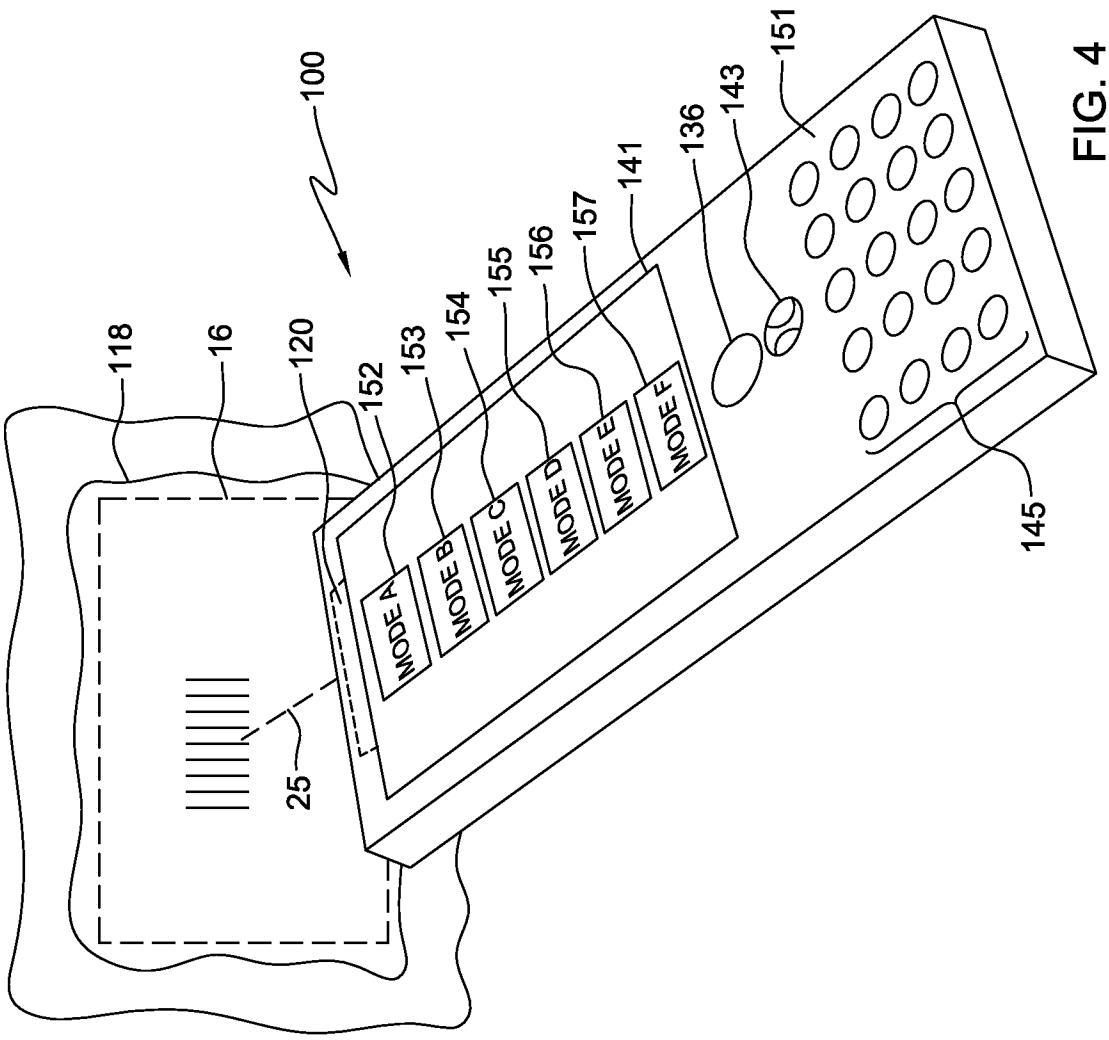


FIG. 2

FIG. 3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MODE A
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MODE C
MODE D
MODE E
MODE F
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FIG. 4

FIG. 5

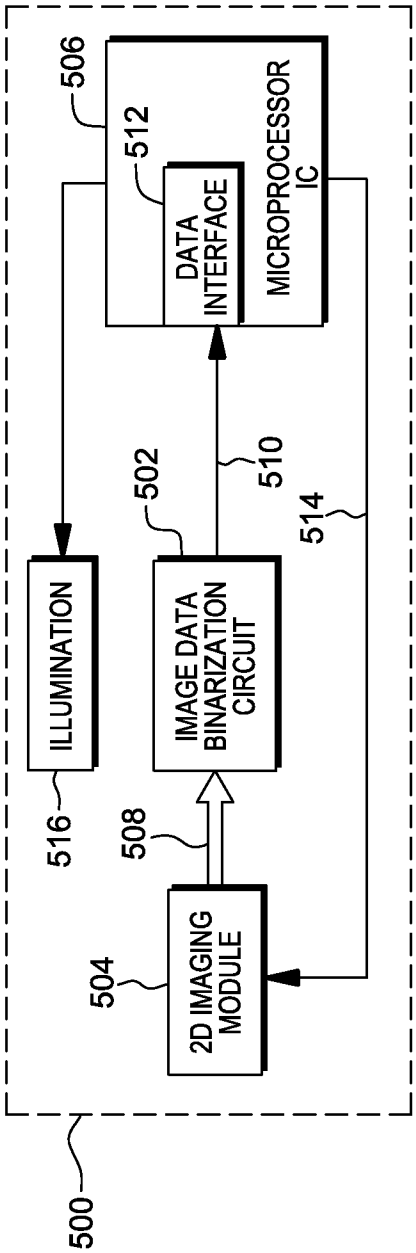


FIG. 6

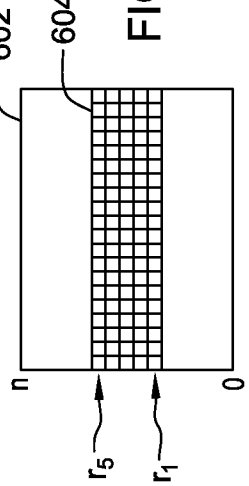
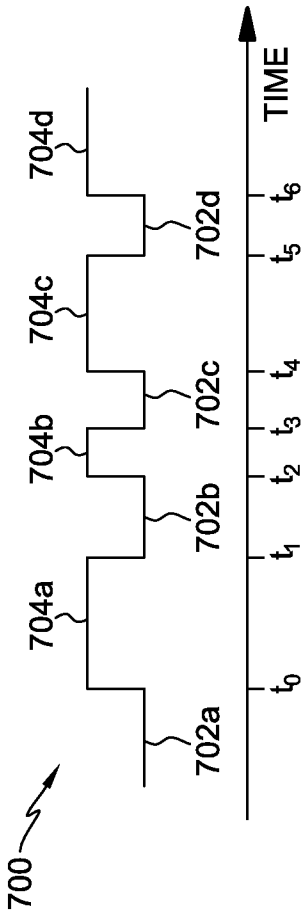


FIG. 7



INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2012/074954

A. CLASSIFICATION OF SUBJECT MATTER

G06K 9/36(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G06K 9/, G06K 7/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CPRSABS, CNKI,VEN,USTXT: indicia, bar code, read+, scan+, binariz+, cpu, processor? , processing unit, image, sensor, array, address+, decod+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US2006274171 A1(WANG Y et al.) 07 Dec.2006(07.12.2006) description paragraphs [0081]-[0191] and figures 1A-16C	1-20
A	US6575367 B1(WELCH ALLYN DATA COLLECTION INC) 10 Jun.2003(10.06.2003) the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 Jan. 2013(08.01.2013)	**31 Jan. 2013 (31.01.2013)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer QU, Fengli Telephone No. (86-10)62411737

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2012/074954

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US6575367 B1	10.06.2003	NONE	