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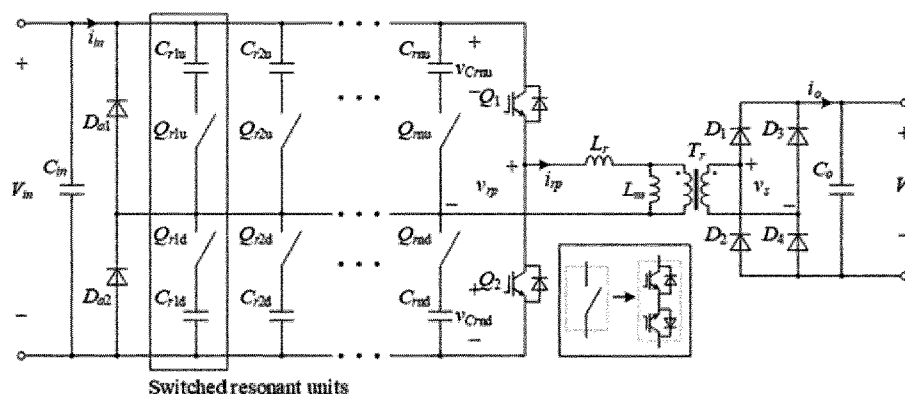


FIGURE 2

(57) Abstract: This invention provides an isolated DC-DC converter for use in power supply applications. The converter comprises an input filter capacitor; an output filter capacitor; a transformer; a plurality n of switched resonance units, SRUs, wherein each SRU comprises at least two switch-capacitor pairs, each switch-capacitor pair comprising a switch and an associated resonant capacitor; and a switching arrangement operatively-coupled to the transformer and to the plurality of SRUs. The switches in each of the plurality of SRUs, in combination with the switching arrangement, are operable to, in turn, operatively connect their associated capacitors with the transformer, to achieve resonance. A corresponding method for operating / controlling the converter is also provided.



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TOPOLOGY AND CONTROL METHOD FOR AN ISOLATED DC-DC
CONVERTER

Field of the Invention

This invention relates to aspects of a power supply system, and particularly to a DC-DC converter suitable for use in DC power supply systems, particularly but non-
5 exclusively high-power systems. This invention also relates to methods for controlling the DC-DC converter.

Background of the invention

In power-conversion circuits, such as those of DC/DC
10 converters, capacitive filters are typically needed to counter fluctuations (ripples). These fluctuations arise as a result of noise / interference, and can be attributed to a variety of sources. One common source of ripples is switching, which is carried out as a matter of course in
15 DC-DC converters when performing their primary functions (for example, in the rectification of AC). Designs usually try to mitigate this ripple as much as possible, but it cannot be completely eliminated. As a general principle, filter capacitors are utilised within such DC-DC converter
20 circuits to absorb and discharge the energy associated with these fluctuations on a continuous basis, and so minimize the peaks and troughs.

In high current (usually above hundreds of Amperes), low voltage (typically less than 3kV)
25 applications of DC-DC converters, a strict ripple current requirement has to be respected. However, since ripple current and filter capacitance are inversely proportional, in such implementations, the filter capacitors that are used to manage the input and/or output ripple currents
30 need to be correspondingly larger. This results in an

associated increase in the cost and volume / weight of components of the converter.

It is against this background that the present disclosure has been set.

5

Summary of the Invention

According to an aspect of the invention, there is provided an (isolated) DC-DC converter comprising: an input filter capacitor; an output filter capacitor; and a transformer. The converter further comprises a plurality n of switched resonance units (SRUs), wherein each SRU comprises two or more switch-capacitor pairs (i.e., paired switches and resonant capacitors, each switch-capacitor pair comprising a switch and an associated resonant capacitor). The converter further comprises a switching arrangement or element operatively-coupled to the transformer, and to the plurality of SRUs. The switches in each of the plurality of SRUs, in combination with the switching arrangement, are operable to, in turn, operatively connect their associated capacitors (i.e., the capacitors associated with the switches in the SRUs) with the transformer, to achieve resonance.

In some embodiments, the converter also comprises a resonant inductor operatively coupled to the transformer, such that the capacitors in the SRUs may also be operatively connected to the resonant inductor to achieve resonance.

The above-described arrangement allows for resonant capacitors to be inserted into the circuit and then subsequently bypassed in turn, such that resonance (with the inductor, where applicable) 'repeats' multiple times over a switching period of the switching arrangement. This causes the frequency of the input and output ripple currents to increase, which in turn means that the

corresponding input and output capacitors / capacitance may be decreased. A corresponding reduction in cost and volume of the resulting circuitry can thereby be achieved.

5 In some instances, the plurality of SRUs are connected in parallel with one another, and in parallel with the input capacitor. In some instances, each of the plurality of SRUs is connected in parallel with the switching arrangement.

10 It is also possible for the SRUs to be connected in parallel with the output capacitor in some instances. For example, where a diode rectifier is provided between the transformer and the output capacitor, an SRU may take the place of some of the diodes.

15 In some instances, a midpoint of each SRU is connected as an AC point; and the transformer (and resonant inductor, where applicable) are connected in series with the midpoint of each SRU. The midpoints of adjacent SRUs may also be connected to one another.

20 Optionally, switches in the switching arrangement have a first duty cycle D_0 , and the switches in each of the plurality (n) of SRUs have a second duty cycle of $1/n$ of the first duty cycle D_0 . Multiple resonances can thereby be achieved (n times) per half switching period, since resonance is achieved each time one of the SRUs is
25 activated / inserted into the circuit.

30 Optionally, the switching arrangement corresponds to a half-bridge circuit comprising a pair of switches (Q_1 , Q_2) and is operated using a first driving signal having an associated first switching frequency. In some cases, the switches in each of the plurality of SRUs are operated using a second driving signal having an associated second switching frequency.

In some embodiments, especially those where more than two SRUs are utilised, the second switching frequency

is double the first switching frequency. This means that resonance can be achieved twice in a switching period by each SRU.

5 In some embodiments, especially those where more than two SRUs are utilised, each switch-capacitor pair in a given SRU comprises a resonant capacitor and a bi-directional switch.

10 Optionally, input driving signals for the switches in each of the plurality of SRUs are rotated in turn before being provided to the respective switches. This enables voltage balancing to be achieved in a circuit with multiple SRUs connected in parallel.

15 In some embodiments, especially when (only) two SRUs are utilised, the first and second switching frequencies are substantially the same. This optimises the switching frequency: it is sufficiently high to enable multiple resonances to be achieved (one in each half of the switching period), but avoids too high a switching frequency. High efficiency of the converter is thereby
20 achieved.

In some embodiments, where (only) two SRUs are utilised, each switch-capacitor pair in a given SRU comprises a resonant capacitor and a uni-directional switch, where the switches in any given SRU are connected
25 in opposition to one another. Additionally, in such embodiments, the switches in adjacent SRUs are connected in opposition to one another. In embodiments where two uni-directional switches are utilised in each SRU, conduction losses in switches are reduced, compared with
30 embodiments with more than two SRUs having two anti-series connected switches (since this would effectively involve four switches).

Optionally, input driving signals provided to the SRUs are offset from input driving signals for the

switches of the switching arrangement by a quarter of a switching period of the switching arrangement. This helps to ensure that the resonance is achieved for an optimal time period, taking into account the switching period of the switching arrangement.

In some instances, typically where the converter comprises only two SRUs, the converter further comprises a pair of diodes connected in parallel between the plurality of SRUs and the input filter capacitor. This configuration provides a conducting path for the magnetizing current when switches in the SRUs are turned off.

According to another aspect of the present invention, there is provided a method of operating an isolated DC-DC converter for use in power supply. The DC-DC converter comprises an input filter capacitor; an output filter capacitor; and a transformer. The converter further comprises a plurality n of switched resonance units (SRUs), wherein each SRU comprises two or more switch-capacitor pairs (i.e., paired switches and resonant capacitors, each switch-capacitor pair comprising a switch and an associated resonant capacitor). The converter further comprises a switching arrangement operatively-coupled to the transformer, and to the plurality of SRUs, and comprising first and second switches. The method comprises the following steps: (i) turning on the first switch of the switching arrangement and the switches of a first one of the plurality of SRUs; whilst the first switch of the switching arrangement remains on, (ii) turning off the switches of the first SRU and turning on the switches of a second (adjacent) SRU; (iii) repeating step (ii) for pairs of (adjacent) SRUs in turn; (iv) turning off the first switch of the switching arrangement; (v) turning on the second switch of the switching arrangement and turning on the switches of the first SRU;

and (vi) whilst the first switch of the switching arrangement remains on, repeating steps (ii) and (iii) for pairs of (adjacent) SRUs in turn.

The above-described method allows for resonant capacitors to be inserted in turn into the circuit (as their corresponding switch is turned on) and then bypassed subsequently (as their corresponding switch is turned off), such that resonance 'repeats' multiple times over a switching period of the switching arrangement. This causes the frequency of the input and output ripple currents to increase, which in turn means that the corresponding input and output capacitors / capacitance may be decreased. A corresponding reduction in cost and volume of the resulting circuitry can thereby be achieved.

In some instances, a phase of driving signals for the first SRU is substantially synchronised with driving signals of the first switching arrangement switch; and a time delay of $1/(nf_s)$ is applied for driving signals of adjacent SRUs. Multiple resonances can thereby be achieved (n times) per half switching period, since resonance is achieved each time one of the SRUs is activated.

Additionally, the number of times that resonance can be achieved in any given switching period is maximised.

It will be appreciated that aspects of the system, and their associated advantages, will also be equally applicable to the above-described method; and vice versa.

Brief Description of the Drawings

Figures 1A and 1B respectively schematically illustrate a DC-DC converter topology and a configuration in which this converter may be used in some known power supply applications;

Figure 2 schematically illustrates a DC-DC converter topology according to an aspect of the present invention;

Figure 3 schematically illustrates a DC-DC converter topology according to another aspect of the present invention;

Figure 4 illustrates an example modulation strategy that may be used during implementation of the DC-DC converter of Figure 2;

Figure 5 illustrates example modulation signals that may be used during implementation of the modulation strategy of Figure 4;

Figure 6 schematically illustrates conduction paths through the DC-DC converter of Figure 2 during implementation of the modulation strategy of Figure 4;

Figure 7 illustrates example modulation signals that may be used during implementation of a modulation strategy for the converter topology of Figure 3;

Figure 8 illustrates simulation results for an example implementation of the DC-DC converter shown in Figure 3; and

Figure 9 illustrates simulation results for an example implementation of the DC-DC converter shown in Figure 4.

These drawings depict one or more implementations in accordance with the present teachings, by way of example only, not by way of limitation. In the figures, like reference numerals refer to the same or similar elements.

Detailed Description of the Drawings

Figures 1A and 1B schematically illustrate example DC-DC converter configurations that may be utilised in some conventional prior art systems.

Figure 1A shows an isolated DC-DC converter comprising an input filter capacitor C_{IN} , a bridge-circuit (comprising four switches Q_{A-D}), an inductor L_S , a transformer (N_P and N_S), a diode rectifier (D_{1-4}) and an

output filter capacitor (C_{out}). In more detail, the bridge circuit of switches Q_{A-D} is connected in parallel to the input filter capacitor C_{IN} . The inductor L_s and transformer are connected in series to the mid-points of the bridge circuit, and to the midpoints of the diode rectifier D_{1-4} . The diode rectifier D_{1-4} is in turn connected in parallel to the output filter capacitor C_{OUT} .

Figure 1B illustrates an example configuration for use in a power supply application, whereby a plurality of the above-described DC-DC converters are combined in an interleaved manner. As shown in Figure 1B, a single pair of input and output filter capacitors (C_{IN} and C_{out}) are provided. Operatively coupled in parallel between this pair of filter capacitors is a plurality of 'modules', whereby each module may take the form of one of the isolated DC-DC converters described above in relation to Figure 1A (albeit with the individual filter capacitors from each converter removed, since all of the converters will use the same main input and output filter capacitors). When operating the arrangement of Figure 1B, a phase lag can be applied to the driving signals of two adjacent converters in order to allow the input and output ripple currents to be increased. This in turn means that the input and output filter capacitors may be reduced. Examples of such interleaved implementations may be found in CN 113890366 A and US 2007/086224 A1.

The setup shown in Figure 1B presents a simplistic illustration for ease of understanding; however it will be appreciated that for practical purposes, utilization of an interleaved structure in converters typically involves the incorporation of numerous switches, diodes, transformers and auxiliary circuits, including driving circuits and power supply sources, in order to manage the operation of the different modules and electronic components. The

additional electronic components required reduces the compactness of the converter's structure overall, and can thereby also increase the associated cost of the converter.

5 As an alternative to this more complicated interleaved structure solution, a reduction in filter capacitance could potentially be achieved by increasing the switching frequency. However this in turn has its own associated drawbacks, notably that of causing an
10 associated increase in switching losses and eddy current losses, which reduces the efficiency of the converter. Moreover, improving the operation frequency is difficult, due to a poor high-frequency switching characteristic of high-power semiconductor switches. For example, the
15 switching frequency of 4500V IGBT (insulated-gate bipolar transistor), which can be utilised in such high-power applications, is usually below 5kHz. Increasing the switching frequency above this value may result in damage to the switches due to a high junction temperature caused
20 by high switching losses. Furthermore, increasing the operating (switching) frequency increases the manufacturing difficulty of the (isolation) transformer.

The present applicants have appreciated the limitations that are associated with the above solutions
25 of interleaving converters or increasing operation (switching) frequency, and have developed an improved solution that instead alters the topology of the DC-DC converter itself.

An example of such improved topologies according to
30 aspects of the present invention are illustrated in **Figure 2** and **Figure 3**.

As shown in **Figure 2**, the DC-DC converter once again comprises input and output filter capacitors (C_{IN} and C_{OUT}), a diode rectifier D_{1-4} connected in parallel with the

output filter capacitor C_{OUT} , an inductor L_R , and a transformer T_R connected in series to the midpoint of the diode rectifier D_{1-4} . In this particular instance, the converter shown in Figure 2 utilises a switching arrangement corresponding to a half-bridge circuit comprising two switches (Q_{1-2}), rather than the bridge circuit comprising four switches (as was shown in the prior art converter of Figure 1A). Nevertheless, the inductor L_R and the transformer T_R are still connected in series to the mid-points of the half-bridge circuit. More importantly, however, the converter of Figure 2 comprises a plurality (n) of switched resonance units or SRUs, that were not present in the prior art converter. These SRUs are connected in parallel with one another, and have their positive / negative poles connected together. Each SRU comprises two resonant capacitors (C_{rnu} and C_{rnd}) and two bi-directional switches (Q_{rnu} and Q_{rnd}), whereby each of the resonant capacitors is associated with one of the switches. In other words, each SRU comprises at least two switch-capacitor pairs (two switches, each with an associated capacitor). The half-bridge circuit (Q_{1-2}) is connected in parallel to the plurality of SRUs. The mid-points of each of the plurality of SRUs are connected as an AC-point; and the mid-points of the SRUs are connected together. The inductor L_R and transformer T_R are connected in series to the mid-points of each of the SRUs. As will be described in more detail subsequently, the combination of the half-bridge switching arrangement and the switches in each of the SRUs, when operated appropriately allows the respective capacitors within the SRUs to be inserted into or bypassed from the converter circuit as desired. It will be appreciated that there may be more than two switch-capacitor pairs present in each SRU, and/or more than one capacitor associated with each switch, provided

the following criteria are met: that a mid-point of the SRU is connected as an AC-point; and that the circuit configuration on either side of this mid-point is mirrored (i.e., corresponding components are provided on each side of the mid-point). A pair of diodes (D_{a1} and D_{a2}) are also included in the circuit, connected to the SRUs such that a first diode D_{a1} is connected in parallel with one capacitor-switch pair (C_{rnu} and Q_{rnu}) and a second diode D_{a2} is connected in parallel with the other capacitor-switch pair (C_{rnd} and Q_{rnd}). This pair of diodes is utilised to provide a conducting path for the magnetizing current when the switches in the SRUs are turned off.

In some cases, it may also be possible for one or more SRUs to replace some of the diodes in the diode rectifier (e.g., D_3 and D_4); this would result in the SRUs also being connected in parallel to the output capacitor C_o .

A particular embodiment of the above general topology, in which only two SRUs are implemented, is illustrated in **Figure 3**. It will be appreciated that this particular implementation involves a few modifications compared with the more general topology of Figure 2. The bi-directional switches (Q_{rnu} and Q_{rnd}) in each SRU are replaced by uni-directional switches having parallel-connected diodes; additionally, the directions of the switches in the two (adjacent) SRUs are opposite to one another. Moreover, the directions of the two switches *within* each SRU - i.e., on either side of the mid-point of the SRU - are also opposite to one another (e.g., as can be seen from Figure 3, the diodes in switches Q_{r1u} and Q_{r2u} are oppositely oriented to one another, as are the diodes in switches Q_{r1d} and Q_{r2d}). When the resonant capacitors are inserted into or bypassed from the circuit, their corresponding (anti-parallel) diodes may conduct current.

This could cause short circuits of the resonant capacitors, and damage to the switches and other components; such effects can be reduced / minimised if the switches are connected in opposition to one another.

5 Furthermore, in this specific embodiment, the pair of diodes (D_{a1} and D_{a2}) are no longer present as they are no longer required. This is because the anti-parallel diodes associated with the switches in the SRUs provide a potential conducting path for currents regardless of
10 whether the capacitors are inserted into the circuit or not.

The above-described embodiments both have the benefit of being operable utilising modulation strategies that change and optimise the resonant capacitances during
15 each switching period. In particular, these embodiments allow such a result to be achieved via the control of the switches in each of the SRUs so as to regulate the insertion / bypassing of resonant capacitors from the overall circuit. In this manner, the proportion of time
20 during which resonance is achieved during the overall use time of the converter is increased. As a result, large increases in frequency of the input and output current ripples can be achieved via the use of just a single isolated DC-DC converter. Given the inverse relationship
25 between filter capacitance and ripple current, this in turn allows the input and output filter capacitances to be reduced.

The benefits / advantages provided by the aspects and embodiments of the present invention can best be
30 appreciated when considering example use cases. Some of these will now be described with reference to Figures 4, 5 and 6. **Figure 4** illustrates an example modulation strategy for the general topology of Figure 2; and **Figure 5** illustrates corresponding example modulation signals.

Figure 6 illustrates schematically current flow paths that correspond to those example modulation signals and strategy.

Considering **Figure 4**, a first carrier wave having a driving / switching frequency f_s (and a switching period T_s) is defined for the two switches (Q_1 and Q_2) in the half-bridge circuit switching arrangement, and a corresponding duty cycle D_{Q1} is defined. Driving signals G_{Q1} and G_{Q2} are thereby obtained for those two switches (Q_1 and Q_2)- these driving signals are the same in frequency but are complementary to one another (i.e., when one of the switches is turned on, the other is not - they are in anti-phase). Typically, the duty cycle D_{Q1} would be set to 0.5, such that each of the switches is on for half of the switching period T_s (i.e., each of G_{Q1} and G_{Q2} are output sequentially / in turn for $0.5T_s$). However in some cases the duty cycle D_{Q1} can be set to less than 0.5; in such cases, G_{Q2} can be obtained by shifting G_{Q1} by $0.5T_s$ such that the driving signals are still offset from one another by the same amount.

Regarding the operation of the SRUs, a second carrier wave having a driving / switching frequency double that of the first carrier wave - i.e., $2f_s$ - is defined for each pair of switches (Q_{rnu} and Q_{rnd}) of the SRUs. The first and second carrier waves are synchronised with one another, such that they start at the same time. A corresponding duty cycle D_{Qa} is also defined for each pair of switches (Q_{rnu} and Q_{rnd}) of the SRUs; this is set at D_{Q1}/n , where n is the number of SRUs. Additionally, a time delay of $D_a T_s / 2$ is introduced between the carrier waves for the driving signals of adjacent SRUs. Driving signals G_1 , G_2 , etc... up to G_n are thereby obtained for the pair of switches in each SRU, and it will be appreciated that the driving signals for the two switches in the pair (G_{Qrnu} and

G_{Qrnd}) are the same. To maintain voltage balancing amongst the resonant capacitors, the driving signals are rotated in turn before being given to the switches. A simple rotation process, using $n = 3$ (i.e., 3 SRUs) as an example, could occur as follows:

- (1) During the first half-operation period, driving signals G_1 , G_2 , and G_3 are given to G_{Qr1u} , G_{Qr2u} , and G_{Qr3u} , respectively.
- (2) During the second half-operation period, the sequence changes to G_{Qr3u} , G_{Qr1u} and G_{Qr2u} .
- (3) During the third positive half-operation period, the sequence changes to G_{Qr2u} , G_{Qr3u} and G_{Qr1u} .
- (4) During the next half-operation period, the sequence changes back to G_{Qr1u} , G_{Qr2u} and G_{Qr3u} .

The modulation signals and the resulting conduction paths that are associated with the above-described modulation strategy will now be set out with reference to **Figures 5 and 6**. As a general point, because of the way in which the respective duty cycles have been defined above, it will be appreciated from Figure 5 that each half of a switching period T_s corresponds to the duty cycle of one of the switches Q_1 and Q_2 ; and that there are n operation modes during half of a switching period T_s . Now, what happens at specific points of time t_0 , t_1 , t_2 ... within a given switching period T_s (as shown in Figure 5) will be described:

- (a) From t_0 to t_1 : Half-bridge switch Q_1 , and the switches Q_{r1u} and Q_{r1d} in the first SRU are turned on at time t_0 . As a result, the capacitors C_{r1u} and C_{r1d} in the first SRU are connected to the resonant inductor L_R and transformer T_R . The switches in the other SRUs are turned off to bypass the other capacitors. At t_1 , the resonance among capacitors C_{r1u} , C_{r1d} , and inductor L_R ceases. The switches Q_{r1u} and Q_{r1d} in that first SRU are then turned off, and

zero-current-switching (ZCS) is realized. The conduction path during this time period is illustrated in Figure 6(a).

(b) From t_1 to t_2 : Half-bridge switch Q_1 remains on. At t_1 , switches Q_{r2u} and Q_{r2d} in the second SRU are turned on to insert the corresponding capacitors C_{r2u} and C_{r2d} of the second SRU into the circuit. The switches in the other SRUs remain turned off. Hence, the inductor L_R resonates with the capacitors C_{r2u} and C_{r2d} in the second SRU. At t_2 , the resonance ceases and switches Q_{r2u} and Q_{r2d} are turned off with zero current. The conduction path during this time period is illustrated in Figure 6(b).

(c) From t_{n-1} to $T_s/2$: Half-bridge switch Q_1 remains on. At t_{n-1} , switches Q_{rnu} and Q_{rnd} in the n th SRU (i.e., the final SRU in the sequence) are turned on to insert the corresponding capacitors C_{rnu} and C_{rnd} of the n th SRU into the circuit. The switches in the other SRUs remain turned off. Hence, the inductor L_R resonates with the capacitors C_{rnu} and C_{rnd} in the n th SRU. The conduction path during this time period is illustrated in Figure 6(c). At $T_s/2$, the resonance ceases and switches Q_{rnu} and Q_{rnd} are turned off with zero current; their corresponding capacitors are thereby bypassed from the circuit. Additionally, at $T_s/2$, the half-bridge switch Q_1 is turned off and the first half switching period ends.

(d) From $T_s/2$ to $(t_1 + T_s/2)$: The next half switching period starts at $T_s/2$. At this time, half-bridge switch Q_2 , and the two switches Q_{r1u} and Q_{r1d} in the first SRU, are switched on. As a result, the capacitors C_{r1u} and C_{r1d} in the first SRU are once again connected to the resonant inductor L_R and transformer T_R . The switches in the other SRUs are

turned off to bypass the other capacitors. At $t_1 + T_s/2$, the resonance among capacitors C_{r1u} , C_{r1d} , and inductor L_r ceases. The switches Q_{r1u} and Q_{r1d} in that first SRU are turned off, and zero-current-switching (ZCS) is realized. The conduction path during this time period is illustrated in Figure 6(d).

It will be appreciated that the sequence of switching on and off of the rest of the SRUs in turn (as set out in (b) and (c) above) will repeat over this next half switching period until time T_s is reached. At this point, Q_2 is switched off and Q_1 is switched back on again. The sequence of steps (a) to (d) is then repeated over the next switching period. It is also noted that although the above strategy involves switching on and off adjacent SRUs, this does not necessarily have to be the case.

The above modulation strategy enables the resonant capacitors to be sequentially inserted into the circuit, and then bypassed when their resonance ceases; as a result, the resonance repeats n times in half of the switching period. Achieving multiple resonances in each switching period leads to a huge increase in the frequency of input and output current ripples; which in turn means that the filter capacitors may be significantly decreased in value.

Example modulation signals for the specific implementation involving 2 SRUs (as described above in relation to Figure 3) are illustrated in **Figure 7**. In this particular implementation, because there are only 2 SRUs, the switching frequencies of the two half-bridge circuit switches (Q_1 and Q_2) can be defined to be the same as the switching frequencies of the switch pairs in the SRUs; additionally, the duty cycles of each of the switches in both the half-bridge circuit as well as in the SRUs can also be the same - namely, 0.5. As a result, it will be appreciated that not only are the driving signals of Q_1 and

Q_2 complementary (as was the case with the more general implementation described previously); but additionally the switches of the SRUs Q_{riu} and Q_{rid} (where $i=1, 2$) are also operated according to opposite / complementary driving signals. Furthermore, as can be seen from Figure 7, the driving signal of the switches in the SRUs lags or leads (i.e., is offset from) the driving signal of Q_1 by half of the switching period T_s .

The use of only two SRUs, and the corresponding modulation strategy that is employed, has the associated benefit of using a lower switching frequency (as compared with the example implementation of Figures 4 to 6 in which the value of n is 3 or more). Lowering the switching frequency avoids any extra switching losses associated with high switching frequencies, and thereby also increases the efficiency of the converter. Furthermore, where only 2 SRUs are utilised, there is no need to rotate the driving signals; this results in a simpler operation strategy for the converter.

The proposed isolated DC-DC converters described hereinabove have been simulated / tested with the software PLECS, for two example implementations - one having 2SRUs and one having 3SRUs - and the results of these tests / simulations are presented below and in Figures 8 and 9.

For the example implementation involving two SRUs, the following parameters were input:

Input terminal voltage $V_M = 2\text{kV}$

Output terminal voltage $V_L = 1\text{kV}$

Transmission power $P_t = 5\text{MW}$

Switching frequency $f_s = 500\text{Hz}$

Transformer ratio $K:1=1:1$

Resonant capacitor $C_r = 400\mu\text{F}$

Resonant inductor $L_r = 20\mu\text{H}$

Magnetization inductance of transformer: 20mH

Output capacitor $C_{LV} = 100\text{mF}$

The results of the simulation are shown in **Figure 8**. The duty cycle of Q_1 is 0.5 and the output voltage maintains stable at 1kV. The switching frequency of the switches in the SRUs (Q_{r1u} and Q_{r1d}) is the same as that of Q_1 , albeit offset by a time delay. The frequency of the ripple of input and output currents I_{in} and I_o are 2kHz, which is four times the switching frequency. As shown in the figure, two half sine-waves are observed for the currents in each half switching period, indicating that the capacitors in the two SRUs are resonating with the resonant inductor. With the output capacitor set to 100 mF, the peak-to-peak output voltage ripple is 8.506V. This accounts for around 0.85% of the rated output voltage, which could usually meet load requirements. By contrast, to achieve a corresponding output voltage ripple for the conventional converter in Figure 1A, the output filter capacitance would need to be doubled (200mF). Considering the system shown in Figure 1B, two submodules would be required to realise the same output voltage ripple. It will therefore be appreciated that the proposed converter topology and operation reduces the volume and cost of the filter capacitor, and/or reduced the cost and complexity associated with any additional auxiliary circuitry required.

For the example implementation involving three SRUs, the same parameter values were input, with the following exceptions:

Resonant capacitor $C_r = 450\mu\text{F}$

Resonant inductor $L_r = 10\mu\text{H}$

The results of the simulation are shown in **Figure 9**. The same duty cycle of 0.5 is utilised for Q_1 , and the output voltage also maintains stability at 1kV. However, the switching frequency of the switches in the SRUs (Q_{r1u} and Q_{r1d}) is doubled, as can be seen from Figure 9 where the

driving signals of the SRU switches peak twice over the switching period of Q_1 . Moreover, the frequencies of input and output currents I_{in} and I_o are 3kHz, which is six times the switching frequency. As shown in the figure, three half
5 sine-waves are observed for the currents in each half switching period: as the peaks indicate that the capacitors in the three SRUs are resonating with the resonant inductor, resonance is shown to be achieved three times in each half switching period. With the output capacitor set to 100 mF,
10 the peak-to-peak output voltage ripple is 5.294V. This result verifies the feasibility of the proposed converter, and its control method, in reducing the filter capacitance required.

By comparing these two example implementations, it will
15 be appreciated that with the increase in number of SRUs used, the frequency of input and output currents increases, and the input and output voltage ripple decreases. This corresponds to a reduction in the required input and output filter capacitance, taking into consideration the same input
20 / output voltage ripple. There are hence also certain advantages to be obtained by implementing an increased number of SRUs.

In view of the benefits that are achieved by the above-described embodiments, it will be appreciated that the
25 proposed DC-DC converters have high current capacity, and are suitable for use in low-voltage DC applications with a voltage typically below 5kV and a current above hundreds of Amperes. Compared with existing isolated DC converters for such high current applications, the proposed DC converters
30 described above possess smaller filter capacitors and high efficiency simultaneously, leading to a reduction in the cost and volume / weight.

The proposed converters of the present invention can be utilised to realise voltage conversion and galvanic

insulation between two DC terminals. In particular, the potential applications of the proposed converters include the power supply for water electrolyzers or interconnection in DC collection systems where this converter topology could
5 be repeatedly used in series or parallel (e.g., solar farms with DC cabling, offshore or onshore wind farms with DC inter-array cabling, etc.).

While many possible variations of the isolated DC-DC converter topology and its implementation have been
10 described above, it will be clear to the skilled person that additional variations and modifications can be made without departing from the scope of the invention as claimed in the appended claims.

- 21 -

C L A I M S

1. An isolated DC-DC converter comprising:

an input filter capacitor;
an output filter capacitor;
a transformer;

5 a plurality n of switched resonance units, SRUs,
wherein each SRU comprises at least two switch-capacitor
pairs, each switch-capacitor pair comprising a switch and
an associated resonant capacitor; and

10 a switching arrangement operatively-coupled to the
transformer and to the plurality of SRUs;

wherein the switches in each of the plurality of
SRUs, in combination with the switching arrangement, are
operable to, in turn, operatively connect their associated
capacitors with the transformer, to achieve resonance.

15

2. A DC-DC converter as claimed in claim 1, further
comprising a resonant inductor operatively coupled to the
transformer.

20

3. A DC-DC converter as claimed in claim 1 or claim 2,
wherein the plurality of SRUs are connected in parallel
with one another, and in parallel with the input
capacitor.

25

4. A DC-DC converter as claimed in any preceding claim,
wherein the plurality of SRUs are connected in parallel
with the switching arrangement.

30

5. A DC-DC converter as claimed in any preceding claim,
wherein:

a midpoint of each SRU is connected as an ac point;
and

the transformer is connected in series with the
midpoint of each of the plurality of SRUs.

5

6. A DC-DC converter as claimed in any preceding claim,
wherein:

10

switches in the switching arrangement have a first
duty cycle D_0 , and the switches in each of the plurality
(n) of SRUs have a second duty cycle of $1/n$ of the first
duty cycle D_0 .

7. A DC-DC converter as claimed in any preceding claim,
wherein:

15

the switching arrangement corresponds to a half-
bridge circuit comprising a pair of switches (Q_1 , Q_2) and
is operated by a first driving signal having a first
switching frequency; and

20

the switches in each of the plurality of SRUs are
operated by a second driving signal having a second
switching frequency.

25

8. A DC-DC converter as claimed in claim 7, wherein the
second switching frequency is double the first switching
frequency.

30

9. A DC-DC converter as claimed in any preceding claim,
wherein each switch-capacitor pair comprises a resonant
capacitor and a bi-directional switch.

10. A DC-DC converter as claimed in any preceding claim,
wherein input driving signals for the switches in each of
the plurality of SRUs are rotated in turn before being
provided to the respective switches.

11. A DC-DC converter as claimed in any preceding claim,
further comprising at least one pair of diodes connected
in parallel between the input capacitor and the plurality
of SRUs.

12. A DC-DC converter as claimed in any of claims 1 to 8,
wherein:

two SRUs are utilised; and

each switch-capacitor pair comprises a resonant
capacitor and a uni-directional switch, wherein the
switches within each SRU are connected in opposition to
one another; and the switches in adjacent SRUs are
connected in opposition to one another.

13. A DC-DC converter as claimed in claim 12, wherein:

the first and second switching frequencies are
substantially the same.

14. A DC-DC converter as claimed in claim 12 or claim 13,
wherein input driving signals provided to the SRUs are
offset from input driving signals for the switches of the
switching arrangement by a quarter of a switching period.

15. A method of operating an isolated DC-DC converter for
use in power supply, the DC-DC converter comprising:

an input filter capacitor;

an output filter capacitor;

a transformer;

a plurality n of switched resonance units, SRUs,
wherein each SRU comprises at least two switch-capacitor
pairs, each switch-capacitor pair comprising a switch and
an associated resonant capacitor; and

a switching arrangement operatively-coupled to the transformer, and to the plurality of SRUs, and comprising first and second switches;

the method comprising:

5 (i) turning on the first switch of the switching arrangement and the switches of a first one of the plurality of SRUs, such that the associated capacitors in the first SRU are operatively connected to the transformer to achieve resonance;

10 whilst the first switch of the switching arrangement remains on:

 (ii) turning off the switches of the first SRU and turning on the switches of a second SRU such that the associated capacitors in the second SRU are operatively
15 connected to the transformer to achieve resonance;

 (iii) repeating step (ii) sequentially for pairs of SRUs in turn;

 (iv) turning off the first switch of the switching arrangement;

20 (v) turning on the second switch of the switching arrangement and turning on the switches of the first SRU such that the associated capacitors in the first SRU are operatively connected to the transformer to achieve resonance;

25 (v) whilst the second switch of the switching arrangement remains on, repeating steps (ii) and (iii) sequentially for pairs of SRUs in turn.

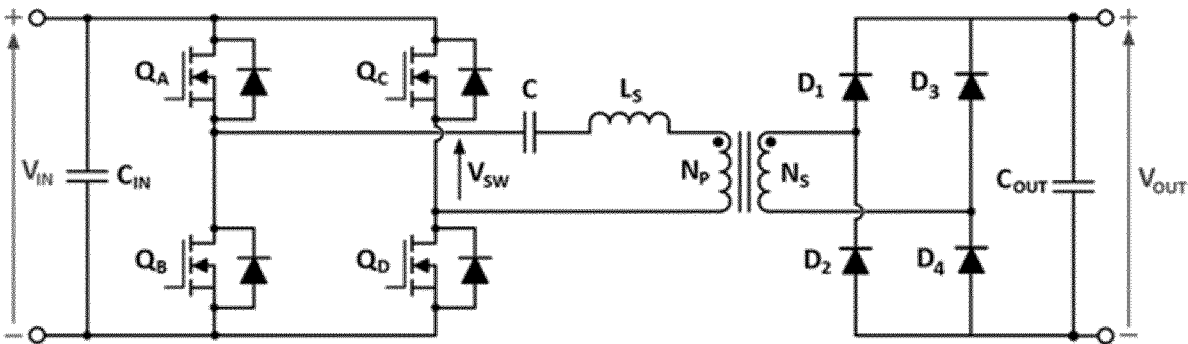


FIGURE 1A (Prior Art)

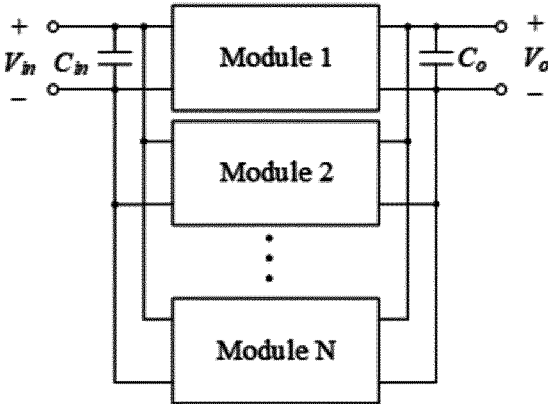


FIGURE 1B (Prior Art)

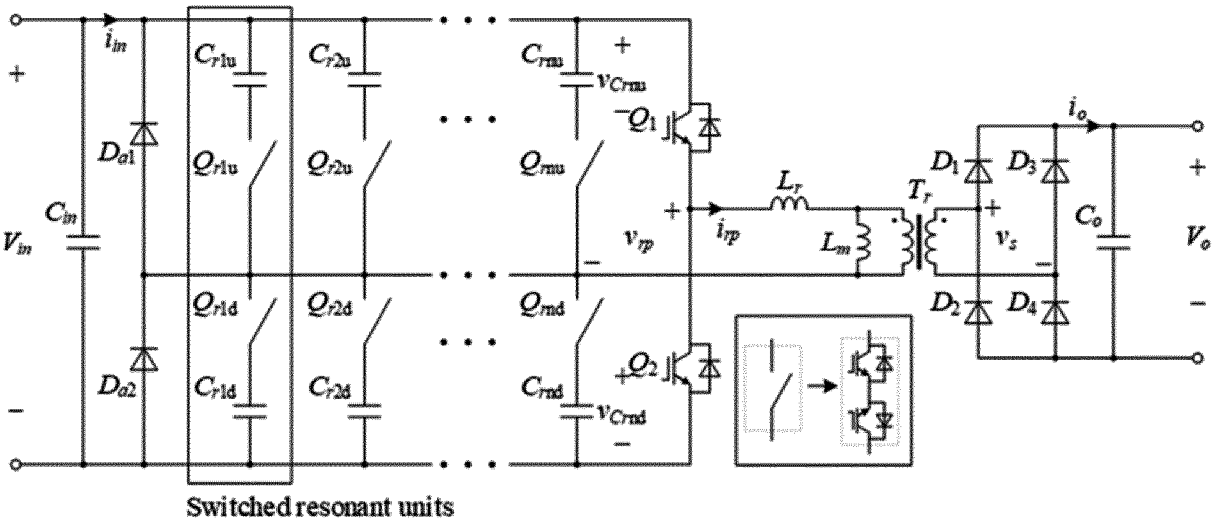


FIGURE 2

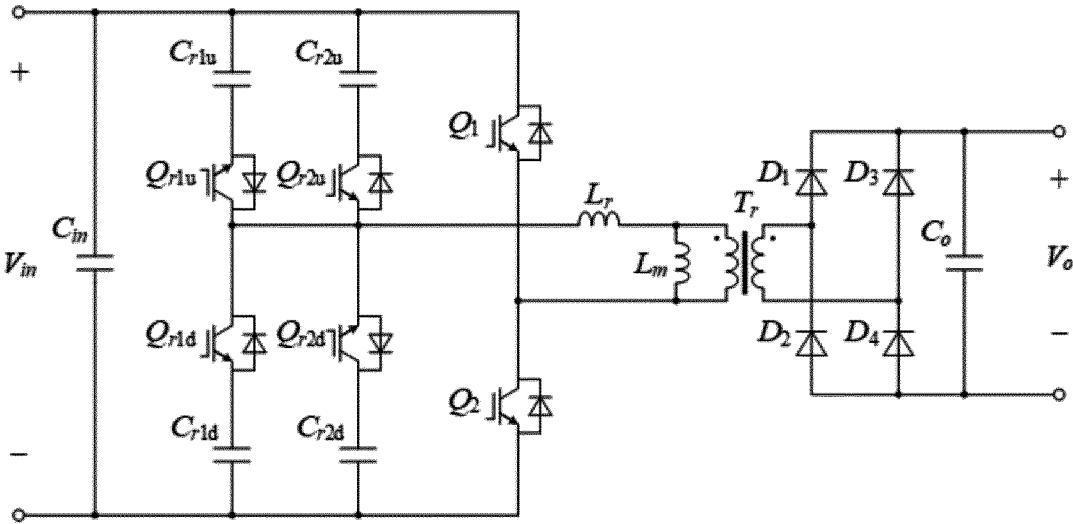


FIGURE 3

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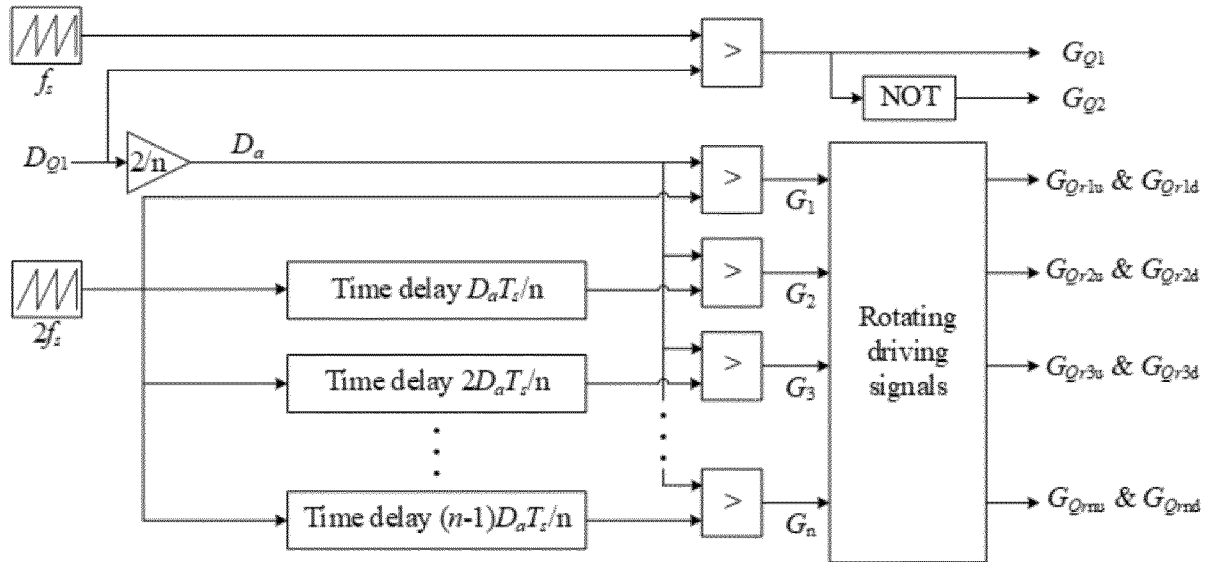


FIGURE 4

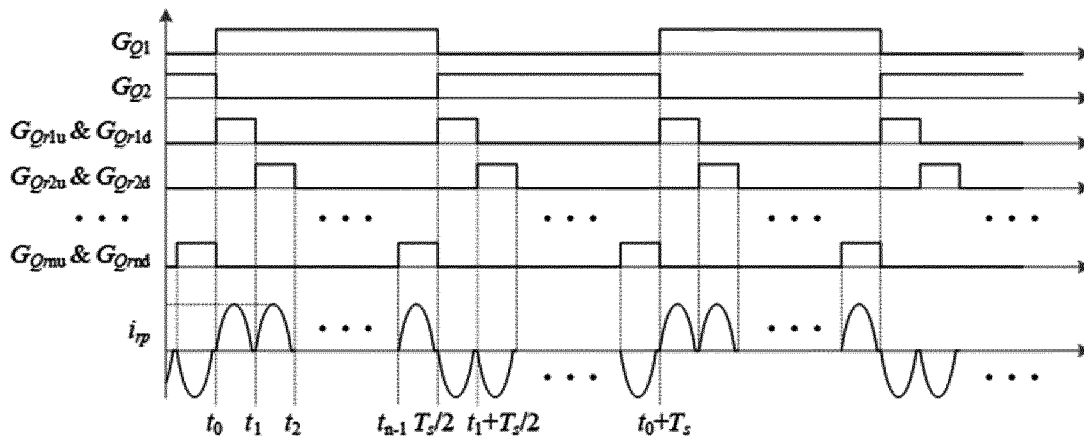


FIGURE 5

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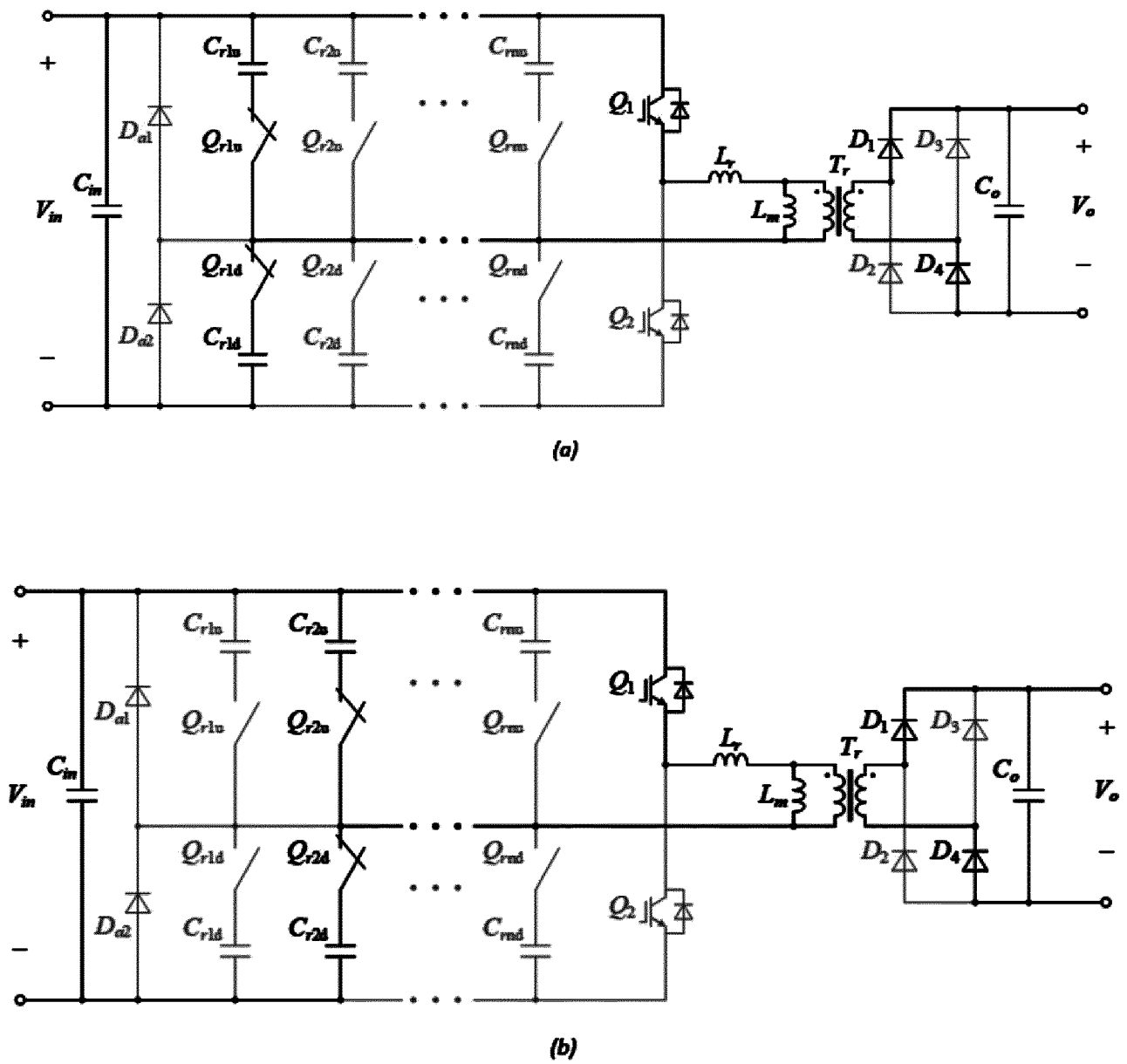


FIGURE 6

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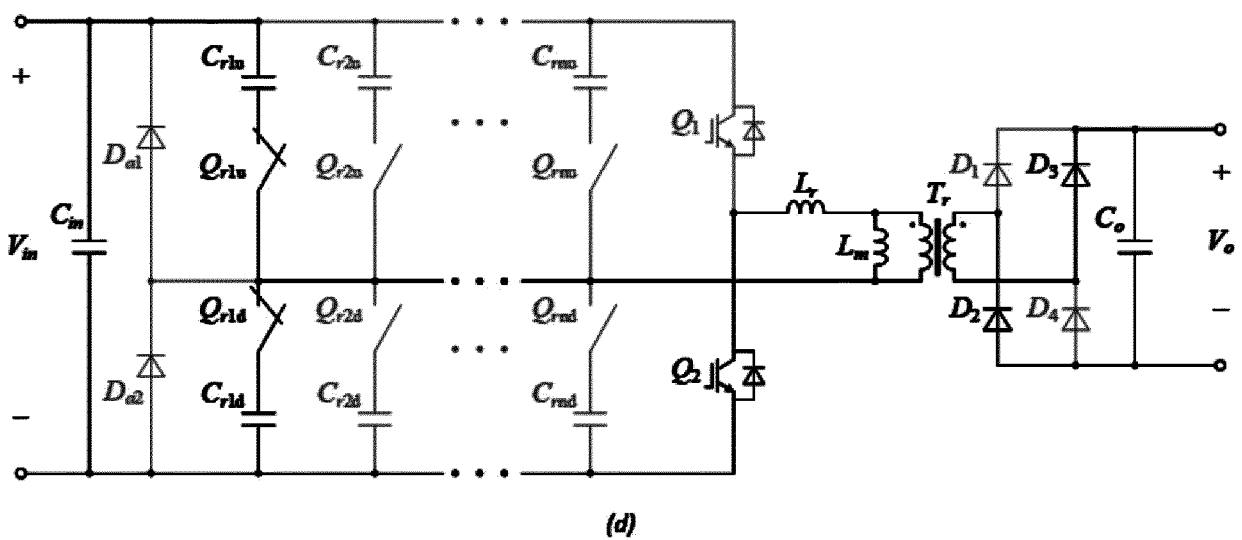
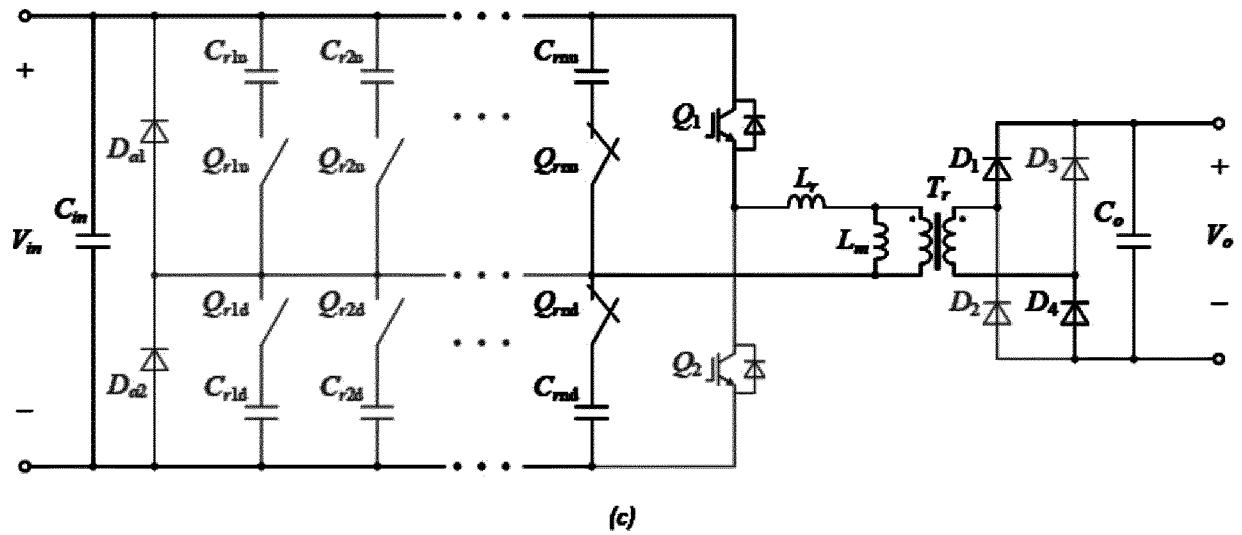


FIGURE 6
(continued)

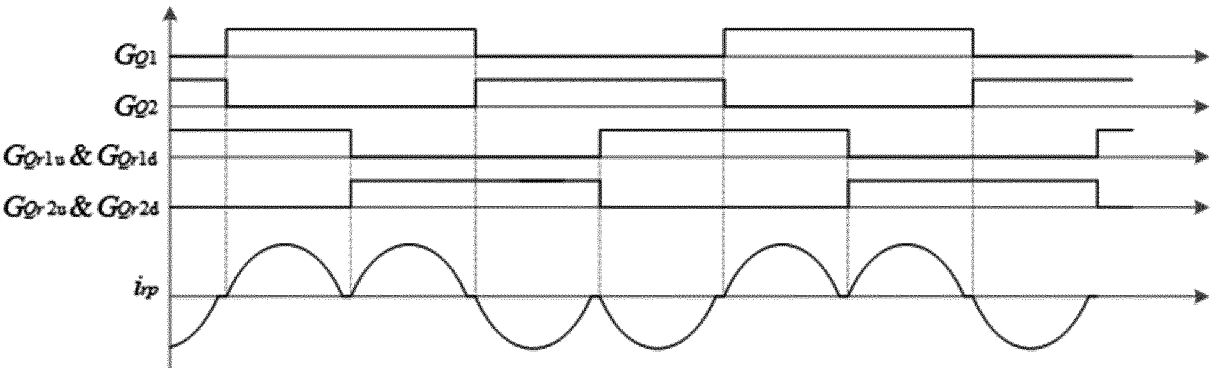


FIGURE 7

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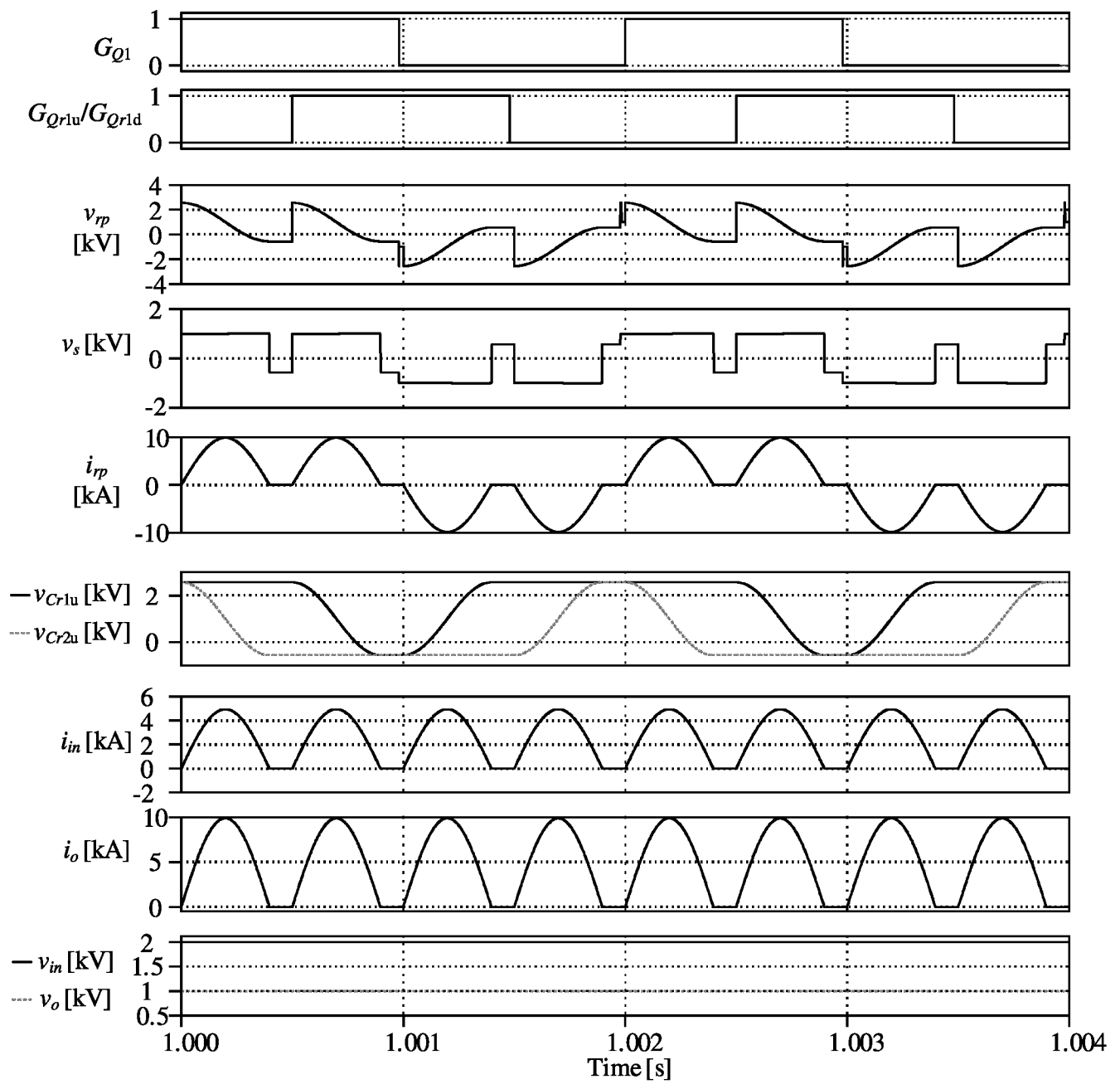


FIGURE 8

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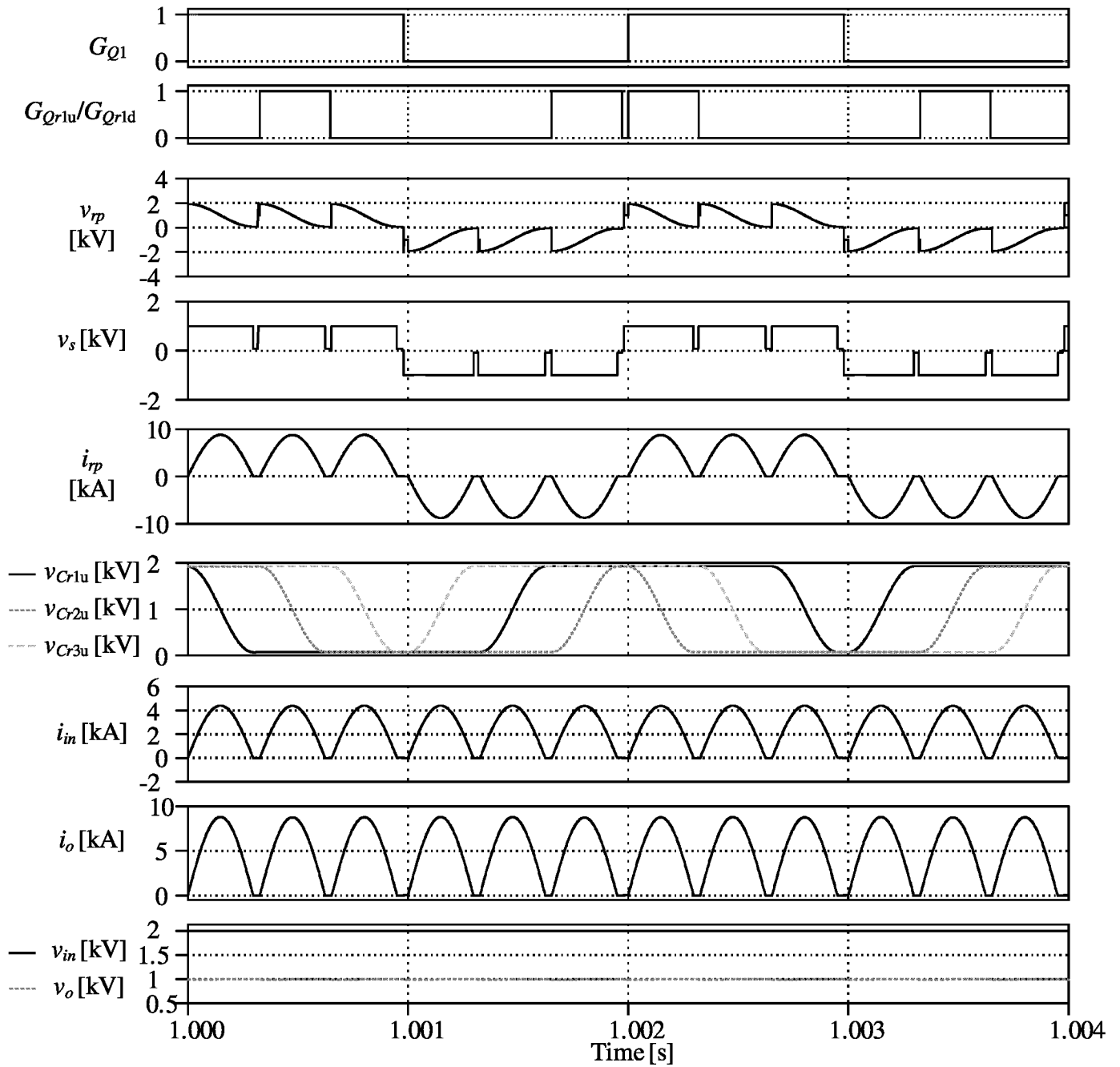


FIGURE 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2024/084676

A. CLASSIFICATION OF SUBJECT MATTER					
INV.	H02M3/00	H02M3/02	H02M3/145	H02M1/00	H02M1/15
	H02M3/335				
ADD.					
According to International Patent Classification (IPC) or to both national classification and IPC					
B. FIELDS SEARCHED					
Minimum documentation searched (classification system followed by classification symbols)					
H02M					
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched					
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)					
EPO-Internal, WPI Data					
C. DOCUMENTS CONSIDERED TO BE RELEVANT					
Category*	Citation of document, with indication, where appropriate, of the relevant passages				Relevant to claim No.
X	CN 114 665 705 A (MEDIUM ELECTRICITY PREY ELECTRIC POWER ENGINEERING LTD COMPANY ET AL.) 24 June 2022 (2022-06-24)				1-7, 9-11,15
A	paragraph [0004] - paragraph [0036]; figures 1-12 paragraph [0080] - paragraph [0095] -----				8,12-14
☐ Further documents are listed in the continuation of Box C.					
☒ See patent family annex.					
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"A" document defining the general state of the art which is not considered to be of particular relevance			"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention		
"E" earlier application or patent but published on or after the international filing date			"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone		
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Date of the actual completion of the international search			Date of mailing of the international search report		
7 January 2025			16/01/2025		
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016			Authorized officer Roussel, Maxime		

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2024/084676

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
CN 114665705	A	24-06-2022	NONE
