

[54] **FAIL-SAFE TIME DELAY RELAY**

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307/293

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[58] Field of Search..... **317/142 R, 141 S; 307/293**

[56] **References Cited**

UNITED STATES PATENTS

3,407,340 10/1968 Hufnagel..... **317/141 S**

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[57] **ABSTRACT**

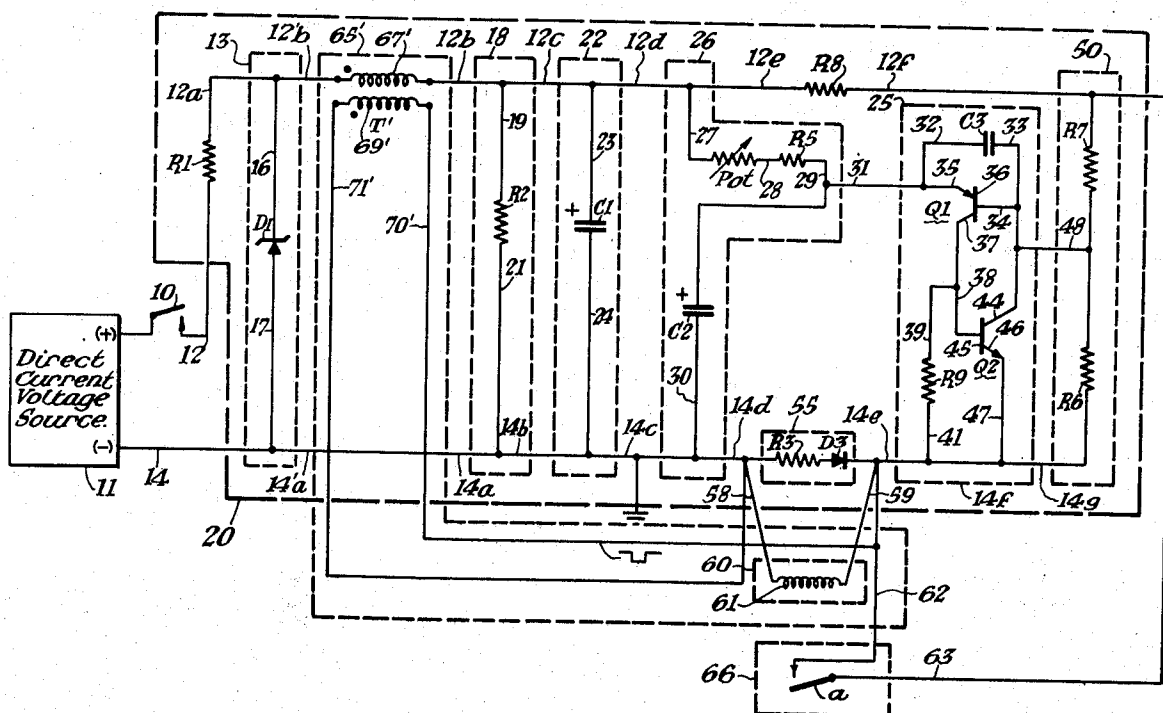
This invention relates to a fail-safe solid state time element relay circuit to prevent relay energization and pickup where there has been an open circuit condition during the timing cycle. The circuit includes the following components, electrically connected respective-

ly to each other: an externally controlled direct current voltage source, a predetermined time delay voltage storage means, a solid state relay energization control means and a relay. In addition there is safety voltage storage means respectively electrically connected to the direct current voltage source and to a pulse source which is in turn electrically coupled to the relay to offset the charge of the predetermined time delay storage means in the event that the direct current voltage source should be momentarily disconnected from the remainder of the time element relay circuit to thereby ensure there would not be a relay actuation before the end of the predetermined time delay.

In one embodiment of the invention the discharge means is a current transformer which produces a pulse and has a primary winding electrically connected in series with the externally controlled direct current voltage source and a secondary winding electrically connected to the relay.

In the second embodiment the pulse transformer is a voltage transformer with its primary winding connected in series with the externally controlled direct current voltage source and in series with the predetermined time delay voltage storage means and the solid state relay energization control means.

3 Claims, 2 Drawing Figures



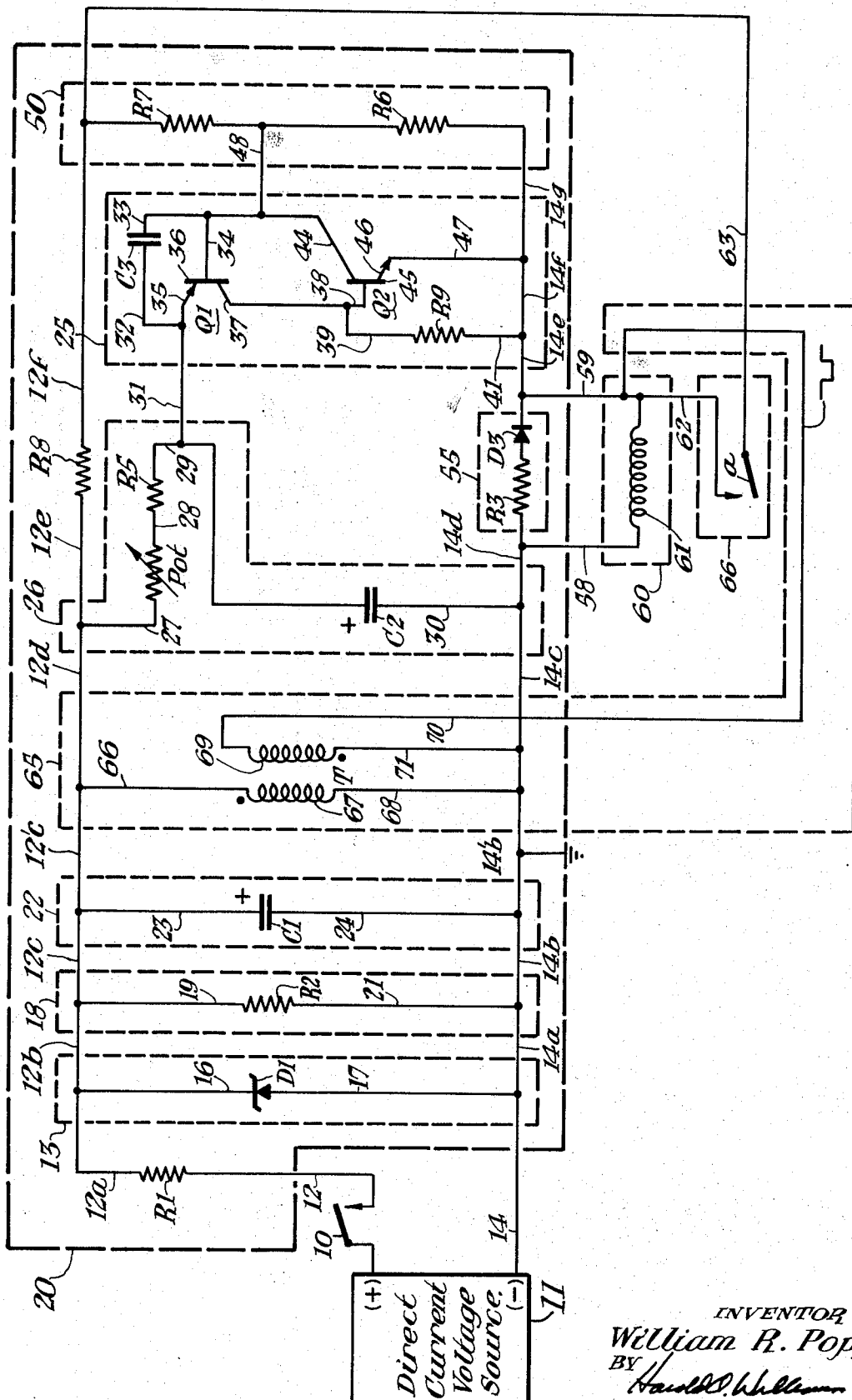


Fig. 1.

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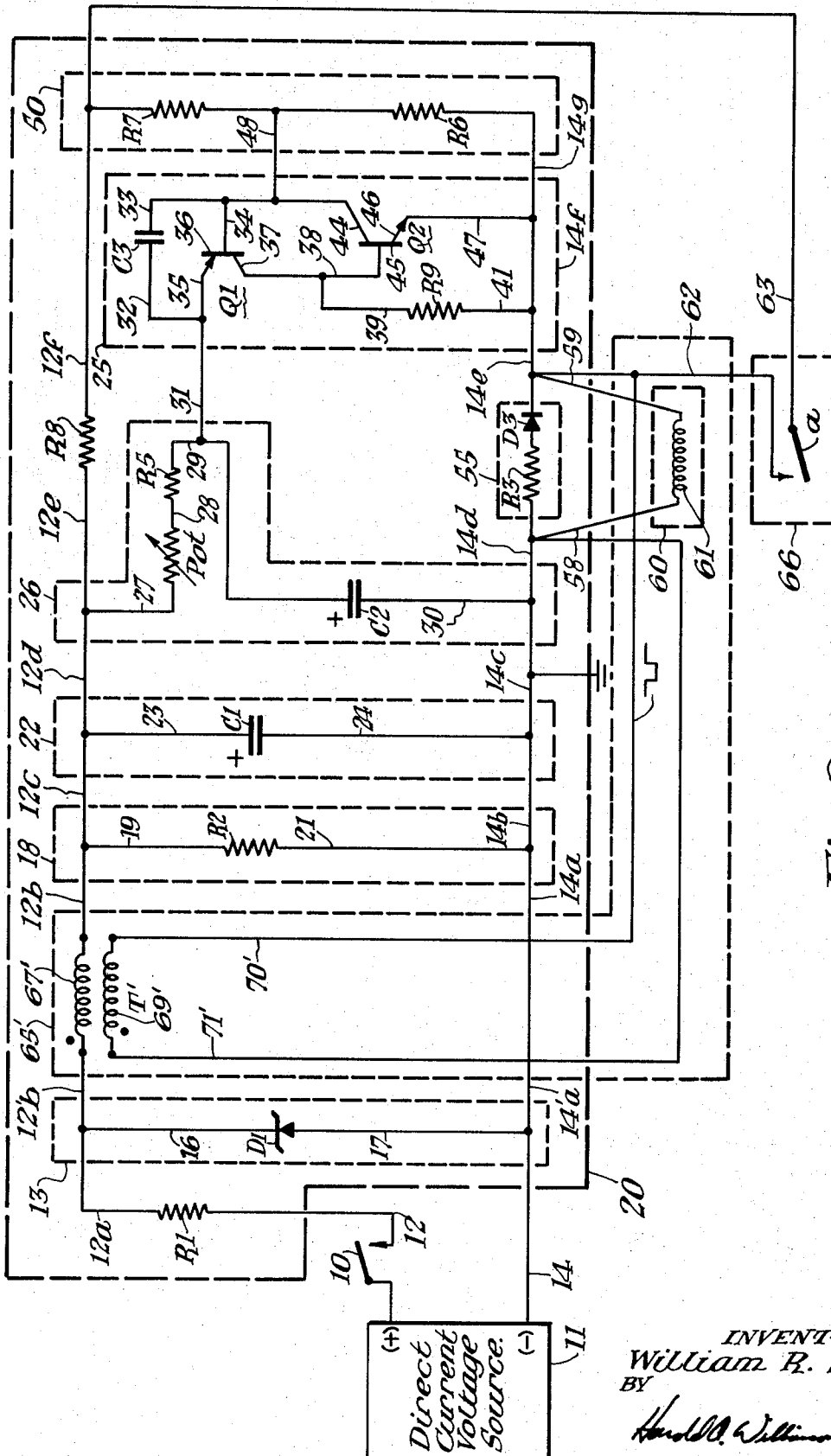


Fig. 2.

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FAIL-SAFE TIME DELAY RELAY

This invention relates to a fail-safe solid state time element relay circuit.

More specifically this invention relates to a fail-safe solid state time element relay circuit to prevent relay energization and pickup during the timing cycle. A pulse source is electrically coupled to the relay and a pair of circuits which provide both the means to establish a predetermined time delay and means to energize the relay from a direct current voltage source. The pulse source comes into operation in the event that there is a momentary interruption in power from an externally controlled direct current voltage source.

This invention is an improvement over U.S. Pat. No. 3,407,340, issued Oct. 22, 1968, to Andrew Hufnagel, for Fail-Safe Time Delay Relay, and assigned to the assignee of the present application.

This invention finds particular application in railway wayside equipment where the track involved is divided into track sections with each track section having a signal at its exit end to control movement of trains in the block or track section. It is desirable in heavy traffic density areas of mass transit to provide minimal headways between trains. It is imperative that when a train enters a track section or block the signal at the exit end not be cleared immediately so that the train may pass into the next section or block. From the standpoint of safety there must be some predetermined delay in changing the signal in order that the train, if it must, be able to stop or proceed within the track section at some reduced headway speed dictated by the aspect of the signal at the exit end of the track section or block. Prior art relays of the mechanical time delay type have been utilized to provide such a delay once the train has entered the track section. In view of the above discussion it can be appreciated that the time period of delay under no circumstances should be reduced in length of time because this would be an unsafe failure since the signal at the end of the track section entered will clear and this is an unsafe condition because the train may then proceed into the next track section which may place the train in a position too close to the train ahead. This reduced headway is a dangerous condition. The signal at the exit end of the track section entered is controlled by a track relay which also controls the actuation of the time delay relay which in turn controls the signal at the exit end of the track section. A major problem arises in the control of the time delay relay when there arises a temporary unshunting of the rails in the track section and the track relay becomes energized momentarily, thereby disconnecting the power source to the time delay relay. The loss of shunt across the rails may occur due to foreign deposits on the rails themselves. Should this unshunting occur near the end of the timing period, there may be sufficient stored energy present to energize the time delay relay which results in a shortened time delay and time delay relay actuation with a concomitant clearing of the signal at the exit end in a shorter period than is considered safe.

The improvement invention to be described hereinafter removes this problem by assuring that the time delay relay never is actuated by loss of track circuit shunt at any time during the preselected time delay. In addition, should there be a momentary loss of track rail shunt, the time delay will restart its time delay period which of course is a failure to safe condition.

It is therefore a primary object of this invention to provide a fail-safe time delay relay which will always start a new timing cycle should there be any momentary interruption in delivery of power to the relay circuitry.

A further object of this invention is to provide a pulse source which offsets the charge of a time delay capacitor used in conjunction with a solid state relay energization circuit in the event that there is a momentary or permanent interruption in the delivery of power to the relay circuitry.

In the attainment of the foregoing objects this invention provides a fail-safe solid state circuit and relay to prevent relay energization and pickup where there has been an open circuit condition during the timing cycle. The time element relay has in combination an externally controlled direct current voltage source and a solid state relay energization control circuit. A predetermined time delay voltage storage circuit is electrically connected to the solid state relay energization control circuit, which control circuit has in turn a relay electrically connected thereto. A pulse source is provided for the time delay voltage storage circuit. A safety voltage storage circuit is electrically connected to the direct current voltage source and to the pulse source. The pulse source is in turn electrically connected to the safety voltage storage circuit and the predetermined time delay storage circuit. The pulse source is electrically coupled to the relay to provide a pulse source which offsets a charge from the predetermined time delay storage circuit in the event that the direct current voltage source should be momentarily disconnected from the remainder of the time element relay circuit to thereby ensure that there would not be a relay actuation before the end of the predetermined time delay.

The safety voltage storage circuit noted earlier is provided to store energy from the direct current voltage source to thereby provide a standby reference voltage to the solid state relay energization control circuit. An excess voltage drainoff circuit is provided for the time delay voltage circuit and is electrically connected thereto. A reference voltage control circuit is electrically connected to the solid state relay energization control circuit. Finally there is provided a bypass circuit for the solid state relay energization control circuit and the reference voltage control circuit. The bypass circuit is electrically connected to the direct current voltage source and is controlled by the relay to provide a bypass circuit to maintain the relay energized.

In one embodiment of the invention the pulse source is a current transformer which produces a pulse and has a primary winding electrically connected in series with the externally controlled direct current voltage source and a secondary winding electrically connected to the relay. The current transformer's pulse offsets any charge that may be developed by the time delay storage circuit.

In the second embodiment the pulse transformer is a voltage transformer with its primary winding connected in series with the externally controlled direct current voltage source and in series with the predetermined time delay voltage storage circuit and the solid state relay energization control circuit.

Other objects and advantages of the present system will become apparent from the ensuing description of illustrative embodiments thereof, in the course of which reference is had to the accompanying drawings in which:

FIG. 1 is a circuit embodying the invention.

FIG. 2 is a circuit with a second embodiment of the invention.

A description of the above embodiments will follow and then the novel features of the invention will be presented in the appended claims.

Reference is now made to FIG. 1. In FIG. 1 there is depicted a circuit which provides the variable time delay sought by this invention. It will be noted that there appear not only the basic components of the circuitry set forth here but there are a number of blocks or boxes shown in dotted outline. Each of these blocks or boxes shown in dotted outline is intended to include one or more of the various means to be referred to hereafter. It is hoped that this approach will aid in the understanding of what is intended to be included in the various means recited hereafter, and what is intended to be included within each of the various means as the description ensues. Furthermore, it is believed that this approach will facilitate an understanding of the claims which appear appended hereafter, and set forth the precise invention as claimed.

Accordingly, there is presented here a direct current voltage source 11. In this instance the direct current voltage source may be a 10, 12 or 16-volt source and the delay for this system, as shown in this preferred embodiment, may range from 3 to 30 seconds and from ½ to 5 minutes in duration. It will be appreciated that while these are suggested ranges of time delay, they may be varied to be longer or shorter dependent upon the circuit parameters selected by those wishing to employ the invention.

Accordingly, it is seen that there is a direct current voltage source 11 which supplies the power to operate a relay 60, shown here in dotted outline in the right-hand portion of FIG. 1. This relay 60 and its coil 61 is the principal component to be operated at the end of a predetermined time delay which has been designed into the system. It will be seen that two electrical leads 12 and 14 emanate from the direct current voltage source 11. The electrical lead 12 has a portion thereof interrupted by the presence of a switch 10 which will control the application of the direct current energy to the various components in the circuit to be described. In actual practice this switch 10 may be controlled by the track relay in the section of track entered by the train. Accordingly, this normally open switch 10 will close when a train enters the track section and the track relay is deenergized due to the shunting of the rails by the train's wheels and related axles. The electrical leads 12 and 14, to the extent that they are the same electrical leads, have portions thereof designated 12a through 12f and 14a through 14g, respectively, as well as 12c' and 14b'. This has been done to further enhance the understanding of the theory of the circuit operation which will now ensue.

Serially connected to the input lead 12 is a resistor R1, which resistor R1 limits the power input to the circuitry and has a value selected to match the nominal supply voltage. Connected across the electrical leads

12a and 14 is a Zener diode D1 which limits the voltage which will appear across the electrical leads 12a and 14 to a predetermined maximum level. This Zener diode D1, which is incorporated in the dotted outline portion of this figure, has been designated a voltage limiting means 13 and this voltage limiting means 13, which includes the Zener diode D1, provides the capacity to prevent the delivery of momentary increases in power to the remaining portions of the circuitry depicted to the right of the Zener diode D1. In other words, momentary increases in power supply voltage from the direct current voltage source 11 will be clipped off by the Zener diode D1. This increase which may arise may trace its source to a sudden voltage pulse in the line wires when the direct current voltage source and its related system is involved in railway signaling. It goes without saying that any sudden voltage increase will have its effectiveness controlled by the Zener diode D1 of the voltage limiting means 13.

Connected across the electrical leads 12b and 14a is a resistor R2 which is enclosed in a dotted outline block which will be designated as the excess voltage drainoff means, the precise function of which will be made clear hereafter. The electrical leads 12b and 14a and their extensions 12c and 14b convey the supply voltage to the capacitor C1 connected by electrical leads 23 and 24 to the leads 12c and 14b. The capacitor C1 is shown enclosed in the dotted outline box 22 and will be referred to hereafter as a safety voltage storage means 22. Adjacent to the safety voltage storage means there is a box shown in dotted outline and designated by the reference numeral 65 and is referred to as a pulse source. Its function will be described more fully hereinafter. The pulse source 65 is electrically connected to the safety voltage storage means 22 by leads 12c' and 14b' and a transformer T via leads 66 and 68, respectively. The pulse transformer T has a primary winding 67 connected to the leads 66 and 68 and a secondary winding 69 connected by lead 71 to lead 14b' and via lead 70 to lead 59 of the relay 60 with its relay coil 61 in series therewith.

Adjacent to the pulse source 65 there is a box shown in dotted outline and designated by the reference numeral 26. This will be hereafter referred to as an adjustable time delay storage means. This adjustable time delay storage means includes a variable resistance potentiometer connected electrically by lead 27 to the lead 12d. There is also a resistor R5 in series with the variable potentiometer connected thereto by electrical lead 28. The resistor R5 and its function in the system will be explained hereafter. The resistor R5 is connected electrically via the electrical lead 29 to a capacitor C2, as well as by an electrical lead 21 to the emitter 35 of a transistor Q1. This transistor Q1 will be referred to hereafter as the first transistor. The capacitor C2 is in turn connected to the electrical lead 14c by lead 30. It will be appreciated that the electrical lead 14, as well as leads 14a, 14b, 14b', 14c and 14d, is respectively electrically connected to a ground depicted here at the bottom of the figure. This ground is a connection to a magnetic shielding 20 shown in dotted outline. This magnetic shielding 20 and its function will be explained more fully hereafter.

The adjustable time delay storage means 26 is connected via electrical lead 12e, a resistor R8, and lead

12f, to the reference voltage control means 50, which reference voltage control means 50 is shown in dotted outline. The reference voltage control means 50 includes a pair of resistors R6 and R7. Interposed between the reference voltage control means 50 and the adjustable time delay storage means 26 is a solid state relay energization control means 25, which solid state relay energization control means 25 has a pair of transistors Q1 and Q2. The emitter 35 of first transistor Q1, as has been noted, is electrically connected via the lead 31 to the adjustable time delay voltage storage means 26. The base 36 of the transistor Q1 is connected by lead 34 to a lead 33 which in turn is connected by lead 48 to the reference voltage control means 50. The collector 37 of the transistor Q1 is electrically connected via the lead 38 to the base 45 of the second transistor Q2, while the collector 44 of the second transistor Q2 is electrically connected to the lead 33 which in turn is electrically connected to the lead 34 and the base 36 of the transistor Q1. The collector 37 of the first transistor Q1, as well as the base 45 of the second transistor Q2, is mutually electrically connected via the lead 38 and the lead 39 to a resistor R9, and lead 41 to electrical lead 14e.

Interposed in the circuitry between the adjustable time delay storage means 26 and the solid state relay energization control means 25 is a signal transient suppression means 55. This signal transient suppression means 55, shown in dotted outline, includes a resistor R3 and a diode D3 in series between the electrical leads 58 and 59 which emanate from the leads 14d and 14e, respectively. Leads 58 and 59 are connected to the opposite ends of the relay coil 61 of the relay 60 shown in dotted outline. Directly beneath the relay 60 is a box shown in dotted outline which will be referred to hereafter as a bypass means 66. This bypass means 66 includes a contact a which completes a circuit between the right-hand end of the relay coil 61 and the reference voltage control means 50 over the electrical lead 63 which enters at the top right-hand corner of the reference voltage control means 50. It will be appreciated that when the relay 60 is energized it is intended that the contact a be picked up and complete a circuit over the front contact a of this relay 60, and at this point the bypass means 66 will complete a circuit, as noted earlier, and there will be a circuit completed from the reference voltage control means 50 through the lead 63, front contact a of the relay 60, lead 62, coil 61, lead 58, leads 14d, 14c, 14b', 14b, 14a and 14 to the direct current voltage source to thereby provide a circuit which will maintain the relay 60 energized.

Reference is now made to FIG. 2 in which many of the components are the same as in FIG. 1. Accordingly, no discussion will be made with reference to components which have already been mentioned and named earlier in the description. This embodiment of the invention differs in that there is a pulse source 65' interposed between the voltage limiting means 13 and the voltage drainoff means 18 connected respectively by leads 12b' and 12b. The pulse source includes a transformer T' having its primary coil 67' connected in series with the direct current voltage source 11. The primary coil 67' of transformer T' is also electrically connected in series with the predetermined time delay means 26.

Turning now to the operation of the circuits just described, when a train enters a track section, as noted earlier, and the wheels and axle of the train shunt the rails, the track relay for this section is deenergized and releases switch 10, thereby completing a circuit between the voltage source 11 and the adjustable time delay relay circuitry depicted to the right in each of FIGS. 1 and 2.

Upon the closing of the switch 10 the voltage level, which is controlled as has been noted by the voltage limiting means 13, will therefore appear across some of the remaining components depicted to the right of the voltage limiting means 13. The direct current voltage selected for this particular design would be approximately 7.5 volts. the resistors R6 and R7, which form the reference voltage control means 50, act as a voltage divider for the transistors Q1 and Q2. These resistors R6 and R7, which are much higher in resistance than the resistor R8 and the resistance of the coil 61, provide a trigger reference voltage for the transistors Q1 and Q2 of the solid state relay energization control means 25. The resistors R6 and R7 function as a conventional voltage divider which provides the reference voltage to be applied to the base 36 of the first transistor Q1 via the leads 34, 33 and 32.

The adjustable time delay storage means 26, as has been noted, includes a capacitor C2. This capacitor C2 charges gradually through the time adjustment variable resistance potentiometer over the electrical leads 27, 28, resistor R5, lead 29, to the capacitor C2 which is connected via the lead 30 to ground. Resistor R5 limits the minimum time adjustment for the time delay function of the circuit while the variable resistance potentiometer may be varied to control the time required to charge the capacitor C2 and therefore provide the adjustable time delay for the time delay relay circuitry being described.

The transistor Q1 of the solid state relay energization control means 25 will conduct when the emitter 35 becomes more positive than the base 36. This will occur after the capacitor C2 under ideal conditions in the adjustable time delay storage means 26 has been charged to a point where the voltage present in the capacitor C2 exceeds the reference voltage provided by the reference voltage control means 50 and its related resistor R6 and R7. In other words, when the emitter 35 of the transistor Q1 becomes more positive than the base 36 of the transistor Q1, transistor Q1 will conduct and the capacitor C2, in a manner to be described hereafter, will discharge through the lead 29, lead 31, to the transistor Q1. The transistor Q1, in this embodiment of the invention, is normally nonconducting until capacitor C2 has charged to a level which approaches and then exceeds the voltage reference level provided by the resistors R6 and R7 of the reference voltage control means 50. When transistor Q1 conducts it will bias transistor Q2 into conduction. In other words, the base 45 of the transistor Q2 will become more positive than its emitter 46.

With transistor Q2 conducting, transistor Q1 will be further biased into conduction. This further biasing of transistor Q1 into conduction is a regenerative action and therefore drives both transistors Q1 and Q2 into saturation, and they will remain triggered until the current through them is reduced to some small value in-

herent in the transistors selected. As has been noted, once the capacitor C2 of the adjustable time delay storage means 26 has been charged to a level which exceeds the reference voltage supplied by the reference voltage control means 50, the capacitor C2 will discharge through electrical leads 29, 31, transistor Q1, and transistor Q2 to leads 14f, 14e, 59, through relay coil 61 of relay 60, lead 58, leads 14d, 30 to the capacitor C2, thereby causing the relay 60 to pick up due to energy from capacitor C2, and close the contact *a* of the bypass means 66 which therefore completes a circuit from the right-hand end of coil 61 over the lead 62, the front contact *a* of the relay 60, lead 63, to the lead 12f, where the lead 12f enters the reference voltage control means 50. This completed circuit just noted will hold the relay 60 picked up by the circuit just described, due to energy from the direct current voltage source. This completed circuit causes the reference voltage at the junction of the resistors R6 and R7 to go to zero, and the transistors Q1 and Q2 remain conductive due to a very small current which is above the cutoff current of the transistors Q1 and Q2, which current passes through the variable resistance potentiometer and the resistance R5 of the adjustable time delay storage means 26, and the transistors Q1, Q2 and the leads 14f, 14e, 59, coil 61, lead 58, 14d, lead 14c to ground. It is therefore to be appreciated that the relay 60 is maintained energized by the bypass circuit which includes the bypass means 66 but there is an additional path in which a low level of current is constantly flowing. That path includes the transistor Q1 and Q2 just noted.

In the preferred embodiment the voltage drop in the transistors Q1 and Q2 at this point in the operation is about 0.4 of a volt, and the voltage drop in the coil 61, due to the holding current, is about 2.7 volts. Accordingly, the capacitor C2 stabilizes at a charge of 2.7 volts plus 0.4 of a volt or 3.1 volts.

In FIG. 1 the transformer T with its primary 67 and secondary 69 of the pulse source 65 form a critical component in the circuit to provide fail-safe operation in the event that the timing cycle is interrupted due to momentary unshunting of the track circuit and related relay which controls switch 10. As noted earlier once switch 10 is closed there is a controlled voltage level impressed across all the circuit components depicted to the right of voltage limiting means 13. Accordingly, the pulse source 65 has a voltage impressed across it also. Therefore, if for any reason there should be a momentary unshunting of the track relay mentioned earlier with the concomitant temporary opening of switch 10, there would be created a collapsing field around primary coil 67 which would induce a pulse in secondary coil 69. In this case, because of the relationship of the windings in primary coil 67 to those in the secondary coil, there would result a negative going pulse on lead 70 which is connected to lead 59 of relay 60 and to the relay coil 61 which in turn is connected to ground through leads 58, 14d and 14c. Should this momentary loss of d.c. power occur especially during the last 20 percent of the timing period, it has been found that absent the pulse source 65 the capacitor C2 has the tendency to discharge through the relay energization means 25 causing relay 60 to pick up contact *a* of the relay bypass means 66, thereby creating an unsafe con-

dition. But when the discharge means 65 induces a negative going pulse, this pulse will appear across the relay coil 61 and offset the charge from capacitor C2. The negative pulse causes the voltage on lead 59 to go more negative than the voltage on lead 14c, causing transistors Q1 and Q2 to conduct because of the forward bias provided by capacitor C2. Therefore, capacitor C2 will drain to zero volts and at such time transistors Q1 and Q2 will cease conducting.

Thus, for every momentary circuit opening, the timing capacitors will be discharged to zero volts, requiring the timing cycle to begin anew which creates a safe operation.

In the FIG. 2 embodiment of this invention, pulse source 65' is shown in the circuitry in series with the direct current voltage source 11 and in series with the time delay storage means 26 and the relay energization means 25. The operation of the embodiment of the invention in FIG. 2 is similar to that of FIG. 1, but differs substantially from FIG. 1 and includes an additional advantage to be mentioned hereinafter. The primary coil 67' of transformer T' is connected in series to the direct current voltage source 11 via leads 12b', 12a, resistor R1, lead 12, and switch 10. The secondary 69' of transformer T' is connected to ground via lead 71' at a point where lead 58 of relay 60 connects with lead 14d which in turn is connected to ground. The secondary coil 69' is connected to lead 62 which in turn is connected to lead 59 of the relay 60 where lead 59 connects with lead 14e.

In a similar fashion, as in the operation of FIG. 1, where there is a momentary interruption in power from the direct current voltage source 11 a negative going pulse is induced in coil 69' and lead 70'. The same conditions as in FIG. 1 arise with reference to the capacitor and transistors shown and capacitor C2 drains to zero volts requiring the timing cycle to begin again.

This series application of FIG. 2 is unique because it provides a check on the continuity of the pulse transformer's primary 67'. Accordingly, in the event the primary should open, there would be no energy available for circuit operation and therefore there would be a failure to a safe condition.

The resistor R2, which forms the heart of the excess voltage drainoff means 18, performs the important function of providing a rapid drainoff of residual charges that appear on the capacitor C2 of the adjustable time delay storage means 26. Since whether or not a circuit triggers the transistors Q1 and Q2 it will be observed that any residual charges at the capacitor C2 will drain off more rapidly through the resistor R2 which, by design, is about 5K, to ground than through resistors R6 and R7 of the reference voltage control means which combined resistance is about 2,700K, to ground. In other words, there is a preferential path through the resistor R2 which provides the important function of draining off excess voltage which will appear on the capacitor C2 which when fully charged discharges through the transistors Q1 and Q2 to energize the relay 60 in a manner described earlier.

The capacitor C1 which is connected across the leads 12c and 14b via leads 23 and 24 provides what is termed a safety voltage storage function and therefore the designation of this capacitor as a safety voltage storage means 22. The capacitor C1 of the safety volt-

age storage means 22 stores enough energy to prevent early triggering of the transistors Q1 and Q2 due to loss of the reference voltage during any momentary interruption of input power during the early stages of charging the timing capacitor C2. In other words, the capacitor C1 stores sufficient energy to maintain the reference voltage at a level that will not permit the transistors Q1 and Q2 to fire when there appears a momentary interruption in power from the direct current voltage source 11. The capacitor C1 of the safety voltage storage means 22 is also important from the standpoint that should there be an induced pulse impressed in the line wires that supply the direct current voltage source from the power supply and should this pulse be of a negative nature, this would cause a reduction in the reference voltage which could cause early triggering of the transistors Q1 and Q2 if the safety voltage storage means capacitor C1 were not present within the circuitry and did not have available the stored energy needed to maintain this reference voltage. Again, it should be appreciated that this provides a feature of fail-safe operation which is of great importance to the safety and the integrity of the time delay circuitry involved here.

When the direct current voltage source 11 and the circuits that supply the power to the relay are opened, as when the switch 10 is opened, the reference voltage which, as has been noted, is zero due to the bypass circuitry around the reference voltage control means 50, the capacitor C2 discharges completely through transistors Q1 and Q2, and the relay coil 61, thus causing the relay 60 to release. The resistor R3 of the signal transient suppression means 55 is important for the following reasons. If the resistor R3 were shunted so that it were out of the circuit, the transistors Q1 and Q2 would cease to conduct at some low value of current. This would leave a small positive charge on the capacitor C2. Accordingly, if resistor R3 were removed, i.e., R3 were opened, collapse of the electromagnetic field of the relay coil 61 would prolong the discharge of capacitor C2 of the time delay storage means 26 until it assumed a small negative charge. This, of course, would affect the time period of the next delay which would be bad. Accordingly, it can be seen that by adjusting the value of the resistor R3 in the signal transient suppression means 55, the capacitor C2 can be left with exactly a zero charge. The signal transient suppression means 55 includes a diode D3. This diode D3 is important for it prevents current from being shunted around the relay coil 61, which would tend to prevent the relay from picking up, and also prevent the early triggering of the transistors Q1 and Q2 due to an induced signal which may appear within the system upon the release of an adjacent relay. While, for purposes of example, this sudden transient voltage just noted might be induced by the release of an adjacent relay, it should be recognized that this suddenly induced voltage spike might come from any source externally of the relay here being described.

If the resistance R3 and the diode D3 were not present, a voltage spike induced in the coil 61 of the relay 60 could add to the voltage present on the capacitor C2 to produce a total voltage exceeding the reference voltage which, of course, would cause the transistors Q1 and Q2 to be triggered which would

result in the premature pickup of the relay which, of course, must never occur in this type of fail-safe environment.

The capacitor C3, which is connected across the emitter 35 and the base 36 of the transistor Q1 by the leads 32 and 33, functions as a buffer to the transistor Q1 should there be an induced voltage spike which somehow reaches this first transistor Q1. The capacitance of the capacitor C3 cooperates with a magnetic shield 20, referred to earlier, to protect the transistor Q1 from such a voltage spike. Accordingly, the capacitor C3 prevents the early triggering of the transistor Q1 due to instantaneous voltages at the transistor Q1, magnetically or electrostatically induced which could cause a sudden variation in the reference voltage which would, of course, possibly cause transistor Q1 to be triggered into conduction presenting the premature pickup of the relay which at all cost must be avoided.

The resistor R8, which is in the circuit between the electrical leads 12e and 12f, limits the holding current which will appear in the bypass circuit which includes the contact a of the relay 60, and this resistor R8 is selected merely to provide some nominal level of holding current in the coil 61 of the relay 60.

The resistor R9 electrically connected via the leads 39 and 41 to the leads 38 and 14e, respectively, is needed to stabilize the bias on the transistor Q2 to prevent leakage from the transistor Q1 from triggering transistors Q1 and Q2 early due to some high ambient temperatures. The inclusion of this resistor R9 is a standard technique involved to obviate this possible early triggering due to elevated ambient temperatures experienced by the system.

It will therefore be appreciated that the circuitry just described sets forth embodiments of a time element relay that includes pulse source arrangements for a predetermined time delay circuit in the event that a direct current voltage source for the relay should be disconnected momentarily from the remainder of the time element relay at a point in time near completion of the predetermined time delay to thereby ensure that there would not be a relay actuation before the end of the predetermined time delay. This invention will therefore always provide for a failure to a safe condition.

Obviously, certain modifications and variations of the invention as hereinbefore set forth may be made without departing from the spirit and scope thereof, and therefore only such limitations should be imposed as are indicated in the appended claims.

Having thus described my invention, what I claim is:

1. A fail-safe solid state time element relay circuit to prevent relay energization and pickup where there has been an open circuit condition during the timing cycle, said time element relay having in combination,
 - a. an externally controlled direct current voltage source,
 - b. solid state relay energization control means,
 - c. a predetermined time delay voltage storage means electrically connected to said solid state relay energization control means,
 - d. a relay electrically connected to said solid state relay energization control means,
 - e. a pulse source means for said time delay voltage storage means,

- f. a safety voltage storage means electrically connected to said direct current voltage source and to said pulse source means, said pulse source means electrically connected to said safety voltage storage means and said predetermined time delay storage means, said pulse source means electrically coupled to said relay to offset the charge of said predetermined time delay storage means in the event that said direct current voltage source should be momentarily disconnected from the remainder of said time element relay circuit to thereby ensure that there would not be a relay actuation before the end of said predetermined time delay,
- said safety voltage storage means storing energy from said direct current voltage source to thereby provide a standby reference voltage to said solid state relay energization control means,
- g. an excess voltage drainoff means for said predetermined time delay voltage storage means electrically connected to said predetermined time delay voltage storage means,
- h. reference voltage control means electrically connected to said solid state relay energization control means,
- i. a bypass means for said solid state relay energization control means and said reference voltage control means,
- said bypass means electrically connected to said direct current voltage source and controlled by said relay to provide a bypass circuit to maintain

said relay energized.

2. The fail-safe solid state time element relay circuit of claim 1 wherein said pulse source means for said time delay storage means is a pulse transformer with a primary winding electrically connected to said externally controlled direct current voltage source and a secondary winding electrically connected to said relay to thereby provide a negative going pulse to said relay which offsets the charge on said predetermined time delay voltage storage means through said solid state relay energization control means to ensure no relay energization should there be a momentary interruption of power from said externally controlled direct current voltage source.

3. The fail-safe solid state time element relay circuit of claim 1 wherein said pulse source means is a pulse transformer with a primary winding electrically connected in series with said externally controlled direct current voltage source and in series with said excess voltage drainoff means and said voltage limiting means and with a secondary winding electrically connected to said relay to thereby provide a negative going pulse to said relay which induces a voltage for offsetting the charge on said predetermined time delay voltage storage means which is supplied by said solid state relay energization control means to thereby ensure no relay energization should there be a momentary interruption of power from said externally controlled direct current voltage source.

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