



(51) International Patent Classification:
H03K 5/15 (2006.01) **H03D 7/00** (2006.01)

(21) International Application Number:
PCT/US2010/020155

(22) International Filing Date:
5 January 2010 (05.01.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/285,900 11 December 2009 (11.12.2009) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: DIGITAL SAMPLING MIXER WITH MULTIPHASE CLOCKS

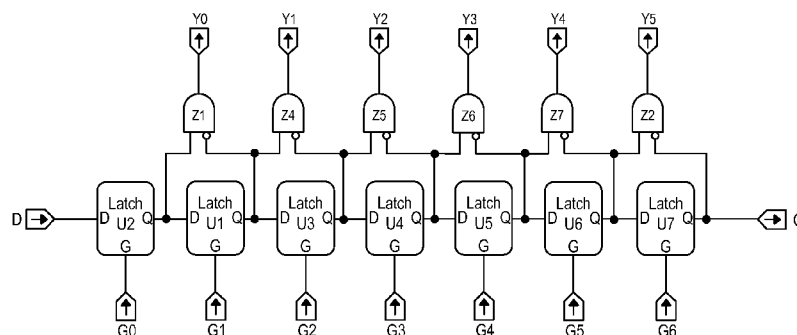


FIG. 3

(57) Abstract: A multiphase clock generates pulses at a rate much higher than the clock frequency.

DIGITAL SAMPLING MIXER WITH MULTIPHASE CLOCKS**BACKGROUND OF THE INVENTION**

5 **[0001]** In a digital sampling mixer (DSM) samples of a signal are taken at high speed in order to down-convert what is typically a radio frequency (RF) signal to a lower, more manageable rate. Such sampling requires activation of switches at a rate higher than the RF signal itself. For example, in a TV tuner application the highest RF signal may be 1GHz and the samples taken at 2.4GHz or higher. Such a high speed clock is
10 inconvenient and costly.

[0002] US Patent No. 7,028,070 relies on a delay line, the output of which activates a series of SHA (sample and hold amplifiers) in sequence. However, an imperfection arises due to the mismatch of delay time in the delay line. This mismatch, being random, executes a classic “random walk” around an ideal graph of sample time vs position in the
15 sequence. Such a classic random walk exhibits a nominal (or expected) deviation of \sqrt{N} where N is the length of the sequence. Therefore given a sequence of say 100 delay elements, each element having a delay of, for example 1nanosecond, and further having a random deviation of say 100picoseconds, the mean deviation from the ideal linear progression vs. time is $\sqrt{100} \times 100\text{picoseconds} = 1\text{nanosecond}$. But in practice
20 the deviation is well over 10nanoseconds. In an actual example, a chip with 320 picoseconds delay with 30 picoseconds deviation and 121 elements exhibits a 2 nanosecond deviation, well over the theoretical mean deviation of $\sqrt{121} \times 30$ picoseconds = 330 picoseconds.

[0003] The delay line does not exhibit the characteristic of a random walk. The
25 error, the 100picoseconds in the first example, is correlated along the sequence. For example, the first 50 delay elements are all 0.9 nanoseconds and the last 50 delay elements are all 1.1nanoseconds. There is still 100nanoseconds of total delay. However, although the mid point of the delay chain is expected to be at 50nanoseconds, the mid point of the delay chain is in fact occurring at $0.9\text{ nanoseconds} \times 50 = 45\text{nanoseconds}$, or
30 5 nanoseconds away from the expected point. That is 5 times the value predicted by the expected random-walk.

SUMMARY OF THE INVENTION

[0004] Various embodiments relate to multiphase clock generates pulses at a rate much higher than the clock frequency.

[0005] One apparatus embodiment includes clock circuitry, a plurality of latches, and combinational logic:

[0006] clock circuitry generating a plurality of clock signals having an odd number of clock signals being three or more, the plurality of clock signals having a common frequency, and a phase delay corresponding to the odd number of clock signals evenly separating the first plurality of clock signals;

[0007] a plurality of latches connected in series, wherein adjacent latches of the series are connected such that an output of a preceding latch of the adjacent latches in the series is connected to an input of a following latch of the adjacent latches in the series, the plurality of latches being clocked by the plurality of clock signals and inverted versions of the plurality of clock signals such that half of the phase delay separates clock signals of the preceding latch and the following latch of the adjacent latches in the series;

[0008] combinational logic coupled to outputs of the plurality of latches, the combinational logic generating pulses at a rate of two times the odd number of clock signals times the common frequency of the plurality of clock signals.

[0009] In another embodiment, the apparatus is a digital sampling mixer, and the pulses control sample and hold circuitry of the digital sampling mixer.

[0010] In another embodiment, the pulses are overlapping.

[0011] In another embodiment, the pulses are non-overlapping.

[0012] Another apparatus embodiment includes clock circuitry, a plurality of latches, and combinational logic:

[0013] clock circuitry generating a plurality of clock signals having an even number of clock signals being four or more, the plurality of clock signals having a common frequency, and a phase delay corresponding to the even number of clock signals evenly separating the first plurality of clock signals;

[0014] a plurality of latches connected in series, wherein adjacent latches of the series are connected such that an output of a preceding latch of the adjacent latches in the series is connected to an input of a following latch of the adjacent latches in the series,

the plurality of latches being clocked by the plurality of clock signals such that the phase delay separates clock signals of the preceding latch and the following latch of the adjacent latches in the series;

[0015] combinational logic coupled to outputs of the plurality of latches, the combinational logic generating pulses at a rate of the even number of clock signals times the common frequency of the plurality of clock signals.

[0016] In another embodiment, the apparatus is a digital sampling mixer, and the pulses control sample and hold circuitry of the digital sampling mixer.

[0017] In another embodiment, the pulses are overlapping.

10 [0018] In another embodiment, the pulses are non-overlapping.

[0019] Another aspect of the technology is a method with the following steps:

[0020] clocking series-connected latches, with a plurality of clock signals having an odd number of clock signals being three or more and with inverted versions of the clock signals, the plurality of clock signals having a common frequency, and a phase delay corresponding to the odd number of clock signals evenly separating the first plurality of clock signals; and

[0021] generating pulses from the series-connected latches at a rate of two times the odd number of clock signals times the common frequency of the plurality of clock signals.

20 [0022] One embodiment further comprises:

[0023] clocking a digital sampling mixer with the pulses.

[0024] In one embodiment, the pulses are overlapping.

[0025] In one embodiment, the pulses are non-overlapping.

[0026] Another aspect of the technology is a method with the following steps:

25 [0027] clocking series-connected latches, with a plurality of clock signals having an even number of clock signals being four or more, the plurality of clock signals having a common frequency, and a phase delay corresponding to the even number of clock signals evenly separating the first plurality of clock signals; and

[0028] generating pulses from the series-connected latches at a rate of two times the even number of clock signals times the common frequency of the plurality of clock signals.

- [0029] One embodiment further comprises:
[0030] clocking a digital sampling mixer with the pulses.
[0031] In one embodiment, the pulses are overlapping.
[0032] In one embodiment, the pulses are non-overlapping.

5

BRIEF DESCRIPTION OF THE DRAWINGS

- [0033] Figure 1 is a block diagram of a latch.
[0034] Figure 2 is a block diagram of a chain of latches.
[0035] Figure 3 is a block diagram of a chain of latches with gates added to the latch
10 outputs to generate non-overlapping pulses.
[0036] Figure 4 is a graph of a three phase clock used to clock the chain of latches.
[0037] Figure 5 is a graph of the non-overlapping pulses output from the chain of
latches, such as the one of Figure 4.
[0038] Figure 6 is a block diagram of a chain of latches with gates added to the latch
15 outputs to generate overlapping pulses.
[0039] Figure 7 is a graph of a three phase clock used to clock the chain of latches.
[0040] Figure 8 is a graph of the overlapping pulses output from the chain of latches,
such as the one of Figure 6.
[0041] Figure 9 is a graph of a five phase clock used to clock the chain of latches.
20 [0042] Figure 10 is a graph of the overlapping pulses output from the chain of
latches, resulting from the five phase clock such as the one of Figure 9.
[0043] Figure 11 is a block diagram of a digital sampling mixer with the improved
multiphase clock circuit.

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DETAILED DESCRIPTION

- [0044] Various embodiments use multiple copies of a lower frequency clock to
activate switches at a rate much higher than the clock frequency.
[0045] An example of a digital sampling mixer is discussed in US Patent No.
7,028,070, incorporated by reference herein. Figure 11 shows a modified version of such
30 a digital sampling mixer. A chain of gates (14) is the timing element that activates the
sample and hold (SHA) circuits (11).

[0046] In the present technology, with a chain of latches, a signal propagates down the chain at a rate higher than the clock frequency of the clocks. If adjacent devices are gated together, a precisely timed series of pulses with time separations less than that of the clock is generated. A 'latch' is an electronic element with state. The state of the latch persists indefinitely if a certain control input is, for example, high, and copies an externally applied state if the control input is, for example, low.

[0047] An example latch element is shown in Figure 1. If 'G' is high, the output state 'Q' copies that of the input state 'D'. If 'G' is low, then the output state remains as it last was just prior to the 'G' input going low.

[0048] A chain of latches is created by connecting 'Q' to 'D' as shown in Figure 2:

[0049] A model demonstrates the operation of clocking a DSM with a multi-phase clock. The model of the latch is:

[0050] A Q Q 0 v=if V(G)>0 then

[0051] if V(D)>0 then 1 else -1

[0052] else

[0053] if V(Q)>0 then 1 else -1

[0054] Example with three clock phases and non-overlapping outputs

[0055] An embodiment further includes gates added to the Q outputs, as shown in Figure 3.

[0056] A multi-phase clock is defined by these statements:

[0057] .param fa=500meg aa=1.0

[0058] VA A 0 'aa*sin(0)' sin(0 aa fa 0 0 0)

[0059] VB B 0 'aa*sin(2/3*pi)' sin(0 aa fa 0 0 120)

[0060] VC C 0 'aa*sin(4/3*pi)' sin(0 aa fa 0 0 240)

[0061] EG0 G0 0 A 0 1

[0062] EG1 G1 0 B 0 -1

[0063] EG2 G2 0 C 0 1

[0064] EG3 G3 0 A 0 -1

[0065] EG4 G4 0 B 0 1

[0066] EG5 G5 0 C 0 -1

[0067] EG6 G6 0 A 0 1

[0068] A,B,C are a three phase clock with 120° phase difference as shown in Figure 4. The clocks are connected in the sequence A, -B, C, -A, B, -C, etc where the minus sign indicates inversion. A signal falls through the latches at a rate of six times the clock as shown in Figure 5. Six non-overlapping pulses are generated for one cycle of the clock.

[0069] The advantage of the non-overlapping output version is that one sampling capacitor is connected at any one time. Consequently the load seen by the driving circuit is low, as it only every needs to drive one switch and capacitor.

[0070] In other embodiments, any odd number of clock phases is used. Other embodiments generate overlapping output pulses of any desired width.

[0071] Example with three clock phases and overlapping outputs

[0072] In Figure 6, the circuit gates are modified to “leap over” the latches. Any degree of overlapping pulses can be created:

[0073] A,B,C are a three phase clock with 120° phase difference as shown again in Figure 7. In Figure 8, six overlapping pulses are generated for one cycle of the clock.

[0074] The advantage of overlapping output is as follows. In an example, the SHA is a switch that turns on for nominally 1nanosecond and then goes off, while at the same time the next switch comes on. The mathematical instant of sampling is, to a first order, the time when the switch turns off. At that time the charge is trapped and the sample has been taken. There is a second order effect. The on resistance of the switch and the value of the capacitor make a finite bandwidth, and this bandwidth limits the rate-of-change of the signal. Suppose the SHA has been at -1 volt and now must go to +1v. If the switch opens for 1nanosecond the RC of the switch and capacitor may not be fast enough, the signal may be truncated by the switch going off, when the signal is part way up the exponential rise. Since only the moment of turning off the switch matters from the sample point of view, the switch can be allowed to stay on longer. But the rate of switch operation is maintained, rather than slowing down the whole circuit. So the solution is overlapping pulses. However, the driving device now sees more than one capacitor connected at any time and this presents a higher, more difficult to drive, load.

[0075] Example with five clock phases and overlapping outputs

[0076] The previous circuit has modified clocks as follows:

[0077] .param fa=500meg aa=1.0

[0078] VA A 0 'aa*sin(0)' sin(0 aa fa 0 0 0)

[0079] VB B 0 'aa*sin(2/5*pi)' sin(0 aa fa 0 0 72)

[0080] VC C 0 'aa*sin(4/5*pi)' sin(0 aa fa 0 0 144)

5 [0081] VD D 0 'aa*sin(6/5*pi)' sin(0 aa fa 0 0 216)

[0082] VE E 0 'aa*sin(8/5*pi)' sin(0 aa fa 0 0 288)

[0083] EG0 G0 0 A 0 1

[0084] EG1 G1 0 C 0 -1

[0085] EG2 G2 0 E 0 1

10 [0086] EG3 G3 0 B 0 -1

[0087] EG4 G4 0 D 0 1

[0088] EG5 G5 0 A 0 -1

[0089] EG6 G6 0 C 0 1

[0090] EG7 G7 0 E 0 -1

15 [0091] EG8 G8 0 B 0 1

[0092] EG9 G9 0 D 0 -1

[0093] A,B,C,D,E are a five phase clock with 72° phase difference as shown in

Figure 9. Ten overlapping pulses are generated for one cycle of the clock. Figure 10 shows only seven, but the fact that ten occur in one cycle is evident. One cycle is 2

20 nanoseconds. In between the time indexes 10.0 nanoseconds and 11.2 nanoseconds, the leading edges of pulses occur, or 1 pulse leading edge every 0.2 nanoseconds. So $(2 \text{ nanoseconds} / \text{cycle}) * (1 \text{ pulse leading edge} / 0.2 \text{ nanoseconds}) = (10 \text{ pulse leading edges} / \text{cycle})$.

[0094] Figure 11 shows an example digital sampling mixer with the present

25 multiphase clocking technology.

[0095] Conclusion

[0096] Sampling pulses suitable to activate the sample and hold of a digital sampling mixer are generated for every phase of a multiphase clock. This is effective for odd numbers of phases where two times the number of phases of pulses occur in one cycle.

30 The pulses are generated by a chain of latches, each connected to an appropriate phase of the clock, such that the data “falls through” on every phase rotation. A gate is connected

to detect the position of the changing data as it passes down the chain, described as follows.

[0097] When the “wave” of 1’s (or 0’s) passing down the chain has reached any given position, the output the output will be ‘1’ (or ‘0’). Further down the chain is still
5 ‘0’ (or ‘1’) since the ‘wave’ has not reached there yet. Therefore, the detection of a ‘1’ (or ‘0’) at the local position in conjunction with a ‘0’ (or ‘1’) at the next adjacent position indices that a pulse is required now. The gate therefore is an AND gate with one input inverted (i.e. it creates a ‘1’ when the input is “10”. Conversely, another embodiment uses the negative edge and searches for a 0 locally and a 1 remaining at the next adjacent
10 position. If the test is applied not at the immediately adjacent position then an overlapping pulse results.

[0098] The gate output activates the sample and hold. The gate outputs may be single pulses or overlapping pulses depending on whether the gate inputs are adjacent or not.

CLAIMS

We Claim:

1. An apparatus, comprising:
clock circuitry generating a plurality of clock signals having an odd number of
clock signals being three or more, the plurality of clock signals having a common
frequency, and a phase delay corresponding to the odd number of clock signals evenly
separating the first plurality of clock signals;
a plurality of latches connected in series, wherein adjacent latches of the series are
connected such that an output of a preceding latch of the adjacent latches in the series is
connected to an input of a following latch of the adjacent latches in the series, the
plurality of latches being clocked by the plurality of clock signals and inverted versions
of the plurality of clock signals such that half of the phase delay separates clock signals
of the preceding latch and the following latch of the adjacent latches in the series;
combinational logic coupled to outputs of the plurality of latches, the
combinational logic generating pulses at a rate of two times the odd number of clock
signals times the common frequency of the plurality of clock signals.

2. The apparatus of claim 1, wherein the apparatus is a digital sampling mixer, and
the pulses control sample and hold circuitry of the digital sampling mixer.

3. The apparatus of claim 1, wherein the pulses are overlapping.

4. The apparatus of claim 1, wherein the pulses are non-overlapping.

5. A method, comprising:
clocking series-connected latches, with a plurality of clock signals having an odd
number of clock signals being three or more and with inverted versions of the clock
signals, the plurality of clock signals having a common frequency, and a phase delay
corresponding to the odd number of clock signals evenly separating the first plurality of
clock signals; and

7 generating pulses from the series-connected latches at a rate of two times the odd
8 number of clock signals times the common frequency of the plurality of clock signals.

1 6. The method of claim 5, further comprising:
2 clocking a digital sampling mixer with the pulses.

1 7. The method of claim 5, wherein the pulses are overlapping.

1 8. The method of claim 5, wherein the pulses are non-overlapping.

1 9. An apparatus, comprising:
2 clock circuitry generating a plurality of clock signals having an even number of
3 clock signals being four or more, the plurality of clock signals having a common
4 frequency, and a phase delay corresponding to the even number of clock signals evenly
5 separating the first plurality of clock signals;
6 a plurality of latches connected in series, wherein adjacent latches of the series are
7 connected such that an output of a preceding latch of the adjacent latches in the series is
8 connected to an input of a following latch of the adjacent latches in the series, the
9 plurality of latches being clocked by the plurality of clock signals such that the phase
10 delay separates clock signals of the preceding latch and the following latch of the
11 adjacent latches in the series;
12 combinational logic coupled to outputs of the plurality of latches, the
13 combinational logic generating pulses at a rate of the even number of clock signals times
14 the common frequency of the plurality of clock signals.

1 10. The apparatus of claim 9, wherein the apparatus is a digital sampling mixer, and
2 the pulses control sample and hold circuitry of the digital sampling mixer.

1 11. The apparatus of claim 9, wherein the pulses are overlapping.

1 12. The apparatus of claim 9, wherein the pulses are non-overlapping.

- 1 13. A method, comprising:
2 clocking series-connected latches, with a plurality of clock signals having an even
3 number of clock signals being four or more, the plurality of clock signals having a
4 common frequency, and a phase delay corresponding to the even number of clock signals
5 evenly separating the first plurality of clock signals; and
6 generating pulses from the series-connected latches at a rate of two times the even
7 number of clock signals times the common frequency of the plurality of clock signals.
- 1 14. The method of claim 13, further comprising:
2 clocking a digital sampling mixer with the pulses.
- 1 15. The method of claim 13, wherein the pulses are overlapping.
- 1 16. The method of claim 13, wherein the pulses are non-overlapping.

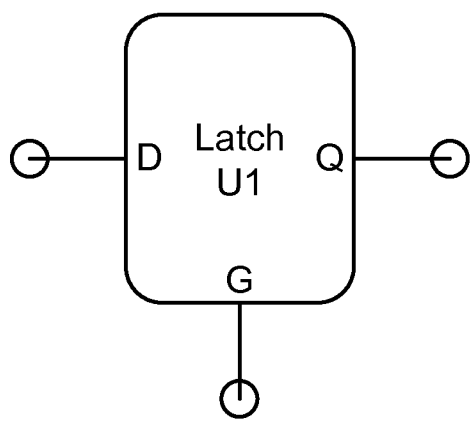


FIG. 1

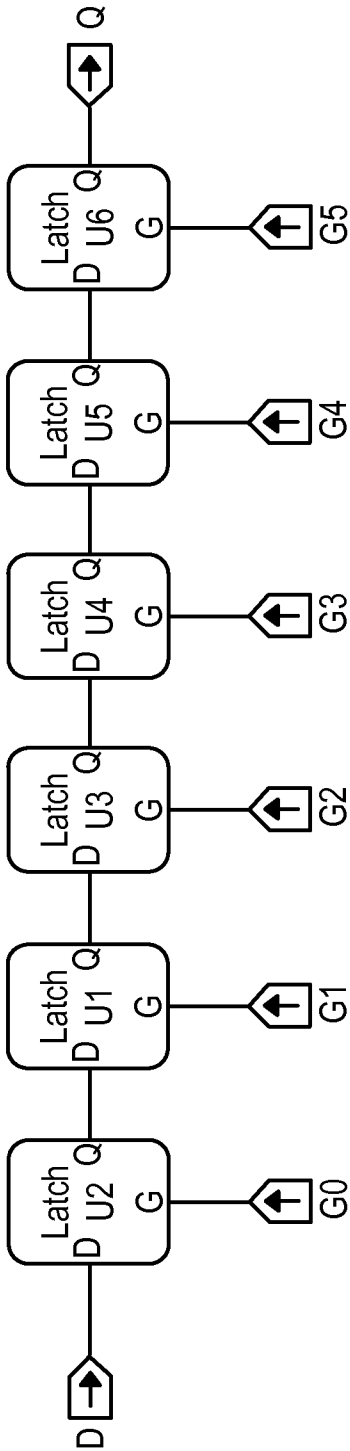


FIG. 2

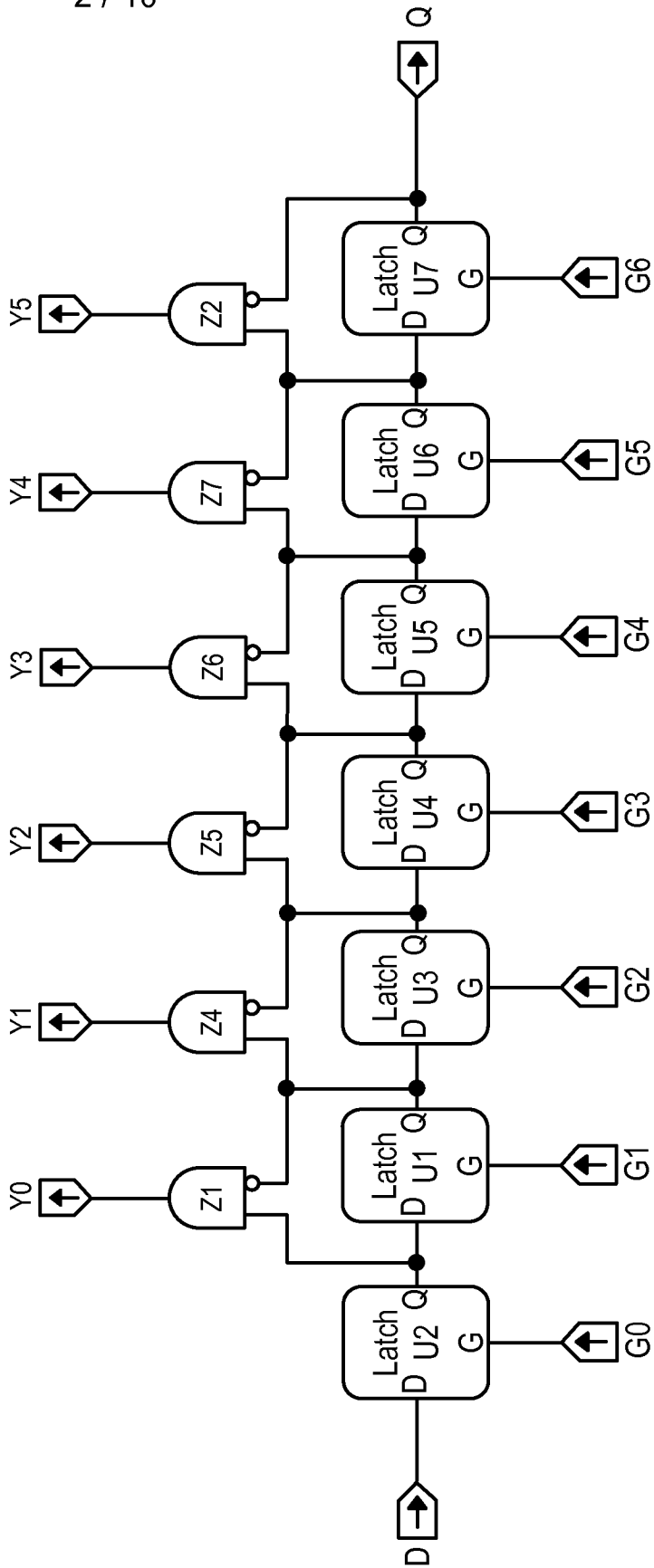


FIG. 3

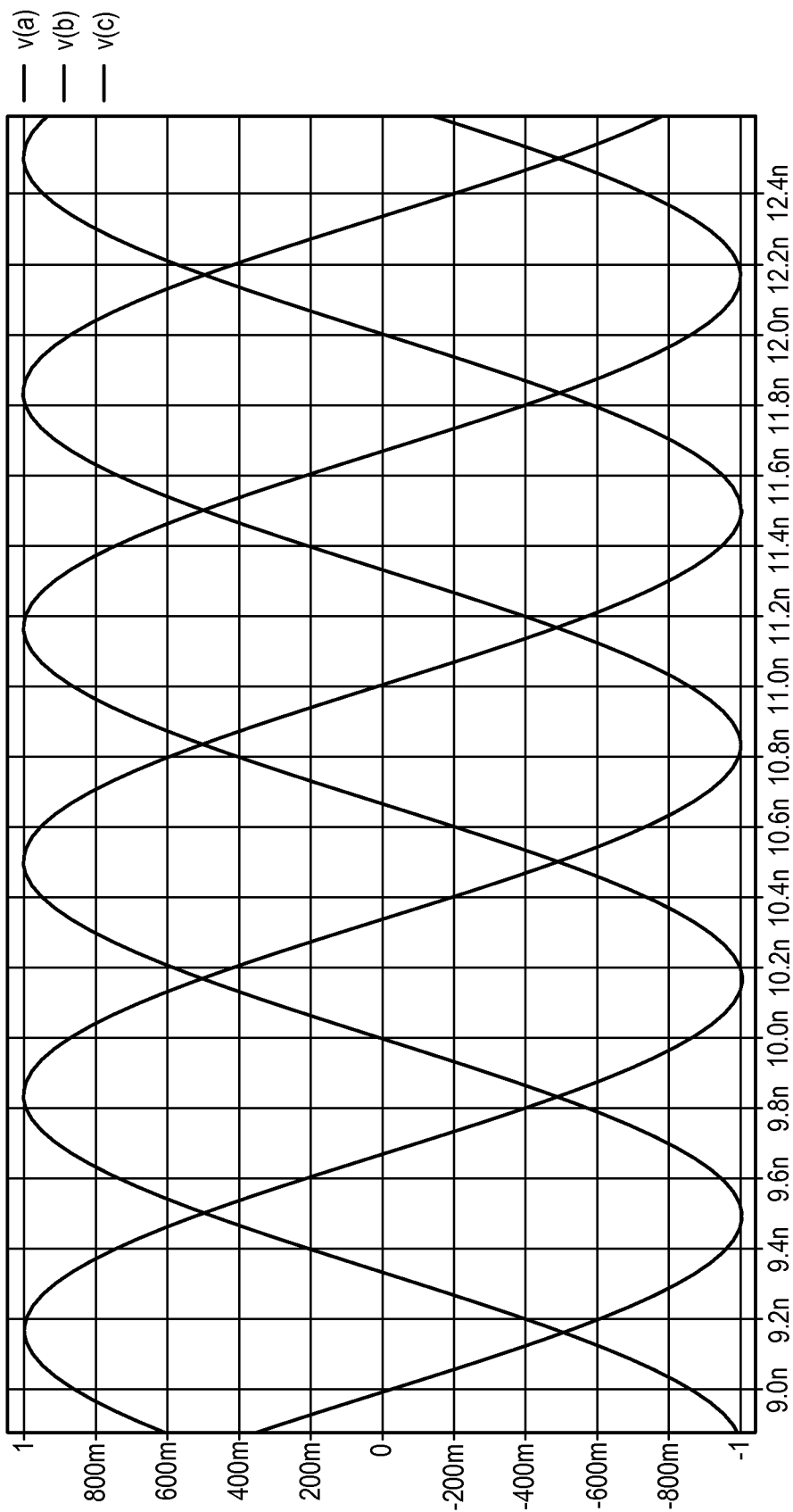


FIG. 4

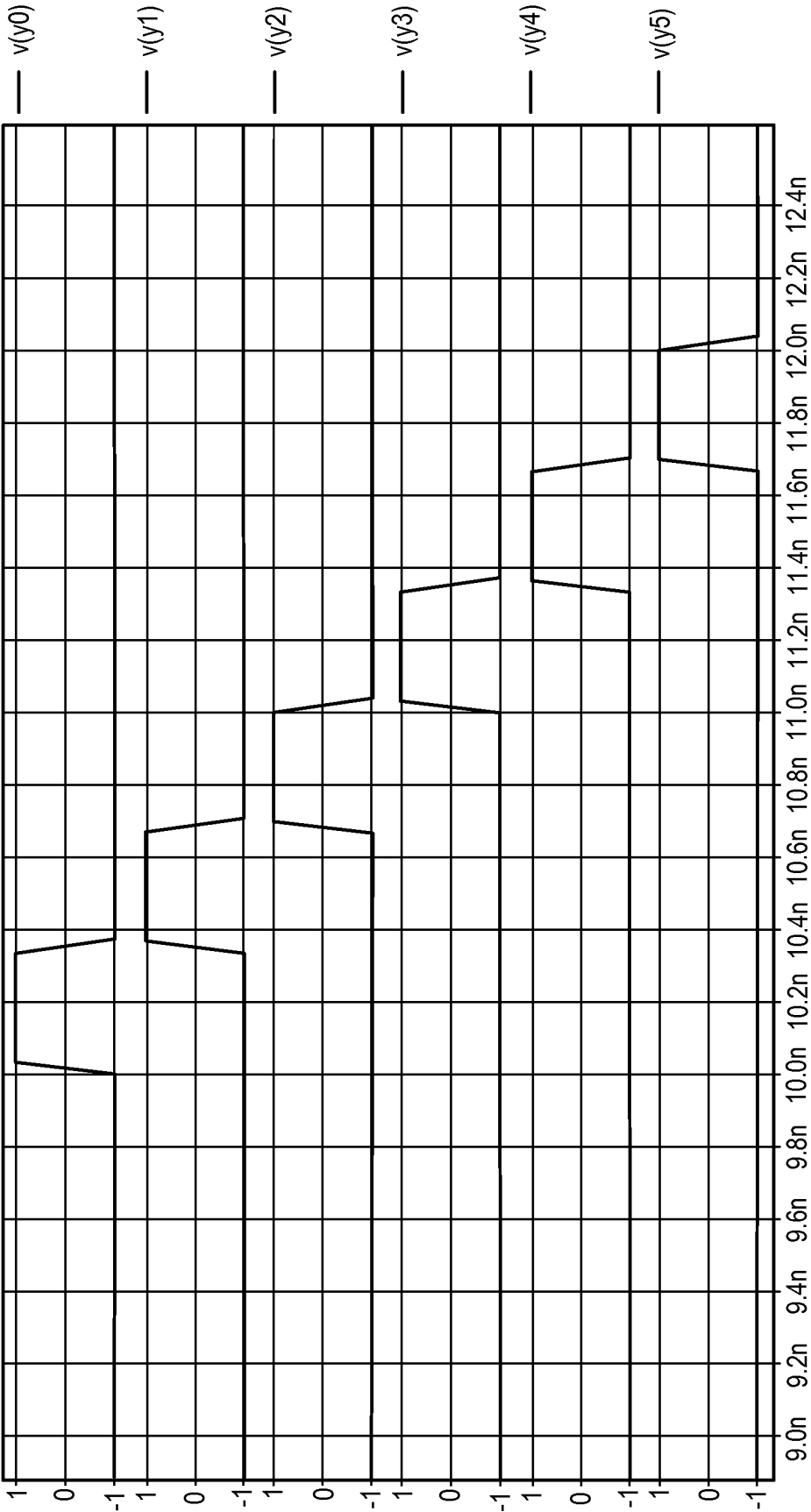


FIG. 5

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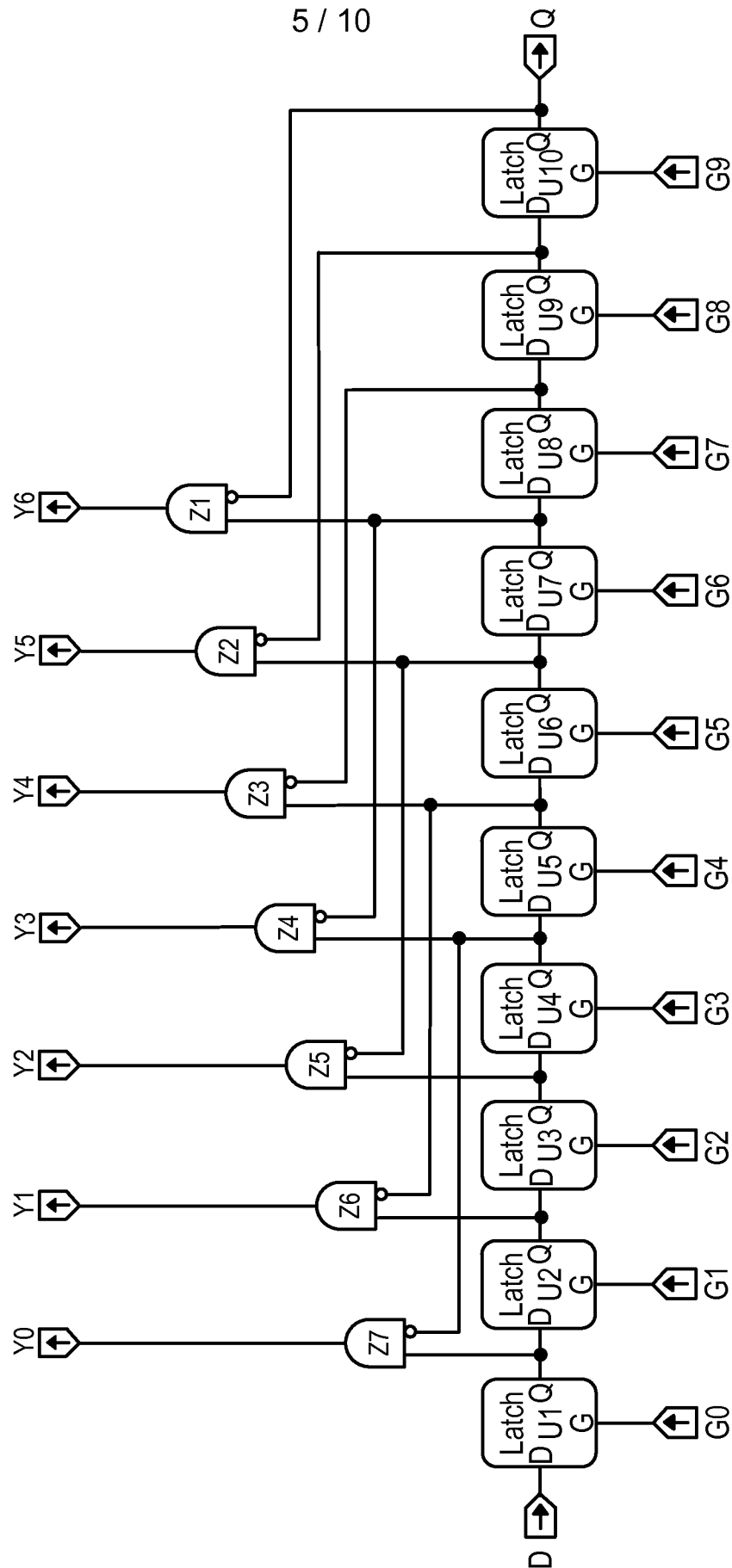


FIG. 6

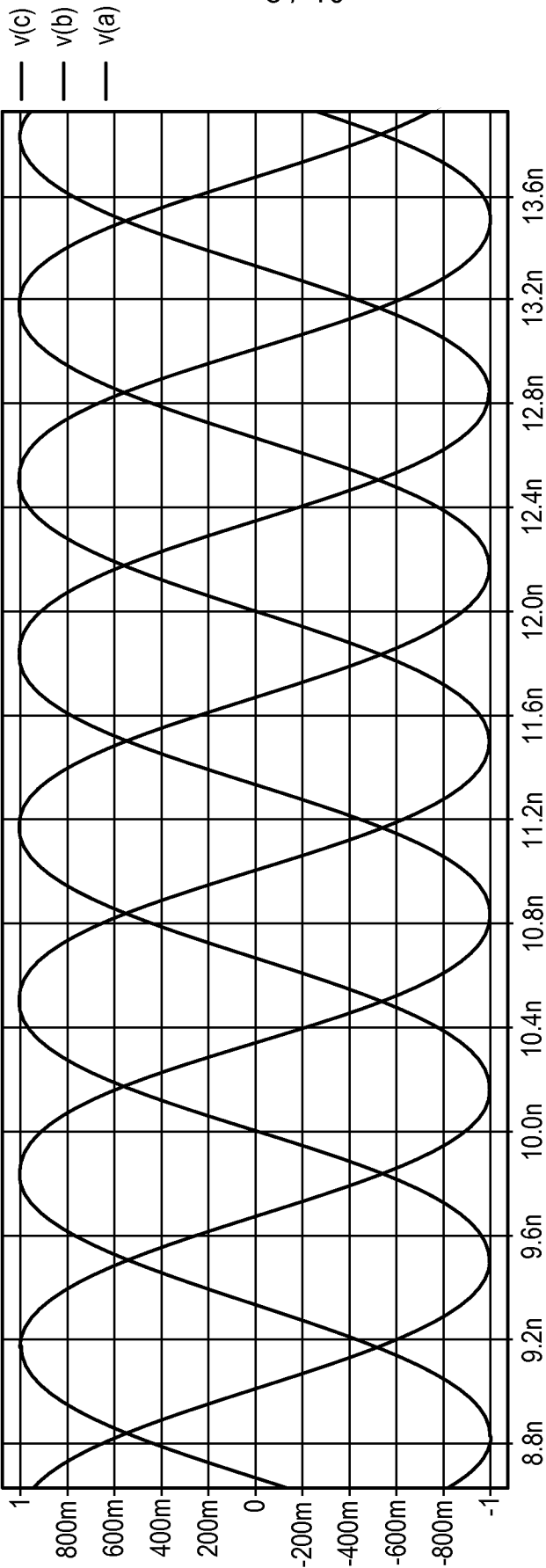


FIG. 7

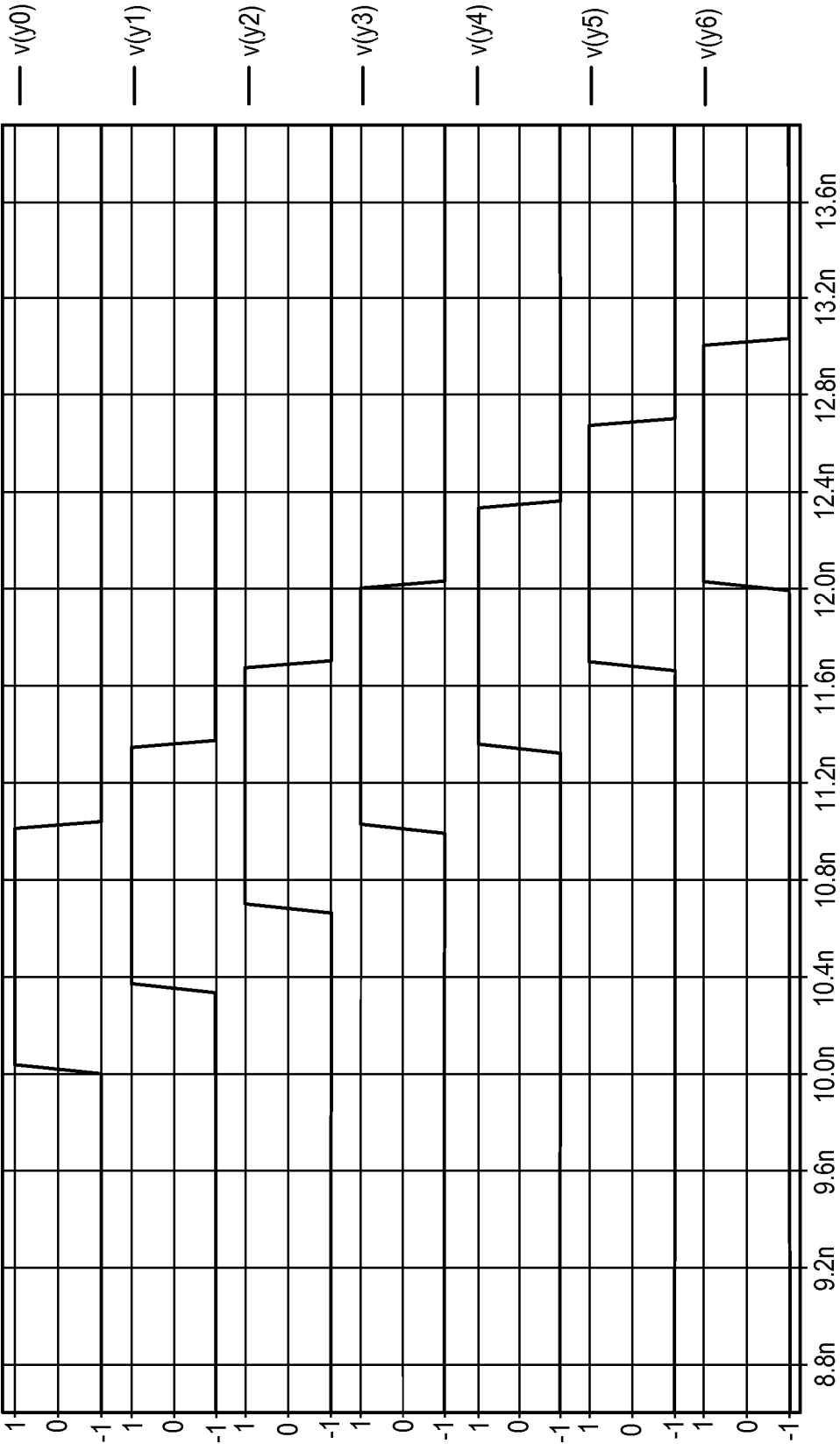


FIG. 8

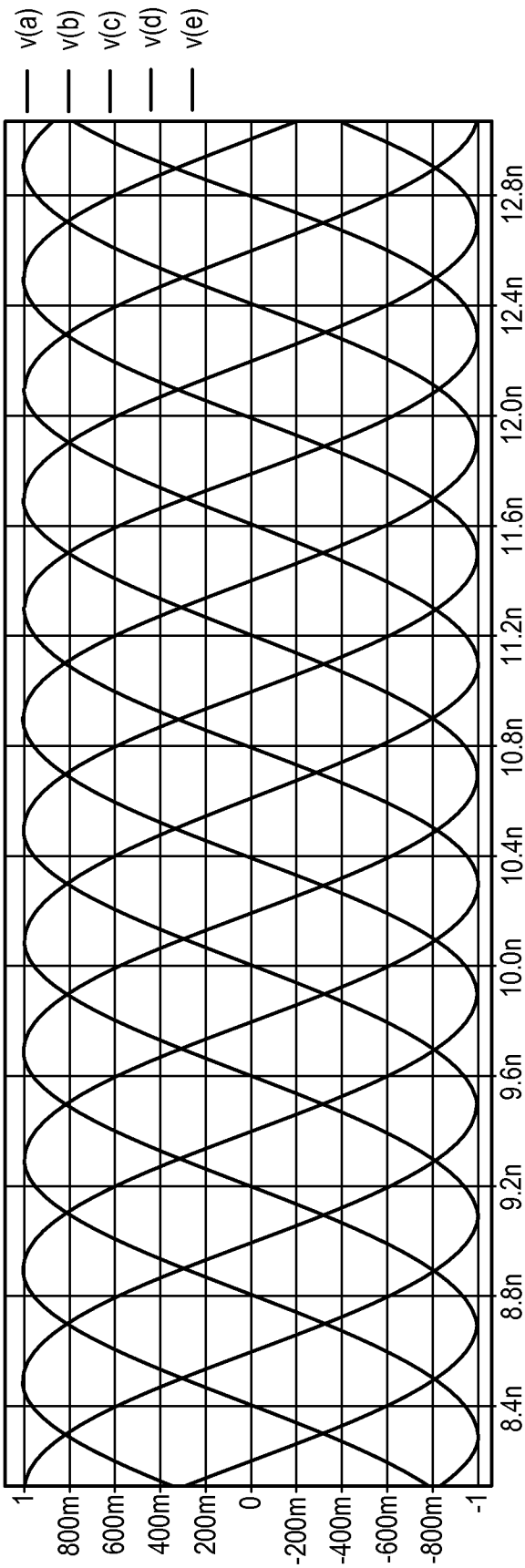


FIG. 9

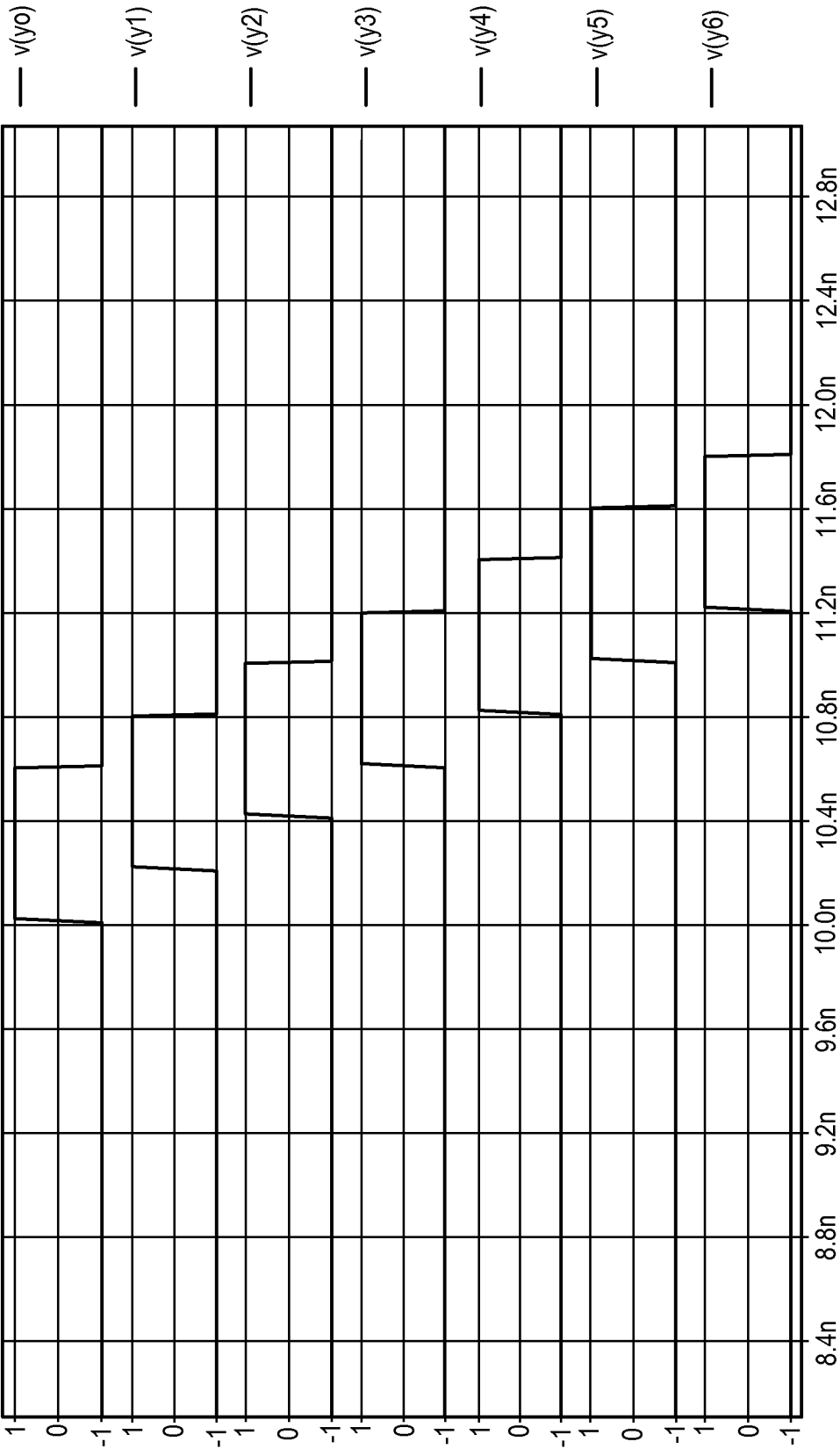
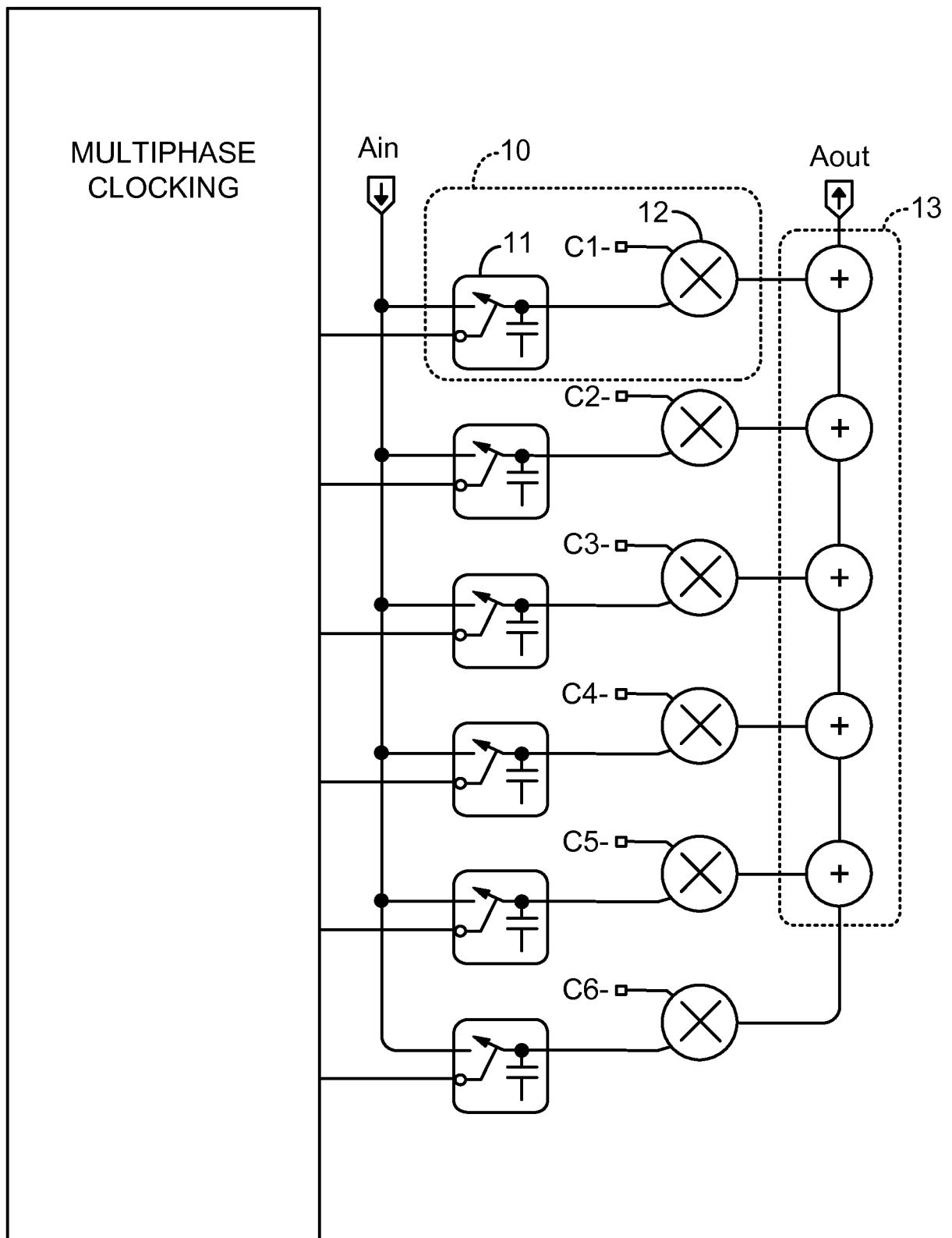


FIG. 10

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**FIG. 11**

A. CLASSIFICATION OF SUBJECT MATTER***H03K 5/15(2006.01)i, H03D 7/00(2006.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03K 5/15; G06F 1/06; H03K 3/00; H03L 7/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: multiphase clock, latch, phase delay

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2004-056717 A (RENESAS TECHNOLOGY CORP et al.) 19 February 2004 See abstract; para.39-50; claims 8-9 and figures 6-7.	1-16
A	JP 2001-318731 A (MATSUSHITA ELECTRIC IND CO LTD) 16 November 2001 See abstract; claims 1-2 and figures 1-4.	1-16
A	US 2001-0030565 A1 (TSUYOSHI EBUCHI et al.) 18 October 2001 See abstract; claims 1, 3 and figures 5-7.	1-16
A	KR 10-2006-0044539 A (FUJITSU LIMITED) 16 May 2006 See abstract; claims 1, 3 and figure 4.	1-16



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

31 DECEMBER 2010 (31.12.2010)

Date of mailing of the international search report

03 JANUARY 2011 (03.01.2011)

Name and mailing address of the ISA/KR

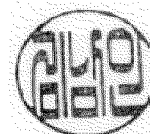
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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