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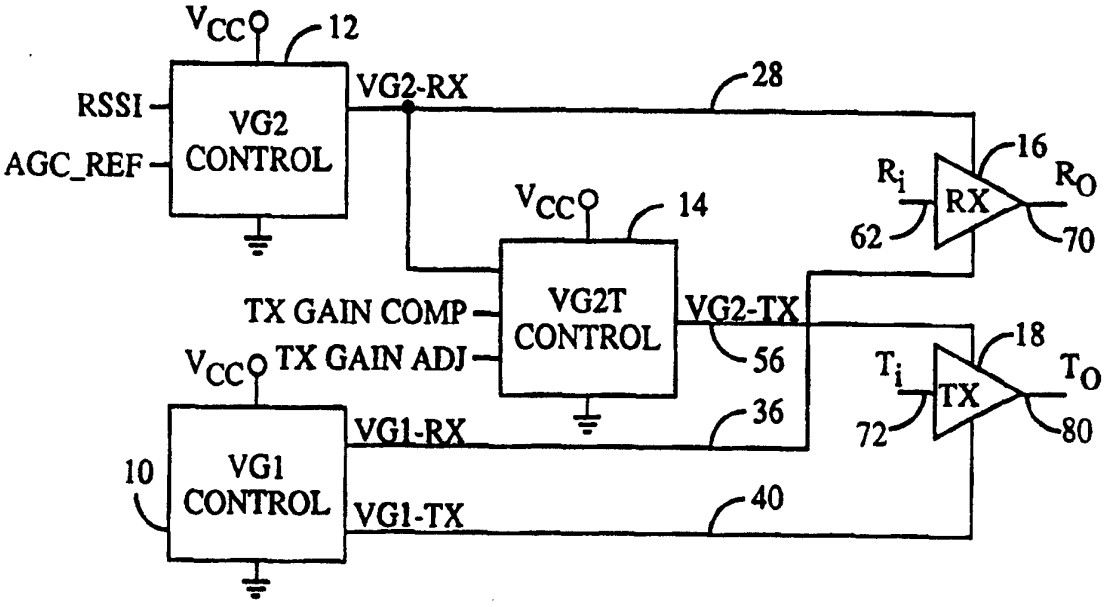

(57) Abstract

A high dynamic range linear automatic gain control (AGC) circuit that has independent means for temperature compensation. The temperature compensation circuit of this invention can be used in a closed-loop AGC circuit such as is required in a transceiver for compensating the gains of receiver and transmitter amplifiers (16, 18) to ensure that both track closely over ranges of temperature, frequency and load impedance. The temperature compensation signal is coupled to one of the two gates in a field effect transistor (FET) amplifier to maintain a constant gain function over ranges of temperature, frequency and load impedance. Thermal compensation for the transmitter amplifier (18) is derived from the thermal compensation signal (28) for the receiver amplifier (16).

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TEMPERATURE-COMPENSATED GAIN-CONTROLLED AMPLIFIER HAVING A WIDE LINEAR DYNAMIC RANGE

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to automatic gain control (AGC) circuits for linear amplifiers and, more specifically, to an improved temperature-compensated AGC circuit having a wide linear dynamic range.

2. Description of the Related Art

The use of automatic gain control (AGC) circuits to control amplifier gain in communication transceivers has been accomplished by various circuit designs. Typically, the dynamic range of gain control in such amplifiers is somewhat limited. This is especially true with field-effect transistor (FET) linear amplifier circuits because of the somewhat constrained linear operating region of the typical single and dual gate FET.

Amplifier gain control is also known to drift substantially with changes in circuit temperature. Temperature compensation for AGC of linear amplifiers has also been accomplished by various circuit designs. Compensation for temperature-induced drift imposes requirements different from those associated with compensation for nonlinearities in device characteristics at signal amplitude extremes.

In certain applications, such as in code division multiple access (CDMA) cellular telephone or personal communications device transceivers, where transmitter power control and receiver AGC are essential to proper system operation, the transmitter and receiver amplifiers must both track each other in gain over a relatively high dynamic signal range. In such an environment, the receiver amplifier may be required to respond linearly to a gain control signal over an 80dB range of gain.

In U.S. Patent 5,099,204, issued March 24, 1992 entitled "LINEAR GAIN CONTROL AMPLIFIER" assigned to the assignee hereof, and entirely incorporated herein by this reference, Charles E. Wheatley III et al. discloses a linear gain control amplifier design having a compensation circuit that generates a compensation signal according to predetermined device characteristics. Wheatley's compensation signal serves to linearize the nonlinear FET device characteristics at the extremes of the dynamic operating region, thereby ensuring linear amplifier gain control over a wide

dynamic range. Wheatley also suggests the use of a thermistor in the AGC compensation circuit to compensate for thermal drift.

In many digital communication systems, the transceiver AGC loop must provide a signal that is a logarithmic indication of a measured received signal power over a range of signal power levels. In a digital receiver, the amplified received signal power must be limited for proper signal processing of the received signal. In the cellular transceiver environment, a digital receiver may receive a signal that experiences rapid variations in signal power over a wide range. This rapid linear AGC requirement is made more difficult by the gain-tracking requirement for both receiver amplifier and transmitter amplifier in a CDMA cellular telephone transceiver. That is, in a typical digital receiver, the level of received signal power is detected, digitized and then measured. The measured value is then typically compared with a predetermined control value and an error signal generated in digital form. This error signal is then used to control the gain of both the receiver amplifier and the transmitter amplifier so as to adjust both received and transmitted signal strength to coincide with the respective desired signal powers. The receive amplifier gain is carefully controlled to permit proper signal processing of the received signal. The transmitter amplifier gain is also carefully controlled to ensure sufficient signal strength in the channel without unnecessary power consumption. This demanding set of transceiver amplifier gain requirements is further exacerbated by variations in thermal drift characteristics throughout the transceiver.

Practitioners have proposed various techniques for overcoming the cellular telephone transceiver amplifier gain linearity problem. For instance, in U.S. Patent 5,107,225, issued April 21, 1992 entitled "HIGH DYNAMIC RANGE CLOSED LOOP AUTOMATIC GAIN CONTROL CIRCUIT" assigned to the assignee hereof and fully incorporated herein by this reference, Charles E. Wheatley, III, et al disclose a high dynamic range closed-loop AGC circuit that automatically controls transmitter and receiver amplifier gain responsive to an indication of the strength of a received signal. Wheatley, et al teach a method for combining the received signal strength indication (RSSI) with device characteristic compensation signals to provide a system wherein both the receiver and transmitter amplifier gains in decibels vary linearly with respect to a control signal over a broad dynamic range.

In these and other applications, a clear felt need is present in the art for a method for compensating amplifier gain for variations in temperature

to ensure that two such amplifiers can track each other over a wide dynamic operating region. The related unresolved problems and deficiencies are clearly-felt in the art and are solved by this invention in the manner described below.

SUMMARY OF THE INVENTION

This invention solves the temperature-compensated gain tracking problem by adding a gain independent compensation circuit for creating a second compensation signal responsive to temperature according to a predetermined characteristic. The method of this invention can be used with low-cost amplifiers employing dual-gate FET devices or with any other suitable linear amplification device known in the art.

The compensation circuit employs a thermistor to provide a receiver gain compensation signal for use in adjusting the receiver amplifier gain responsive to temperature. This receiver gain compensation signal is then modified according to a second predetermined characteristic to create a transmitter amplifier gain compensation signal suitable for adjusting transmitter amplifier gain responsive to temperature.

The temperature compensation method of this invention can be applied to the dual-gate FET linear gain control amplifier taught by Wheatley in the above-cited patent 5,099,204 and to the receiver and transmitter amplifier AGC loop taught by Wheatley et al. in the above-cited patent 5,107,225 by adding a second compensation circuit according to this invention and then applying the resulting temperature-compensation control signals to the first gate circuit in each amplifier stage.

It is an object of the circuit of this invention to compensate the gain of two linear amplifiers in a transceiver in a manner that preserves the linear gain tracking features of such amplifiers. It is a feature of the circuit of this invention that the temperature compensation control signals are applied to the first gate of each FET stage, thereby being isolated from the device characteristic gain compensation signals applied to the second gate thereof according to the above-cited patents.

The foregoing, together with other objects, features and advantages of this invention, will become more apparent when referring to the following specification, claims and the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of this invention, reference is now made to the following detailed description of the embodiments as

illustrated in the accompanying drawings, wherein:

Figure 1 shows a functional block diagram of an illustrative gain-controlled transceiver amplifier circuit incorporating the thermal compensation method of this invention;

Figure 2 provides a simple block diagram of a single two-stage amplifier employing the temperature compensation circuit of this invention;

Figure 3 and 4 are illustrative embodiments of the temperature and device compensation control circuits from Figures 1 and 2;

Figure 5 is an illustrative embodiment of the receiver amplifier from Figure 1;

Figure 6 is an illustrative embodiment of the transmitter amplifier from Figure 1;

Figure 7 shows a logarithmic device gain control ratio as a function of temperature;

Figure 8 shows the effect of first gate voltage on the slope of the gain control; and

Figure 9 shows the linear gain error in decibels as a function of device gain compensation voltage after adding the temperature compensation control circuit of Figure 3.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 provides a functional block diagram of selected elements of a typical transceiver, including the temperature compensation circuit 10 of this invention. The receiver amplifier device compensation circuit 12 and transmitter amplifier device compensation circuit 14 are configured in accordance with the teachings of Wheatley et al. in the above-cited U.S. patent 5,107,225 incorporated herein. In cases where the required linear gain does not exceed the linear gain region of amplifiers 16 and 18, circuits 12 and 14 need not compensate for the nonlinearities. The receiver amplifier 16 and the transmitter amplifier 18 are each shown having two compensation signal inputs in accordance with the thermal compensation method of this invention.

Figure 2 provides a simple block diagram of a single two-stage amplifier employing the temperature compensation circuit 10 of this invention. A first amplifier stage 20 is coupled through a filter 22 to a second amplifier stage 24 in a configuration that can be best appreciated with reference to the teachings of Wheatley in the above-cited U.S. patent No. 5,099,204 incorporated herein. The single amplifier device gain

compensation circuit 26 functions similarly to circuits 12 and 14 (Figure 1) except that one device gain compensation signal is provided on line 28 to both amplifiers 20 and 24. Note that circuit 26 need not compensate for nonlinearities in cases where the amplifiers do not exceed their range of linear operation.

Figures 3 and 4 provide preferred embodiments of the temperature compensation circuit 10 and device compensation circuits 12 and 14 from Figure 1. Figure 3 shows circuit 10 having a single operational amplifier (op amp) 30 and a thermistor 32. In operation, circuit 10 first divides the power supply voltage V_{CC} across the resistor R1 and thermistor 32 to create intermediate voltage 34. Intermediate voltage 34 is divided across a voltage divider formed by the resistors R2 and R3. The resulting voltage on line 36 is the thermal compensation signal (VG1-RX) for the receiver amplifier 16 (Figure 1) and for amplifiers 20 and 24 (as VG1) in Figure 2.

The thermal gain compensation signal is also presented to the noninverting input of operational amplifier 30, which is configured to operate as a unity gain isolation amplifier. Thus, the output signal on line 38 is equal in amplitude to temperature gain compensation signal 36 created at the amplifier output. The output signal on line 38 is divided by the resistors R4 and R5 to create second thermal compensation signal on line 40. The second thermal compensation signal is provided as the transmitter amplifier thermal compensation signal (VG1-TX) shown in Figure 1. The thermal compensation signals for transmit and receive in this example are different due to difference in the transmit and receive amplifiers. The difference which causes the creation of two thermal compensation signals can include the device type, the impedance that the device drives, or the frequency at which the device operates. In the general case, the thermal compensation signal could be the same for the receive and transmit circuitry.

Figure 4 shows a preferred embodiment of receiver amplifier device compensation circuit 12 (Figure 1). Circuit 12 employs an operational amplifier 42 to compare an AGC reference signal at line 44 and a received signal strength indicator (RSSI) signal at line 46, producing on line 28 the amplifier device gain compensation signal (VG2-RX of Figure 1 and VG2 of Figure 2). In operation, circuit 12 accepts on line 46 the RSSI signal from a high impedance source at the inverting input of operational amplifier 42. The device compensation signal provided on line 28 is fed back through capacitor C1 to the noninverting input of op amp 42. Thus op amp 42 is configured as an integrator with resistor R6 setting the time constant. The

AGC reference signal provided on line 44 is divided by the resistors R7 and R8, and the resulting divided signal 48 is presented to the noninverting input of operational amplifier 42. The capacitor C2 coupled across resistor R8 acts as a roll-off filter at higher frequencies. Thus, the device compensation signal represents the difference between the low-frequency components of the RSSI and AGC reference signals.

Figure 4 also provides a preferred embodiment for transmitter amplifier device compensation circuit 14 from Figure 1. Circuit 14 is not used in Figure 2. An operational amplifier 50 is employed to combine the receiver amplifier device gain compensation signal with a transmitter gain adjustment signal, provided at line 52, and a transmitter gain control signal provided at line 54 to produce the transmitter amplifier device gain compensation signal (VG2-TX) at line 56 as shown in Figure 1. The receiver amplifier device gain compensation signal on line 28 is presented to the low pass voltage divider made up of resistors R10 and R11 and bypass capacitor C3, which removes all significant AC components from the receiver amplifier device gain compensation signal. The divided filtered signal at line 56 is presented to the noninverting input of operational amplifier 50.

The transmitter gain control signal on line 54 and the transmitter gain adjustment signal on line 52 are combined through resistors R13 and R14 respectively and presented on line 58 to the inverting input of operational amplifier 50. The op amp output signal presented on line 60 is fed back through the nonlinear divider network made up of R15 and C4 to inverting input of op amp 50 such that op amp 50 operates as a low pass summer. Finally, the op amp output signal on line 60 is divided through the network made up of resistor R16 and capacitor C5 to produce on line 56 the transmitter amplifier device gain compensation signal (VG2-TX). Each of the above linear and nonlinear voltage divider networks interact to provide the necessary characteristics for proper device gain compensation signal level at line 56.

Figure 5 provides an illustrative three-stage embodiment of receiver amplifier 16 from Figure 1. Each of the three stages employs a dual-gate field effect transistor (FET). A received signal is input to amplifier 16 at line 62 and is amplified through a first stage employing the FET 64, a second stage employing the FET 66 and a third stage employing the FET 68, which creates the output signal at line 70. The receiver amplifier thermal compensation signal (VG1-RX of Figure 1 and VG1 of Figure 2) as provided on line 36 of Figure 5 is introduced through a series resistor to the first gate G1 of each FET 64, 66, and 68, as shown in Figure 5. Similarly, the receiver amplifier

device gain compensation signal (VG2-RX of Figure 1 and VG2 of Figure 2) as provided on line 28 of Figure 4 is presented through a series resistor to the second gate G2 of each FET. The nonlinear circuits coupled to the drains of each FET stage are tuned networks designed to present a purely resistive load to the drain of each FET stage. Receiver amplifier 16 is tuned to an intermediate carrier frequency predetermined for the transceiver illustrated in Figure 1, which could be 70 MHz, for instance.

Figure 6 shows an illustrative embodiment of transmitter amplifier 18 from Figure 1. Amplifier 18 is very similar to amplifier 16 (Figure 5) in that it is a three-stage dual-gate FET tuned amplifier. Amplifier 18 is tuned to the transmitter intermediate carrier frequency predetermined for the transceiver illustrated in Figure 1, which could be 115 MHz, for instance. The transmitter intermediate carrier signal is presented at amplifier input 72, and is subsequently amplified by the three FET stages, which include FETs 74, 76, and 78. The third stage output signal is at line 80. Again, as in Figure 5, the transmitter amplifier thermal compensation signal (VG1-TX of Figure 1) as provided on line 40 of Figure 3 is coupled through a series resistor at the first gate G1 of each FET. The transmitter amplifier device gain compensation signal (VG2-TX of Figure 1) as provided on line 56 of Figure 4 is independently coupled through a series resister at the second gate G2 of each FET.

In both Figures 5 and 6, the two independent signals, one setting the gain of the device and the other for compensating for changes in the gain as a function of temperature, are introduced into each FET stage by exploiting the dual-gate feature of each FET. This architecture provides for compensation with a simple temperature compensation signal that is independent of the gain control mechanism of the device.

Figure 7 illustrates the need for temperature compensation in a FET circuit that is being used as a variable gain amplifier. In Figure 7, experimental data is presented at three different temperatures. The horizontal axis represents the voltage level applied to the second gate G2 of the FET stages and the vertical axis represents the gain of the FET stages normalized such that the highest measured gain is 0 dB. The portion of the curve from about 0.5 Volts up to about 3.5 Volts, where the response of the circuit is nearly linear, is representative of the useful range of the FET stages. (The range could be extended using the techniques described in previously mentioned in U.S. Patent No. 5,107,225.) Curve 102 graphs the normalized gain as a function of the second gate G2 voltage of a set of FET's at room temperature. Curve 100 graphs the normalized gain of the same circuit at a

reduced temperature. Curve 100 is linear over a similar region as curve 102 but is steeper in slope. Curve 100 diverges from curve 102 causing a temperature error of more than 7 dB at a second gate G2 voltage of about 3.5 Volts. Curve 104 graphs the normalized gain of the same circuit at an elevated temperature. Curve 104 is linear over a similar voltage as curve 102 but is less steep in slope. Curve 104 diverges from curve 102 causing a temperature error of more than -6 dB at a second gate G2 voltage of 3.5 Volts. The temperature compensation mechanism of the present invention seeks to compensate for the change in slope seen in Figure 7.

Figure 8 graphs the slope of the same FET stages of Figure 7 over a range of first gate G1 voltages at a fixed temperature. The measured data reflects the ability of first gate G1 voltage to change the slope of the gain curve. In Figure 8 the horizontal axis represents the voltage level applied to the first gate G1 the FET stages in Volts. The vertical axis represents the change in gain from a second gate G2 equal to one Volt to a second gate G2 equal to two Volts and has units of dB/Volt. Since first gate G1 voltage can be used to change the slope of the gain curve, first gate G1 voltage can be used to compensate for the effect of temperature on the slope of the gain curve independent of any specific value of second gate G2 voltage. The present invention creates a G1 voltage that is a function of temperature and thus compensates for the slope change caused by temperature by counteracting the temperature change with a change in first gate voltage G1 having the opposite effect on slope.

In Figure 7, the first gate G1 voltage was held constant over temperature. In Figure 9 using the same FET stages, the value of the voltage applied to the first gate G1 is changed as a function of temperature and the curves of Figure 9 track tightly over temperature. Curve 112 represent the gain curve a room temperature while Curves 110 and 114 represent the gain curve at a reduced and elevated temperature respectively. The error over the usefully range to the FET stages is a reduced function of temperature and the slope of the three curves is nearly identical. The error between the three lines is about 1dB which is a significant improvement over Figure 7.

Clearly, other embodiments and modifications of this invention will occur readily to those of ordinary skill in the art in view of these teachings. For instance, if an even smaller error is desired than the results shown in Figure 9, it may be advantageous to add a temperature dependence to the gain compensation signal also. Simply adding the temperature compensation signal (or a scaled version thereof) to the gain compensation signal achieves a temperature dependence of the gain compensation signal.

The effect of such compensation would be to overlay the parallel lines of Figure 9.

The previous description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. The various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

CLAIMS

1. A method for amplifying an input signal having a large dynamic range such that the signal gain control in decibels is a linear function of a power control signal, said method comprising the steps of:

(a) generating a first compensation signal corresponding to said power control signal according to a first predetermined characteristic;

(b) generating a second compensation signal corresponding to temperature according to a second predetermined characteristic; and

(c) amplifying said input signal by a signal gain factor corresponding to a combination of said first and said second compensation signals and providing a corresponding output signal, said signal gain factor in decibels being a linear function of said power control signal independent of temperature over a predetermined range.

2. The method of Claim 1 wherein said amplifying step (c) comprises the steps of:

(c.1) amplifying said input signal at an input gain level determined by said first and said second compensation signals and providing a corresponding first amplified signal;

(c.2) filtering said first amplified signal; and

(c.3) amplifying said filtered first amplified signal at an output gain level determined by said first and said second compensation signals and providing a said corresponding output signal.

3. A method of Claim 2 wherein said first generating step (a) comprises the steps of:

(a.1) modifying said power control signal according to a first gain compensation function when said power control signal is below a first predetermined level; and

(a.2) modifying said power control signal according to a second gain compensation function when said power control signal is above said first predetermined level.

4. A circuit for amplifying an input signal having a signal gain in decibels that is a temperature-independent linear function of a power control signal, said circuit comprising:

first compensator means for receiving said power control signal and for creating a corresponding first compensation signal responsive thereto according to a first predetermined characteristic;

second compensator means for creating a second compensation signal responsive to temperature according to a second predetermined characteristic; and

amplifier means coupled to said first and said second compensator means for receiving said input signal and said first and second compensation signals, for amplifying said input signal by a signal gain factor corresponding to a combination of said first and second compensation signals and for providing a corresponding output signal, said signal gain factor in decibels being a linear function of said power control signal and independent of temperature over a predetermined range.

5. The circuit of Claim 4 wherein said amplifier means comprises:

input amplifier means for receiving said input signal and said first and second compensation signals, for amplifying said input signal at an input gain corresponding to a combination of said first and second compensation signals and for providing a corresponding input amplifier means output signal;

filter means coupled to said input amplifier means for receiving and filtering said input amplifier means output signal; and

output amplifier means coupled to said filter means for receiving said filtered input amplifier means output signal and said first and second compensation signals, for amplifying said filtered input amplifier means output signal at an output gain level corresponding to the combination of said first and second compensation signals and for providing a corresponding output amplifier means output signal.

6. The circuit of Claim 5 wherein:

said filter means has a predetermined input and output impedance;

said input amplifier means is further for providing a selected output impedance so as to match said filter means input impedance; and

said output amplifier means is further for providing a selected input impedance so as to match said filter means output impedance.

7. The circuit of Claim 6 wherein said input and output amplifier means each comprises a field effect transistor (FET) amplifier.

8. The circuit of Claim 4 wherein said first compensator means comprises:

an operational amplifier having a noninverting input capable of

receiving a reference voltage, having an inverting input capable of receiving an AGC signal and having an output; and

a nonlinear feedback network coupled between said operational amplifier output and said inverting input.

9. The circuit of Claim 4 wherein said second compensator means comprises:

an operational amplifier having a noninverting input capable of receiving a reference voltage, having an inverting input and having an output; and

a thermistor coupled to said noninverting input.

10. An amplifier circuit for use with an automatic gain control (AGC) circuit that generates an AGC signal for providing power gain control of an input signal over a high dynamic range responsive to said AGC signal such that said input signal power gain in dB is a linear function of said AGC control signal, said amplifier circuit comprising:

a first compensation circuit having an input and an output, said first compensation circuit being capable of receiving said AGC signal at said first compensation circuit input and capable of modifying said AGC signal according to one or more predetermined gain compensation characteristics so as to provide a modified AGC signal at said first compensation circuit output;

a second compensation circuit having an output, said second compensation circuit being capable of sensing the ambient temperature of said amplifier circuit and being capable of providing a temperature compensation signal according to one or more predetermined temperature compensation characteristics at said second compensation circuit output; and

an amplifier having a plurality of inputs and at least one output, a first one of said amplifier inputs being coupled to said first compensation circuit output, a second one of said amplifier inputs being coupled to said second compensation circuit output and a third one of said amplifier inputs being capable of receiving said input signal, said amplifier having portions of a gain range that are piecewise linear in decibels with respect to said AGC signal and said amplifier gain range being linear with respect to said modified AGC signal independent of said ambient amplifier circuit temperature.

11. The amplifier circuit of Claim 10 wherein said amplifier comprises:

a first amplifier having a plurality of inputs and an output, a first one of said amplifier inputs being coupled to said first compensation circuit output, a second one of said first amplifier inputs being coupled to said second compensation circuit output and a third one of said first amplifier inputs being capable of receiving said input signal, said first amplifier having portions of a gain range that are piecewise linear in decibels with respect to said AGC signal and said first signal amplifier gain range being linear in dB with respect to said modified AGC signal;

a filter having an input coupled to said first amplifier output and having an output; and

a second amplifier having a plurality of inputs and an output, a first one of said second amplifier inputs being coupled to said first compensation circuit output, a second one of said second amplifier inputs being coupled to said second compensation circuit output and a third one of said second amplifier inputs being coupled to said filter output, said second amplifier having portions of a gain range that are piecewise linear in decibels with respect to said AGC signal and said second amplifier gain range being linear in dB with respect to said modified AGC signal.

12. The circuit of Claim 11 wherein said first and second amplifiers each comprise a dual-gate field effect transistor (FET) amplifier.

13. The amplifier circuit of Claim 11 wherein said first compensation circuit comprises:

an operational amplifier having a noninverting input capable of receiving a reference voltage, having an inverting input capable of receiving an AGC signal and having an output; and

a nonlinear feedback network coupled between said operational amplifier output and said inverting input.

14. The amplifier circuit of Claim 11 wherein said second compensation circuit comprises:

an operational amplifier having a noninverting input capable of receiving a reference voltage, having an inverting input and having an output; and

a thermistor coupled to said noninverting input.

15. In a transceiver having a receiver amplifier and a transmitter amplifier, a method for amplifying a transmitter signal responsive to the measured amplitude of a received signal such that the amplified transmitter signal amplitude varies inversely with said measured received signal amplitude over a predetermined range of amplitude and temperature, said method comprising the unordered steps of:

(a) creating a received signal strength indicator (RSSI) signal responsive to said received signal representing said measured received signal amplitude in decibels;

(b) creating a first receiver compensation signal (RCS) and a first transmitter compensation signal (TCS) responsive to said RSSI signal according to at least one predetermined characteristic;

(c) creating a second RCS and a second TCS responsive to the ambient temperature of said transceiver according to at least one predetermined characteristic; and

(d) amplifying said transmitter signal by a signal gain factor corresponding to a combination of said first TCS and said second TCS.

16. The method of Claim 15 wherein said second creating step (b) comprises the steps of:

(b.1) creating said first RCS responsive to said RSSI signal according to a predetermined receiver characteristic; and

(b.2) creating said first TCS responsive to said first RCS according to a first predetermined transmitter characteristic.

17. The method of Claim 16 wherein said third creating step (c) comprises the steps of:

(c.1) creating said second RCS responsive to said ambient temperature according to a predetermined temperature characteristic; and

(c.2) creating said second TCS responsive to said second RCS according to a second predetermined transmitter characteristic.

18. In a transceiver having a receiver amplifier and a transmitter amplifier, said transmitter amplifier having a transmitter input signal and producing a transmitter output signal, a transmitter amplifier automatic gain control (AGC) circuit comprising:

measurement means coupled to said receiver amplifier for measuring a variable-power received signal from said receiver amplifier and for creating a received signal strength indicator (RSSI) signal

representing said received signal power;

integration means coupled to said measurement means for receiving a power control signal corresponding to a desired power level of said transmitter amplifier output signal, for integrating with respect to time a difference between said RSSI signal and said power control signal and for creating a first control signal;

first compensator means coupled to said receiver amplifier and to said transmitter amplifier for receiving said first control signal and for creating a corresponding first compensation signal responsive thereto according to a first predetermined characteristic;

second compensator means for creating a second compensation signal responsive to the ambient temperature of said transceiver according to a second predetermined characteristic; and

amplifier means coupled to said first and said second compensator means for receiving said transmitter input signal and said first and said second compensation signal, for amplifying said transmitter input signal by a signal gain factor corresponding to a combination of said first and said second compensation signals and for producing said transmitter output signal, said signal gain factor in decibels being a linear function of said receiver signal power in decibels over a predetermined range of signal power and temperature.

19. The AGC circuit of Claim 18 wherein said amplifier means comprises:

input amplifier means for receiving said input signals and said first and second compensation signals, for amplifying said input signal at an input gain corresponding to a combination of said first and second compensation signals and for providing a corresponding input amplifier means output signal;

filter means coupled to said input amplifier means for receiving and filtering said input amplifier means output signal; and

output amplifier means coupled to said filter means for receiving said filtered input amplifier means output signal and said first and second compensation signals, for amplifying said filtered input amplifier means output signal at an output gain level corresponding to the combination of said first and second compensation signals and for providing a corresponding output amplifier means output signal.

20. The AGC circuit of Claim 19 wherein:
said filter means has a predetermined input and output impedance;
said input amplifier means is further for providing a selected output impedance so as to match said filter means input impedance; and
said output amplifier means is further for providing a selected input impedance so as to match said filter means output impedance.

21. The AGC circuit of Claim 20 wherein said input and output amplifier means each comprises a field effect transistor (FET) amplifier.

22. An circuit comprising:
a temperature sensing circuit having a output;
a gain setting circuit having an output; and
a dual gate field effect transistor circuit having a first gate terminal coupled to said temperature sensing circuit output and a second gate terminal coupled to said gain setting circuit output.

23. The circuit of Claim 22 wherein said dual gate field effect transistor circuit further comprises:
a biasing circuit coupled to a drain terminal and to a source terminal of said dual gate field effect transistor circuit;
an analog signal reception circuit coupled to said first gate terminal; and
an amplified output signal circuit coupled to said drain terminal.

24. The circuit of Claim 23 wherein said analog signal reception circuit comprises an inductor providing a resonate tank having a resonate frequency.

25. The circuit of Claim 23 wherein said amplified signal output circuit comprises an inductor providing a resonate tank having a resonate frequency.

26. The circuit of Claim 22 wherein said temperature sensing circuit comprises a thermistor.

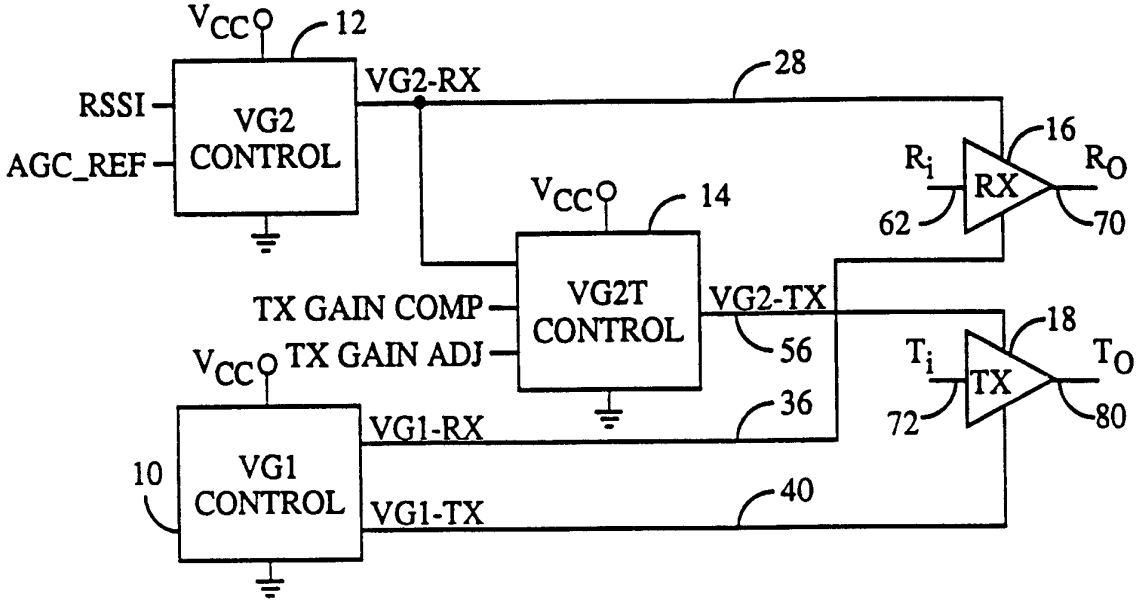
V_{CC}
12
RSSI
AGC_REF
VG2
CONTROL
VG2-RX
28
16
R_i
RX
R_O
62
70
V_{CC}
14
VG2T
CONTROL
TX GAIN COMP
TX GAIN ADJ
VG2-TX
56
18
T_i
TX
T_O
72
80
V_{CC}
VG1
CONTROL
10
VG1-RX
36
VG1-TX
40

FIG. 1

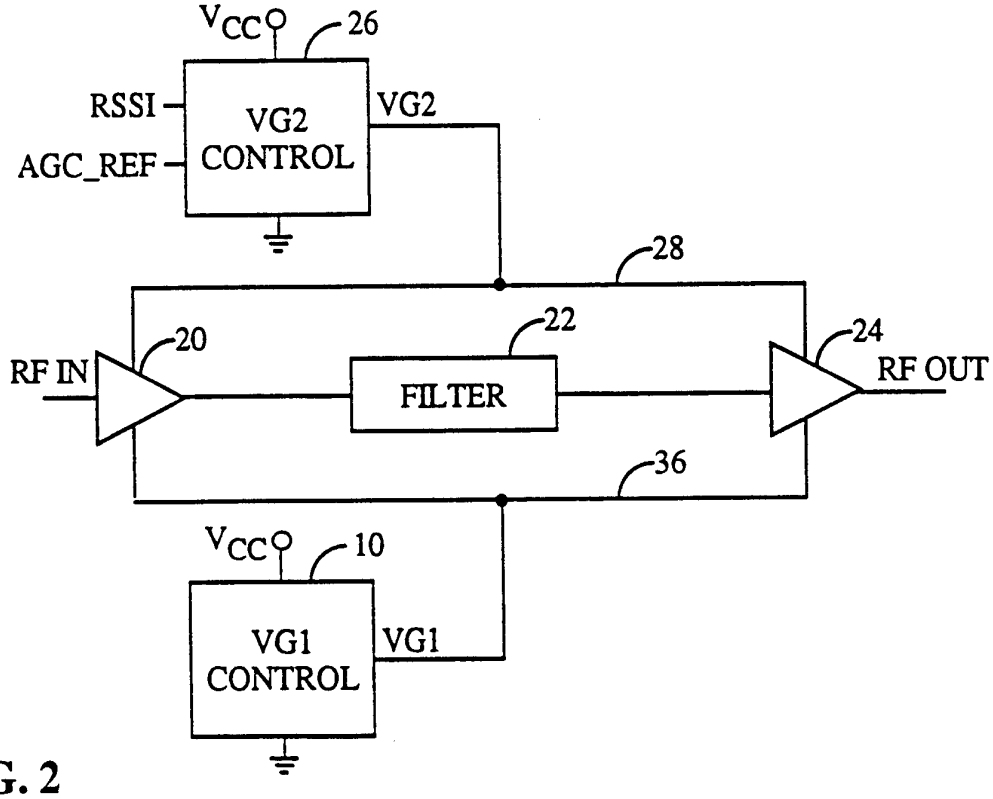
V_{CC}
26
RSSI
AGC_REF
VG2
CONTROL
VG2
28
RF IN
20
22
FILTER
24
RF OUT
36
V_{CC}
10
VG1
CONTROL
VG1

FIG. 2

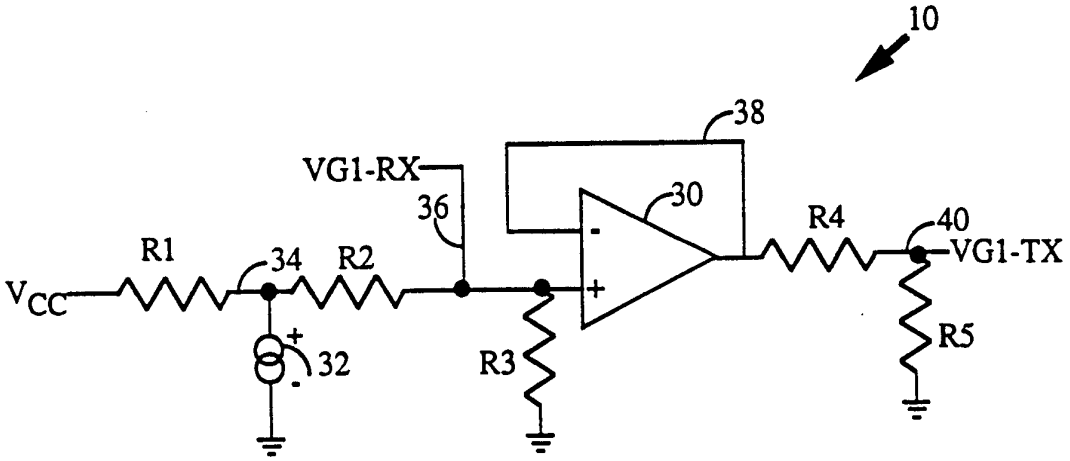
10
38
VG1-RX
36
30
R4
40
VG1-TX
R1
34
R2
V_{CC}
32
R3
R5

FIG. 3

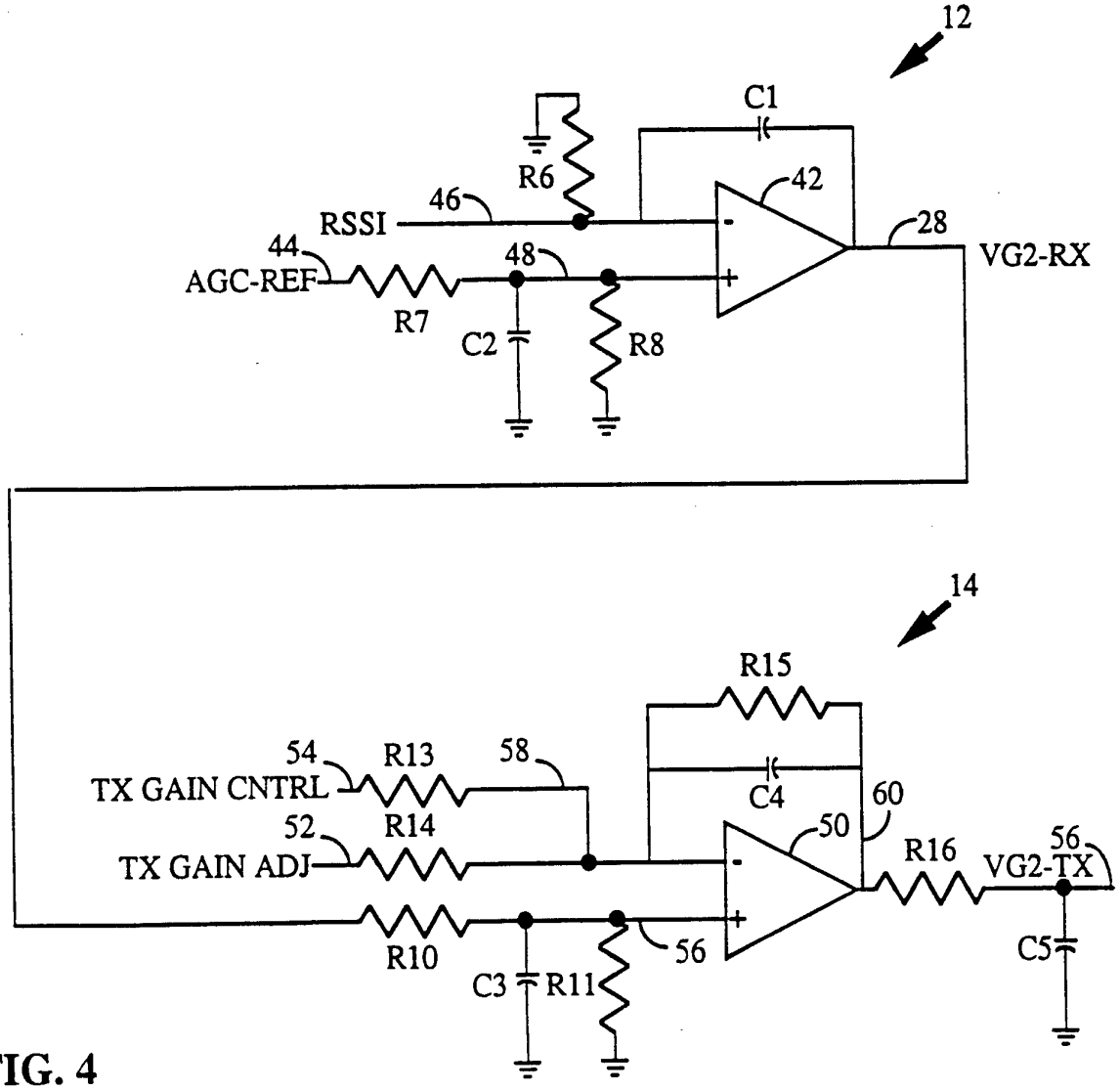
12
C1
R6
42
46
RSSI
28
VG2-RX
44
AGC-REF
48
R7
C2
R8
14
R15
54
R13
58
TX GAIN CNTRL
C4
60
52
R14
50
R16
56
VG2-TX
TX GAIN ADJ
R10
56
C5
C3
R11

FIG. 4

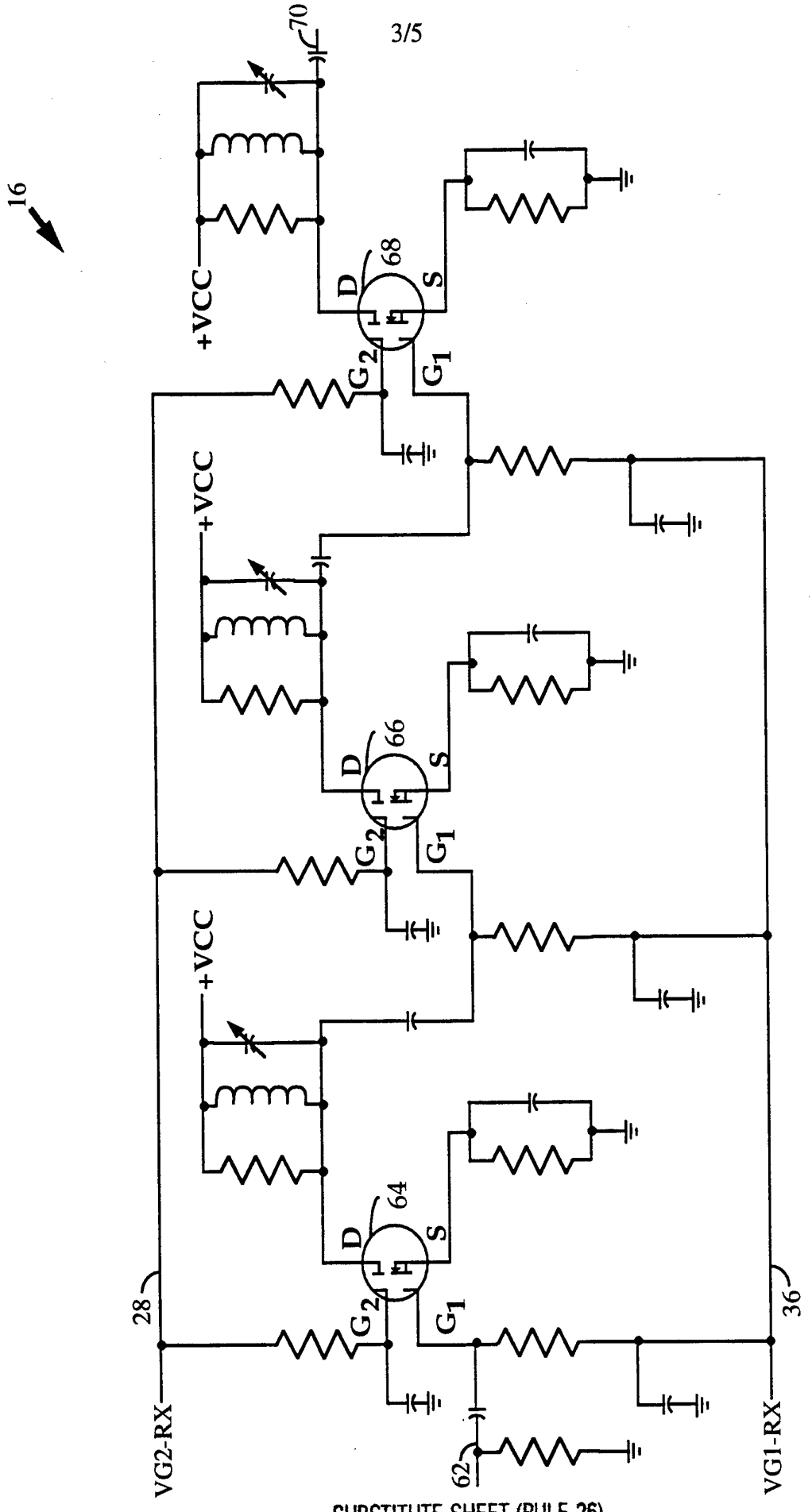
16
70
+VCC
68
D
S
G2
G1
+VCC
66
D
S
G2
G1
+VCC
64
D
S
G2
G1
28
36
VG2-RX
VG1-RX
62

FIG. 5

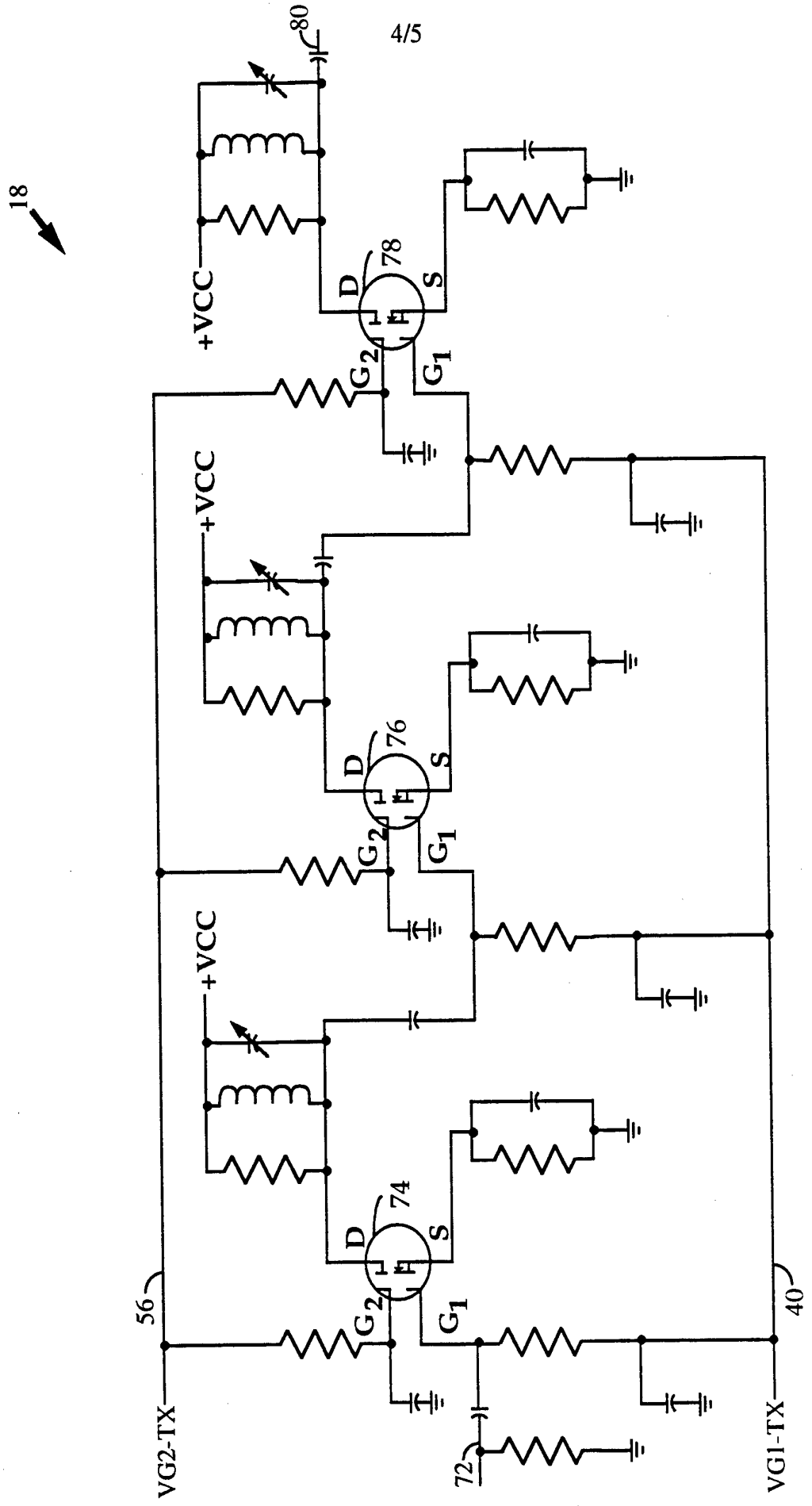
18
80
+VCC
78
D
S
G2
G1
+VCC
76
D
S
G2
G1
+VCC
74
D
S
G2
G1
56
40
72
VG2-TX
VG1-TX

FIG. 6

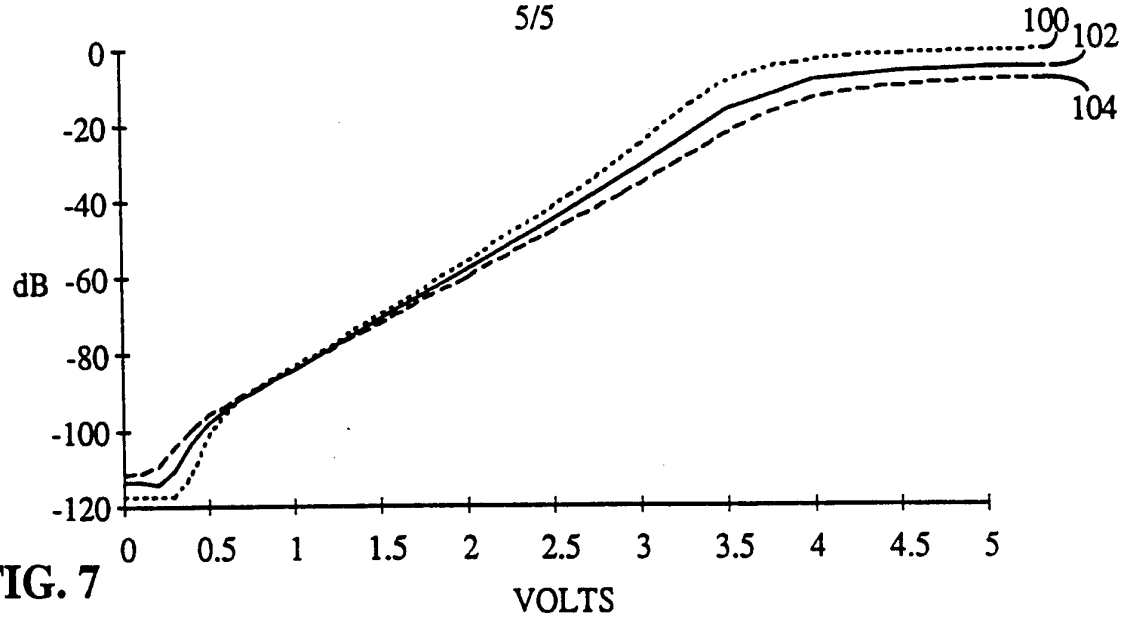

FIG. 7

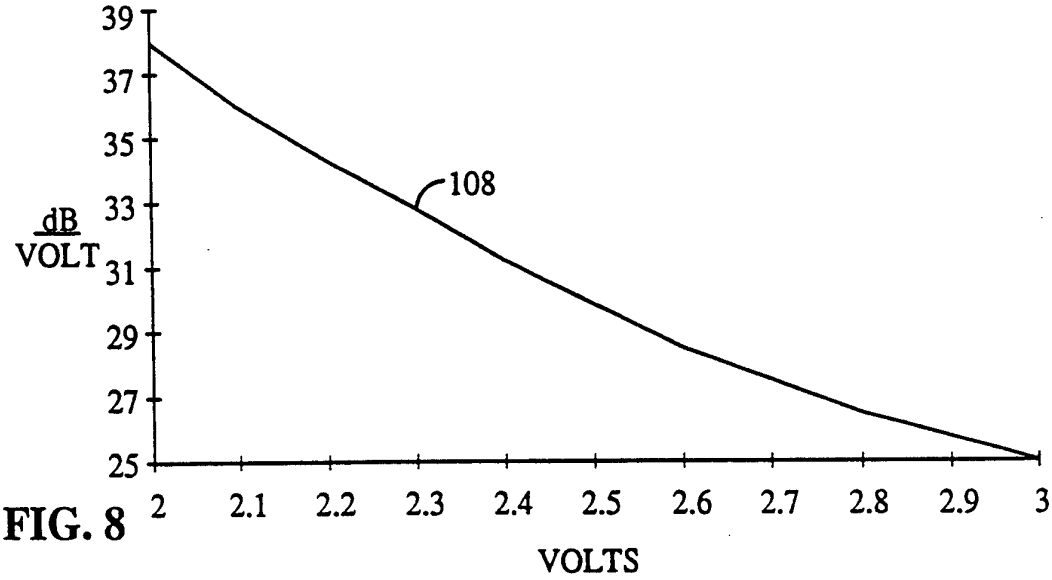

FIG. 8

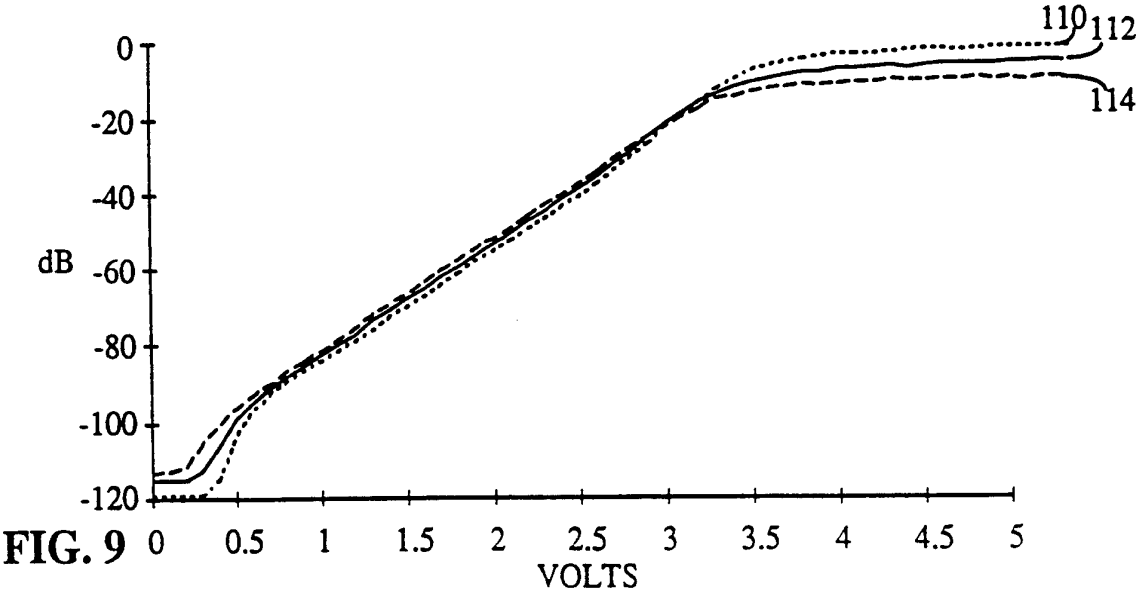

FIG. 9

INTERNATIONAL SEARCH REPORT

Interna .l Application No
PCT/US 94/06796

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 H03G1/04 H03F1/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 H03G H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,5 107 225 (C. E. WHEATLEY ET AL.) 21 April 1992 cited in the application see the whole document ---	1-26
X	US,A,5 099 204 (C. E. WHEATLEY) 24 March 1992 cited in the application see the whole document ---	1-14
X	EP,A,0 537 733 (FIAR FABBRICA ITALIANA APPARECCHIATURE RADIOELETTRICHE) 21 April 1993 see the whole document -----	1,4,8-10

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
6 October 1994	21. 10. 94
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+ 31-70) 340-3016	Authorized officer Blaas, D-L

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

..formation on patent family members

Inter. nal Application No
PCT/US 94/06796

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A-5107225	21-04-92	AU-B-	652807	08-09-94
		AU-A-	1241692	25-06-92
		BG-A-	97790	25-04-94
		CA-A-	2093638	31-05-92
		EP-A-	0559840	15-09-93
		FI-A-	932238	17-05-93
		JP-T-	6505138	09-06-94
		US-A-	5283536	01-02-94
		WO-A-	9210028	11-06-92
US-A-5099204	24-03-92	AU-B-	648364	21-04-94
		AU-A-	8943091	20-05-92
		CA-A-	2094133	16-04-92
		EP-A-	0553300	04-08-93
		JP-T-	6504653	26-05-94
		WO-A-	9207424	30-04-92
EP-A-0537733	21-04-93	NONE		