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(71) Applicant: INVENSENSE, INC. [US/US]; 1745 Technology Drive, San Jose, California 95110 (US).

(72) Inventors: LEE, Daesung; 1712 Hogar Drive, San Jose, California 95124 (US). CUTHBERTSON, Alan; 1771 Magnolia Lake Court, San Jose, California 95131 (US).

(74) Agent: TABARROK, Amir et al.; 2445 Faber Place, Suite 250, Palo Alto, California 94303 (US).

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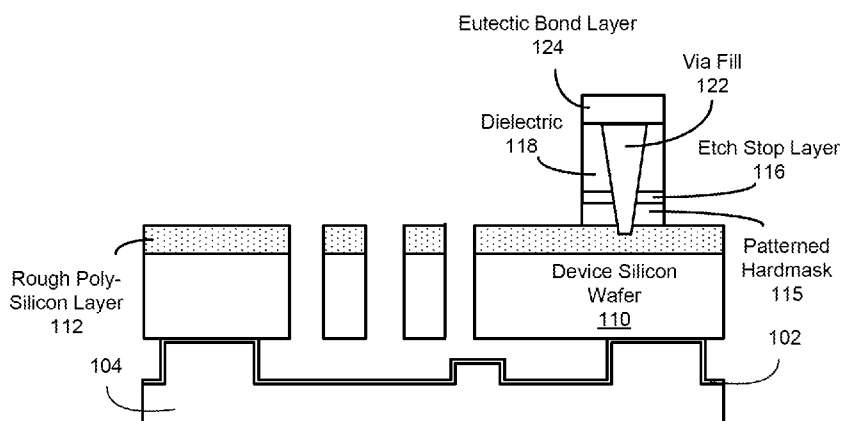


Figure 15

(57) **Abstract:** A method including fusion bonding a handle wafer to a first side of a device wafer. The method further includes depositing a hardmask on a second side of the device wafer, wherein the second side is planar. An etch stop layer is deposited over the hardmask and an exposed portion of the second side of the device wafer. A dielectric layer is formed over the etch stop layer. A via is formed within the dielectric layer. The via is filled with conductive material. A eutectic bond layer is formed over the conductive material. Portions of the dielectric layer uncovered by the eutectic bond layer is etched to expose the etch stop layer. The exposed portions of the etch stop layer is etched. A micro-electro-mechanical system (MEMS) device pattern is etched into the device wafer.



ACTUATOR LAYER PATTERNING WITH TOPOGRAPHY

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority of U.S. Patent Application Serial No. 17/195,346 filed March 8, 2021, entitled “ACTUATOR LAYER PATTERNING WITH TOPOGRAPHY.”, and claims the benefit of U.S. Provisional Patent Application Serial No. 63/198,251 filed October 6, 2020, entitled “ACTUATOR LAYER PATTERNING WITH TOPOGRAPHY.”

BACKGROUND

[0002] MEMS (“micro-electro-mechanical systems”) are a class of devices that are fabricated using semiconductor-like processes and exhibit mechanical characteristics. For example, MEMS devices may include the ability to move or deform. In many cases, but not always, MEMS interact with electrical signals. A MEMS device may refer to a semiconductor device that is implemented as a micro-electro-mechanical system. A MEMS device includes mechanical elements and may optionally include electronics (e.g. electronics for sensing). MEMS devices include but are not limited to, for example, gyroscopes, accelerometers, magnetometers, pressure sensors, etc. As technology advances, it is desirable to reduce the size of the MEMS devices, thereby resulting in die size reduction.

SUMMARY

[0003] Provided herein is a method including fusion bonding a handle wafer to a first side of a device wafer. The method further includes depositing a hardmask on a second side of the device wafer, wherein the second side is planar. An etch stop layer is deposited over the hardmask and an exposed portion of the second side of the device wafer. A dielectric layer is formed over the etch stop layer. A via is formed within the dielectric layer. The via is filled with conductive material. A eutectic bond layer is formed over the conductive material. Portions of the dielectric layer uncovered by the eutectic bond layer is etched to expose the etch

stop layer. The exposed portions of the etch stop layer is etched. A micro-electro-mechanical system (MEMS) device pattern is etched into the device wafer.

[0004] Provided herein is another method including fusion bonding a handle wafer to a first side of a device wafer. A hardmask is deposited on a second side of the device wafer, wherein the second side is planar. A dielectric layer is deposited over the hardmask and an exposed portion of the second side of the device wafer. A via is formed within the dielectric layer. The via is filled with conductive material. A eutectic bond layer is formed over the conductive material. Portions of the dielectric layer uncovered by the eutectic bond layer is etched to expose the hardmask. A micro-electro-mechanical system (MEMS) device pattern is etched into the device wafer.

[0005] Provided herein is a device including a handle wafer and a device wafer having a first side that is opposite to a second side, wherein the first side of the device wafer is fusion bonded to the handle wafer. The second side of the device wafer has a first portion and a second portion, wherein the second portion comprises a dielectric layer including a via formed therein, and wherein the via is filled with conductive material, and wherein the second portion of the second side of the device wafer further includes a eutectic bond layer formed on the dielectric layer and further on the via and the conductive material.

[0006] These and other features and advantages will be apparent from a reading of the following detailed description.

BRIEF DESCRIPTION OF DRAWINGS

[0007] Figure 1 shows a MEMS wafer at an early stage of manufacture according to one aspect of the present embodiments.

[0008] Figure 2 shows the MEMS wafer after hardmask deposition according to one aspect of the present embodiments.

[0009] Figure 3 shows the MEMS wafer after patterning the hardmask according to one aspect of the present embodiments.

[0010] Figure 4 shows the MEMS wafer after etch stop layer deposition according to one aspect of the present embodiments.

[0011] Figure 5 shows the MEMS wafer after formation of a dielectric layer over the etch stop layer according to one aspect of the present embodiments.

[0012] Figure 6 shows the MEMS wafer after deposition of a photoresist over the dielectric layer according to one aspect of the present embodiments.

[0013] Figure 7 shows the MEMS wafer after formation of a via therein according to one aspect of the present embodiments.

[0014] Figure 8 shows the MEMS wafer after removal of the photoresist according to one aspect of the present embodiments.

[0015] Figure 9 shows the MEMS wafer after filling the via according to one aspect of the present embodiments.

[0016] Figure 10 shows the MEMS wafer after formation of a eutectic bond layer according to one aspect of the present embodiments.

[0017] Figure 11 shows the MEMS wafer after forming a photoresist layer over a eutectic bond layer according to one aspect of the present embodiments.

[0018] Figure 12 shows the MEMS wafer after an etch process to expose the etch stop layer according to one aspect of the present embodiments.

[0019] Figure 13 shows the MEMS wafer after removal of the etch stop layer according to one aspect of the present embodiments.

[0020] Figure 14 shows the MEMS wafer after etching MEMS device pattern according to one aspect of the present embodiments.

[0021] Figure 15 shows the MEMS wafer after removing the patterned hard mask according to one aspect of the present embodiments.

[0022] Figure 16 shows a MEMS wafer at an early stage of manufacture according to one aspect of the present embodiments.

[0023] Figure 17 shows the MEMS wafer after hardmask deposition according to one aspect of the present embodiments.

[0024] Figure 18 shows the MEMS wafer after patterning the hardmask according to one aspect of the present embodiments.

[0025] Figure 19 shows the MEMS wafer after etch stop layer deposition according to one aspect of the present embodiments.

[0026] Figure 20 shows the MEMS wafer after formation of a dielectric layer over the etch stop layer according to one aspect of the present embodiments.

[0027] Figure 21 shows the MEMS wafer after deposition of a photoresist over the dielectric layer according to one aspect of the present embodiments.

[0028] Figure 22 shows the MEMS wafer after formation of a via therein according to one aspect of the present embodiments.

[0029] Figure 23 shows the MEMS wafer after removal of the photoresist according to one aspect of the present embodiments.

[0030] Figure 24 shows the MEMS wafer after filling the via according to one aspect of the present embodiments.

[0031] Figure 25 shows the MEMS wafer after formation of a eutectic bond layer according to one aspect of the present embodiments.

[0032] Figure 26 shows the MEMS wafer after forming a photoresist layer over a eutectic bond layer according to one aspect of the present embodiments.

[0033] Figure 27 shows the MEMS wafer after an etch process to expose the etch stop layer according to one aspect of the present embodiments.

[0034] Figure 28 shows the MEMS wafer after removal of the etch stop layer according to one aspect of the present embodiments.

[0035] Figure 29 shows the MEMS wafer after etching MEMS device pattern according to one aspect of the present embodiments.

[0036] Figure 30 shows the MEMS wafer after removing the patterned hard mask according to one aspect of the present embodiments.

[0037] Figure 31 shows a MEMS wafer at an early stage of manufacture according to one aspect of the present embodiments.

[0038] Figure 32 shows the MEMS wafer after hardmask deposition according to one aspect of the present embodiments.

[0039] Figure 33 shows the MEMS wafer after patterning the hardmask according to one aspect of the present embodiments.

[0040] Figure 34 shows the MEMS wafer after formation of a dielectric layer over the patterned hardmask according to one aspect of the present embodiments.

[0041] Figure 35 shows the MEMS wafer after deposition of a photoresist over the dielectric layer according to one aspect of the present embodiments.

[0042] Figure 36 shows the MEMS wafer after formation of a via therein according to one aspect of the present embodiments.

[0043] Figure 37 shows the MEMS wafer after removal of the photoresist according to one aspect of the present embodiments.

[0044] Figure 38 shows the MEMS wafer after filling the via according to one aspect of the present embodiments.

[0045] Figure 39 shows the MEMS wafer after formation of a eutectic bond layer according to one aspect of the present embodiments.

[0046] Figure 40 shows the MEMS wafer after forming a photoresist layer over a eutectic bond layer according to one aspect of the present embodiments.

[0047] Figure 41 shows the MEMS wafer after an etch process to expose the patterned hardmask according to one aspect of the present embodiments.

[0048] Figure 42 shows the MEMS wafer after etching MEMS device pattern according to one aspect of the present embodiments.

[0049] Figure 43 shows the MEMS wafer after removing the patterned hard mask according to one aspect of the present embodiments.

[0050] Figure 44 shows an exemplary flow diagram for actuator layer patterning with topography according to one aspect of the present embodiments.

[0051] Figure 45 shows another exemplary flow diagram for actuator layer patterning with topography according to one aspect of the present embodiments.

DESCRIPTION

[0052] Before various embodiments are described in greater detail, it should be understood that the embodiments are not limiting, as elements in such embodiments may vary. It should likewise be understood that a particular embodiment described and/or illustrated herein has elements which may be readily separated from the particular embodiment and optionally combined with any of several other embodiments or substituted for elements in any of several other embodiments described herein.

[0053] It should also be understood that the terminology used herein is for the purpose of describing the certain concepts, and the terminology is not intended to be limiting. Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood in the art to which the embodiments pertain.

[0054] Unless indicated otherwise, ordinal numbers (e.g., first, second, third, etc.) are used to distinguish or identify different elements or steps in a group of elements or steps, and do not supply a serial or numerical limitation on the elements or steps of the embodiments thereof. For example, “first,” “second,” and “third” elements or steps need not necessarily appear in that order, and the embodiments thereof need not necessarily be limited to three elements or steps. It should also be understood that, unless indicated otherwise, any labels such as “left,” “right,” “front,” “back,” “top,” “middle,” “bottom,” “beside,” “forward,” “reverse,” “overlying,” “underlying,” “up,” “down,” or other similar terms such as “upper,” “lower,” “above,” “below,” “under,” “between,” “over,” “vertical,” “horizontal,” “proximal,” “distal,” and the like are used for convenience and are not intended to imply, for example, any particular fixed location, orientation, or direction. Instead, such labels are used to reflect, for example, relative location, orientation, or directions. It should also be understood that the singular forms of “a,” “an,” and “the” include plural references unless the context clearly dictates otherwise.

[0055] Terms such as “over,” “overlying,” “above,” “under,” etc. are understood to refer to elements that may be in direct contact or may have other elements in-between. For example, two layers may be in overlying contact, wherein one layer is over another layer and the two layers

physically contact. In another example, two layers may be separated by one or more layers, wherein a first layer is over a second layer and one or more intermediate layers are between the first and second layers, such that the first and second layers do not physically contact.

[0056] The existence of standoffs in MEMS sensors causes non-uniform thicknesses of photoresist, leading to lithography variations. Previous solutions have focused on increasing the distance between standoffs and key MEMS features, however these solutions increase the die size. Other solutions have focused on reducing the standoff height, however these solutions have used larger standoffs on the bond pair, thereby increasing the processing complexity of corresponding complementary metal-oxide semiconductor (“CMOS”) wafers. In yet other solutions a hard mask coated on the MEMS surface is used during fabrication in order to reduce the distance between the conductive standoffs and key MEMS features. That hard mask is used to create a planar topography in order to reduce or prevent photoresist buildup around the standoffs. Conductive standoffs (e.g. polysilicon) require the deposition of the thick standoff layer and doping. An alternative approach is to use a nonconductive standoff (e.g. oxide) but yet to form a via therein to provide the desired electrical connection. It is desirable to use the nonconductive layer in comparison to the conductive layer to form the thick standoff layer in terms of the manufacturability.

[0057] Referring now to Figure 1, a MEMS wafer at an early stage of manufacture according to one aspect of the present embodiments is shown. In some embodiments, a fusion bond oxide 102 fusion bonds a handle silicon wafer 104 to a first side of a device silicon wafer 110 (may also be referred to as the actuator layer). A second side of the device silicon wafer 110 is planar and opposite the first side. In some embodiments, a rough polysilicon layer 112 is deposited on the second side of the device silicon wafer 110. In some embodiments, the rough polysilicon layer 112 is deposited directly on the second side of the device silicon wafer 110. It is appreciated that the rough polysilicon layer 112 is optional and it improves stiction. In other embodiments, the rough polysilicon layer 112 may be absent. It is appreciated that the rough polysilicon layer 112 may be substituted with a different material in order to improve stiction. In other embodiments, the partial etch step is added on the rough polysilicon to increase the roughness. It is appreciated that this step is optional and it improves stiction further. In other

embodiments, the device silicon is patterned to provide the macroscopic topography (e.g. dimple) prior to the rough polysilicon deposition. It is appreciated that this step is optional and it improves stiction further.

[0058] Figure 2 shows the MEMS wafer after hardmask deposition according to one aspect of the present embodiments. A hardmask 114 is deposited on the second side of the device silicon wafer 110. In various embodiments the hardmask 114 includes oxide and is a different material than the device silicon wafer 110. In some embodiments, the hardmask 114 is deposited directly on the rough polysilicon layer 112 that covers the second side of the device silicon wafer 110.

[0059] Figure 3 shows the MEMS wafer after patterning the hardmask according to one aspect of the present embodiments. The hardmask 114 is etched to form a patterned hardmask 115 that corresponds to MEMS device pattern. The etching of the hardmask 114 etches the full thickness of the hardmask 114, thereby exposing portions of the rough polysilicon layer 112.

[0060] Figure 4 shows the MEMS wafer after etch stop layer deposition according to one aspect of the present embodiments. An etch stop layer 116 is deposited over the patterned hardmask 115 and the exposed portions of the rough polysilicon layer 112. It is appreciated that use of the etch stop layer 116 may be eliminated by using a different material for the hardmask 114 layer and the standoff that is formed in a later stage (as discussed in other embodiments). It is appreciated that the etch stop layer 116 may include nitride, oxy-nitride, or poly-silicon.

[0061] Figure 5 shows the MEMS wafer after formation of a dielectric layer over the etch stop layer according to one aspect of the present embodiments. A dielectric 118 is deposited over the etch stop layer 116. The dielectric 118 is used to form a standoff (discussed later below). The dielectric 118 may include a material similar to the hardmask 114. It is appreciated that as described above, the etch stop layer 116 may be eliminated if the hardmask 114 and the dielectric 118 are formed from different material (described in an embodiment later in this application). It is appreciated that the dielectric 118 may be deposited to form the standoff using plasma-enhanced chemical vapor deposition (PECVD)-oxide. In some embodiments, the

dielectric 118 is optionally planarized through a chemical mechanical polishing process. In other embodiments, the additional dielectric deposition and planarization through a chemical mechanical polishing process is optionally added prior to the deposition of the dielectric 118. The advantage is to better control the thickness of the dielectric 118 in comparison to adding a chemical mechanical polishing process after the deposition of the dielectric 118.

[0062] Figure 6 shows the MEMS wafer after deposition of a photoresist over the dielectric layer according to one aspect of the present embodiments. A photoresist 119 is deposited over the dielectric 118 and patterned.

[0063] Figure 7 shows the MEMS wafer after formation of a via therein according to one aspect of the present embodiments. The exposed portion of the dielectric 118 (uncovered by the photoresist 119) corresponds to the via that will be formed. As such, a via 120 is formed through the exposed portion of the dielectric 118, e.g., through lithography. In some embodiments, the via 120 extends through the etch stop layer 116. In some embodiments, the via 120 further extends through a portion of the rough polysilicon layer 112. It is appreciated that in some embodiments, the via 120 may extend to reach a top surface of the second side of the device silicon wafer 110.

[0064] Figure 8 shows the MEMS wafer after removal of the photoresist according to one aspect of the present embodiments. After the via 120 is formed, the photoresist 119 is removed.

[0065] Figure 9 shows the MEMS wafer after filling the via according to one aspect of the present embodiments. The via 120 is filled with via fill 122, e.g., conductive material such as tungsten, copper, polysilicon, Titanium Nitride, etc., to provide electrical connection between the MEMS and a CMOS once eutectically bonded to one another.

[0066] Figure 10 shows the MEMS wafer after formation of a eutectic bond layer according to one aspect of the present embodiments. A eutectic bond layer 124, e.g., Germanium, Aluminum, etc., may be deposited over a portion of the dielectric layer 118 and the via 120 that

is filled with via filled 122. In some embodiments, the eutectic bond layer 124 is formed through a sputtering process.

[0067] Figure 11 shows the MEMS wafer after forming a photoresist layer over a eutectic bond layer according to one aspect of the present embodiments. A photoresist 123 is deposited/patterned to cover a portion of the eutectic bond layer 124 that corresponds to the standoff. In this embodiment, the photoresist 123 covers the via 120, the via filled 122, and a portion of the dielectric 118 in proximity and surrounding the via 120. The photoresist 123 layer protect the eutectic bond layer 124 that lies underneath.

[0068] Figure 12 shows the MEMS wafer after an etch process to expose the etch stop layer according to one aspect of the present embodiments. The exposed portions of the eutectic bond layer 124 and the dielectric layer 118 underneath it are etched to expose the etch stop layer 116 underneath. In some embodiments, the eutectic bond layer 124 that is covered by the photoresist 123 remains in place while the exposed dielectric layer 118 (not covered by the photoresist 123) is etched and removed.

[0069] Figure 13 shows the MEMS wafer after removal of the etch stop layer according to one aspect of the present embodiments. The etch stop layer 116 that is exposed is removed to expose the patterned hardmask 115 underneath as well as the exposed portion of the rough polysilicon layer 112.

[0070] Figure 14 shows the MEMS wafer after etching MEMS device pattern according to one aspect of the present embodiments. MEMS device pattern corresponding to the device silicon wafer 110 and/or the rough polysilicon layer 112 that is not covered by the patterned hardmask 115 layer is etched. In other words, the exposed portions of the rough polysilicon layer 112 and/or the device silicon wafer 110 is etched to form the MEMS device pattern.

[0071] Figure 15 shows the MEMS wafer after removing the patterned hard mask according to one aspect of the present embodiments. The exposed patterned hardmask 115 is removed after forming the MEMS device pattern. In further steps (not shown), the standoffs (where the

eutectic bond layer 124 and underlying layers reside) of the device silicon wafer 110 are eutectically bonded to a CMOS wafer with eutectic bonds. In various embodiments, the eutectic bond metal 124 (e.g. germanium) on the standoffs may form the eutectic bonds with another eutectic bond metal (e.g. aluminum) on the CMOS wafer.

[0072] Figure 16 shows a MEMS wafer at an early stage of manufacture according to one aspect of the present embodiments. In some embodiments, a fusion bond oxide 102 fusion bonds a handle silicon wafer 104 to a first side of a device silicon wafer 210 (may also be referred to as the actuator layer). A second side of the device silicon wafer 210 is planar and opposite the first side.

[0073] Figure 17 shows the MEMS wafer after hardmask deposition according to one aspect of the present embodiments. A hardmask 214 is deposited on the second side of the device silicon wafer 210. In various embodiments the hardmask 214 includes oxide and is a different material than the device silicon wafer 210. In some embodiments, the hardmask 214 is deposited directly on the second side of the device silicon wafer 210.

[0074] Figure 18 shows the MEMS wafer after patterning the hardmask according to one aspect of the present embodiments. The hardmask 214 is etched to form a patterned hardmask 215 that corresponds to MEMS device pattern. The etching of the hardmask 214 etches the full thickness of the hardmask 214, thereby exposing portions of the device silicon wafer 210.

[0075] Figure 19 shows the MEMS wafer after etch stop layer deposition according to one aspect of the present embodiments. An etch stop layer 216 is deposited over the patterned hardmask 215 and the exposed portions of the device silicon wafer 210. It is appreciated that use of the etch stop layer 216 may be eliminated by using a different material for the hardmask 214 layer and the standoff that is formed in a later stage (as discussed in other embodiments). It is appreciated that the etch stop layer 216 may include nitride, oxy-nitride, or poly-silicon.

[0076] Figure 20 shows the MEMS wafer after formation of a dielectric layer over the etch stop layer according to one aspect of the present embodiments. A dielectric 218 is deposited

over the etch stop layer 216. The dielectric 218 is used to form a standoff (discussed later below). The dielectric 218 may include a material similar to the hardmask 214. It is appreciated that as described above, the etch stop layer 216 may be eliminated if the hardmask 214 and the dielectric 218 are formed from different material (described in an embodiment later in this application). It is appreciated that the dielectric 218 may be deposited to form the standoff using plasma-enhanced chemical vapor deposition (PECVD)-oxide. In some embodiments, the dielectric 218 is optionally planarized through a chemical mechanical polishing process.

[0077] Figure 21 shows the MEMS wafer after deposition of a photoresist over the dielectric layer according to one aspect of the present embodiments. A photoresist 219 is deposited over the dielectric 218 and patterned.

[0078] Figure 22 shows the MEMS wafer after formation of a via therein according to one aspect of the present embodiments. The exposed portion of the dielectric 218 (uncovered by the photoresist 219) corresponds to the via that will be formed. As such, a via 220 is formed through the exposed portion of the dielectric 218, e.g., through lithography. In some embodiments, the via 220 extends through the etch stop layer 216. In some embodiments, the via 220 further extends through a portion of a top surface of the second side of the device silicon wafer 210.

[0079] Figure 23 shows the MEMS wafer after removal of the photoresist according to one aspect of the present embodiments. After the via 220 is formed, the photoresist 219 is removed.

[0080] Figure 24 shows the MEMS wafer after filling the via according to one aspect of the present embodiments. The via 220 is filled with via fill 222, e.g., conductive material such as tungsten, copper, polysilicon, Titanium Nitride, etc., to provide electrical connection between the MEMS and a CMOS once eutectically bonded to one another.

[0081] Figure 25 shows the MEMS wafer after formation of a eutectic bond layer according to one aspect of the present embodiments. A eutectic bond layer 224, e.g., Germanium, Aluminum, etc., may be deposited over a portion of the dielectric layer 218 and the via 220 that

is filled with via filled 222. In some embodiments, the eutectic bond layer 224 is formed through a sputtering process.

[0082] Figure 26 shows the MEMS wafer after forming a photoresist layer over a eutectic bond layer according to one aspect of the present embodiments. A photoresist 223 is deposited/patterned to cover a portion of the eutectic bond layer 224 that corresponds to the standoff. In this embodiment, the photoresist 223 covers the via 220, the via filled 222, and a portion of the dielectric 218 in proximity and surrounding the via 220. The photoresist 223 layer protect the eutectic bond layer 224 that lies underneath.

[0083] Figure 27 shows the MEMS wafer after an etch process to expose the etch stop layer according to one aspect of the present embodiments. The exposed portions of the eutectic bond layer 224 and the dielectric layer 218 underneath it are etched to expose the etch stop layer 216 underneath. In some embodiments, the eutectic bond layer 224 that is covered by the photoresist 223 remains in place while the exposed dielectric layer 218 (not covered by the photoresist 223) is etched and removed.

[0084] Figure 28 shows the MEMS wafer after removal of the etch stop layer according to one aspect of the present embodiments. The etch stop layer 216 that is exposed is removed to expose the patterned hardmask 215 underneath as well as the exposed portion of the device silicon wafer 210.

[0085] Figure 29 shows the MEMS wafer after etching MEMS device pattern according to one aspect of the present embodiments. MEMS device pattern corresponding to the device silicon wafer 210 that is not covered by the patterned hardmask 215 layer is etched. In other words, the exposed portions of the device silicon wafer 210 is etched to form the MEMS device pattern.

[0086] Figure 30 shows the MEMS wafer after removing the patterned hard mask according to one aspect of the present embodiments. The exposed patterned hardmask 215 is removed after forming the MEMS device pattern. In further steps (not shown), the standoffs (where the

eutectic bond layer 224 and underlying layers reside) of the device silicon wafer 210 are eutectically bonded to a CMOS wafer with eutectic bonds. In various embodiments, the eutectic bond metal 224 (e.g. germanium) on the standoffs may form the eutectic bonds with another eutectic bond metal (e.g. aluminum) on the CMOS wafer.

[0087] Figure 31 shows a MEMS wafer at an early stage of manufacture according to one aspect of the present embodiments. In some embodiments, a fusion bond oxide 102 fusion bonds a handle silicon wafer 104 to a first side of a device silicon wafer 310 (may also be referred to as the actuator layer). A second side of the device silicon wafer 310 is planar and opposite the first side. In some embodiments, a rough polysilicon layer 312 is deposited on the second side of the device silicon wafer 310. In some embodiments, the rough polysilicon layer 312 is deposited directly on the second side of the device silicon wafer 310. It is appreciated that the rough polysilicon layer 312 is optional and it improves stiction. In other embodiments, the rough polysilicon layer 312 may be absent. It is appreciated that the rough polysilicon layer 312 may be substituted with a different material in order to improve stiction.

[0088] Figure 32 shows the MEMS wafer after hardmask deposition according to one aspect of the present embodiments. A hardmask 314 is deposited on the second side of the device silicon wafer 310. In various embodiments the hardmask 314 includes oxide and is a different material than the device silicon wafer 110. In some embodiments, the hardmask 314 is deposited directly on the rough polysilicon layer 312 that covers the second side of the device silicon wafer 310.

[0089] Figure 33 shows the MEMS wafer after patterning the hardmask according to one aspect of the present embodiments. The hardmask 314 is etched to form a patterned hardmask 315 that corresponds to MEMS device pattern. The etching of the hardmask 314 etches the full thickness of the hardmask 314, thereby exposing portions of the rough polysilicon layer 312.

[0090] Figure 34 shows the MEMS wafer after formation of a dielectric layer over the patterned hardmask according to one aspect of the present embodiments. A dielectric 318 is deposited over patterned hardmask 315 and the exposed portion of the rough polysilicon layer

312. The dielectric 318 is used to form a standoff (discussed later below). The dielectric 318 may include a material that is different from the hardmask 314, thereby eliminating the need to use an etch stop layer unlike previous embodiments. It is appreciated that the dielectric 318 may be deposited to form the standoff using plasma-enhanced chemical vapor deposition (PECVD)-oxide. In some embodiments, the dielectric 318 is optionally planarized through a chemical mechanical polishing process.

[0091] Figure 35 shows the MEMS wafer after deposition of a photoresist over the dielectric layer according to one aspect of the present embodiments. A photoresist 319 is deposited over the dielectric 318 and patterned.

[0092] Figure 36 shows the MEMS wafer after formation of a via therein according to one aspect of the present embodiments. The exposed portion of the dielectric 318 (uncovered by the photoresist 319) corresponds to the via that will be formed. As such, a via 320 is formed through the exposed portion of the dielectric 318, e.g., through lithography. In some embodiments, the via 320 extends through the patterned hardmask 315. In some embodiments, the via 320 further extends through a portion of the rough polysilicon layer 312. It is appreciated that in some embodiments, the via 320 may extend to reach a top surface of the second side of the device silicon wafer 310.

[0093] Figure 37 shows the MEMS wafer after removal of the photoresist according to one aspect of the present embodiments. After the via 320 is formed, the photoresist 319 is removed.

[0094] Figure 38 shows the MEMS wafer after filling the via according to one aspect of the present embodiments. The via 320 is filled with via fill 322, e.g., conductive material such as tungsten, copper, polysilicon, Titanium Nitride, etc., to provide electrical connection between the MEMS and a CMOS once eutectically bonded to one another.

[0095] Figure 39 shows the MEMS wafer after formation of a eutectic bond layer according to one aspect of the present embodiments. A eutectic bond layer 324, e.g., Germanium, Aluminum, etc., may be deposited over a portion of the dielectric layer 318 and the via 320 that

is filled with via filled 322. In some embodiments, the eutectic bond layer 324 is formed through a sputtering process.

[0096] Figure 40 shows the MEMS wafer after forming a photoresist layer over a eutectic bond layer according to one aspect of the present embodiments. A photoresist 323 is deposited/patterned to cover a portion of the eutectic bond layer 324 that corresponds to the standoff. In this embodiment, the photoresist 323 covers the via 320, the via filled 322, and a portion of the dielectric 318 in proximity and surrounding the via 320. The photoresist 323 layer protect the eutectic bond layer 324 that lies underneath.

[0097] Figure 41 shows the MEMS wafer after an etch process to expose the patterned hardmask according to one aspect of the present embodiments. The exposed portions of the eutectic bond layer 324 and the dielectric layer 318 underneath it are etched to expose the patterned hardmask 315 layer underneath. In some embodiments, the eutectic bond layer 324 that is covered by the photoresist 323 remains in place while the exposed dielectric layer 318 (not covered by the photoresist 323) is etched and removed.

[0098] Figure 42 shows the MEMS wafer after etching MEMS device pattern according to one aspect of the present embodiments. MEMS device pattern corresponding to the device silicon wafer 310 and/or the rough polysilicon layer 312 that is not covered by the patterned hardmask 315 layer is etched. In other words, the exposed portions of the rough polysilicon layer 312 and/or the device silicon wafer 310 is etched to form the MEMS device pattern.

[0099] Figure 43 shows the MEMS wafer after removing the patterned hard mask according to one aspect of the present embodiments. The exposed patterned hardmask 315 is removed after forming the MEMS device pattern. In further steps (not shown), the standoffs (where the eutectic bond layer 324 and underlying layers reside) of the device silicon wafer 310 are eutectically bonded to a CMOS wafer with eutectic bonds. In various embodiments, the eutectic bond metal 324 (e.g. germanium) on the standoffs may form the eutectic bonds with another eutectic bond metal (e.g. aluminum) on the CMOS wafer.

[00100] Figure 44 shows an exemplary flow diagram for actuator layer patterning with topography according to one aspect of the present embodiments. The flow diagram corresponds to Figures 1-30, as described above. At step 4402, a handle wafer is fusion bonded to a first side of a device wafer. At optional step 4404, a rough polysilicon layer is deposited directly on the second side of the device wafer. At step 4406, a hardmask is deposited on a second side of the device wafer. At step 4408, the hardmask is patterned to form an exposed portion on the second side of the device wafer. At step 4410, an etch stop layer is deposited over the hardmask and an exposed portion of the second side of the device wafer. At step 4412, a dielectric layer is formed over the etch stop layer. At step 4414, a via is formed within the dielectric layer. At step 4416, the via is filled with conductive material. At step 4418, a eutectic bond layer is formed over the conductive material. It is appreciated that in some embodiments, the eutectic bond layer is deposited over the dielectric layer and the via and is subsequently patterned and etched. At step 4420, a portion of the dielectric layer uncovered by the eutectic bond layer is etched to expose the etch stop layer. At step 4422, an exposed portions of the etch stop layer is etched/removed. At step 4424, a MEMS device pattern is etched into the device wafer. In some embodiments, the remaining exposed hardmask is removed.

[00101] Figure 45 shows another exemplary flow diagram for actuator layer patterning with topography according to one aspect of the present embodiments. The flow diagram corresponds to Figures 31-43, as described above. At step 4502, a handle wafer is fusion bonded to a first side of a device wafer. At optional step 4504, a rough polysilicon layer is deposited directly on the second side of the device wafer. At step 4506, a hardmask is deposited on a second side of the device wafer. At step 4508, the hardmask is patterned to form an exposed portion on the second side of the device wafer. At step 4510, a dielectric layer is formed over the hardmask and the exposed portion of the device wafer and/or the rough polysilicon layer. At step 4512, a via is formed within the dielectric layer. At step 4514, the via is filled with conductive material. At step 4516, a eutectic bond layer is formed over the conductive material. It is appreciated that in some embodiments, the eutectic bond layer is deposited over the dielectric layer and the via and is subsequently patterned and etched. At step 4518, a portion of the dielectric layer uncovered by the eutectic bond layer is etched to expose the hardmask layer. At step 4520, an exposed

portions of the device silicon wafer is etched to form MEMS device pattern. At step 4522, an exposed portions of the hardmask is etched/removed.

[00102] While the embodiments have been described and/or illustrated by means of particular examples, and while these embodiments and/or examples have been described in considerable detail, it is not the intention of the Applicants to restrict or in any way limit the scope of the embodiments to such detail. Additional adaptations and/or modifications of the embodiments may readily appear, and, in its broader aspects, the embodiments may encompass these adaptations and/or modifications. Accordingly, departures may be made from the foregoing embodiments and/or examples without departing from the scope of the concepts described herein. The implementations described above and other implementations are within the scope of the following claims.

CLAIMS

What is claimed is:

1. A method comprising:
fusion bonding a handle wafer to a first side of a device wafer;
depositing a hardmask on a second side of the device wafer, wherein the second side is planar;
depositing an etch stop layer over the hardmask and an exposed portion of the second side of the device wafer;
forming a dielectric layer over the etch stop layer;
forming a via within the dielectric layer;
filling the via with conductive material;
forming a eutectic bond layer over the conductive material;
etching portions of the dielectric layer uncovered by the eutectic bond layer to expose the etch stop layer;
etching exposed portions of the etch stop layer; and
etching a micro-electro-mechanical system (MEMS) device pattern into the device wafer.
2. The method of Claim 1, further comprising depositing a rough poly-silicon layer directly on the second side of the device wafer, and wherein the hardmask is deposited directly on the rough poly-silicon layer.
3. The method of Claim 2, wherein the via extends into the rough poly-silicon layer.
4. The method of Claim 1 further comprising patterning the hardmask to form a patterned hardmask layer that forms the exposed portion of the second side of the device wafer.
5. The method of Claim 4, wherein the MEMS pattern corresponds to patterned hardmask layer.

6. The method of Claim 1, wherein the etch stop layer comprises nitride, oxy-nitride, or poly-silicon.

7. The method of Claim 1, wherein the eutectic bond layer comprises Ge.

8. The method of Claim 1, wherein the conductive material comprises tungsten, copper, poly-silicon, or Titanium Nitride.

9. The method of Claim 1 further comprising etching exposed portions of the hardmask after the etching of MEMS device pattern.

10. A method comprising:
fusion bonding a handle wafer to a first side of a device wafer;
depositing a hardmask on a second side of the device wafer, wherein the second side is planar;
forming a dielectric layer over the hardmask and an exposed portion of the second side of the device wafer;
forming a via within the dielectric layer;
filling the via with conductive material;
forming a eutectic bond layer over the conductive material;
etching portions of the dielectric layer uncovered by the eutectic bond layer to expose the hardmask; and
etching a micro-electro-mechanical system (MEMS) device pattern into the device wafer.

11. The method of Claim 10, further comprising depositing a rough poly-silicon layer directly on the second side of the device wafer, and wherein the hardmask is deposited directly on the rough poly-silicon layer.

12. The method of Claim 11, wherein the via extends into the rough poly-silicon layer.

13. The method of Claim 10 further comprising patterning the hardmask to form a patterned hardmask layer that forms the exposed portion of the second side of the device wafer.

14. The method of Claim 10, wherein the eutectic bond layer comprises Ge.

15. The method of Claim 10, wherein the conductive material comprises tungsten, copper, poly-silicon, or Titanium Nitride.

16. The method of Claim 10 further comprising etching exposed portions of the hardmask after the etching of MEMS device pattern.

17. A device comprising:
a handle wafer; and
a device wafer having a first side that is opposite to a second side, wherein the first side of the device wafer is fusion bonded to the handle wafer,
wherein the second side of the device wafer has a first portion and a second portion, wherein the second portion comprises a dielectric layer including a via formed therein, and wherein the via is filled with conductive material, and wherein the second portion of the second side of the device wafer further includes a eutectic bond layer formed on the dielectric layer and further on the via and the conductive material.

18. The device of Claim 17 further comprising a rough poly-silicon layer disposed directly on the second side of the device wafer.

19. The device of Claim 17, wherein the second portion further includes a hardmask layer disposed on the second side of the device wafer, and wherein the hardmask is disposed between the dielectric layer and the second side of the device wafer.

20. The device of Claim 19, wherein the via extends into the hardmask.

21. The device of Claim 17, wherein the second portion further includes an etch stop layer disposed on the second side of the device wafer, and wherein the etch stop layer is disposed between the dielectric layer and the second side of the device wafer.

22. The device of Claim 21, wherein the via extends into the etch stop layer.

23. The device of Claim 17, wherein the via extends into the second side of the device wafer.

24. The device of Claim 17, wherein the first portion includes a micro-electro-mechanical system (MEMS) device pattern formed therein.

25. The device of Claim 17 further comprising a complementary metal-oxide semiconductor (CMOS) eutectically bonded to the eutectic bond layer of the device wafer.

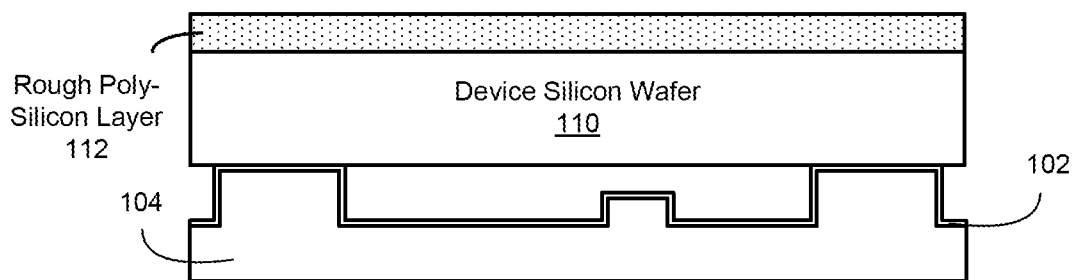


Figure 1

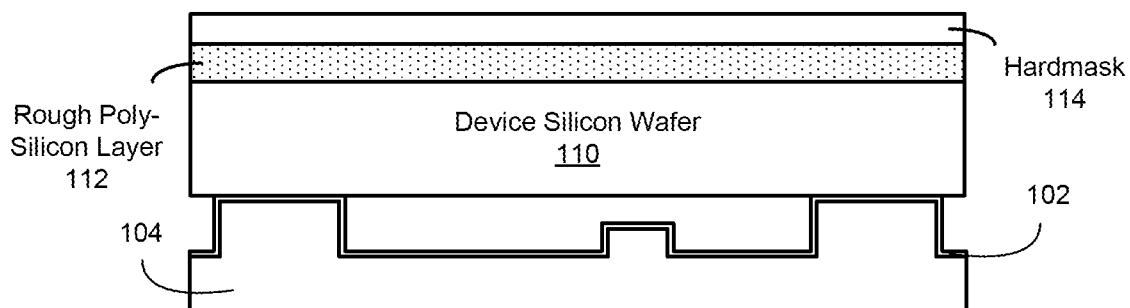


Figure 2

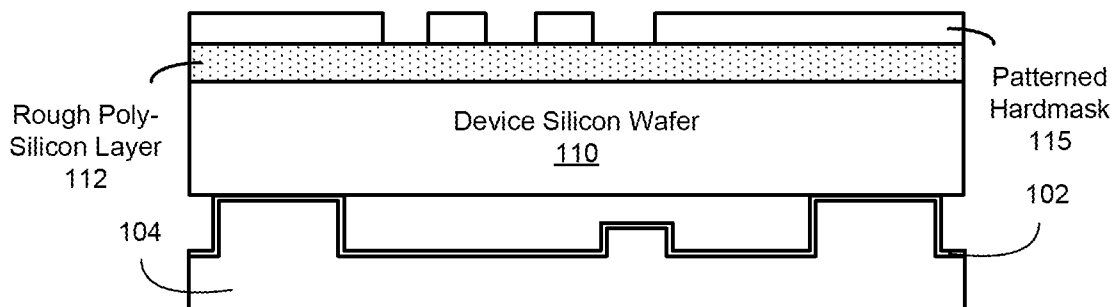


Figure 3

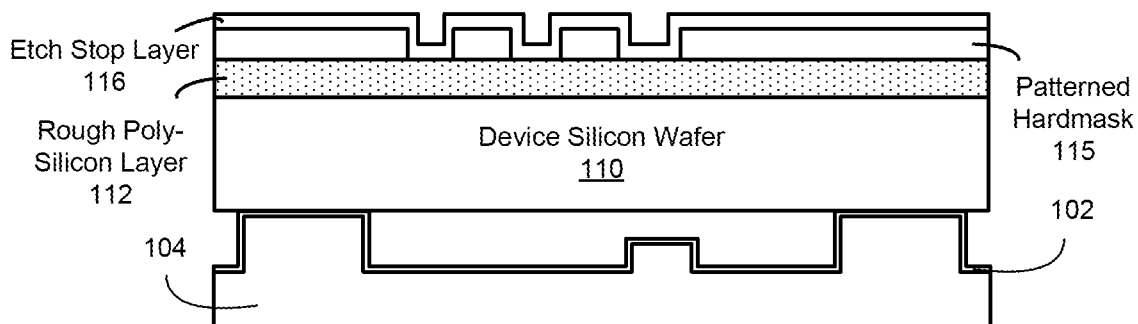


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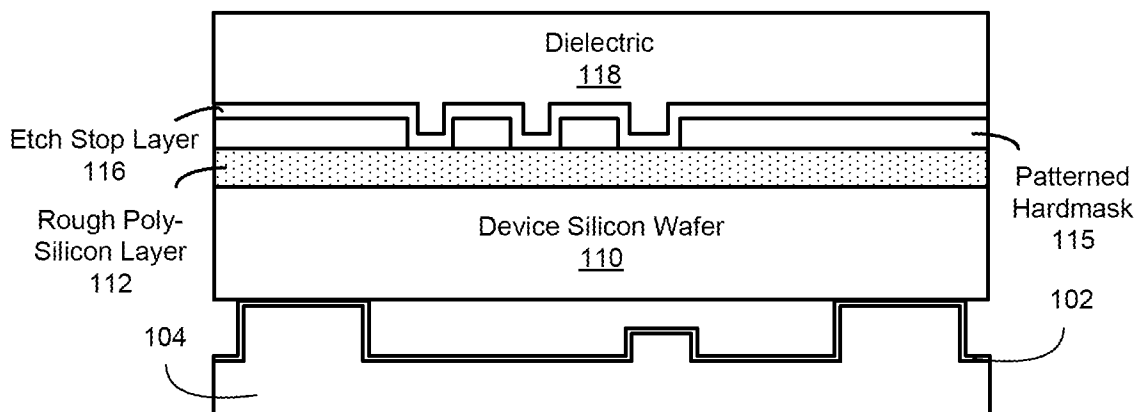


Figure 5

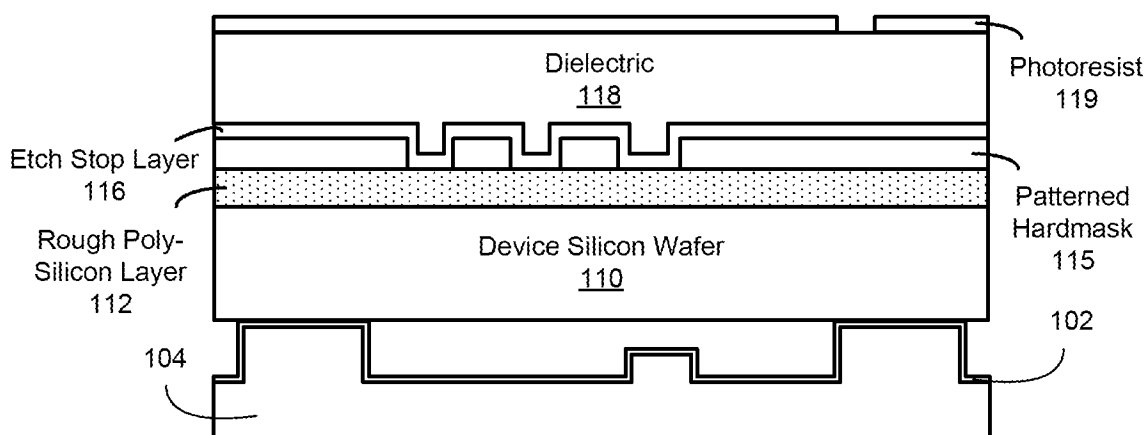


Figure 6

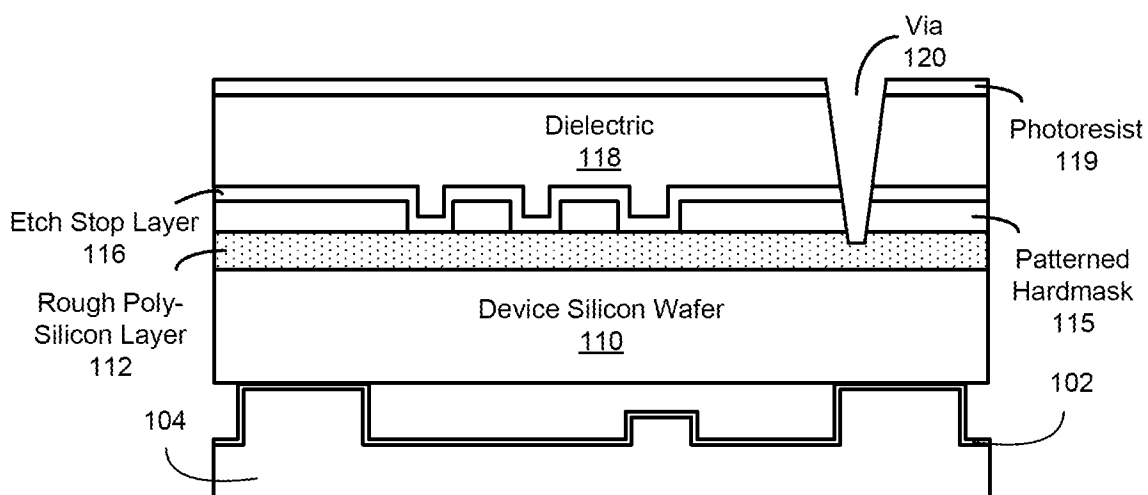


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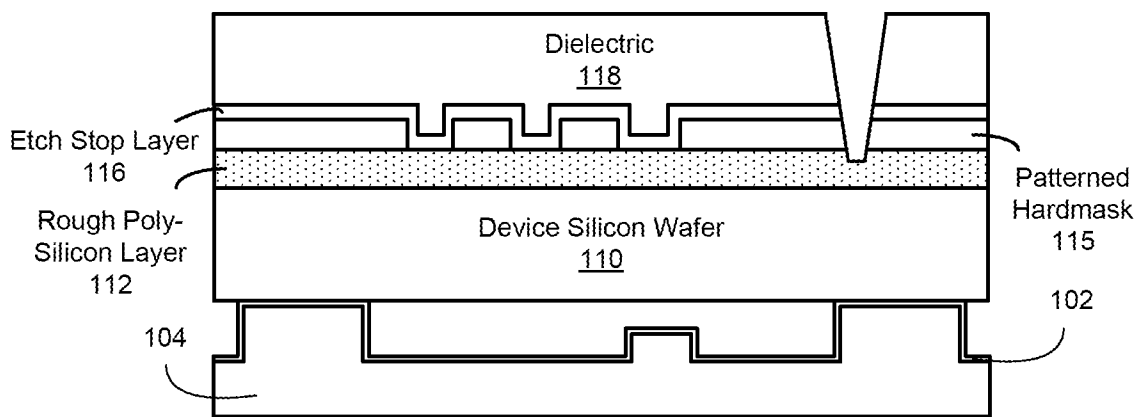


Figure 8

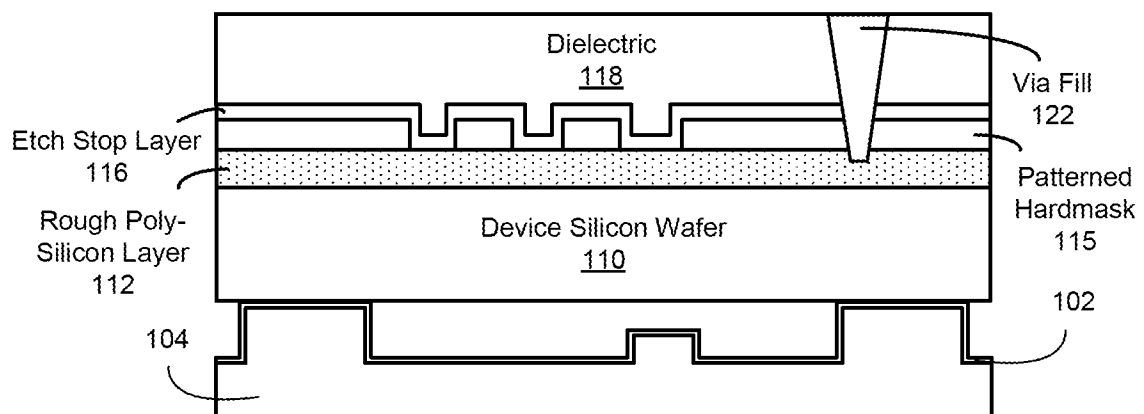


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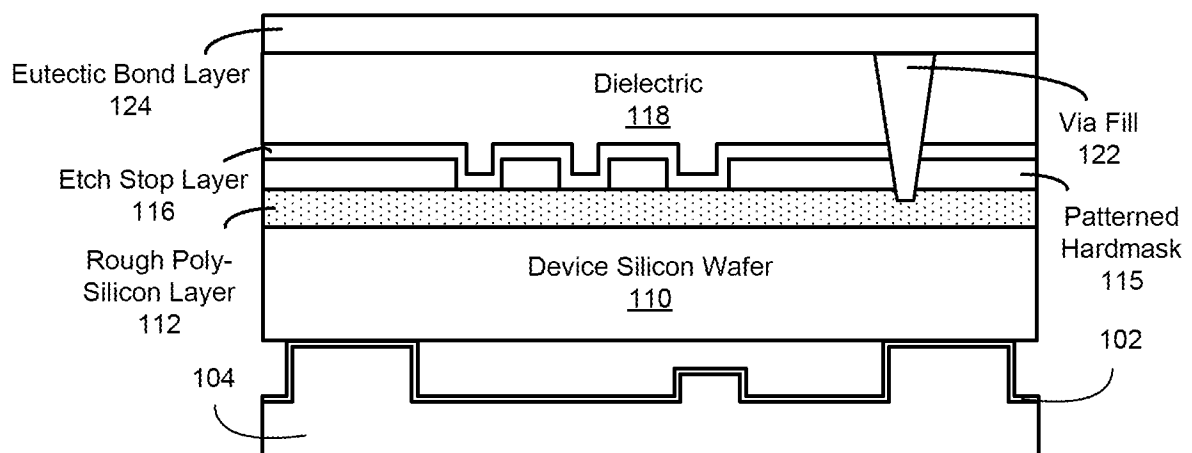


Figure 10

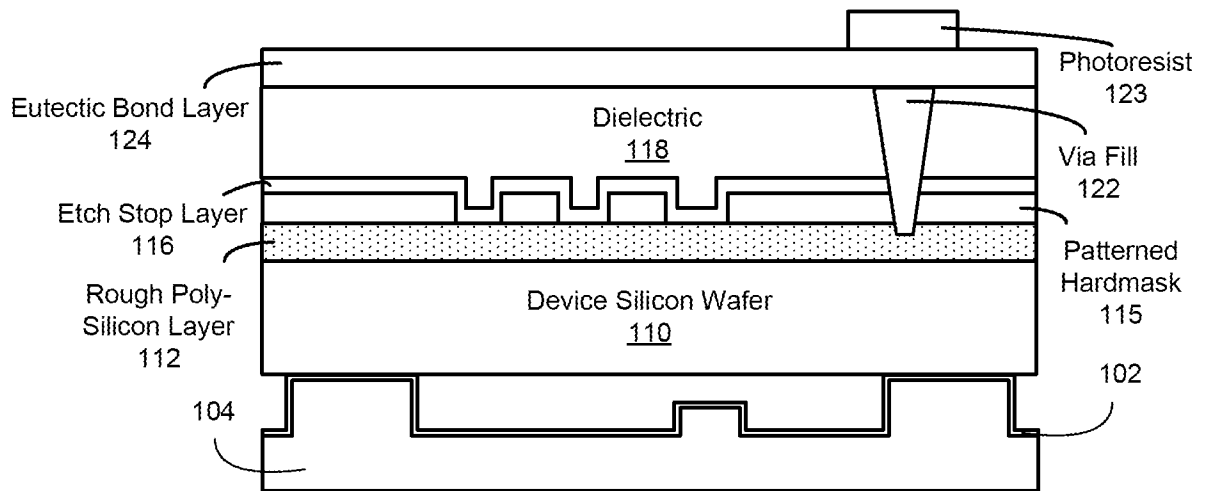


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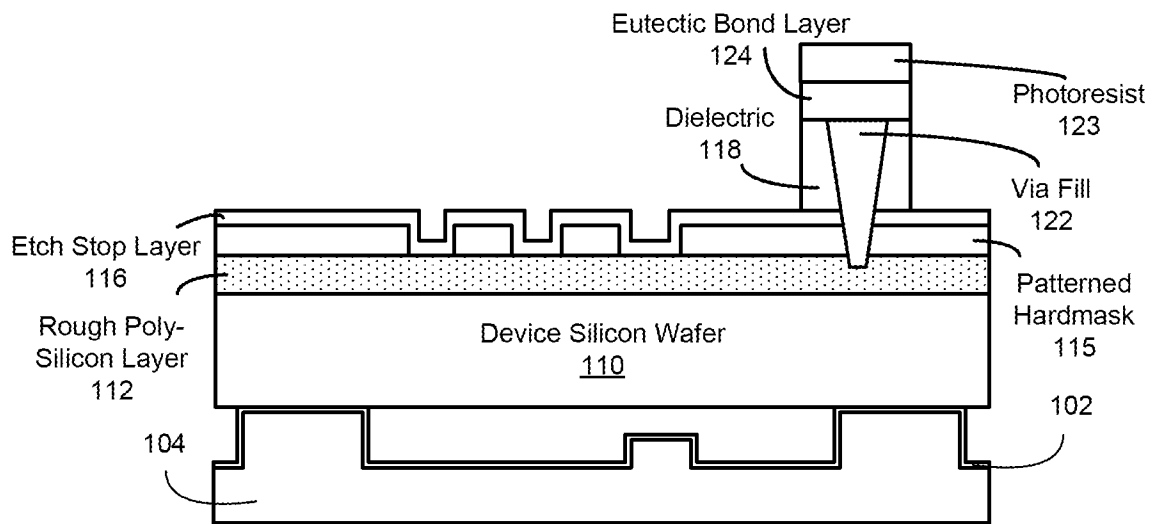


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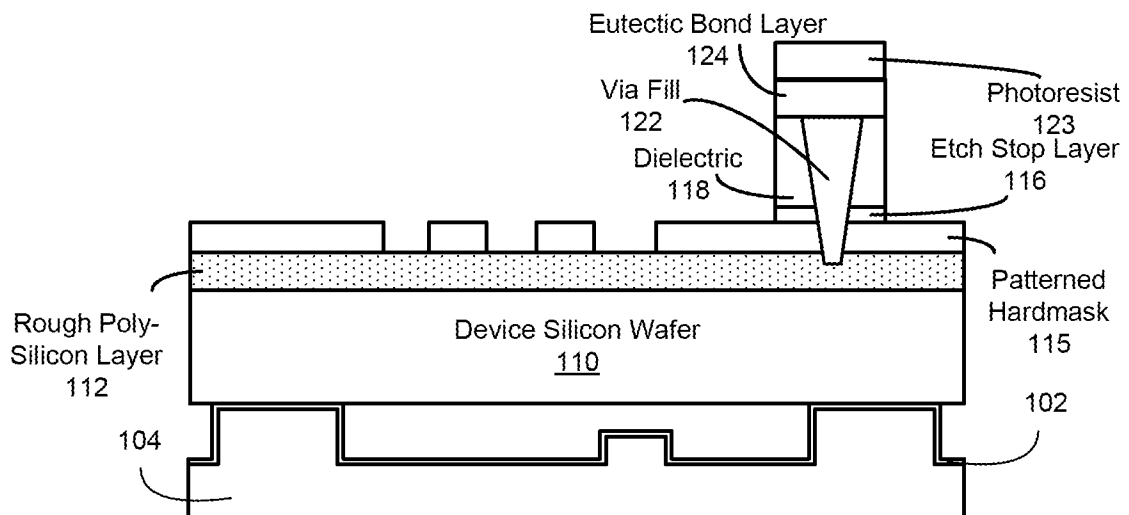


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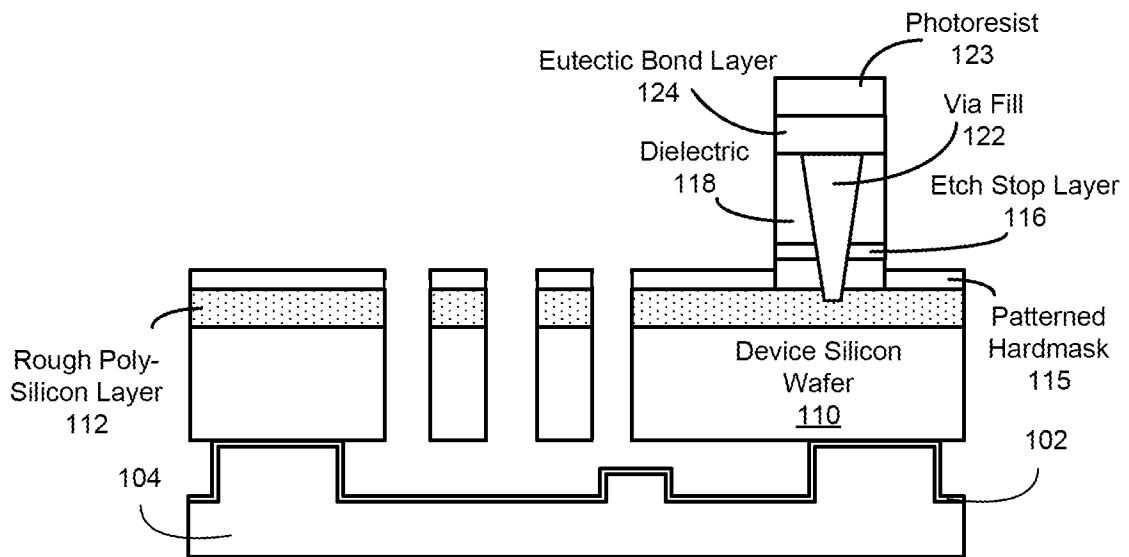


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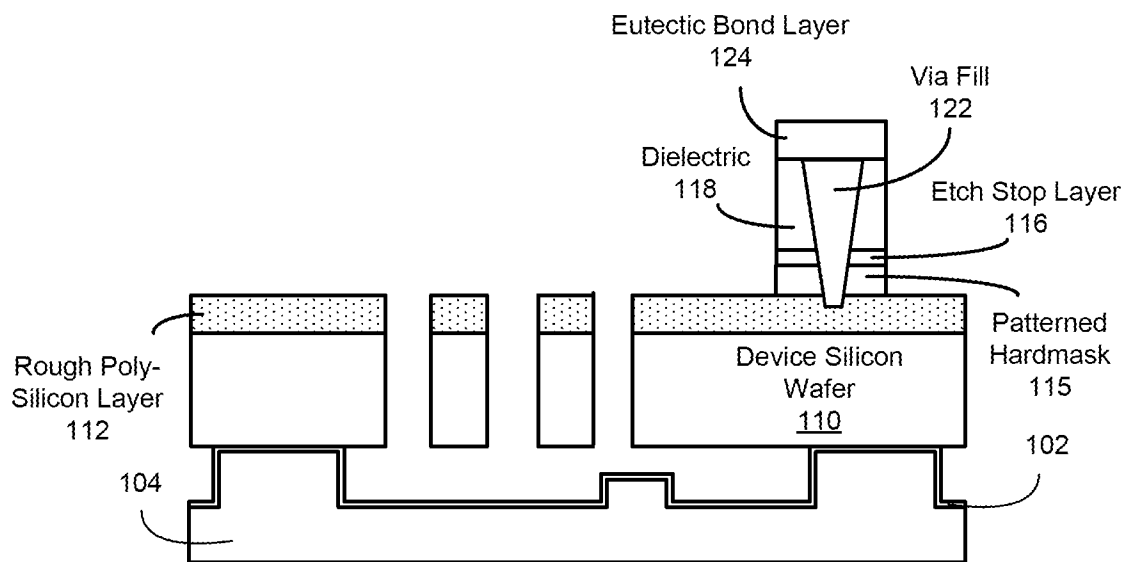


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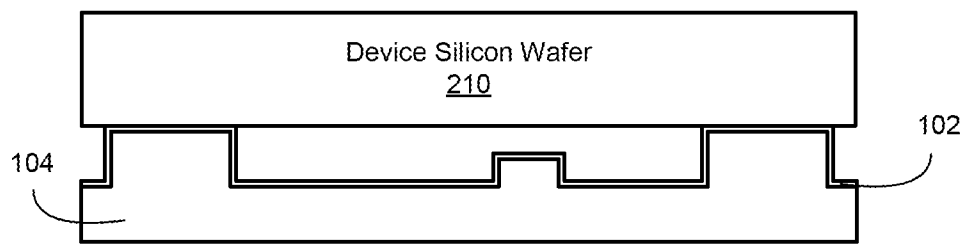


Figure 16

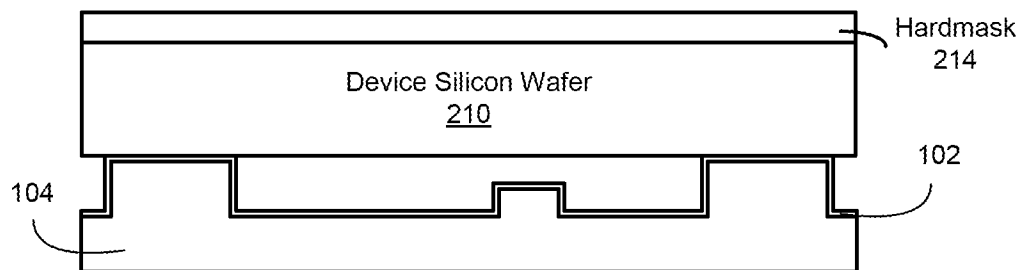


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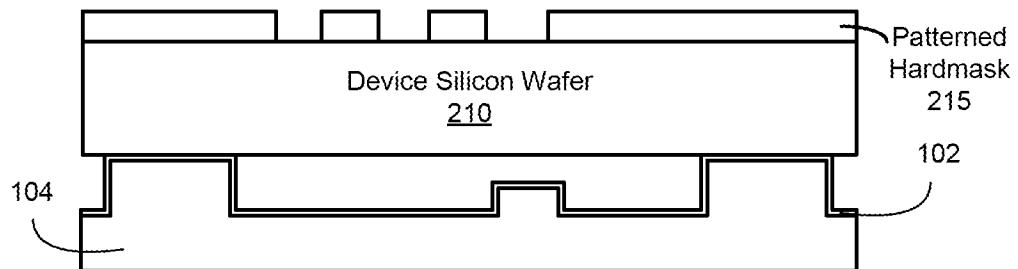


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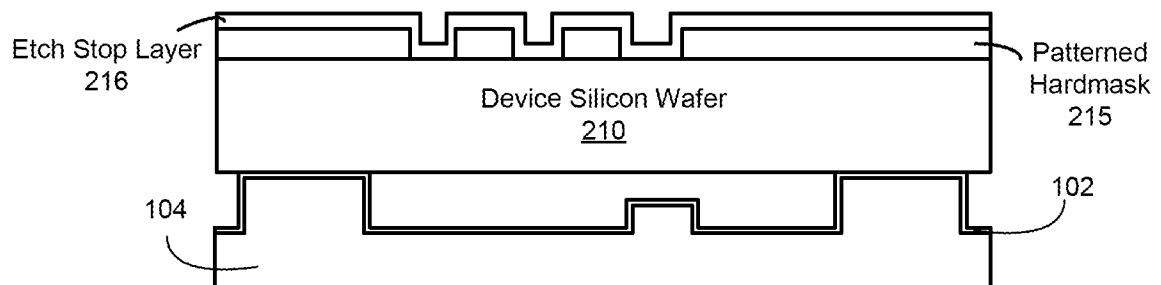


Figure 19

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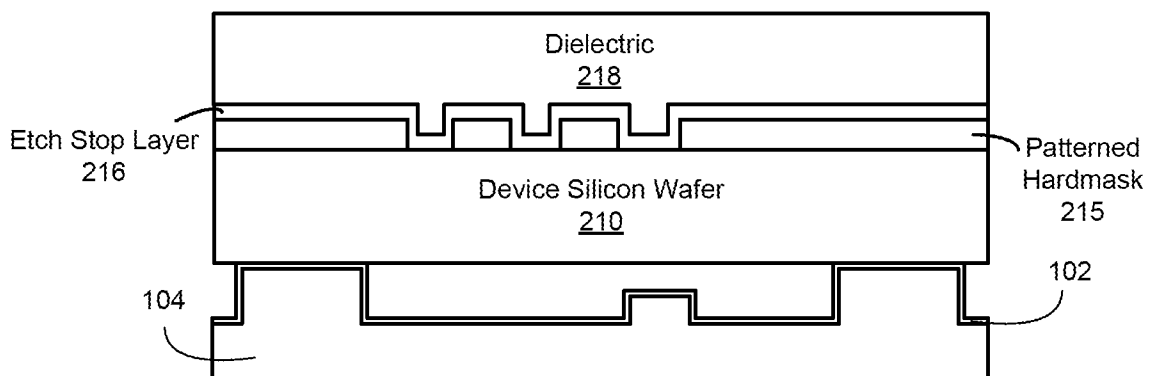


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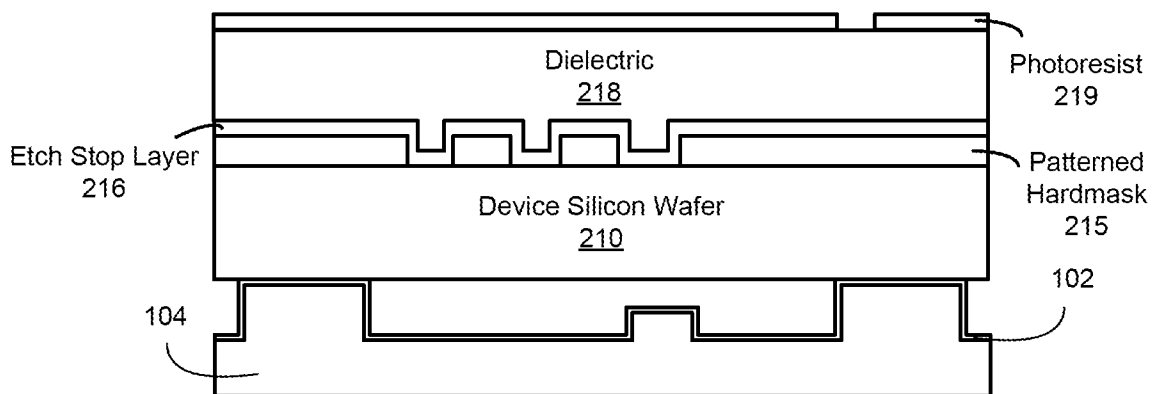


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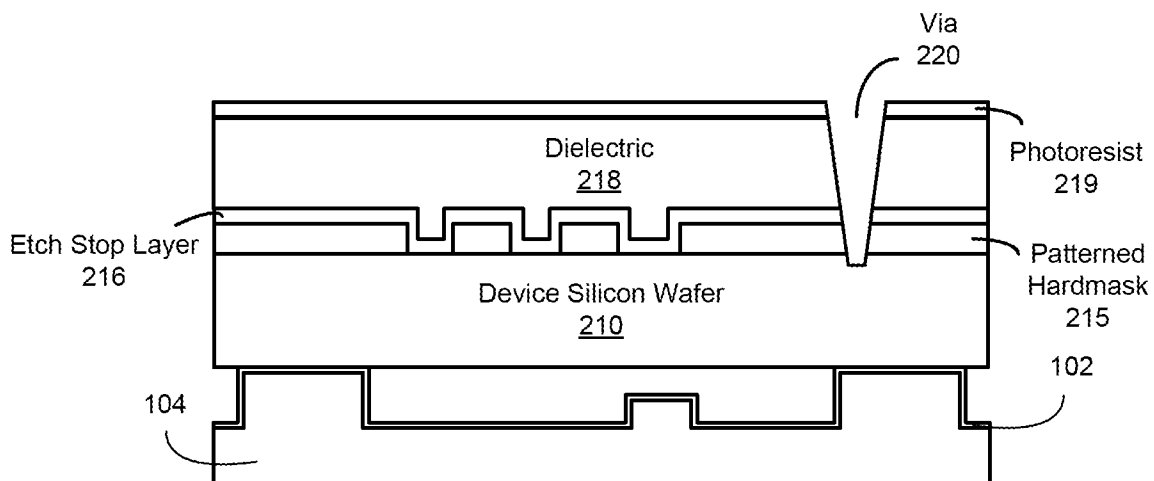


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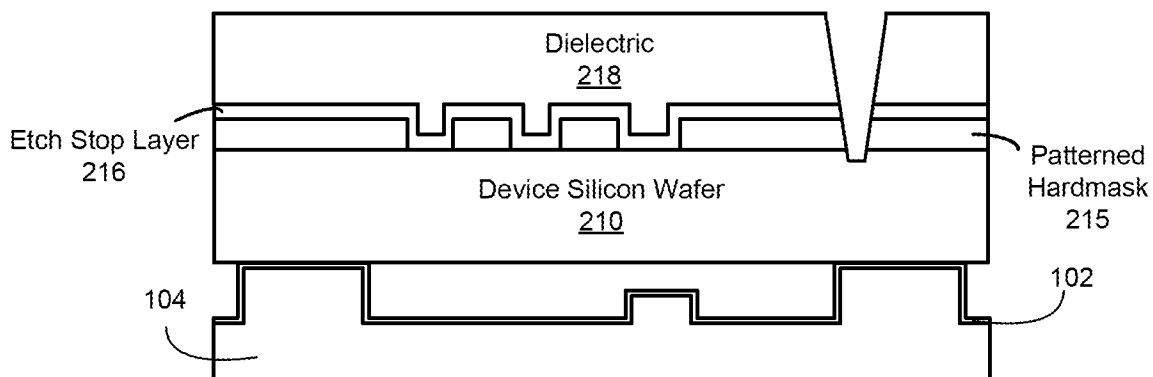


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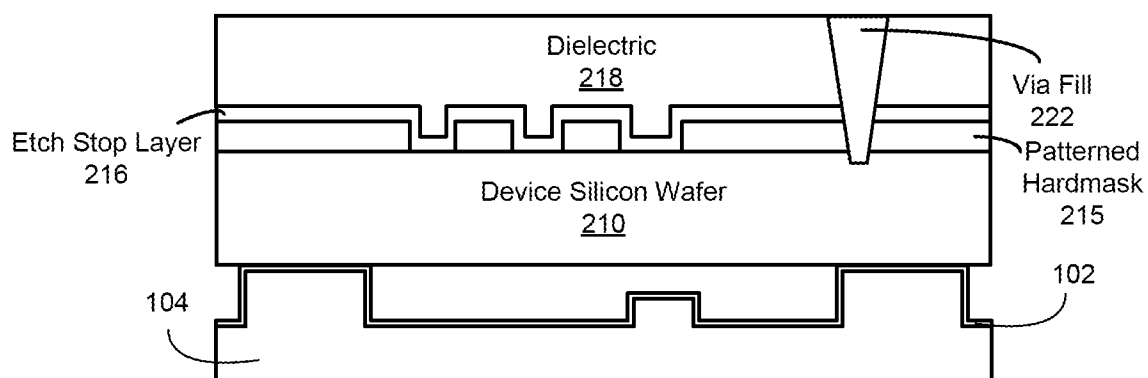


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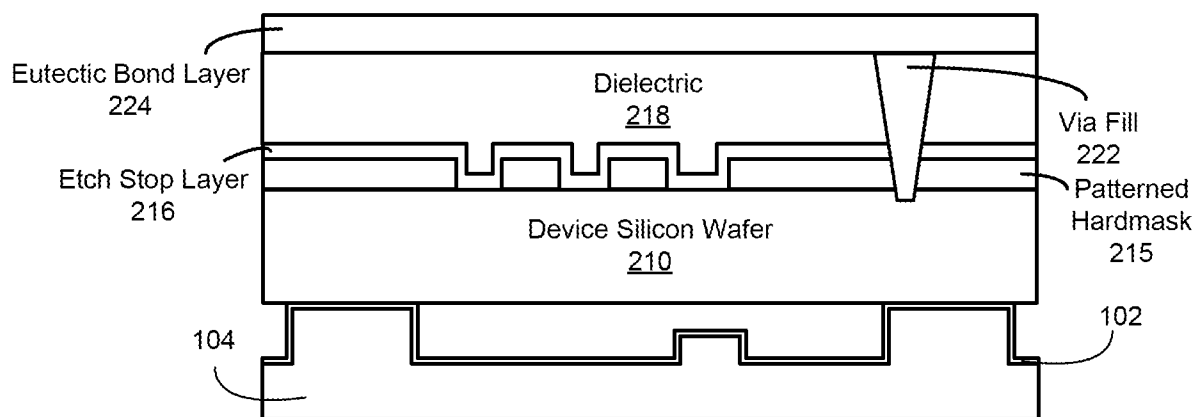


Figure 25

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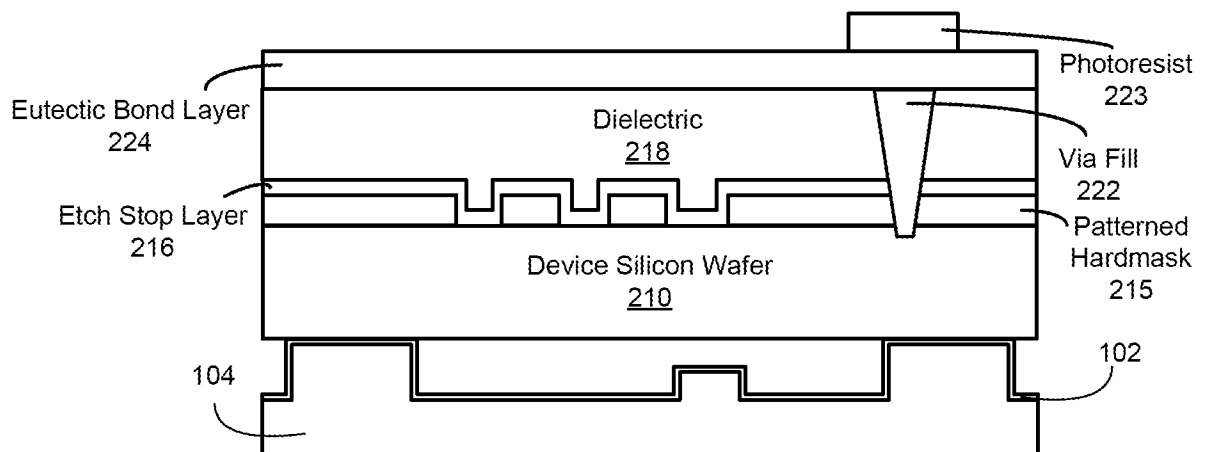


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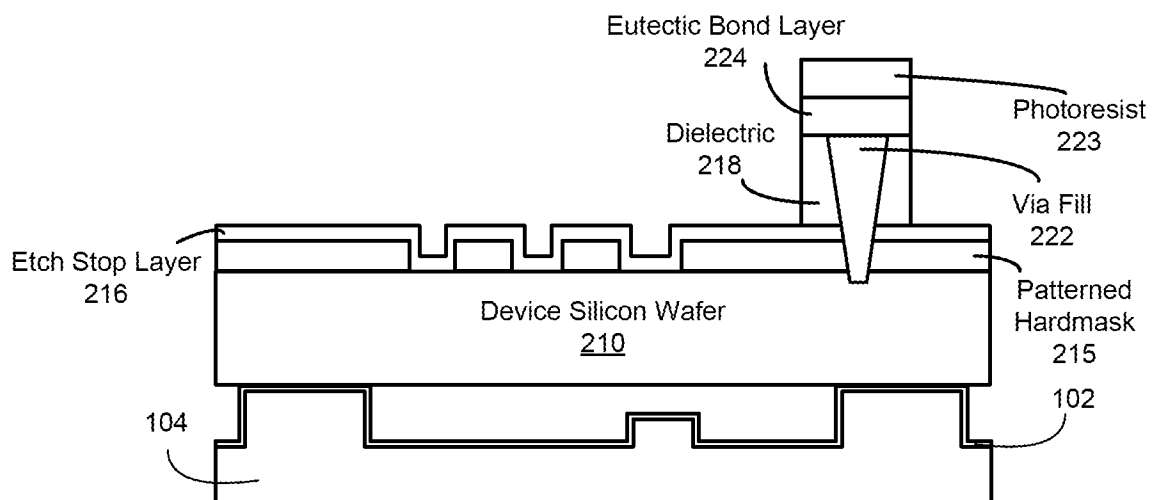


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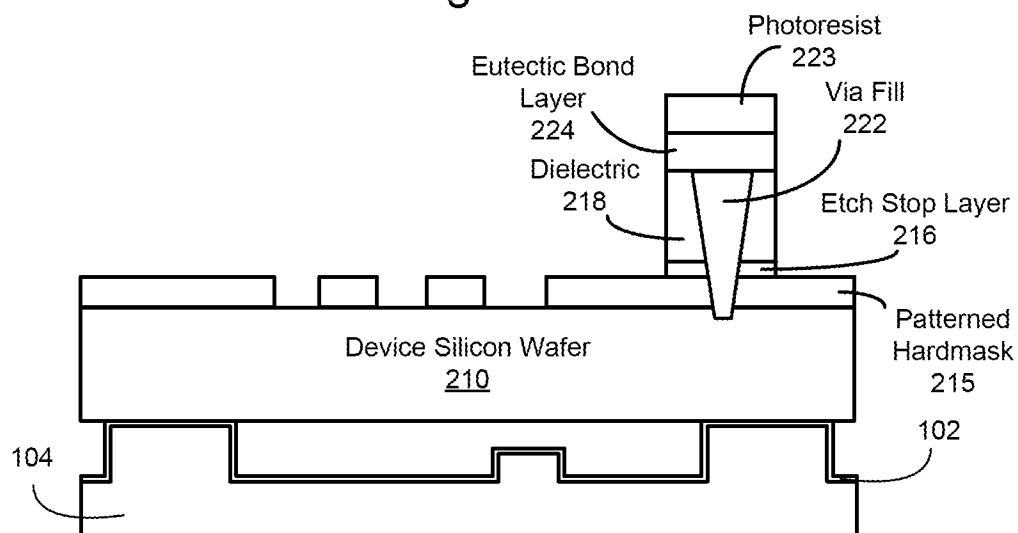


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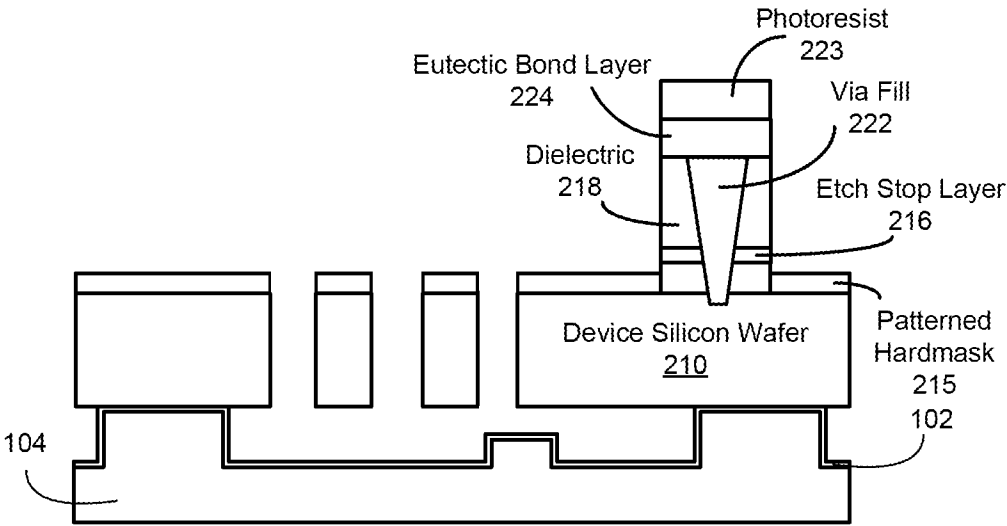


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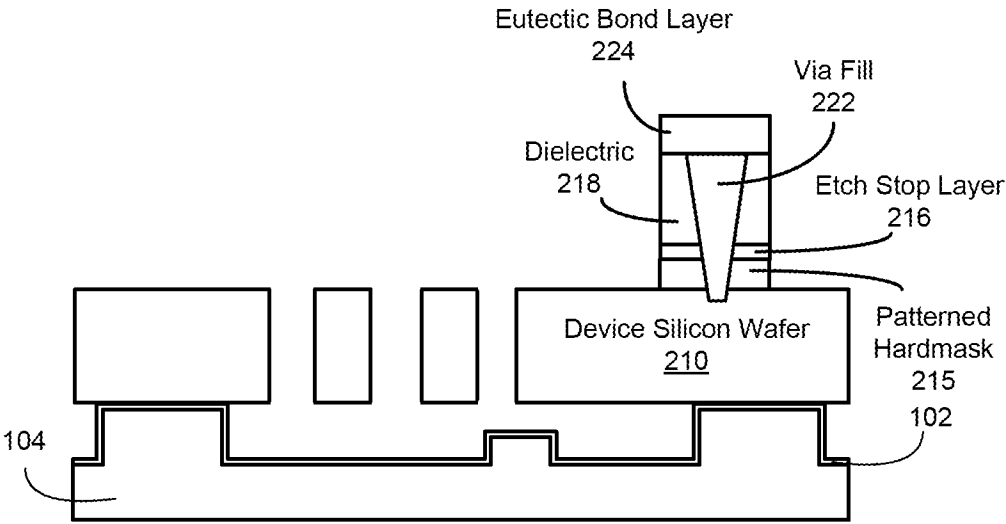


Figure 30

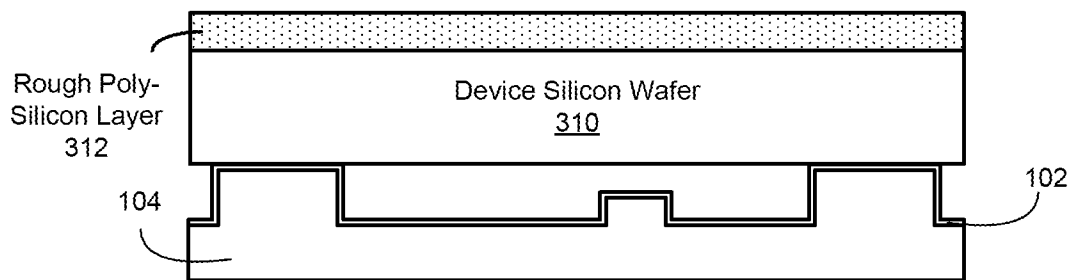


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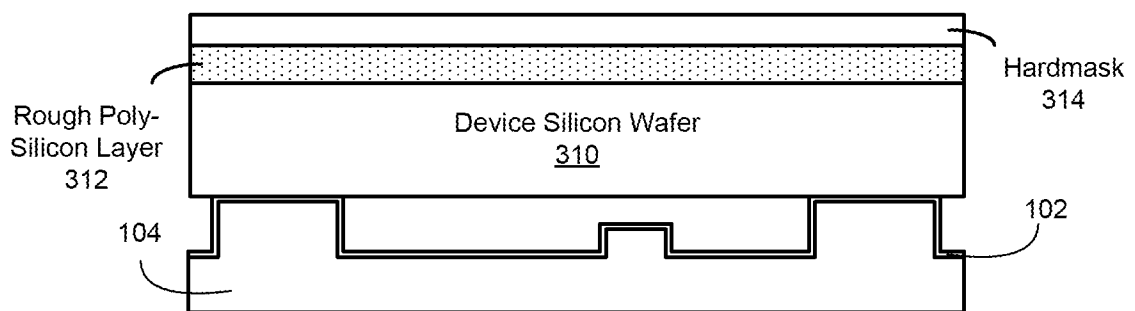


Figure 32

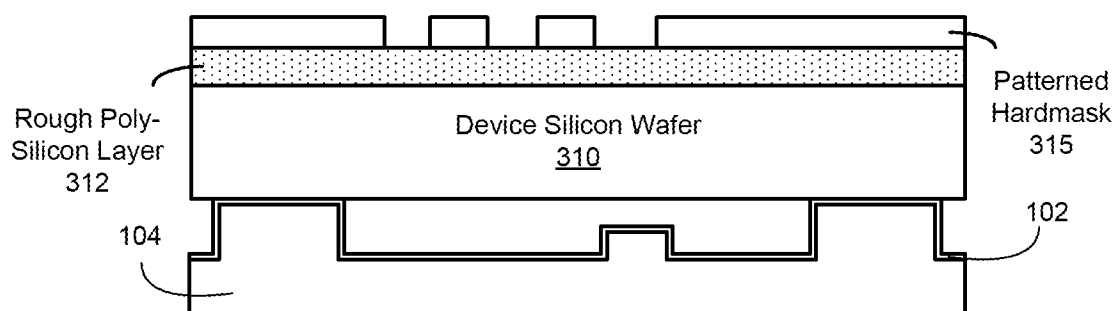


Figure 33

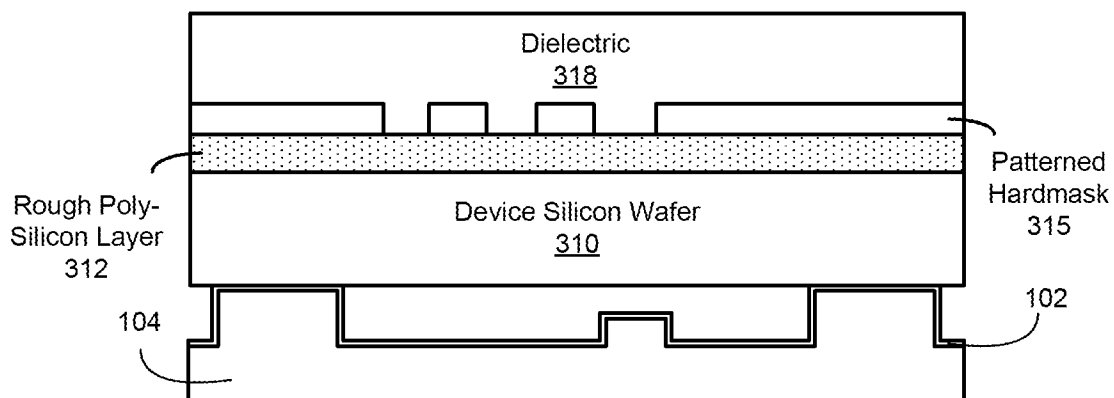


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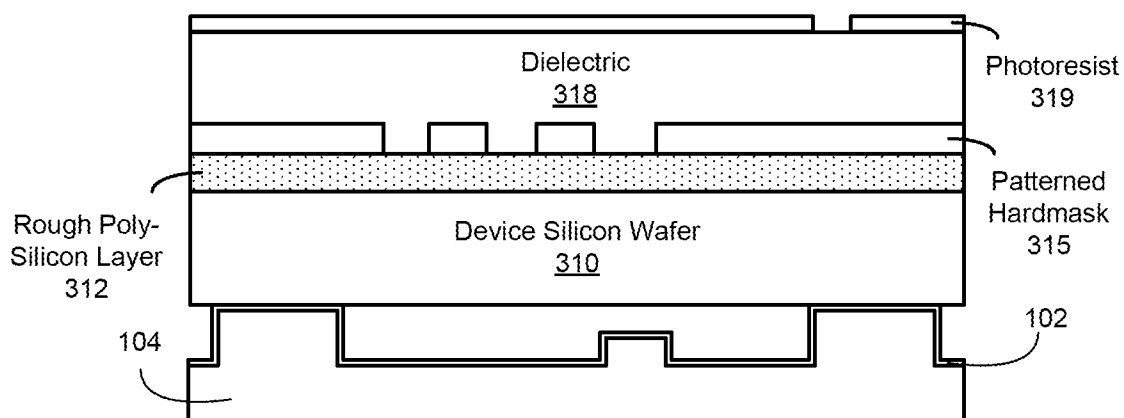


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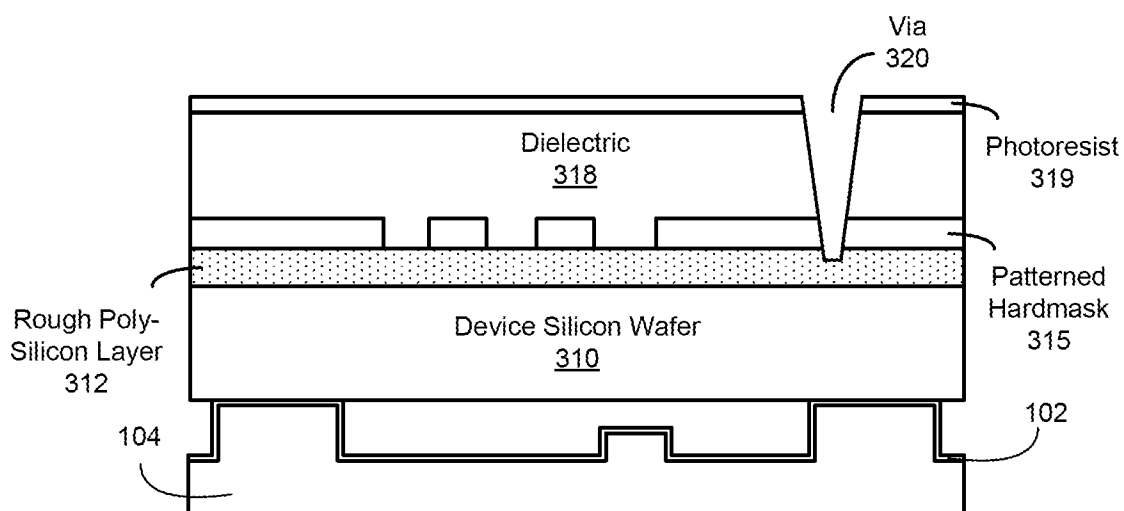


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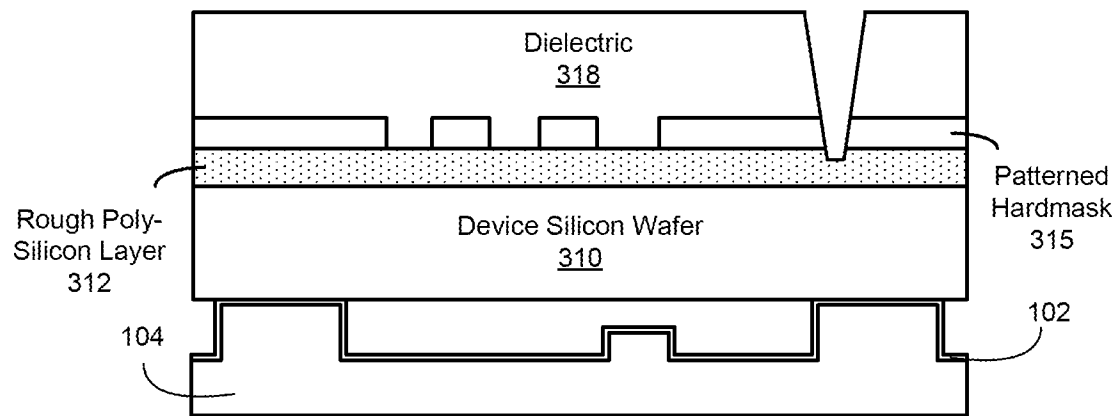


Figure 37

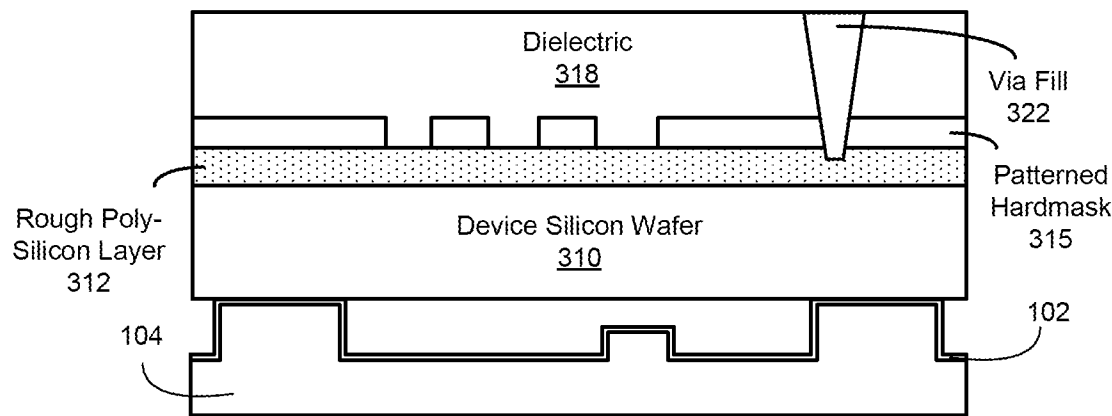


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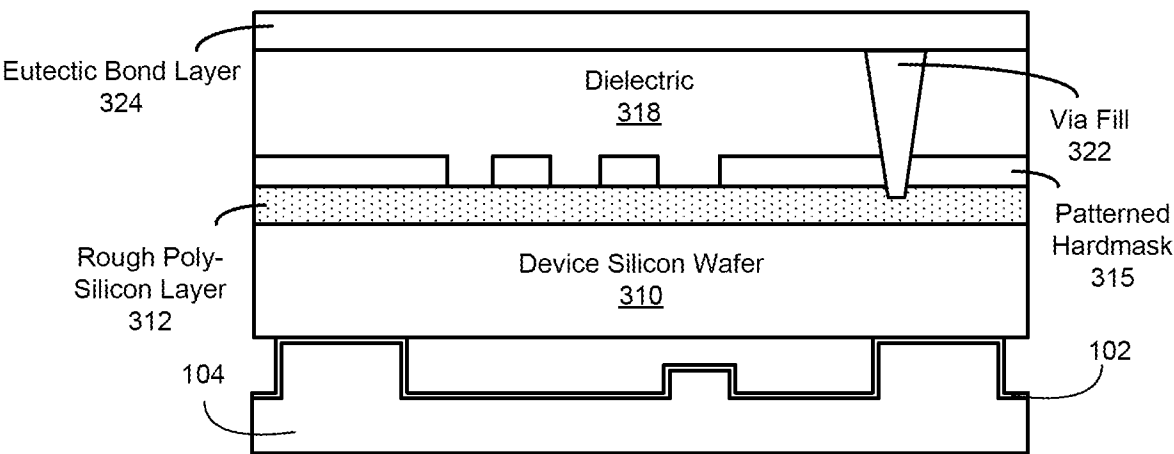


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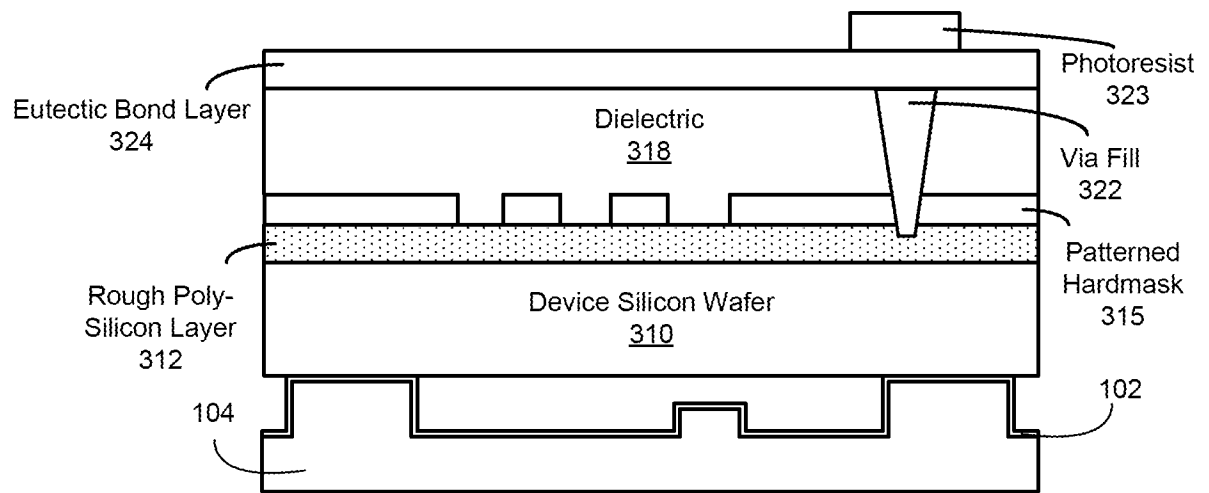


Figure 40

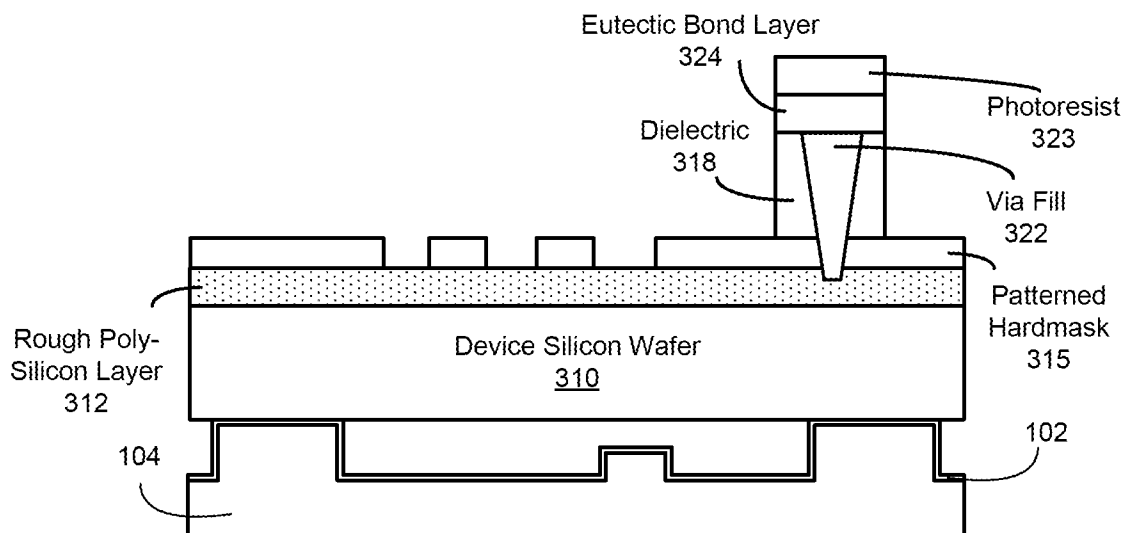


Figure 41

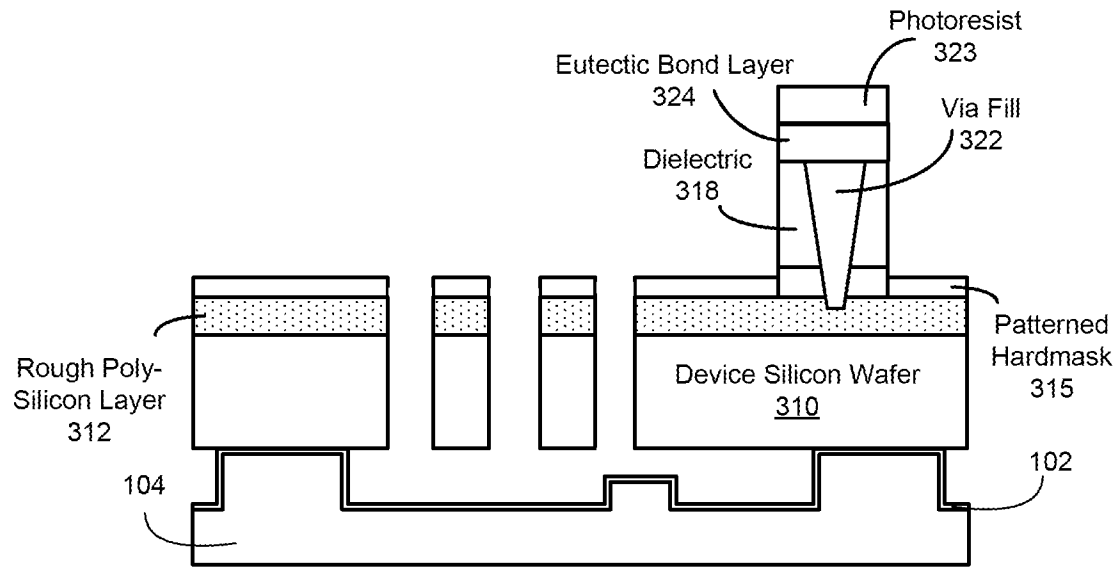


Figure 42

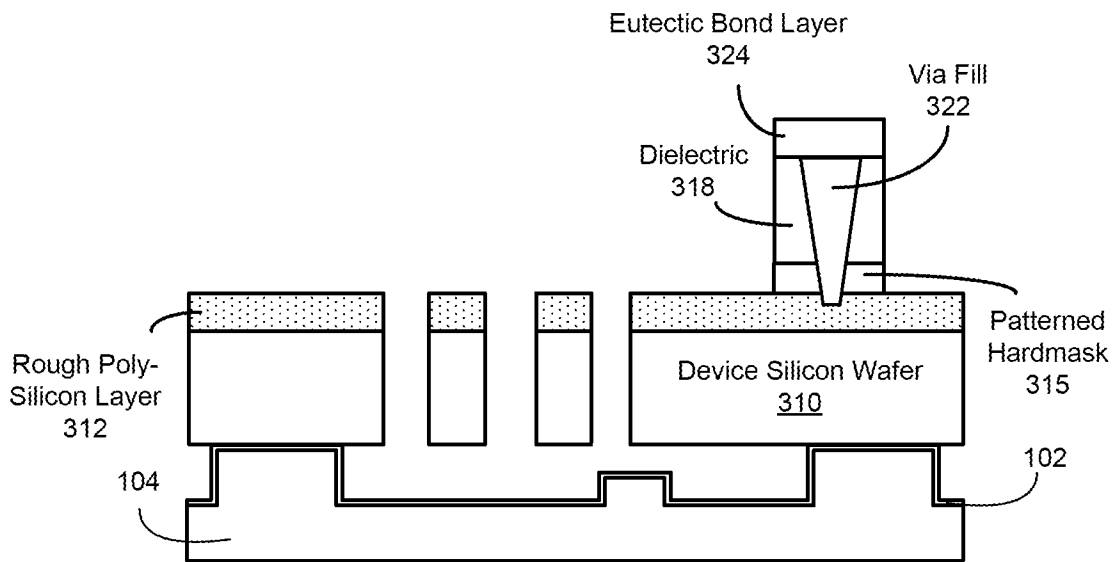


Figure 43

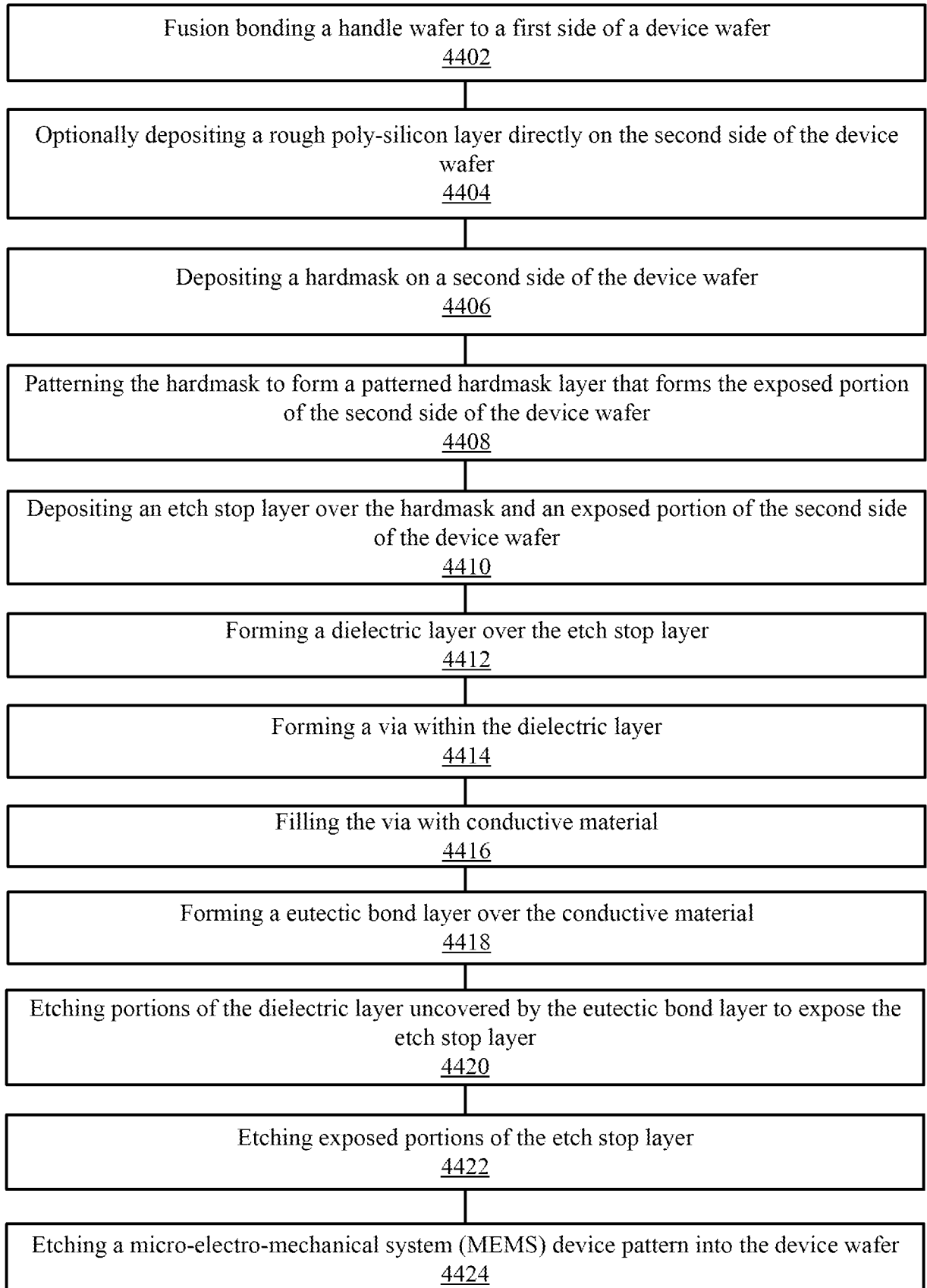


Figure 44

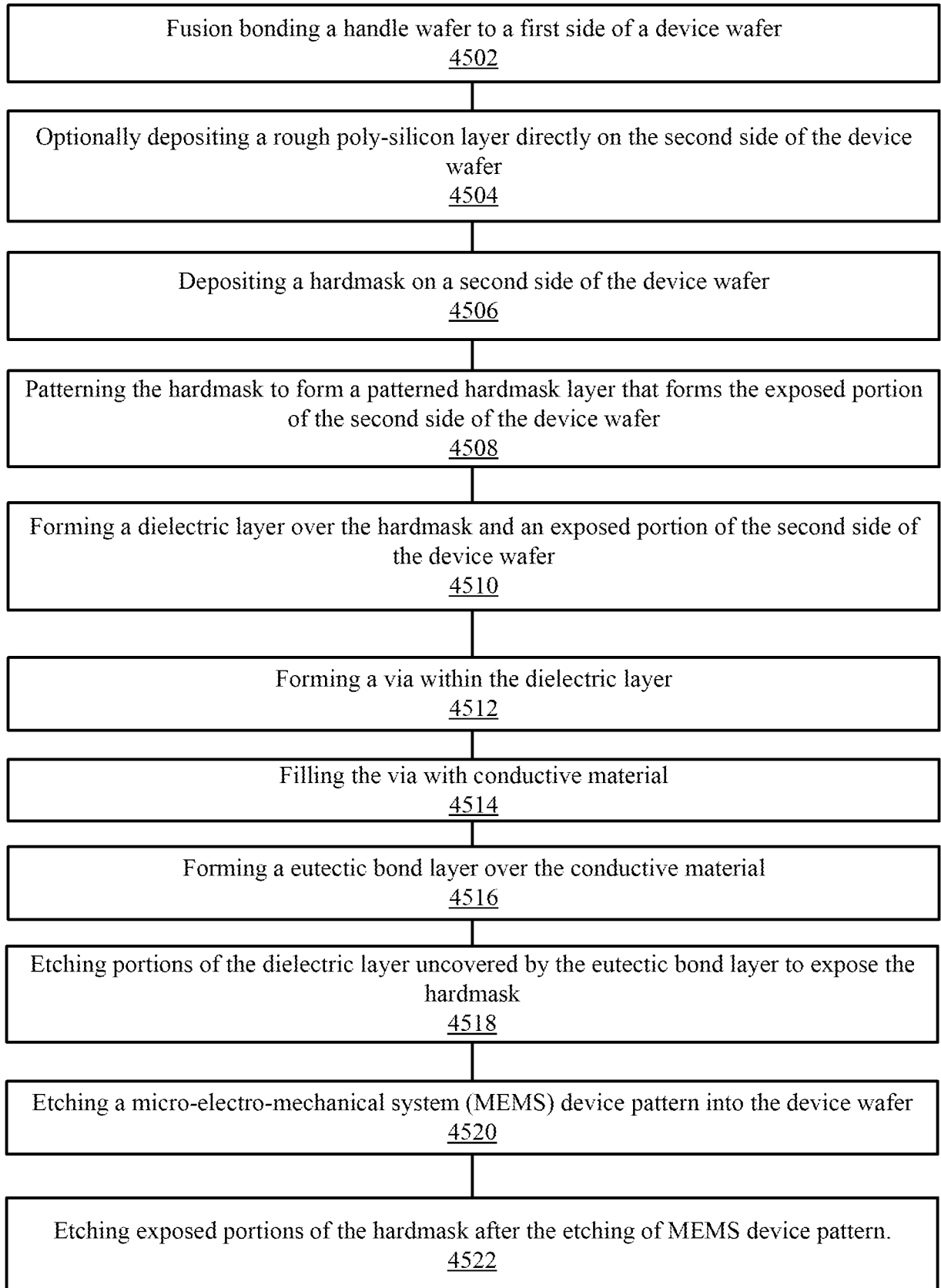


Figure 45

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2021/045428

A. CLASSIFICATION OF SUBJECT MATTER
INV. B81B7/00 B81C1/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
B81B B81C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014/206123 A1 (CHU CHIA-HUA [TW] ET AL) 24 July 2014 (2014-07-24) figures 1-15 -----	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 October 2021

Date of mailing of the international search report

05/11/2021

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

McGinley, Colm

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2021/045428

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014206123 A1	24-07-2014	CN 103964376 A	06-08-2014
		TW 201430974 A	01-08-2014
		US 2014206123 A1	24-07-2014
		US 2015217996 A1	06-08-2015
