United States Patent

Hilsum et al.

[15] **3,667,003**

[45] **May 30, 1972**

[54] THREE VALLEY TRANSFERRED ELECTRON OSCILLATOR

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[22] Filed: **Apr. 21, 1971**

[21] Appl. No.: **136,152**

[30] **Foreign Application Priority Data**

Apr. 22, 1970 Great Britain 19,350/70

[52] **U.S. Cl.** ..... **317/234 R**, 252/62.3 GA, 317/234 N, 317/234 V, 317/235 AP, 331/107 G

[51] **Int. Cl.** **H01l 3/20**, H01l 5/00

[58] **Field of Search** ..... 317/234 V, 235 AP; 252/62.3 GA; 331/107 G

[56] **References Cited**

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Hilsum, " Transferred Electron Amplifiers...," Proc. IRE, Feb. 1962, pp. 185– 189.

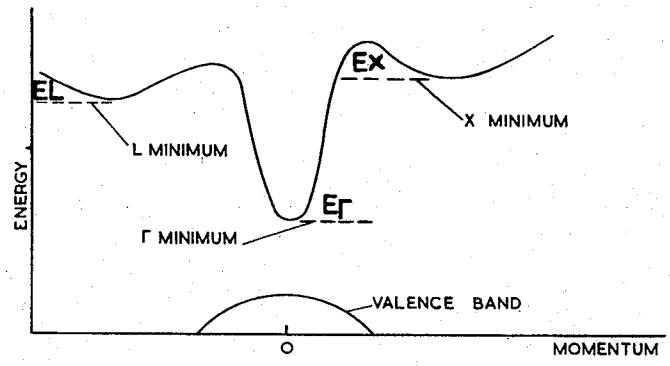
Gunn, " Microwave Oscillations of Current in III– V Semiconductors," Solid State Communications, Vol. 1, pp. 88– 91, (1963).

Primary Examiner—John W. Huckert
Assistant Examiner—William D. Larkins
Attorney—Cushman, Darby & Cushman

[57] **ABSTRACT**

A semiconductor device includes a piece of semiconductor material exhibiting transferred electron effects between three sets of conduction band valleys, which sets consist of a set of lowest energy, a set of highest energy and a set of intermediate energy, and in which the set of lowest energy has an energy density of states smaller than that of either of the other two sets and in which the rate at which electrons are scattered between the set of lowest energy and the set of intermediate energy is less than both the rate at which electrons are scattered between the set of lowest energy and the set of highest energy and the rate at which electrons are scattered between the set of intermediate energy and the set of highest energy, and means for applying voltages across the piece of semiconductor material, whereby electron transfer occurs between the different sets of valleys. Also included in the device are means for controlling the current flowing such that it is free of dipole domains. The semiconductor material may be either InP_xAs_{1-x} ($1 \geq x \geq 0.75$) or $In_6Ga_{1-y}Sb$ ($0.05 \leq y \leq 0.30$).

8 Claims, 16 Drawing Figures



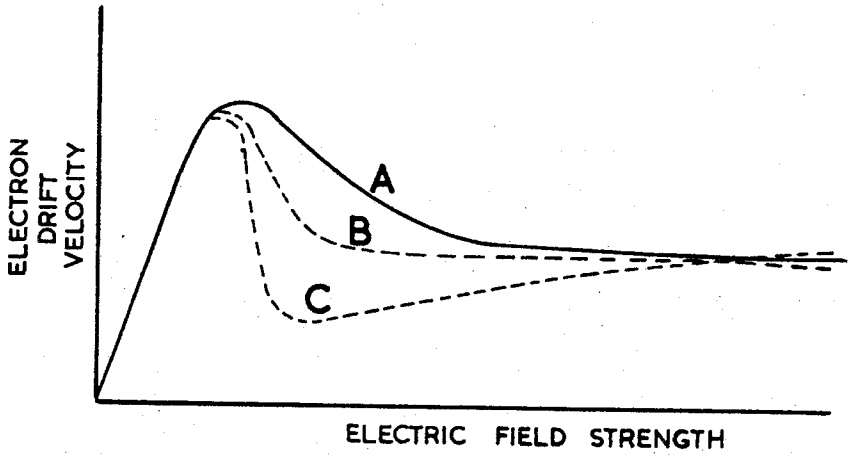

ELECTRON DRIFT VELOCITY
A
B
C
ELECTRIC FIELD STRENGTH

FIG. 1.

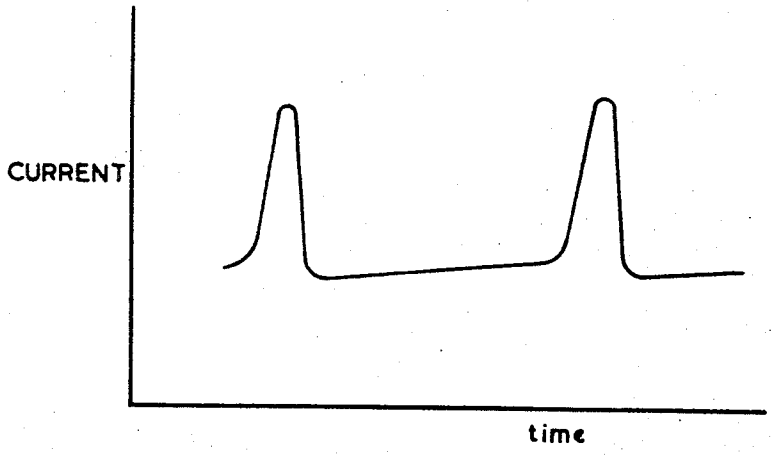

CURRENT
time

FIG. 8.

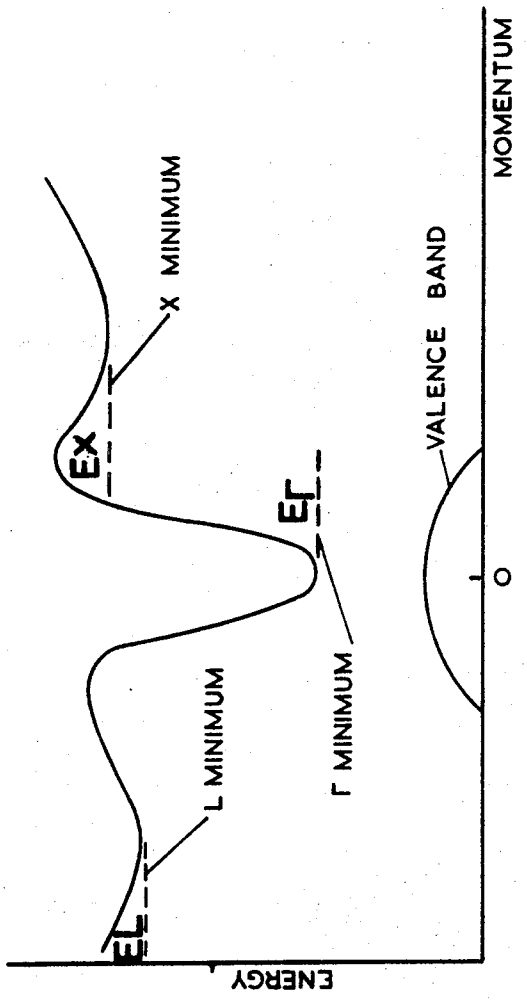

MOMENTUM
VALENCE BAND
X MINIMUM
Γ MINIMUM
L MINIMUM
Ex
Eγ
EL
ENERGY
0

FIG. 2.

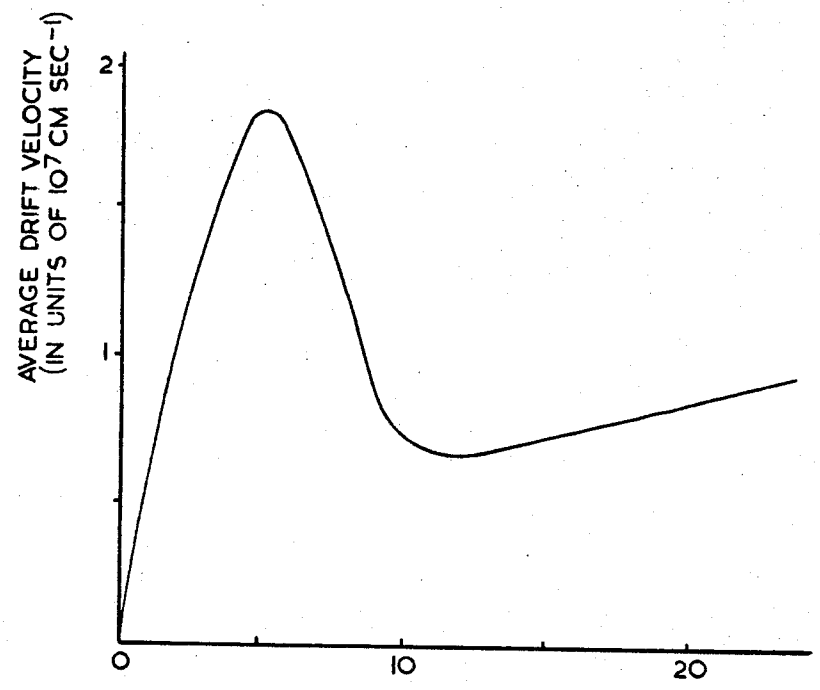

AVERAGE DRIFT VELOCITY
(IN UNITS OF 10^7 CM SEC^{-1})
2
1
0
10
20
FIELD STRENGTH
(K.V. CM^{-1})

FIG. 3.

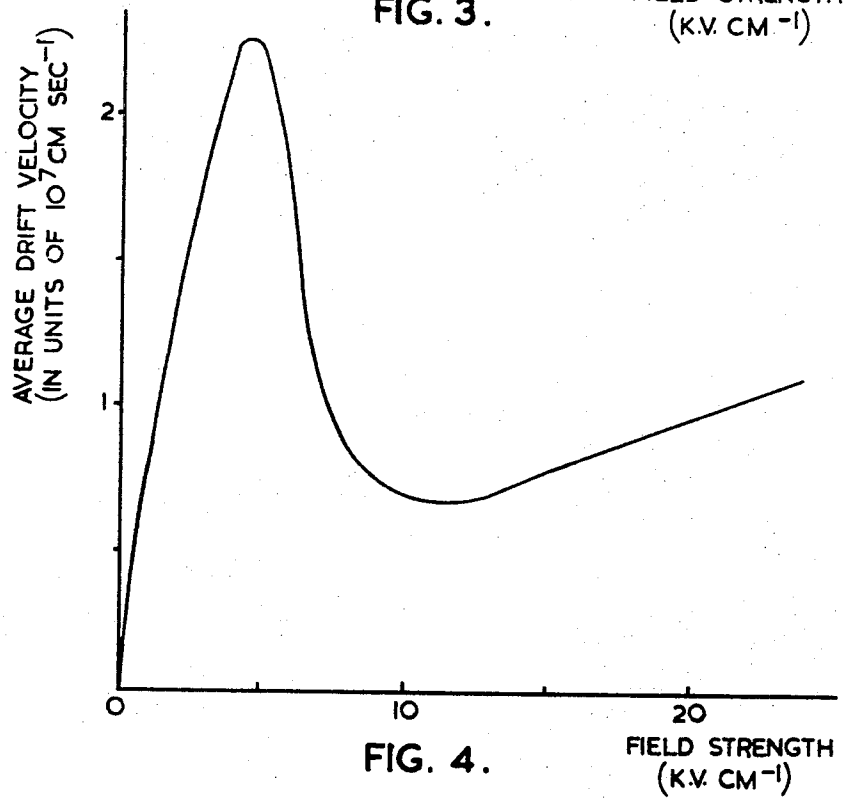

AVERAGE DRIFT VELOCITY
(IN UNITS OF 10^7 CM SEC^{-1})
2
1
0
10
20
FIELD STRENGTH
(K.V. CM^{-1})

FIG. 4.

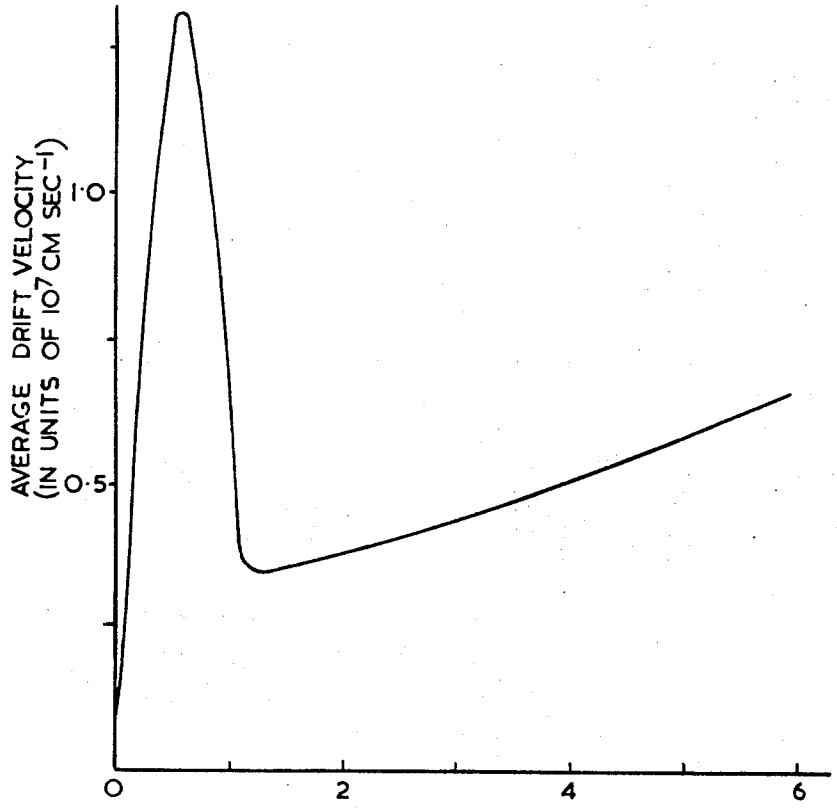

AVERAGE DRIFT VELOCITY
(IN UNITS OF 10^7 CM SEC^{-1})
1·0
0·5
0
2
4
6

FIG. 5.

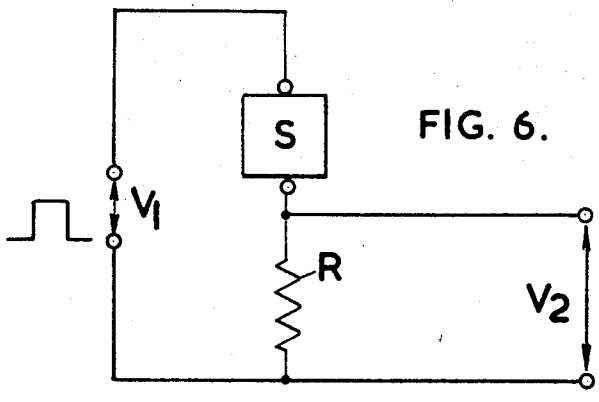
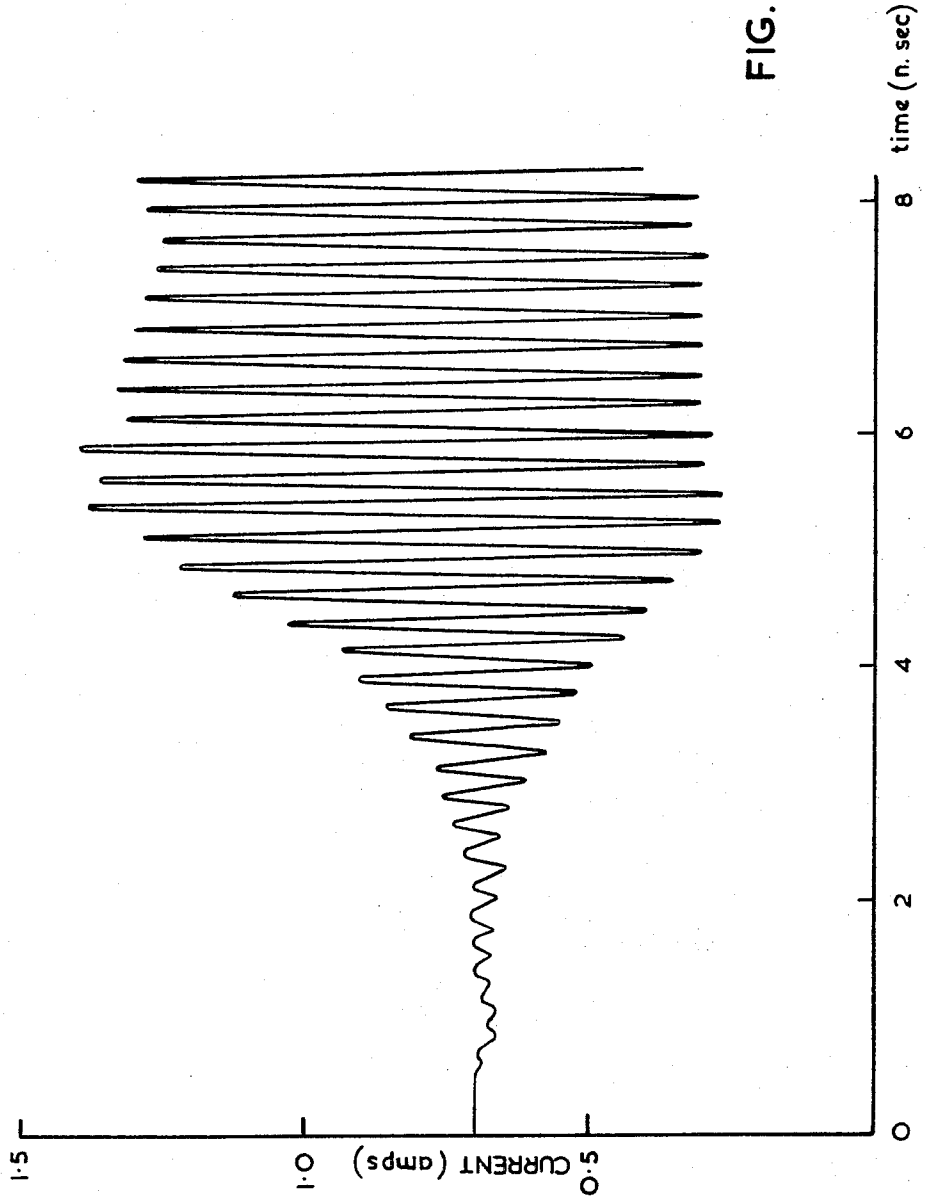

S
V1
R
V2

FIG. 6.

FIG. 7.



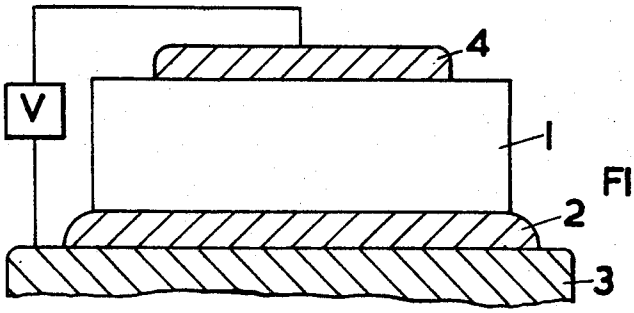


FIG. 9.

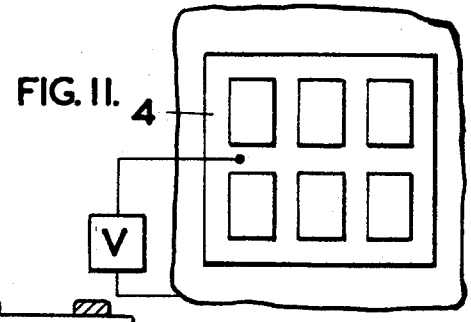


FIG. 11.

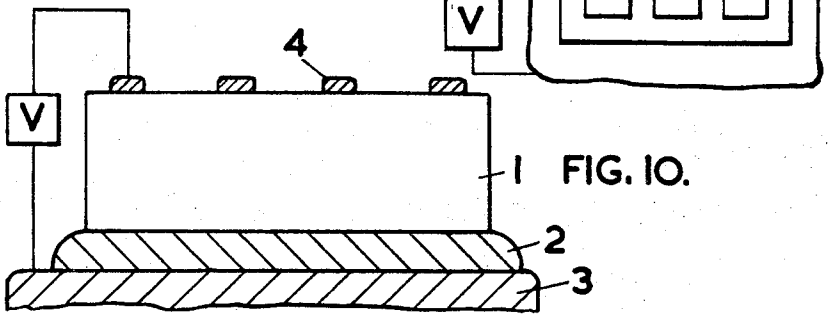


FIG. 10.

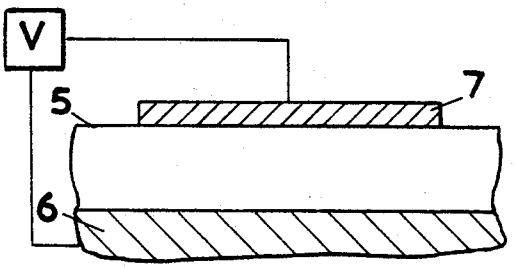


FIG. 12.

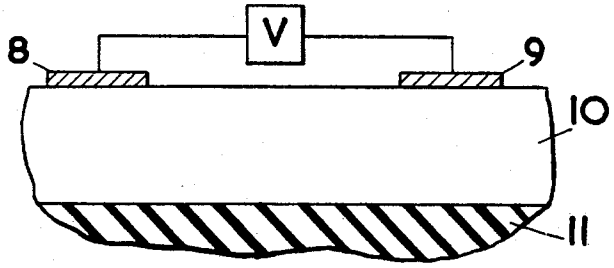


FIG. 13.

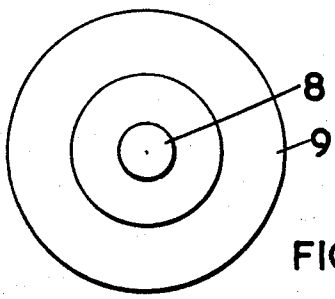


FIG. 15.

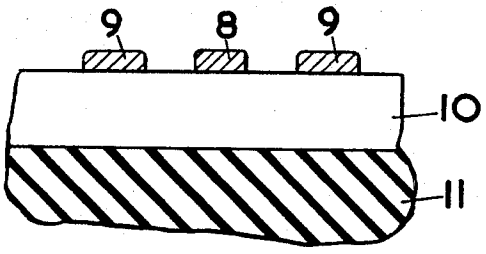


FIG. 14.

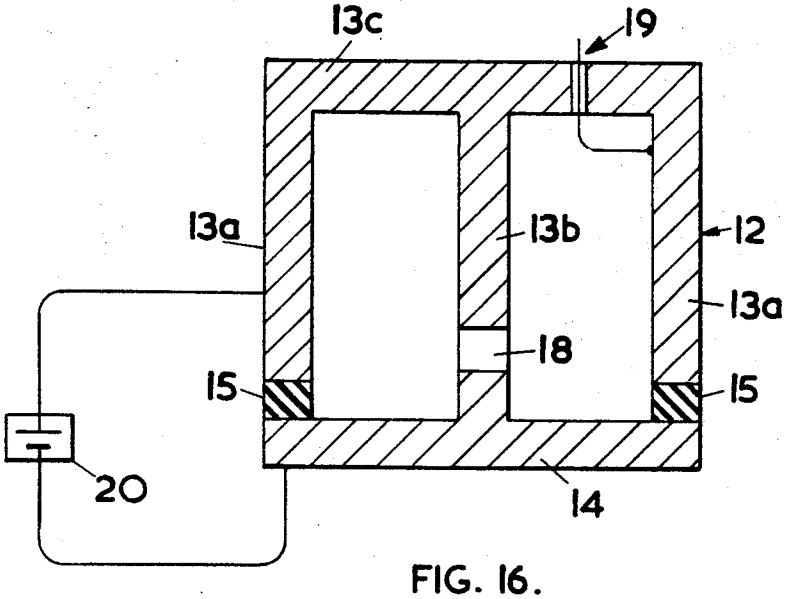


FIG. 16.

THREE VALLEY TRANSFERRED ELECTRON OSCILLATOR

The present invention relates to semiconductor devices.

In recent years there has been increasing interest in semiconductor devices which make use of transferred electron effects in high electric fields. These effects result from the transfer by scattering of electrons to conduction band valleys with higher energies than the valley (or valleys) chiefly occupied in lower fields. When the higher energy valleys have a larger energy density of states than the lower valley(s), it can happen than the electron drift velocity falls with electric field over much of the range of the field where transfer takes place. The electrons consequently exhibit a negative differential conductivity which can be usefully exploited in various devices, notably in microwave oscillators.

Gallium arsenide is an example of a material showing such an effect; the negative differential conductivity begins at a field of about 3 kV per cm. Gallium arsenide of N-type conductivity is widely used in microwave oscillators which make use of this negative differential conductivity. It is generally regarded as being the optimum material. In many oscillators, a high electric field region, called a domain, travels periodically through the gallium arsenide from the cathode (negative electrode) to the anode (positive electrode) at a speed close to 1×10^7 cm/sec. The performance of the oscillator is dictated by the existence of the domain. A strong tendency for domains to form is an inherent property of gallium arsenide. Consequently achieving modes of operation where domain formation is wholly or partially suppressed is difficult, although possible. This difficulty is often a disadvantage since the oscillator efficiency of domain modes is usually low.

It has long been appreciated that the band structure of the semiconductor and the scattering processes acting on the electrons determine the fundamental behavior of the electrons and ultimately the modes of operation of devices, their efficiency and their frequency limitations. It is clearly desirable to select for transferred electron devices a semiconductor whose fundamental parameters yield the most beneficial transferred electron properties. Three desirable properties are (1) a large "peak to valley ratio" (i.e., the ratio of the highest electron velocity attained to the lowest velocity reached at higher fields) to increase the maximum device efficiency, (2) both peak and valley velocities should be reasonably large so that operating frequencies are not unduly limited and (3) the inherent tendency for domain formation should be weak to permit flexibility of modes of operation of devices.

In gallium arsenide two sets of conduction band valleys are effective in determining the transferred electron properties. The present invention is based on the new realization that device performance can in certain respects be made superior by using a semiconductor in which transfer occurs between three sets of valleys.

According to the present invention there is provided a semiconductor device including a piece of semiconductor material exhibiting transferred electron effects between three sets of conduction band valleys, which sets consist of a set of lowest energy, a set of highest energy and a set of intermediate energy, and in which the set of lowest energy has an energy density of states smaller than that of either of the other two sets and in which the rate at which electrons are scattered between the set of lowest energy and the set of intermediate energy is less than both the rate at which electrons are scattered between the set of lowest energy and the set of highest energy and the rate at which electrons are scattered between the set of intermediate energy and the set of highest energy, an anode on the piece of semiconductor material, a cathode on the piece of semiconductor material, means for applying between the anode and the cathode voltages such that electron transfer occurs between the set of lowest energy and the set of highest energy and between the set of highest energy and the set of intermediate energy and means for controlling the current flowing between the cathode and the anode so that the current is free of dipole domains. Examples of semiconductor materials with suitable band structures and scattering rates between sets of valleys are indium phosphide, alloys of indium phosphide and indium arsenide with more than 75 molecular per cent indium phosphide and alloys of gallium antimonide and indium antimonide with between 5 and 30 molecular per cent indium antimonide.

According to an aspect of the present invention there is provided a semiconductor device including a piece of N-type indium phosphide, a first electrode attached to the piece of indium phosphide, a second electrode attached to the piece of indium phosphide and allowing a substantially greater current density in the piece of indium phosphide in the region of the second electrode than in the region of the first electrode and means for biasing the first electrode negatively with respect to the second electrode whereby electron transfer occurs between the different sets of valleys.

A substantially greater current density may be allowed by making the second electrode smaller than the first electrode, by introducing a doping inhomogeneity in the region of the first electrode or by tapering the piece of indium phosphide in that region.

By a "set of valleys" is meant all of those valleys of equal energy which appear at equivalent points on the same Brillouin Zone.

Embodiments of the present invention will be described by way of example with reference to the accompanying drawings in which:

FIG. 1 is a graph of electron drift velocity plotted against electric field strength for three typical semiconductor materials.

FIG. 2 is a schematic diagram of the band structure of a semiconductor material.

FIGS. 3, 4 and 5 are calculated graphs of electron drift velocity plotted against applied electric field strength for InP, $InAs_{0.2}P_{0.8}$ and $In_{0.2}Ga_{0.8}Sb$ respectively FIG. 6 is a circuit diagram of a circuit used to record current oscillations in semiconductor materials.

FIG. 7 is a graph of current plotted against time and is obtained using InP in the circuit of FIG. 6.

FIG. 8 is a graph of current plotted against time showing schematically the type of oscillations obtained using GaAs in the circuit of FIG. 6.

FIGS. 9 to 15 are diagrams illustrating semiconductor device fabrication for operating in given modes.

FIG. 16 is a diagram of a cross-section through the axis of a microwave device embodying the present invention.

FIG. 1 is a graph of electron drift velocity plotted against electric field strength for three typical semiconductor materials. The graph shows qualitatively the characteristics usually obtained with two and three level or set systems. As electric field strength is increased below threshold each of the materials follows Ohm's law. (i.e., with electron drift velocity proportional to applied field strength). At a threshold electric field region the characteristics of the materials follow separate paths. A first curve A is formed with a rather gentle drop in drift velocity after the threshold, the drop becoming gentler until the curve becomes flat at higher electric field strengths. A second curve B is formed with a steeper drop in drift velocity after the threshold and the curve B becomes gradually gentler until it becomes flat. A curve C drops rather steeply after the threshold and forms a distinct valley after which the drift velocity increases again for increasing electric fields. Curve A illustrates a two level or set system and is representative of gallium arsenide. Curve B refers to a similar system but the electron scattering rate between the two sets of valleys is lower. Reducing the scattering increases the transfer to the higher energy valleys but the velocity of electrons in the lower valley increases to a larger value in high fields. Although the negative differential conductivity is greater the ratio of maximum velocity to minimum velocity at higher fields (the peak to valley ratio) is little different from that of curve A. The reduced scattering has the additional disadvantage of permitting electrons in the lower valley to attain much higher energies, which means that avalanche breakdown of the

material can occur at lower fields. Curve C refers to a three level or set system with one low mass (i.e., low energy density of states) valley set as in the case of curve A but with two high mass sets of valleys at two different higher energies relative to the energy of the low mass valley. The scattering between the low mass valley and the lower energy high mass valley(s) is low, but between the other pairs of valleys it is high. In this system the transfer to the upper valleys is even greater than for the weakly coupled two level system, and in addition the strong scattering to the highest energy valleys holds down the electron velocity within the lowest valley and inhibits avalanche breakdown.

There are two other aspects of the three level system. The rise of velocity with field above the minimum value is usually greater than that usually attained in two level systems; this limits the maximum electric fields which can occur and therefore reduces the tendency for device destruction to occur. Also, the weak scattering between the lowest and intermediate energy valleys inhibits the growth of short wavelength fluctuations of electron density. Therefore, the natural tendency for domain formation is lower than normally occurs for two level systems.

For each of InP and the alloys specified above as having the appropriate structure, the lowest energy valley is centered on the Γ point of the Brillouin zone, the set of intermediate energy valleys consists of a valley at each of the four equivalent L points and the set of highest energy valleys consists of a valley at each of the three equivalent X points.

FIG. 2 shows qualitatively part of the band structure of a material illustrative of one of the materials described above, namely InP. The energy of the X minima (or valleys) is higher than the energy of the L minima, and the energy of the Γ minimum is lowest of all. The Γ minimum is narrower than the L or X minima reflecting its lower energy density of states.

FIGS. 3, 4 and 5 are calculated graphs of electron drift velocity against applied electric field strength for InP, $InAs_{0.2}P_{0.8}$, and $In_{0.2}Ga_{0.8}Sb$ respectively. It is apparent that a band structure of the type shown in FIG. 2 leads to a velocity-field strength relationship of a similar form for each of these materials which is the form of the curve C in FIG. 1.

The existence of negative resistance in indium phosphide has been recognized for some time, but it has not been previously suspected that the behavior of InP devices is different in character from that of GaAs devices. In an early publication on oscillations observed in InP and GaAs devices oscillations were reported for only one InP sample. For this sample the oscillations were very weak, which observation would lead those skilled in the art to abandon InP as a suitable material for transferred electron devices because the actual device performance would seem much inferior to that of GaAs. Since this publication no reports have in fact appeared on transferred electron devices fabricated from InP although very large numbers of reports of GaAs devices have appeared.

It is apparent from the early publication that electrical instabilities above a threshold voltage are possible in indium phosphide but it is not apparent that any type of operation other than Gunn effect (dipole domain) operation is possible in this material. Recently, we have conducted experiments using indium phosphide samples, and these help to confirm the theory that the behavior of indium phosphide devices is inherently different in character from gallium arsenide devices under equivalent conditions. This means that simple steps can be taken to produce non-domain mode operation in indium phosphide (see below). Gunn effect (domain mode) operation would continue to occur if such steps alone are taken with gallium arsenide.

FIG. 6 is a schematic circuit diagram of a circuit which was used to record current oscillations across a piece of indium phosphide. The same circuit may be used to test pieces of any other semiconductor material, such as GaAs or InP_xAs_{1-x} and $In_yGa_{1-y}Sb$ (where x and y are in the ranges $1 > x \geq 0.75$ and $0.30 \geq y \geq 0.05$ respectively).

A square voltage pulse V, is applied from a conventional source (not shown) across a series combination of a sample S of the semiconductor material and a resistor R. The resistor R has a resistance of magnitude much smaller than that of the sample S. The output voltage V_2, which indicates oscillations, is taken across the resistor R and is displayed on an oscilloscope (not shown).

FIG. 7 is a graph of current against time and is an oscilloscope trace which was obtained using an InP sample in the circuit of FIG. 6 It represents current obtained as a function of time with a piece of N-type InP of thickness 170 μm and equilibrium carrier density of $5 \times 10^{14} cm^{-3}$ for an applied voltage of 150 volts. The current oscillates nearly sinusoidally with a frequency of 4 GHz, and the oscillations grow to a steady amplitude in a time of about 4×10^{-9} sec. If a GaAs sample with the same thickness and equilibrium carrier density were used the current would oscillate with a frequency of about 0.5 GHz and the waveform would consist of isolated spikes as indicated by the graph of FIG. 8. The spikes coincide with domains reaching the anode (positive terminal of the sample S).

The appearance of the trace shown in FIG. 7 indicates that the domain mode which is a characteristic of GaAs samples is not present.

With devices fabricated from InP or from the specified alloys, both dipole domain mode operation and operation without dipole domains can, however, be readily obtained. This may be contrasted with the case of GaAs where operation without domains is very difficult to realize. Consequently the device fabrication needs to be performed in consideration of the operation mode required, i.e., either dipole domain or non-dipole domain.

It is believed that in indium phosphide and the two specified alloys there is a natural tendency for instabilities to propagate from the cathode to the anode in the form of an electron accumulation layer rather than as a dipole domain. This "accumulation layer" mode is obtained even when there are small fluctuations of doping concentration within the semiconductor. By contrast, small doping fluctuations in gallium arsenide readily initiate dipole domains.

Non-domain mode operation is more suited to oscillator devices than domain mode operation is because the oscillator efficiency can be greater in the non-domain mode. Domain mode operation in a semiconductor transferred electron device occurs when the electrodes of the device are formed in a way that produces a much greater current density in the cathode region than in the anode region.

Non-domain mode operation can easily be produced in indium phosphide and the specified alloys ($InP_xAs_{1-x}, 1 > x \geq 0.75$ and Iny $Ga_{1-y}Sb$, $0.30 \geq y \geq 0.05$) by simply arranging the reverse, i.e., a greater current density in the anode region than in the cathode region. Such an operation mode is also possible with electrode regions of approximately similar current density, but arrangement in the form described (i.e., current density in the cathode region greater than in the anode region) shows a greater tendency of non-domain mode operation.

FIG. 9 is a cross-sectional diagram of one form of semiconductor devices. A piece 1 of N-type semiconductor material (indium phosphide or In P_x As_{1-x} $1 > x \geq 0.75$ or In_y $Ga_{1-y}S$ b $0.05 \leq y \leq 0.30$) has a metallic contact 2 and a metallic contact 4 alloyed thereto. A metal block 3 to which the contact 4 is also alloyed serves as a mechanical substrate, as a heat sink for the device and as an external electrical contact. The alloying processes are carried out by melting the metals of the contacts 4, 2 in contact with the semiconductor and the metal of the block 3 respectively. (The metals of the contacts 2, 4 may be initially deposited by vacuum evaporation). The contact 4 may be of the same material as or of different material from that of the contact 2. Likewise, the contact 2 may be of the same material as or different material from that of the block 4. Suitable metallic materials for the contacts 2, 4 and the block 3 are tin and alloys of tin and indium. (The latter is

more suitable in the case of indium phosphide). These materials form N^+ regions between the contacts **2, 4** and the piece **1** of semiconductor material. Voltages may be applied across the piece **1** of semiconductor material by means of a conventional D.C. voltage source V.

The transverse dimensions of the contacts **2, 4** with respect to each other and to the thickness of the piece **1** of semiconductor material are important. The transverse dimensions of the contact **2** and the contact **4** may be made large compared with the thickness of the piece **1** of the semiconductor material in which case the electrical current density through the semiconductor in the region of the contact **2** is little different from that in the region of the contact **4**. This leads to an inhibition of domain formation.

Alternatively, the transverse dimensions of the contact **2** and the contact **4** may be made comparable to or less than the thickness of the piece **1** of semiconductor material. There are three possible structures in this form. The first is with the contact **2** and the contact **4** of the same lateral dimensions. This produces equivalent current densities in the regions of the piece **1** of semiconductor near the contacts **2** and **4** respectively. Equal current densities tend to inhibit domain formation. The second structure is with one contact (say the contact **4**) of lateral dimensions less than those of the other contact (say the contact **2**) and the smaller one made positive with respect to the larger one. This gives a smaller current density in the region of the anode than the region of the cathode. This structure then has the form suitable for the inhibition of domain formation. The third structure is with one contact (say the contact **4**) of lateral dimensions again less than those of the other (say the contact **2**), but with the voltage source V arranged to make the smaller contact (the contact **4**) the cathode. This structure enhances domain formation. Suitable contact dimensions in both of these second and third structures would be a smaller contact (the contact **4**) having one third the perimeter of the larger contact (the contact **4**). (For example, circular contacts may be used having diameters in the ratio 1:3).

An alternative method of producing a high current density (high electric field) near one of the contacts **2** and **4** is to introduce a doping inhomogeneity such as by using tin with a small percentage of zinc as the contact material (and alloying in the same manner as above). The zinc produces a small region of P-type material. If the contact **4** is formed in this way and the source V is arranged to bias it negatively then domain formation may be enhanced in the region thereof. Likewise, domain formation is inhibited if the contact **4** so formed is alternatively made an anode.

FIG. **10** is a cross-sectional diagram of a device which is a modification of the device of FIG. **10**. FIG. **11** is a part plan view of the device. The contact **4** is here in the shape of a grid. Other patterns may be used such as a series of separate dots. Patterns may be deposited by the standard technique of evaporation through a mask. The advantage of depositing the contact **4** as a pattern is that the lateral dimensions can be kept small giving the above mentioned properties of high current density and high electric field strength in that region while the surface area can be kept large permitting greater operating powers to be used (because contact heating and subsequent breakdown is not such a problem with larger contact areas).

FIG. **12** is a cross-sectional diagram of another semiconductor device. This arrangement is particularly useful when a thin semiconductor operating layer is required. A thin layer **5** of appropriate semiconductor material (InP_xAs_{1-x} $1 \geq x \geq 0.75$ or $In_yGa_{1-y}Sb$ $(0.30 \geq y \geq 0.05)$ is grown epitaxially (in a standard manner) on a highly conducting substrate **6**. The substrate **6** acts as a heat sink and as an electrical contact. A contact **7** is made on the other side of the layer **5**. The contact **7** may be either metal deposited by the standard techniques of vacuum evaporation and alloying or it may be an epitaxially deposited layer of highly conducting semiconductor material. A suitable metal is tin and a suitable semiconductor is the same material as that of the layer **5** but doped N-type. A voltage from a conventional source V may be applied between the substrate **6** and the contact **7**. The contact **7** is made with lateral dimensions small with respect to the thickness of the layer **5** and the lateral dimensions of the contact **6** and so exhibits the high current density property described above (i.e., it forms domains when the source V is arranged to bias it negatively and alternatively inhibits domain formation when the source V is arranged to bias it positively).

FIG. **13** is a cross-sectional diagram of another semiconductor device. This is in the transverse form as opposed to the longitudinal form of the previous devices. A contact **8** and a contact **9** may be made by metal to a layer **10** of semiconductor material deposited epitaxially on an insulating substrate **11** (in a standard manner). The substrate **11** acts as a heat sink. If the layer **10** consists of $InAs_{1-x}P_x(1 \geq x \geq 0.75)$ then a suitable substrate material is chromium doped indium phosphide (which is essentially insulating). The contacts **8, 9** which are formed in the same manner as those described with reference to FIG. **9** are of unequal transverse dimensions (perimeters in the ratio of 1:3). Voltages may be applied between the contacts **8, 9** by means of a source V. This produces a higher current density in the region of the smaller one, the contact **8**, than in the region of the larger one, the contact **9**. If the source V is arranged to make the contact **8** negative then domains tend to form. If the source V is arranged to make the contact **8** positive then domain formation is inhibited. Alternatively, or in addition, high electric fields (high current densities) may be obtained in the region of the contact **8** by producing a small P-type inhomogeneity region therein in the same manner as with the device of FIG. **9**.

FIG. **13** is a cross-sectional diagram of and FIG. **14** is a part plan view of a device which is a modification of the device of FIG. **13**. The contact **9** is formed by evaporation through a suitable mask in a standard manner to surround the contact so that the latter is effectively a small contact. If the source V is arranged to make the contact **8** negative then domains tend to form in the region thereof. If the source V is alternatively arranged to make the contact **8** positive then domain formation is inhibited.

FIG. **16** is a cross-sectional diagram of a device embodying the present invention for generating microwave power.

A microwave cavity **12** is in the form of a coaxial cylinder and consists of two separated portions **13** and **14**. The portion **13** consists of an outer hollow cylindrical region **13***a* with an integral circular ceiling region **13***c* and an inner region **13***b* on the axis of the cylinder formed integrally with and protruding from the ceiling region **13***c*. The region **13***a* of the portion **13** is separated from the portion **14** by a ring **15**. The region **13***b* of the portion **13** is separated from the portion **14** by a piece **18** of semiconductor material which may be indium phosphide or $In\ P_x\ As_{1-x}$ or $In_y\ Ga_{1-y}Sb$ $(1 > x \geq 0.75, 0.30 \geq y \geq 0.05)$. The piece **18** is in the same form as the device of FIG. **9**, i.e., it has contacts of unequal dimensions (not shown) and a longitudinal structure. (In this case the block **3** of FIG. **9** is not needed because the cavity **13** acts as an external electrical contact and heat sink.) The ring **15** is insulating at D.C. but its impedance is negligible at microwave frequencies. Voltages may be applied between the portion **13** and the portion **14** of the cavity **12** by means of a conventional voltage source **20**. The voltage appears across the piece **18** of semiconductor. When the voltage is large enough to bias the piece **18** of semiconductor in its region of instability the current in the piece **18** of semiconductor oscillates at a frequency at which the cavity **12** is resonant. The dimensions of the cavity **12** are chosen to give the required frequency of operation. Microwave power is coupled from the cavity **12** by means of a coupling loop **19**.

In addition to the electrode structures being critical in the inhibition of dipole domain formation the length and purity of the piece of semiconductor material also need to be taken into consideration.

If the active length of the piece of semiconductor material taken is below a critical length in the order of about 500μm then nonedomain mode operation occurs (if steps described in this specification are taken for enhancing non-domain operation). If, however, the active length is greater than that critical length then domain mode operation occurs despite the steps which are taken (unless these are very extreme).

The materials which have been specified as being suitable for use in the present invention are all prepared by standard techniques. However, it is necessary to observe that the total number of impurities contained in the semiconductor material is not greater than 10^{17} per cubic cm. and preferably less than 10^{16} per cubic cm. otherwise operation produces weak results (possibly incoherent domains) or none at all at high impurity levels. To ensure that the desired purity is obtained it is necessary to choose in each respective case one of the conventional methods known for producing semiconductor materials of the desired purity.

Compositions of indium phosphide arsenide throughout the specified range may be obtained by any one of several methods conventionally used for preparing the alloy, including solution growth or vapor or liquid epitaxy.

For example, an InAs substrate may be used at a temperature above 600° C. The appropriate alloy may be grown by vapor epitaxy from HCl passed over indium and a mixture of AsH_3 and PH_3 gases containing the appropriate molecular fraction of PH_3. (0 to 25 percent InP in InP-InAs corresponds to the range of arsine-phosphine mixtures containing below approximately 40 percent phosphine.)

Compositions of indium gallium antimonide throughout the specified range may be obtained by the known method of reacting the constituent elements together in the required proportions and refining the resultant structure by the known techniques of "zone leveling."

Crude indium phosphide can be prepared by reacting phosphorous vapor with liquid indium at an elevated temperature. Indium phosphide of sufficient quality for fabricating devices may be made from crude indium phosphide by heating it to a temperature slightly greater than its melting point of 1,060° C. and bringing a seed crystal, which is usually indium phosphide, into contact with the melt and then withdrawing the crystal slowly. The attachment for supporting the seed crystal conducts away heat and more indium phosphide grows on the seed crystal. At the melting point of indium phosphide, the vapor pressure of phosphorus in equilibrium with the indium phosphide is about 20 atmospheres. Therefore a suitable technique, such as the liquid encapsulation technique, must be employed for maintaining the system at a pressure greater than this pressure. Alternatively epitaxial methods may be used to grow high quality layers of indium phosphide on substrate materials. One possible technique is to pass a gas mixture containing phosphorus and chlorides of indium in an excess of hydrogen over single crystal substrates at an elevated temperature of about 650° C. A suitable way for obtaining a correct gas mixture is to pass phosphorus trichloride vapor in an excess of hydrogen over liquid indium at an elevated temperature of about 750° C. The initial chemical reactions form indium phosphide dissolved in the indium, but when the solution is saturated the gas mixture passing over the solution contains the required amounts of phosphorus, chlorides of indium and hydrogen. Possible seed crystals are indium phosphide, indium arsenide or gallium arsenide. Control of the electron concentration in the layer can be achieved by adding suitable volatile materials to the gas stream. An example is hydrogen sulphide which adds sulphur to the layer. Sulphur is a donor impurity which increases the electron concentration. A different epitaxial method is to tip a saturated solution of indium phosphide in indium over a seed crystal of indium phosphide at an elevated temperature of about 650° C. The system is allowed to cool to a slightly lower temperature, such as 620° C. During the cooling a layer of indium phosphide grows on the seed crystal. The excess solution may then be tipped away from the seed crystal.

Control over the electron concentration may be achieved by incorporating in the semiconductor in each case a controlled amount of N-type impurity such as tin.

We claim:

1. A semiconductor device including a piece of semiconductor material exhibiting transferred electron effects between three sets of conduction band valleys, which sets consist of a set of lowest energy, a set of highest energy and a set of intermediate energy, and in which the set of lowest energy has an energy density of states smaller than that of either of the other two sets and in which the rate at which electrons are scattered between the set of lowest energy and the set of intermediate energy is less than both the rate at which electrons are scattered between the set of lowest energy and the set of highest energy and the rate at which electrons are scattered between the set of intermediate energy and the set of highest energy, said material chosen from the group consisting of InP_xAs_{1-} where x is within the limits $1.00>x\geq 0.75$, the upper limit being exclusive and the lower limit being inclusive and $In_yGa_{1-y}Sb$ where y is within the inclusive limits $0.05\geq y\geq 0.30$, an anode on the piece of semiconductor material, a cathode on the piece of semiconductor material, means for applying between the cathode and the anode voltages such that electron transfer occurs between the set of lowest energy and the set of highest energy and between the set of highest energy and the set of intermediate energy and means for controlling the current flowing between the cathode and the anode such that the current is free of dipole domains.

2. A semiconductor material as claimed in claim 1 and wherein the means for controlling the current flowing between the cathode and the anode includes means for providing a current density in the region of the anode greater than or similar to the current density in the region of the cathode.

3. A semiconductor device as claimed in claim 2 and wherein the area of contact between the anode and the piece of semiconductor material is smaller than the area of contact between the cathode and the piece of semiconductor material.

4. A semiconductor device as claimed in claim 2 and wherein the anode contains a region of doped semiconductor material and wherein the doping is such that it is inhomogeneously distributed.

5. A semiconductor device as claimed in claim 2 and wherein the piece of semiconductor material is wedge shaped, the apex of the wedge being near the anode.

6. A semiconductor device as claimed in claim 1 and wherein the piece of semiconductor material contains less than 10^{17} impurities per cubic centimeter.

7. A semiconductor device as claimed in claim 1 and wherein the distance between the anode and the cathode is less than approximately 500 microns.

8. A semiconductor device as claimed in claim 6 and wherein the distance between the anode and the cathode is less than approximately 500 microns.

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UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,667,003 Dated May 30, 1972

Inventor(s) Cyril Hilsum et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 8, line 28, "InP_xAs_1-" should read

-- InP_xAs_{1-x} --.

Signed and sealed this 12th day of December 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents

FORM PO-1050 (10-69)

USCOMM-DC 60376-P69
* U.S. GOVERNMENT PRINTING OFFICE : 1969 O—366-334.