

April 22, 1969

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3,440,452

TIMING CIRCUIT

Filed Oct. 31, 1966

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Fig. 1A

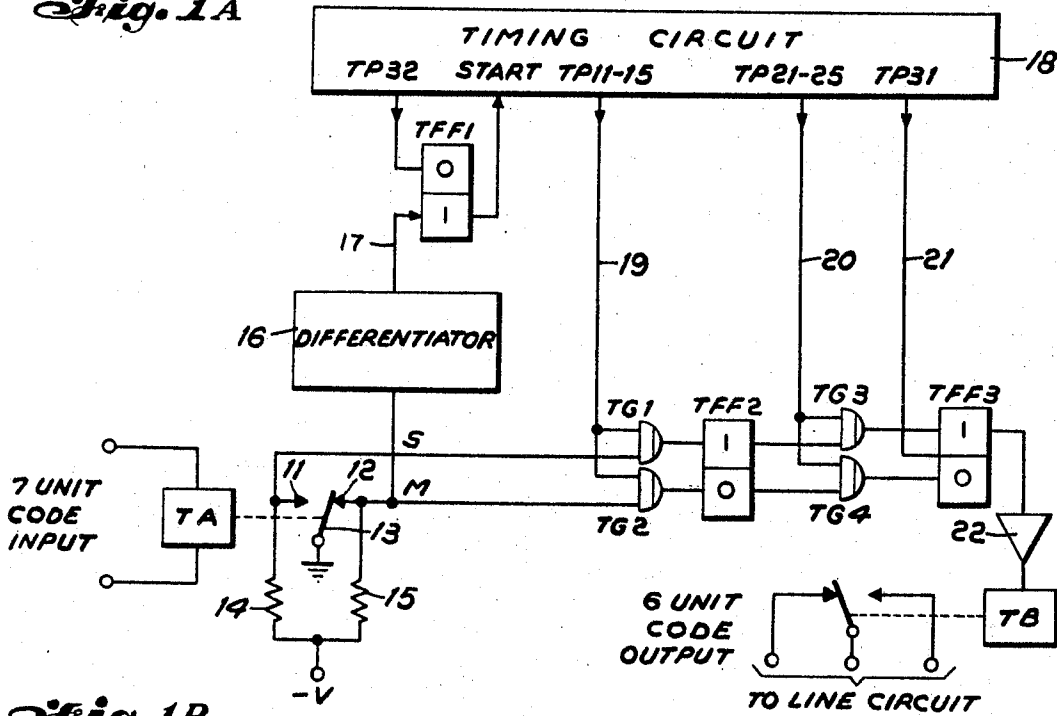
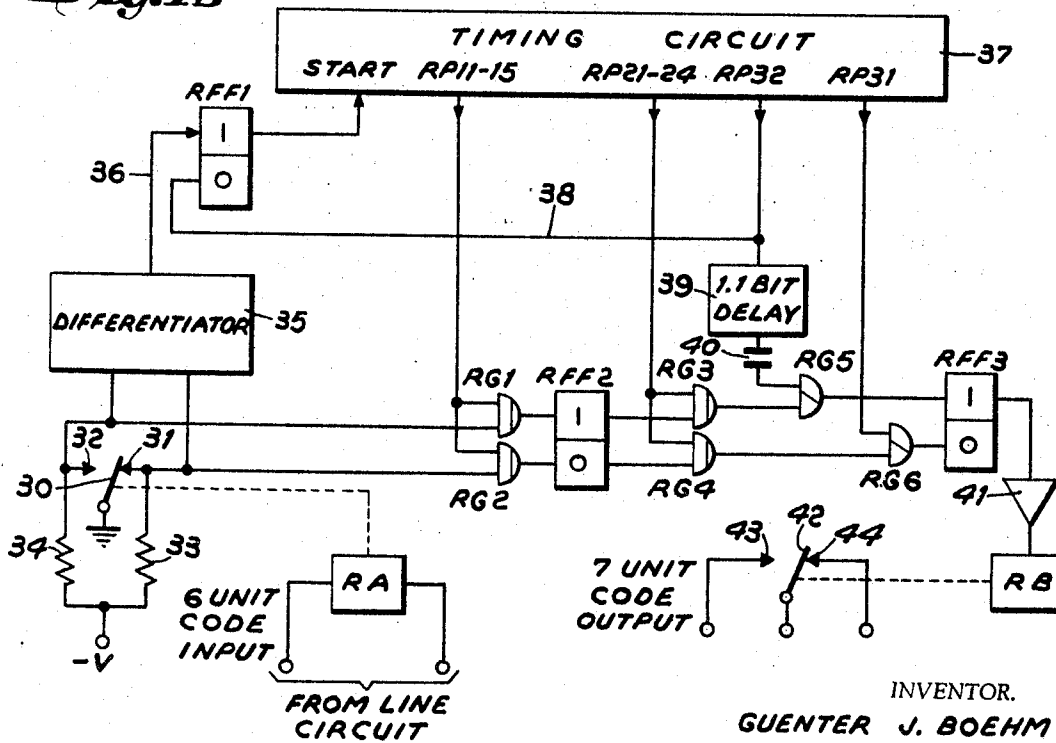


Fig. 1B



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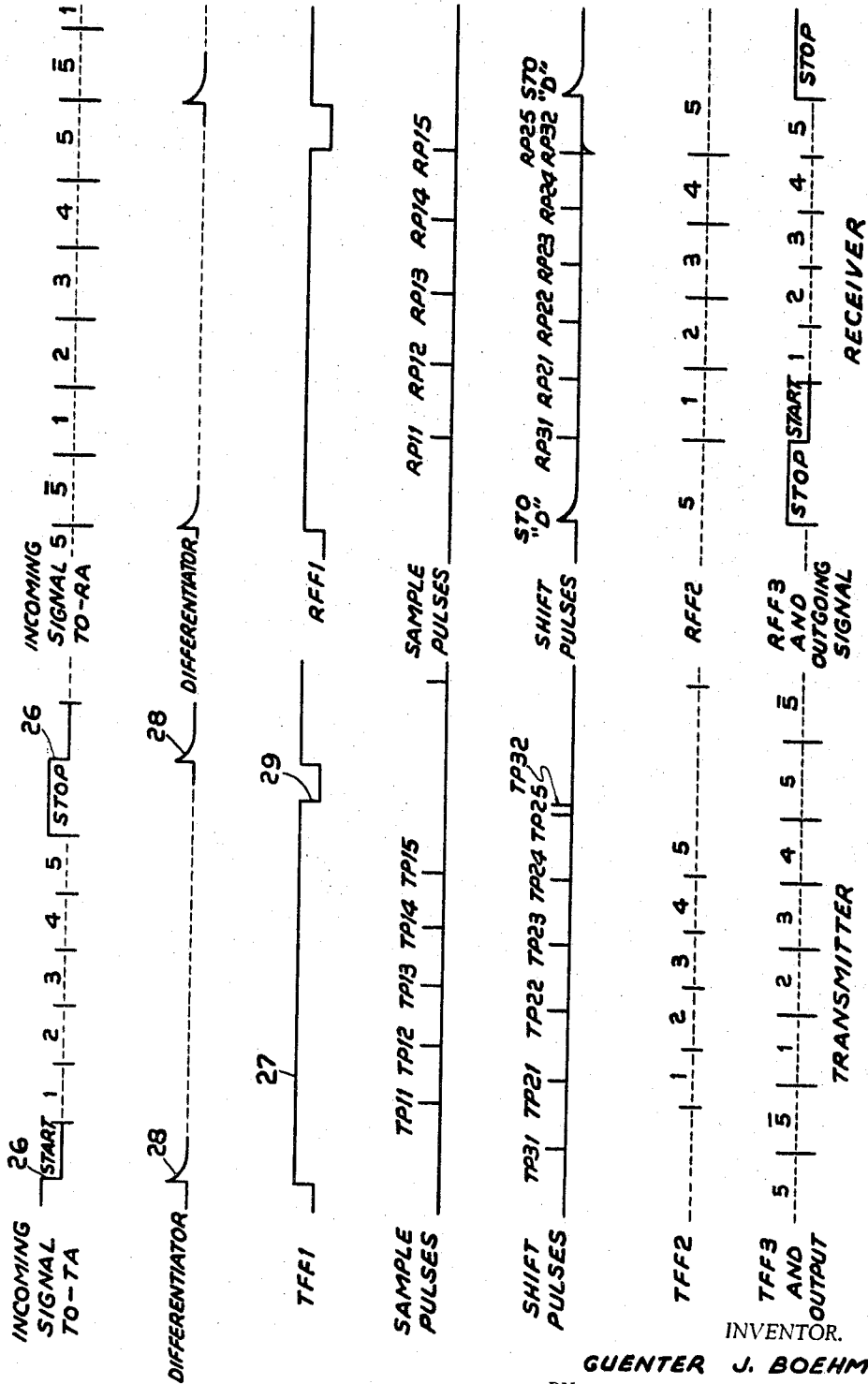
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Fig. 2A

Fig. 2B



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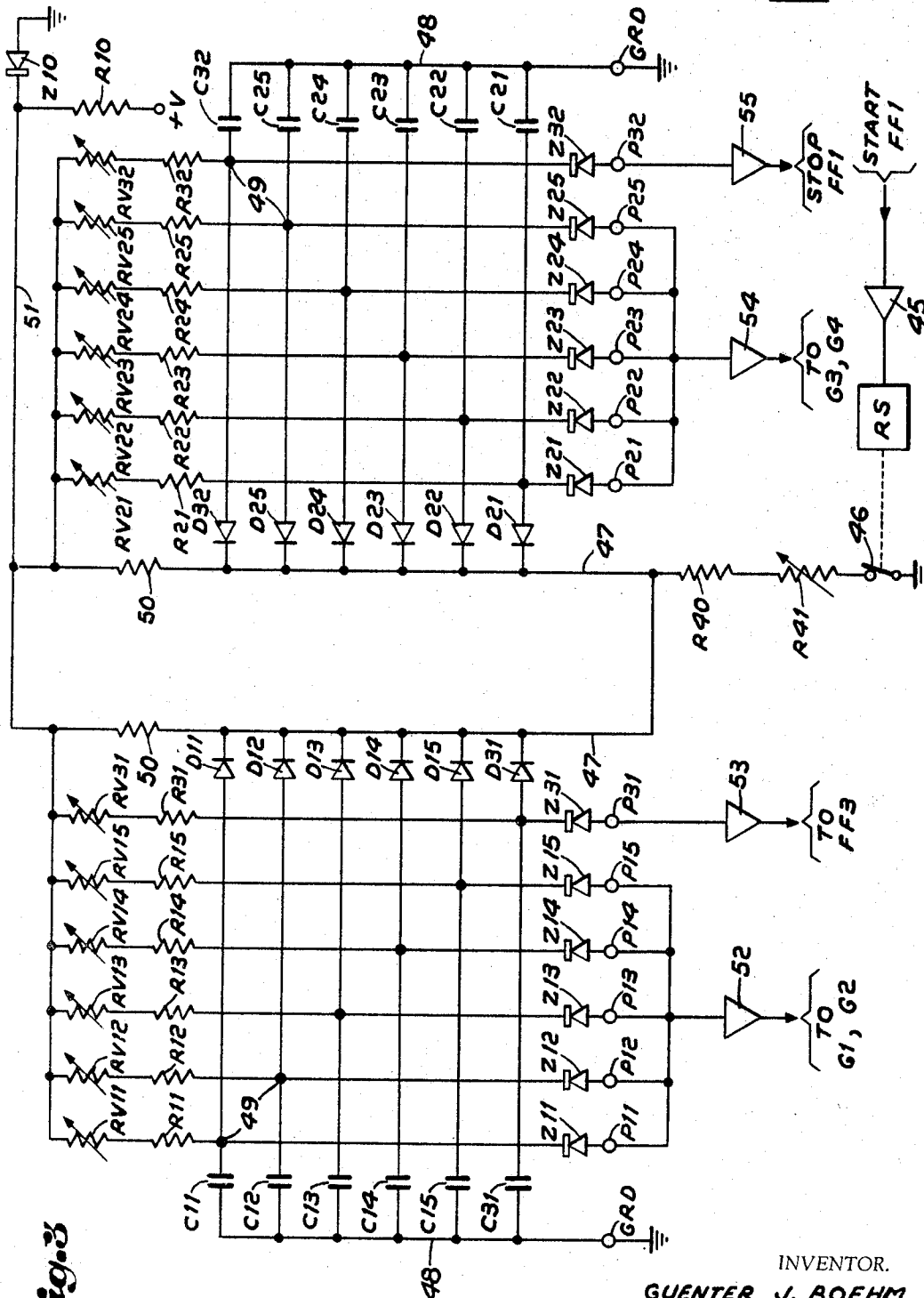


Fig. 3

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3,440,452

TIMING CIRCUIT

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6 Claims

ABSTRACT OF THE DISCLOSURE

The arrangement provides a simple and reliable timer which starts a desired number of independently determinable overlapping time intervals from a common start instant, and which ends the started intervals individually in response to the action of respective critical-potential breakdown devices, from each of the devices a separate control pulse is transmitted to mark the end of its corresponding time interval.

This invention generally relates to a timing circuit, and more particularly to a timing circuit employing critical-potential breakdown devices of the class including Zener diodes.

In a system as disclosed and claimed in the United States Patent 3,149,203 to L. B. Haigh et al., the transmitter and the receiver each require a quick-reset timer, or clock circuit, which is started at the initiation of character transmission in order to generate a series of 12 time-displaced control pulses for each character transmitted. It has been shown in this patent that a seven element code combination can be directly converted to a six unit combination to improve the transmission, and as such, a timer or clock is required to reduce an outgoing start pulse and five recordal-control pulses corresponding to the incoming code elements, and also five transmission-control pulses accurately interspersed with the recordal-control pulses, and a final reset pulse to cause the timing circuit to be reset for another cycle of operation upon the next succeeding character-transmission operation.

Heretofore, the timing circuits available for use in a system of this type have been too expensive because of being too bulky or complicated, along with lacking facilities for independent adjustment of the timing displacement, or have been unreliable because of being exceedingly complex in that errors that occur in the time displacement became cumulative.

According to the invention, the foregoing and other drawbacks are overcome by providing for each of the several noted pulses, a separate timing circuit branch for providing a potential which rises adjustably with time and which includes a critical-potential device for control-pulse generation, and by providing a timer starting arrangement which applied a constant-potential current source to all of the timing circuit branches at the same starting instant, each circuit branch being arranged to reach the critical-potential of its critical-potential device at the end of a predetermined interval from the starting instant.

A principal object of the invention is to provide a simple and reliable timer which starts a desired number of independently determinable overlapping time intervals at a common start instant, and ends the started intervals individually in response to the action of respective critical-potential devices, from each of which a separate control pulse is transmitted to mark the end of its corresponding time interval.

Another object of this invention is to provide a simple and reliable arrangement for separately and independently adjusting the length of the several intervals, to establish

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the desired time displacement of the first control pulse from the start instant, and to establish desired time displacements on the several control pulses.

A further object of this invention is to provide a timer according to the invention which is adapted to furnish the time-displace control pulses, clock pulses, required in the transmitter and receiver of the type as disclosed and claimed in the L. B. Haigh et al. patent.

In carrying out the invention, the elected critical-potential devices are Zener diodes, each of the timing circuit branches includes a timing capacitor charged in series with an adjustable resistor from the noted constant-potential current source, with the Zener diode connected across the capacitor, and the source potential is the critical-potential of a Zener powered diode.

According to a specific feature of the invention, simultaneous starting of the capacitor charging operation is begun by opening a normally closed discharge path for the several timing capacitors, each of which is connected to the common discharge path through a separate discharge diode which is connected so as to pass capacitor discharge current in its forward direction, with sufficient resistance to limit the maximum discharge current through any discharge diode to a value as in the safe current carrying capacity thereof. The timer is reset by closing the common discharge path to each of the timing capacitors to a near-zero normal or starting potential.

A related feature concerns the adjustment of the timing intervals. First, the interval required for any timing capacitor to reach the critical-potential of its associated Zener diode is individually adjustable by adjustment of the adjustable resistor in its charging path. Second, by placing in the common discharge path at least a portion of the noted resistance, a normal starting point potential remains across all the timing resistors after the capacitors have discharged as fully as they can. Then, raising the resistance of this common resistor increases the normal or starting potential of all the timing capacitors, thus decreasing the timing interval thereof, and lowering the resistance of this common resistor has the opposite effect.

The above-mentioned and other features and objects of this invention will become more apparent by reference to the following description taken in conjunction with the accompanying drawings, in which:

FIGURES 1a and 1b show the transmitter and receiver employing the timing circuit according to the invention;

FIGURES 2a and 2b show the timing pulses which occur in the transmitter and receiver of FIGURES 1a and 1b; and

FIGURE 3 shows the timing circuit according to the invention as used with the transmitter and receiver of FIGURES 1a and 1b.

The function of the transmitter shown in FIGURE 1a is to convert a seven unit code input to a six unit code output. The transmitter eliminates the stop bit of the seven unit code, lengthens each remaining bit by one-sixth of the stop bit and generates the start bit always as the inverse of the fifth information bit of the previous character.

Relay TA, having stationary contacts 11, 12, and movable contact 13, receives the incoming seven unit code character. Contacts 11 and 12 are respectively connected through resistors 14 and 15 to a source of negative potential, with respect to the ground potential on movable contact 13. Contact 13 follows the incoming signal and marks the state of the bit on gate TG1 and TG2.

The beginning of the character is marked by a "Mark" (relay TA operated) to a "Space" (relay TA release) transient. When this transient occurs, the differentiator 16 generates a pulse on line 17 to set flip-flop TFF1 to state "1." TFF1, now set to state "1," starts the timing circuit

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18 according to the invention which is hereinafter described with reference to FIGURE 3.

The timing circuit then generates the pulses TP11 to TP15, TP21 to TP25, TP31 and TP32. The pulses TP11 to TP15 are timed to occur in the middle of each information bit (1 to 5). TP11 to TP15 through conductor 19 opens gates TG1 or TG2 in accordance with the state of contact 13. In this manner flip-flop TFF2 is set to the state of the incoming signal. The pulses TP21 to TP25 and TP31 are spaced at intervals corresponding to the bit duration of the outgoing signal. TP21 and TP25 are timed to occur always later than the corresponding TP11 to TP15 pulses. Pulses TP21 to TP25 through conductor 20 and gate TG3 and TG4, shift the signal from TFF2 to TFF3.

Pulse TP31 occurs at the beginning of the timing cycle and changes the state of TFF3 through conductor 21, the state of TFF3 being that of the last stored fifth information bit of the last character. A relay driver 22 is provided to operate relay TB having a movable contact 23, which is connected to either stationary contact 24 or 25, depending on the condition of the relay. Movable contact 23 being permanently connected to a transmitted end terminal of the line circuit while stationary contacts 24 and 25 are respectively connected to sources of space and mark signal potentials which are then selectively impressed on the line circuit.

Pulse TP32 is timed to occur immediately after the last shift pulse TP25 and is used to reset the reset timing circuit 18 through flip-flop TFF1.

Referring additionally to FIGURE 2a, TFF1 is started by a mark to space transient 26, pulse 27 in turn starting the timing circuit. Differentiator 16 consists of a resistor-capacitor-diode network and generates a pulse 28 when contact 13 changes from its operated to its released position. The sample pulses TP11 to TP15 are timed to occur in the middle of each bit information (1 to 5).

The shift pulses TP21 to TP25 are spaced at intervals corresponding to the bit duration of the outgoing signal and are timed to occur later than the corresponding TP11 to TP15 pulses. TP32 is timed to occur immediately after the last shift pulse TP25 and reset TFF1 as indicated by numeral 29. Shift pulse TP31 occurs at the beginning of the timing cycle and changes the state of TFF3, to the inverse of the fifth information bit of the last character, indicated by 5.

TFF2 provides a temporary storage for the incoming information bits when TG1 and TG2 are opened by the sample pulses TB11 to TB15, TFF2 is set of the state of the incoming bits which are indicated by the position of contact 13. TFF3 stores and times the outgoing information and start bits. It is set to the state of TFF2 when gate TG3 and TG4 are opened by TP21 to TP25. The six code output is indicated as 5, 1, 2, 3, 4, and 5.

The function of the receiver, as shown in FIGURE 1b, is to convert the received six bit code back to the original seven bit code. The receiver regenerates the stop bit as a mark and a start bit as a space, and restores the five information bits to their original length. Receiver relay RA selectively couples movable ground contact 32 to either stationary contact 31 or 32. Contacts 32 and 31 are respectively coupled by resistors 33 and 34 to a source of negative potential with respect to ground. Since the receive start bit may be of a positive or negative polarity, differentiator 35 must recognize a transient in either direction. A transient sets RFF1 by conductor 36 to state "1" to start timing circuit 37 which has the same arrangement as timing circuit 18. Gates RG1, RG2, RG3, RG4, RG5, and RG6 operate function in the same manner as explained for the transmitter, as well as flip-flop RFF2 and RFF3.

The timing circuit 37 provides the sample and shift pulses, referring to FIGURE 2b in conjunction with FIGURE 1b, RP11 to RP15 are the sample pulses and are timed to occur in the middle of their appropriate informa-

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tion bits. They open gates RG1 and RG2 to allow flip-flop RFF2 to be set to the state of the incoming signal according to the state of contact 30. RP21 to RP24 are the shift pulses and are always timed to occur later than the corresponding sample pulses.

RP32 shifts the fifth information bit, resets RFF1 via line 38 and energizes the 1.1 bit delay 39 which is coupled by capacitor 40 to gate RG5. The 1.1 bit delay determines the length of the fifth information bit and sets RFF3 via RG5 to one to provide for the stop signal. RP31 occurs at the beginning of the timing cycle and resets RFF3 to zero in order to provide the start signal.

As can be seen from FIGURE 2b, RFF1 and the timing circuit are reset immediately after the last bit is shifted out and the length of the fifth information bit is determined by the delay standard "D." This is done to insure proper operation of the circuit in case of signal distortion and frequency variation. The receiver will except character length variation of plus or minus .4 bit. The length variation of the character will effect the stop bit of the next character. This is caused by the bit standard delay "D."

A driver 41 is used to operate outgoing relay RB consisting of movable contact 42 and stationary contacts 43 and 44 respectively. The seven unit code output is then unsable with a standard page printer or tape perforator.

The timing circuit referenced in FIGURES 1a and 1b as 18 and 37 is shown in FIGURE 3. Since the timing circuit arrangement can be used for either the transmitter or the receiver the pulses P11 to P15, P21 to P25, and P31 and P32 do not have the prescript letters T or R, since the circuit may be used in either the receiver or the transmitter. In addition, prescripts P and R have been removed in reference gates G1, G2, G3 and G4, as well as flip-flops FF1 and FF3.

A start signal from FF1 to amplifier 45 which controls relay RS having a movable grounded contact 46. Prior to the opening of contact 46 by a start pulse from FF1, conductors 47 have been grounded through fixed resistor R40 and variable resistor R41. This common discharge path 47 for capacitors C11 to C15, C21 to C25, C31, and C32 is through their respective diodes D11 to D15, D21 to D25, D31 and D32. The common terminals 48 of the capacitors are grounded and as such the discharge path for each of the capacitors is from each common junction 49 through its individually connected isolated diodes via conductor 47, and then to ground through resistors R40 and R41. The capacitors quickly discharge substantially to a state of equilibrium, wherein a small residual charge potential remains across each of the capacitors, represented by the small potential drop across resistors R40 and R41, caused by the current flow through back bias resistors 50.

When contact 46 is opened due to a start pulse of FF1, the current flow on conductors 47 abruptly ceases and a reverse bias potential is placed on diodes D11 through D32, by virtue of the stabilized voltage source comprised of Zener diode Z-10 and resistor R10 connected to a source of positive potential. Uninterrupted charging current flow over conductor 51 to the capacitors is made through 12 respective resistor pairs, RV11 through RV32 being variable resistors, and R11 through R32 being fixed resistors. The individually paired resistors include a variable resistor and a fixed resistor and are serially connected to a respective common junction 49.

The capacitors immediately build up a potential which approaches the critical-potential value of one of its associated Zener diodes Z11 through Z32, each of the Zener diodes being connected to a respective common junction 49. As each critical-potential Zener diode starts to conduct, 1; transmits a control pulse over one of its associated pulse conductors P11 through P32 to respective amplifiers 52, 53, 54 and 55. The pulses produced in Zener diodes Z11 through Z15 in the timing sequence are transmitted to amplifier 52 which in turn according to FIGURES 1a and 1b is transmitted to gates G1 and G2. In a similar manner,

timing Zener diode Z31 transmits a pulse to amplifier 53 which in turn sets flip-flop FF3 to a reverse condition. Shift pulses P21 through P25 are produced by sequential firing of Z21 through Z25 and transmitted through amplifier 54 to control the gates G3 and G4. Finally, Zener diode Z32 produces pulse P32 which through amplifier 55 sets flip-flop FF1 to condition zero, to restart the timing cycle.

Since the supply voltage is determined by Z10 the timing pulses P11 through P32 may be adjusted by potentiometers RV11 through RV32, the setting of the individual variable resistors respectively sets the fine adjustment to the firing point of each of the individual Zener diodes Z11 through Z32. The individual adjustment of resistors produces relatively accurate timing because each pulse is independent from the other, and no accumulative error is possible. Timing for respective firing of individual diodes is according to the RC time constant.

In summary, when the timing circuit shown in FIGURE 3 is turned off by pulse T32 which sets flip-flop FF1 to condition zero, capacitors C11 through C32 are discharged through their associated diodes D11 through D32 and by means of conductor 47 through resistors R40 and R41 to ground. When the timing circuit is started by a start pulse to FF1 the ground on relay (RS) contact 46 is removed, diodes D11 through D32 are back biased by resistors R50 and the capacitors C11 through C32 charge through their associated resistors RV11 through RV32, and R11 through R32. The Zener diode Z10 and resistor R10 provide for a stabilized charging voltage from a source of positive potential. The Zener diodes Z11 through Z32 start to conduct according to the charging volts of the respective capacitor timing, as adjusted by potentiometers on RV11 to RV32, the pulses as amplified provide the output pulses P11 through P32 which control the enumerated gates and flip-flops. After the last pulse P32, the circuit is reset by applying a ground to contact 46 and discharging capacitor C11 to C32. The resistor R40 limits the discharge current to protect diodes D11 through D32. Variable resistor R41 is used to provide the correct speed of the timing circuit. Normally, when the signals come in at the right speed, a predetermined residual charge will remain on the capacitors in accordance with the value of R41. If the signals come in too slow, this residual charge will be increased, decreasing the timing of the pulses. Thus by means of R41 a speed correction can be obtained.

This arrangement using Zener diodes to produce the control pulses for sampling and shifting the incoming code to the transmitter and receiver FIGURE 1a and 1b, requires a few active components and is accomplished in a relatively inexpensive and simple manner.

While I have described above the principles of my invention in connection with specific apparatus it is to be clearly understood that this description is made only by way of example and not as a limitation to the scope of my invention, as set forth in the objects thereof and in the accompanying claims.

I claim:

1. A timing circuit for producing control pulses comprising:

- a separate timing branch for each of said control pulses;
- a critical-potential device in said branch;
- means for providing a potential to said device which is adjustable in time including a timing capacitor hav-

ing one terminal at ground, and an adjustable resistive arrangement connected to the other terminal of said capacitor to form a common junction and connected to a constant-potential current source to form a charging path of said capacitor;

said critical-potential device is connected to said junction to produce said control pulse when the potential on said capacitor has reached the critical-potential of said device;

a discharge diode is connected between said junction and a common discharge path;

a biasing resistor connects said discharge path to said constant-potential source; and

a timer-starting arrangement which applies said constant potential source to all of the timing circuit branches at the same starting instant including a relay having a movable grounded contact, and a limiting resistor and a speed correction resistor which are serially connected to said common discharge path and to said grounded contact when said relay is off;

whereby each circuit branch is arranged to reach the critical-potential of its critical-potential device at the end of a different predetermined timing interval from the starting instant.

2. A timing circuit according to claim 1 wherein said discharge diode is poled to pass capacitor-discharge current in its forward diode direction to said common discharge path, and during the charging of said capacitor, said discharge diode is back biased.

3. A timing circuit according to claim 2, wherein said speed correction resistor is variable to determine the residual charge on said capacitor, and said limiting resistor is fixed to limit the discharge current through said discharge diode, whereby said timing circuit is turned on by a first signal to said relay causing removal of the ground connection to said common discharge path, and a second signal to said relay applies the ground potential to said common discharge path to cause discharge of said timing capacitor.

4. A timing circuit according to claim 3, wherein said critical-potential device is a Zener diode, said Zener diode in the respective circuit branch producing one of said control pulses upon the critical-potential voltage being reached, and further including the use of an amplifier common to a series of Zener diodes whose corresponding control pulses are delivered to a common point.

5. A timing circuit according to claim 4 wherein said adjustable resistance arrangement comprises a fixed charging resistor and a variable charging resistor serially connected in the charging path of said capacitor, such that the interval required for said timing capacitor to reach the critical potential of said Zener diode is adjustable by adjustment of said variable charging resistor.

6. A timing circuit according to claim 5, wherein said constant-potential current source is the critical potential of a Zener power diode.

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