

Sept. 9, 1958

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2,851,598

CIRCUIT FOR GATING IN RESPONSE TO TIME DURATION

Filed Dec. 15, 1955

2 Sheets-Sheet 1

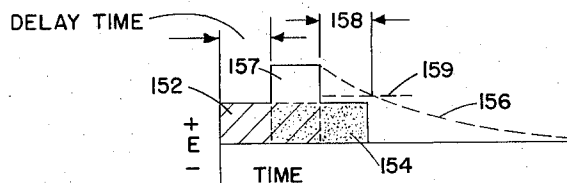


FIG. 4

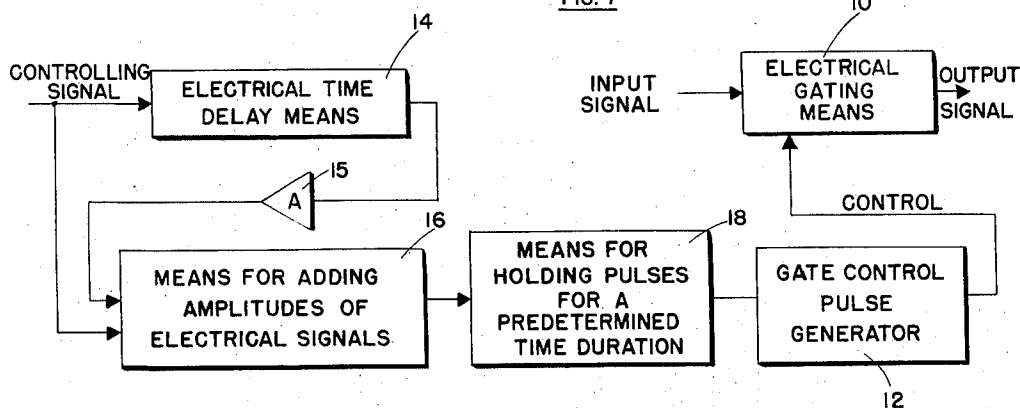


FIG. 1

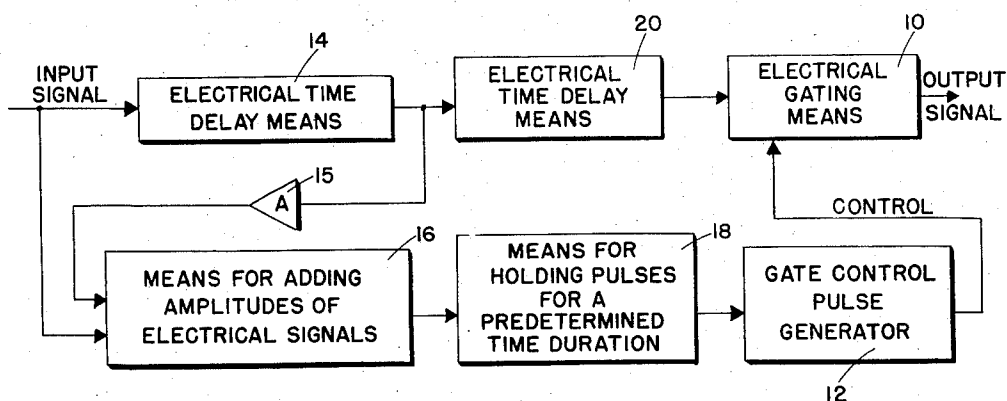


FIG. 2

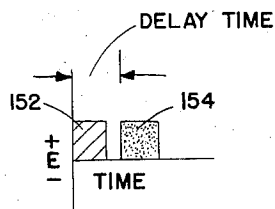


FIG. 5

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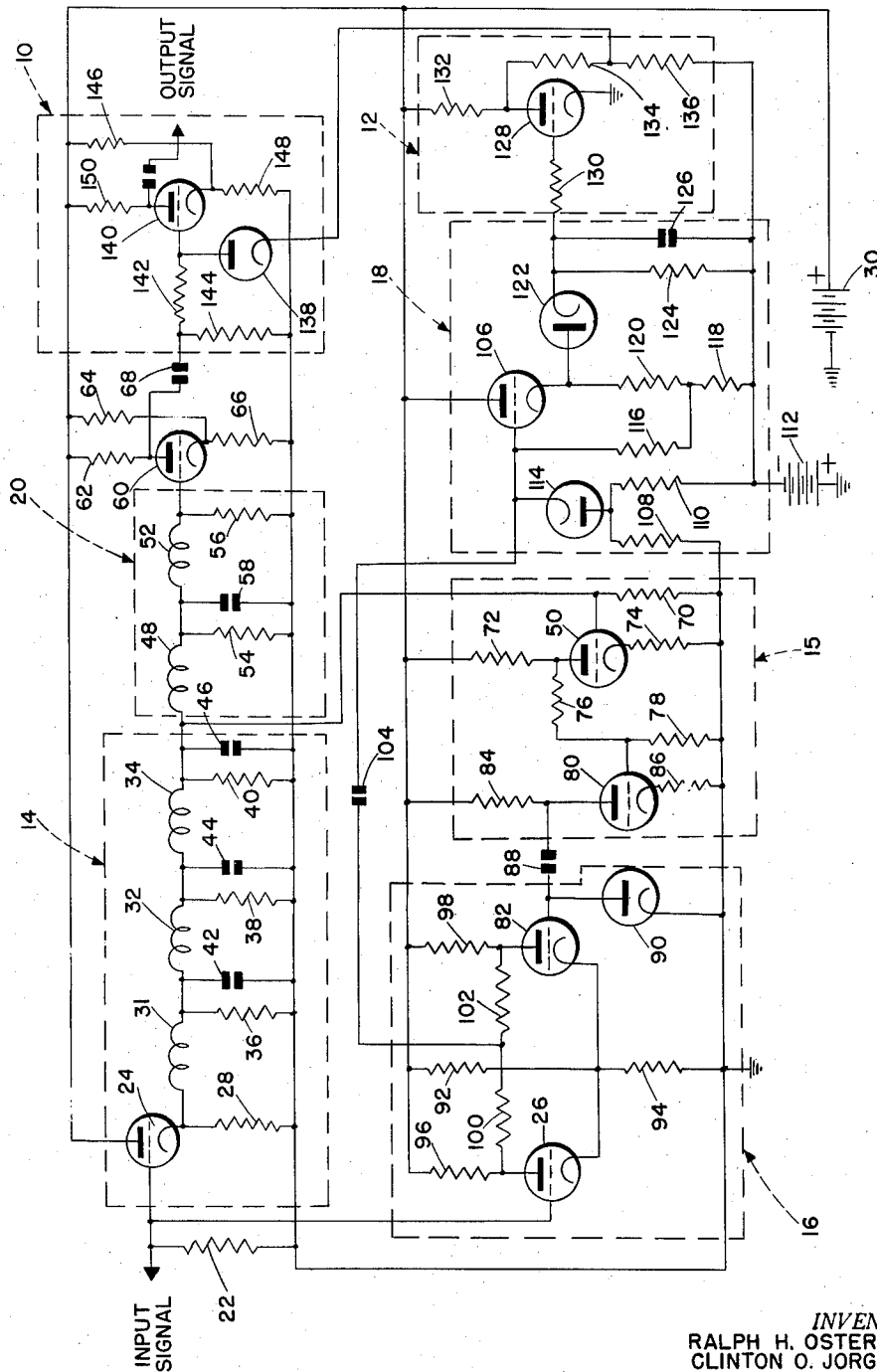
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CIRCUIT FOR GATING IN RESPONSE TO TIME DURATION

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Application December 15, 1955, Serial No. 553,240

2 Claims. (Cl. 250—27)

This invention pertains to a circuit adapted to gate electrical signals in accordance with the time duration of a given signal. The device of this invention may alternatively be designed to reject electrical signals which have a time duration less or greater than a predetermined length.

It is frequently necessary to reject electrical signals which have a time duration greater than a predetermined length or, alternatively, to reject all signals shorter than a predetermined length. For example, a signal of short-time duration is frequently intermingled with other electrical information or electrical noise of long-time duration. The device of this invention is easily adapted to reject the signal and noise of long-time duration while it passes the signal of short-time duration. In other instances the signal may be of long-time duration in the presence of other electrical information or electrical noise which is of short-time duration. The device of this invention is easily adapted to reject the signals and noise of short-time duration while it passes the signal of long-time duration.

In comparison, the device of the invention provides a gating system relatively free from distortion and relatively insensitive to variations in signal amplitude.

It is therefore an object of this invention to provide a means of gating according to the time duration of electrical signals.

It is another object of this invention to provide a means for rejecting electrical signals which have a time duration greater than a predetermined length.

It is another object of this invention to provide a means for rejecting electrical signals which have a time duration which is shorter than a predetermined length.

It is another object of this invention to provide means for selectively conducting and rejecting electrical signals in accordance with their time duration.

It is an object of this invention to pass desired signals with relatively little distortion.

It is still another object of this invention to provide a means responsive to the time duration of an electrical signal for gating.

Still another object of this invention is to provide a gating system relatively insensitive to variations in signal amplitude.

Other objects of invention will become apparent from the following description taken in connection with the accompanying drawings, in which

Fig. 1 is a block diagram of an embodiment of this invention;

Fig. 2 is a block diagram of a second embodiment of this invention;

Fig. 3 is a circuit diagram of a typical circuit of the device of Fig. 2;

Fig. 4 is a waveform produced in the circuit;

And Fig. 5 is another waveform produced in the circuit.

The device of this invention is shown generally in Fig. 1. An input signal is gated through electrical gat-

ing means 10 in accordance with the width of a controlling signal received at time delay means 14. Gating means 10 is controlled in response to a pulse from gate control pulse generator 12. Gate control pulse generator 12 may be adapted to either open or close electrical gating means 10 to control the passage of the input signal to the output of electrical gating means 10. Gate control pulse generator 12 generates pulses in response to a means for detecting the time duration of a controlling signal. The means for detecting the duration of a controlling signal comprises electrical time delay means 14, amplifier 15, means 16 for determining overlap, or coincidence, of the input signal and the delayed signal, and means for holding pulses for a predetermined time duration 18. When a controlling signal is received at the input to delay means 14, it is delayed for a predetermined time. The electrical output of delay means 14 is sent to amplifier 15 which is connected between delay means 14 and one of the inputs to means 16. The controlling signal is also connected directly to a second input to the means 16 for determining overlap between the delayed signal and the incoming signal. In this way, it can be determined if the duration of the incoming signal exceeds or is less than a predetermined value (the time delay of means 14). Means 16, a device having a sharp control characteristic, such as an easily saturable amplifier or a trigger circuit, provides a double amplitude signal if there is overlap and a single amplitude signal if there is no overlap with relative insensitivity to the incoming signal amplitude. The electrical output of means 16 is connected to the input of the means 18 for holding pulse voltage levels for a predetermined time duration. Element 18 is a means for preventing the pulsed voltage level from dropping below a predetermined value until after a predetermined time. In general, the time duration the pulses are held by element 18 is substantially equal to the time duration of the delay of electrical time delay means 14. The electrical output of element 18 is connected to the input of gate control pulse generator 12 to cause gate control pulse generator to generate a pulse when the amplitude of the electrical output of element 18 is double a given unit value, and no pulse when of single unit value. A unit value may, for example, be 40 volts, and double unit value may be 80 volts.

When a controlling signal which has a time duration that is longer than the delay of electrical time delay means 14 is introduced into means 14, the output of amplifier 15 causes a double amplitude pulse to appear at the output of element 16 when coincidence of input pulses occurs. It is generally preferable to adjust the gain of amplifier 15 primarily so that the amplitude losses in element 14 are compensated for and, thus, the amplitude of signals appearing at both inputs to element 16 are equal. The electrical output of element 16 is introduced into the input of element 18. Element 18 holds the signal if a double amplitude signal has been caused to occur. Hence, element 18 receives an original, actuating signal that is stretched or held for a predetermined time duration. Note that if the first signal, the input signal to resistor 22, is of sufficient pulse width as to still be present when the second or delayed signal is received at element 82, a double value pulse is provided during the interval of overlap. Single value pulses at the output of element 16 are provided if there is no overlap. The single and double amplitude pulses are of a relatively constant value and, in this case, are described to be of one and two unit value. Gate control pulse generator 12 is adapted to operate on a pulse and then lengthen or hold this pulse when the input signal thereto is greater than what has been termed a single value pulse.

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Fig. 2 is similar to Fig. 1 except that the input signal to electrical gating means 10 is also the controlling signal that appeared at the input of element 14, except it has been delayed. The signal is further delayed between elements 14 and 10 by electrical time delay means 20. Element 20 introduces an additional operational time delay which provides sufficient time for the gating pulse to be produced and appear at gating means 10.

When a signal is received at the input of element 14, which signal is shorter than the delay caused by electrical time delay 14, the signals at the two inputs of elements 16 arrive at different times and the output pulse never rises above a single unit value. Inasmuch as the pulse value never rises above this single unit value, the gate control pulse generator 12 never generates a gating pulse. Note that, inasmuch as the element 16 is operated into cut-off condition, the circuit operation is unaffected by input amplitude variations and provide unit pulses dependent only upon the time relationship of the two input signals.

It is desirable to correlate the gating signal and the signals to be received so that a desirable signal is allowed to pass through electrical gating means 10 without being cut off at either end. Conversely, an undesirable signal must be completely rejected without any part of the undesirable signal being allowed to pass the gating means 10. Also, the gate having once closed must immediately reopen so as to allow passage of a desired signal. Pulse holding means 18 and delay means 20 aid in accomplishing this objective. Alternatively, of course, once a gating signal is provided indicating whether the signal width is greater than a predetermined value, gating means 10 can be designed to be opened or closed by this signal. If gated open, the device is operating as a low-pass circuit. If gated closed, the device is operating as a high-pass circuit.

A typical circuit diagram of the device of Fig. 2 is shown in Fig. 3. It is to be noted that the same circuit would suffice to detail the block diagram of Fig. 1 by omitting element 20. The electrical input, or controlling signal (a negative signal) is introduced across resistor 22 between the grids of tubes 24 and 26 in parallel and the ground terminal. Vacuum tube 24 is connected by its cathode to resistor 28 to form a cathode follower circuit. The plate of tube 24 is connected to the positive terminal of voltage source 30. The cathode follower circuit comprising tube 24 and resistor 28 is desirable to provide the proper input impedance into the delay line of element 14 and still provide a high impedance input to the grid of tube 26. The delay line of element 14 is connected to the cathode of tube 24. The delay line represented by element 14 comprises a section of a typical cascade circuit comprised of many RLC sections. This is also referred to as an artificial transmission line and comprises, in this case, inductors 31, 32 and 34, resistors 36, 38 and 40, and condensers 42, 44 and 46, connected with the inductors in series and the resistors and condensers in shunt. Other delay devices, such as a mercury delay line, may be used. The output of time delay means 14 is connected to the junction between inductors 34 and 48. The electrical output of time delay means 14 is connected to the grid of tube 50 of amplifier 15. Time delay means 20 comprises inductors 48 and 52, resistors 54 and 56, and condenser 58, connected in cascade with the inductors in series and the resistors and condenser in shunt. Resistor 56 is connected between the junction of inductors 52 and the grid of vacuum tube 60 and the ground terminal. Vacuum tube 24 and its associated resistors form a limiter circuit preventing the amplitude of the input signal to time delay means 14 and 20 from being too great. In addition, vacuum tube 60 and its associated resistors act as a limiter to prevent the output of delay means 20 from being so great that electrical gating means 10 cannot control it. The limiting action provided by tube 60 is not always necessary. The electrical output of time delay means 20 could, in some instances, be connected directly to condenser 68 without a limiter be-

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tween, provided the reversal of polarity were compensated for properly. With the proper input amplitude range and proper band pass frequency characteristics in delay line components, relatively distortion-free signal passage is obtained. The cathode of tube 60 is maintained at a constant positive potential by a voltage dividing network comprising resistors 64 and 66 connected across the voltage source 30. Resistor 62 is connected to the positive terminal of voltage source 30. The limiting action of vacuum tube 60 occurs whenever the grid signal causes vacuum tube 60 to become saturated. Condenser 68 is connected to block D.-C. and couple A.-C. signals into gating means 10 and may alternatively be directly connected, as mentioned above, to the electrical output of time delay means 20. In the embodiment of Fig. 1, the input signal may be conveniently coupled directly into gating means 10 by means of condenser 68. The condenser 68 is selected to allow passage of the lowest frequency signal components desired. Of course, if D.-C. amplification and coupling is employed, the capacitors 68, 88 and 104 may be eliminated.

The electrical output of time delay means 14 is connected to the grid of tube 50 across biasing resistor 70. Tube 50 is an amplifier tube having a plate resistor 72 and cathode resistor 74. The electrical output of vacuum tube 50 is taken at the plate and comprises a voltage dividing network of resistors 76 and 78. The junction between resistors 76 and 78 is connected to the grid input of phase inverter and amplifying tube 80. The voltage dividing and biasing characteristics of resistors 76 and 78 determine the amplifying and operating characteristics respectively of tube 80 so that the amplitude of the signal impressed upon the grid of tube 82 is equal in amplitude to the voltage impressed upon the grid of tube 26. The plate of tube 80 is connected through resistor 84 to the positive terminal of voltage source 30 to provide space current thereto. The cathode of tube 80 is connected to resistor 86 which, in turn, is connected to the ground terminal. The electrical output of amplifier and phase inverter 80 appears across the load resistor 84 and is coupled into the grid of the tube 82 through coupling and blocking condenser 88. Diode 90, which may be either of a vacuum tube or appropriate semiconductor type, is connected between the grid of tube 82 and the ground terminal with the anode of the diode connected to the grid and the cathode of the diode connected to the ground terminal. Diode 90 is a D.-C. restorer which restores the charge to capacitor 88, which charge is lost during the pulse's duration. The diode 90 permits only negative pulses to be impressed on the grid of tube 82. A semiconductor is preferred for diode 90 so that its back resistance provides a grid return for tube 82. A vacuum diode would be satisfactory if shunted by a one or two megohm resistor. When a negative signal is impressed upon the grid of tube 82, diode 90 ceases to conduct allowing low frequencies to be coupled to tube 82. Capacitor 88 is presented a low impedance load during quiescent periods so that capacitor leakage effects on the bias of tube 82 are minimized. When no signal or when a positive signal is impressed upon the grid of tube 82, the grid is grounded through diode 90 and the signal is effectively blocked. The cathodes of tubes 26 and 82 are connected together and are maintained at a constant potential by virtue of their connection to a junction between voltage dividing resistors 92 and 94. Resistors 92 and 94 are connected across voltage source 30. The plate of tube 26 is connected through load resistor 96 to the positive terminal of voltage source 30. The plate of tube 82 is connected through resistor 98 to the positive terminal of voltage source 30. Resistors 100 and 102 are connected in series between the plates of tubes 26 and 82. The signal appearing at the junction between resistors 100 and 102 is, as would be expected, directly proportional to the sum of the voltages appearing upon the plates of tubes 26 and 82. However, both tubes 26

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and 82 are operated in conduction and driven to cutoff by even a minimum signal. Therefore, the output at the junction of resistors 100 and 102 is either single amplitude or double amplitude, depending on whether or not tube 82 provides a signal while the signal from tube 26 is still received. The essence of amplifier tubes 26 and 82 is to provide a sharp control characteristic.

Fig. 4 illustrates a waveform generated at the junction of resistors 100 and 102 as the combined output of tubes 26 and 82. If an incoming negative pulse is received at tube 26, the output to condenser 104 is a positive pulse 152 of the same width. If the incoming pulse is longer than the delay time of delay means 14, tube 82 will conduct and produce waveform 154 which, when added to waveform 152 at the junction of resistors 100 and 102, provides a double value pulse 157. If the incoming pulse is shorter than the delay time of delay means 14, Fig. 5 illustrates that a first pulse of single amplitude followed by a second pulse of single amplitude will be obtained. The two single value pulses do not cause devices 18 and 12 to provide a gating signal, while the double value pulses do by reason of the fact that diode 114 operates to positively clamp the grid of triode 106 and, by conduction of diode 122, holds the grid of tube 128 at the proper negative potential with respect to ground until a double value pulse is received which will cause tube 128 to go from cutoff to saturation. Double value pulse 157, Fig. 4, is obtained at capacitor 126, Fig. 3, and decays as shown by trailing edge 156. The decay time of the capacitor-resistor combination, 126 and 124, provides a means for holding pulses such as 157, a predetermined time 158 before decaying to the critical voltage 159 at which the grid of tube 128 begins to again cut off the plate current. Blocking diode 122, at the end of pulse 157, allows tube 106 to return to its quiescent condition and isolates the time determining components 124 and 126 so that waveform 156 will be applied to the grid of 128.

Inasmuch as tubes 26 and 82, Fig. 3, are operated in conduction and only small pulses are required to drive them to cutoff, amplitude modulation is removed from the pulses. The junction between resistors 100 and 102 is connected through coupling or blocking condenser 104 to the input of the pulse generating means and means for holding pulses for predetermined time duration 18. Condenser 104 is connected to the grid of vacuum tube 106. Resistors 108 and 110 are connected in series across voltage source 112 to form a voltage dividing network. The cathode of diode 114 is connected to the grid of tube 106, while the plate of diode 114 is connected to the junction between resistors 108 and 110. Diode 114 may alternatively be a tube or other appropriate type diode. Diode 114 is a direct current restorer which clamps the grid of tube 106 to a negative bias potential which is negative to the ground terminal. When a positive signal is received on the grid of tube 106, diode 114 is caused to stop conducting and the signal is allowed to control tube 106, but when no signal or when a negative signal is received on the grid of tube 106, it is effectively clamped by the action of diode 114. Diode 122 is conducting except during the short period during which waveform 156, Fig. 4, occurs following the negative-going edge of pulse 157. For the first one or two volts rise of the pulses, capacitor 104 is coupled into a relatively low impedance load, diode 114. For conditions existing above the first one or two volts of the pulses, capacitor 104 is coupled into a high impedance load, namely, the input impedance of tube 106 because the diode 114 is nonconducting. Tube 106 is part of a cathode follower circuit and, more particularly, a bootstrap cathode follower. The grid of tube 106 is connected through tube biasing and degenerative feedback resistors 116 and 118 in series to the negative terminal of voltage source 112 whose positive terminal is grounded. The cathode of tube 106 is connected through resistor 120 to the junction between resistors 116

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and 118 and also to the plate of blocking diode 122. The plate of tube 106 is connected to the positive terminal of voltage source 30 to provide space current thereto. The cathode follower circuit of tube 106 provides a high impedance load for optimum frequency response coupling through capacitor 104. It also provides a low impedance input through diode 122 to resistor 124 and condenser 126 so that condenser 126 can be charged rapidly. Note particularly that, while the input circuit to tube 106 need not supply an appreciable amount of current, the cathode circuit of tube 106 supplies considerable current to cause condenser 126 to charge rapidly. The cathode of diode 122 is connected to one terminal of the parallel combination of resistor 124 and condenser 126, while the other terminal of the parallel combination is connected to the negative terminal of voltage source 112. Resistor 130 is connected from the cathode of diode 122 to the grid of tube 128. Condenser 126 is charged to substantially the voltage which appears upon the cathode of tube 106. However, at the end of the pulse, when the pulse voltage which is upon the cathode of tube 106 drops below the voltage which is stored upon the plates of condenser 126, diode 122 ceases to conduct and condenser 126 holds the charge for a predetermined amount of time shown by line 156, Fig. 4, which largely depends upon the time constant of resistor 124, and capacitor 126 with the shunting value of resistor 130 connected to the grid which conducts during time 158, Fig. 4. This discharging time 158 is made equal to or slightly longer than the delay of time delay means 14. This is done so as to allow the off-gating pulse to last long enough to cut off all undesired signals. Note that, even though the discharge time constant of resistor 124 and capacitor 126 is appreciably long, the charging time constant is relatively short due to the low impedance of the cathode follower circuit of tube 106. Hence, the required operational time delay of means 20 is relatively short being principally equal to the time needed to charge capacitor 126. The voltage which appears on the plates of capacitor 126 also appears on the grid of tube 128 up to the level indicated as 159, Fig. 4, through resistor 130 which is inserted to prevent "loading" resistor-capacitor combination 124 and 126, and excessive grid current from flowing in tube 128. The cathode of tube 128 is grounded. The plate of tube 128 is connected through resistor 132 to the positive terminal of voltage source 30. As explained previously, tube 128 is biased by the clamping action of diode 114 so that when only a single amplitude signal is received from tubes 26 and 82, tube 128 does not conduct, but when tube 128 receives a double amplitude signal, tube 128 quickly saturates to full conduction between the cathode and plate causing the voltage upon the plate of tube 128 to drop. A voltage dividing network of resistors 134 and 136 is connected between the plate of tube 128 and the negative terminal of voltage source 112. The values of resistors 134 and 136 are selected so that the voltage which appears at the junction between them is sufficiently positive so that the positive signals from tube 60 do not cause tube 138 to conduct when tube 128 is not conducting and is negative by the same amount plus the value required to cutoff tube 140 when tube 128 is conducting. Hence, when tube 128 conducts, a negative pulse (the gating pulse) is generated at the junction of resistors 134 and 136. This pulse must be of sufficient amplitude to control any signal likely to be received at tube 140 within maximum allowed signal amplitudes. The junction between resistors 134 and 136 is connected to the cathode of diode 138 whose anode is connected to the grid of vacuum tube 140. Diode 138 may be either a tube or other appropriate type of diode. Condenser 68 is connected through resistor 142 to the grid of tube 140. Resistor 144 is connected to the junction between resistor 142 and condenser 68 and to the ground terminal to provide

a grid return for tube 140. When the cathode of tube 138 is driven negative relative to the anode, tube 140 is effectively driven to cutoff and the gate is closed. No signals pass through gating means 10 during this period. When the cathode of diode 138 is again driven positive, diode 138 does not conduct and the gate is opened. Signals are allowed to pass through gating means 10 during this period. The cathode of tube 140 is maintained at a fixed positive potential by connecting it to the junction between voltage dividing resistors 146 and 148 which are connected across voltage source 30. The plate of tube 140 is connected through load resistor 150 to the positive terminal of voltage source 30. If the gate is open and an input signal is received, tube 140 acts as an amplifier biased just below cutoff and the output signal, which is slightly base-clipped, then appears on the plate of tube 140.

As presently described and shown in Fig. 3, the circuit is adapted to receive negative pulses across resistor 22 at the input to vacuum tube 24 and 26. To adapt the circuit of Fig. 3 to receive a positive pulse across the resistor 22, it is necessary to change either tube 50 or 80 to a position between the input signal and tube 26 and add a phase inverter between tube 60 and capacitor 68. As presently shown in Fig. 3, electrical gating means 10 is adapted to close when a signal is introduced into time delay means 14, whose width is greater than an acceptable time duration determined by the delay of element 14. To adapt the circuit of Fig. 3 to open when a signal of greater than a given width is introduced, it is necessary that the gating pulse operate in a converse manner. One method to reverse this operating mode would entail the reversal of diode 138 and the reversal of blocking pulse polarity between tube 128 and resistor 134 by insertion, for example, of a phase-inverter. Tube 140 would then be operated well into cutoff and caused to become nearly conductive upon receipt of the gating signal to gate the signal through without distortion.

There has thus been described a novel means for controlling a gating circuit to cause the gate to open or close in response to the time duration of an input or controlling signal and, more particularly, when the entire circuit is connected as shown in Figs. 2 and 3 to alternatively allow signals to pass through the entire circuit when they are of a time duration shorter than a predetermined time duration, or by a simple alteration of the circuit to allow signals to pass through the circuits of this invention only when they are longer than a predetermined time duration.

Although the invention has been described and illustrated in detail, it is to be clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of this invention being limited only by the terms of the appended claims.

We claim:

1. Means for gating in response to the time duration of an incoming electrical signal comprising electrical signals in response to the time duration thereof comprising first delay means connected to receive an incoming electrical signal, a first amplifier connected to receive said delayed signal, a second amplifier connected to receive said incoming signal, said amplifiers operated in conduction and additively connected in output whereby a first value pulse is provided upon no overlap on said incoming signal and said delayed signal and a second value pulse is provided upon overlap of said incoming signal and said delayed signal, a gate control pulse generator having a connection to receive the output of said amplifiers and responsive only to said second value pulses, electrical gating means connected to be controlled by said gate control pulse generator, a second time delay means connected to receive said incoming signal and provide said signal to said electrical gating means and means included in the pulse generator for holding a signal for a time duration substantially equalling the predetermined time delay of the delay means to prevent the incoming signal from being cut off at either end.

2. Means for controlling an electrical gating circuit in response to the time duration of an electrical signal comprising an electrical delay device connected to receive said incoming signal, said device having predetermined time delay, a summing amplifier having at least two electrical input terminals, said summing amplifier connected to receive at one terminal said incoming signal and at said other terminal the output of said electrical delay device, said summing amplifier operated in a region of conduction and driven out of conduction by said signals, a resistor-capacitor network with unidirectional clamping means connected to receive the electrical output of said summing amplifier and adapted to be rapidly charged and slowly discharged over a time duration at least equal to the predetermined time duration of said delay device, pulse generating means connected to receive the output of said resistor-capacitor network, said pulse generator means biased to generate pulses when the voltage upon the capacitor of said resistor-capacitor network is above a predetermined amplitude, an electrical gating circuit connected to receive the output of said pulse generating means, a second time delay device connected to receive the output of said first time delay device, and said electrical gating circuit connected to receive the output of said second time delay device whereby said incoming signal is gated through said gating means according to its own time duration.

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