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Semiconductor device.

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Provided is a semiconductor device which can suppress a gate oscillation phenomenon which occurs at the time of switching off the semiconductor device while obviating the external connecting of a capacitance and a resistance between a gate and a drain of the semiconductor device. In a semiconductor device provided with a MOSFET part and a gate pad part, the gate pad part includes: a low resistance semiconductor layer 112; a drift layer 114; a poly-silicon layer 136 constituting a conductor layer and a gate pad electrode 138 formed above the drift layer 114 over the whole area of the gate pad part with a field insulation layer 134 interposed therebetween; and a gate oscillation suppressing structure 132, wherein the gate oscillation suppressing structure 132 includes a p⁺-type diffusion region 132a which is disposed along an outer peripheral portion of the gate pad part and is electrically connected with the a source electrode layer 128, and a p⁺-type diffusion region 132b in a floating state and the p-type impurity non-diffusion regions 132c, 132d which are alternately formed in the region surrounded by the p⁺-type diffusion region 132a.

TITLE OF THE INVENTIONS

Semiconductor device

Background of the Invention

5 1. Field of the Invention

[0001]

The present invention relates to a semiconductor device.

2. Description of the Related Art

10 [0002]

Conventionally, there has been known a semiconductor device where an active element part and a gate pad part are defined on a semiconductor substrate formed by laminating a drain layer (low resistance semiconductor layer) and a drift layer to each other (see Fig. 23 of JP-A-2005-150348 (patent literature 1), for example). Fig. 32A and Fig. 32B are views for explaining a conventional semiconductor device 800. Fig. 32A is a plan view showing an essential part of the semiconductor device 800, and Fig. 32B is a cross-sectional view taken along a line X-X in Fig. 32A.

[0003]

As shown in Fig. 32A and Fig. 32B, the conventional semiconductor device 800 is a semiconductor device provided with an active element part and a gate pad part defined on a semiconductor substrate which is formed by laminating an n^+ drain layer 51 and an n^- drift layer 52 to each other. As shown in Fig. 32B, the active element part includes: the n^+ drain layer 51; the n^- drift layer 52; p base regions 53 formed on a surface of the n^- drift layer 52; n^+ source regions 54 formed on surfaces of the p base regions 53; gate electrodes 57 formed on the p base regions 53 sandwiched between the n^+ source regions 54 and the n^- drift layer 52 with gate insulation films 56 interposed therebetween; and source electrodes 61 formed in contact with surfaces of the n^+ source regions 54 and the p base regions 53 in a state where the source electrodes 61 are insulated from the gate electrodes 57 with interlayer insulation films 58 interposed therebetween.

[0004]

On the other hand, as shown in Fig. 32B, the gate pad part includes: the n^+ drain layer 51, the n^- drift layer 52; a conductor 73 formed of a poly-silicon film formed above the n^- drift layer 52 over the whole area of the gate pad part with an interlayer insulation film 72 interposed therebetween; a gate pad electrode 62 formed on the conductor 73; and a p region 71 formed on the surface of the n^- drift layer 52 over the whole area of the gate pad part. In Fig. 32A and Fig. 32B, symbol 55 indicates a p^+ well region, symbol 59 indicates a source contact hole, symbol 60 indicates

a drain electrode, symbol 70 indicates a poly-silicon film, and symbol 74 indicates a p region contact hole.

[0005]

In the conventional semiconductor device 800, in the gate pad part, the p region 71 is formed on the surface of the n⁻ drift layer 52 over the whole area of the gate pad part. Accordingly, at the time of applying a reverse bias voltage, a depletion layer in the n⁻ drift layer 52 extends toward the n⁺ drain layer 51 over the whole area of the gate pad part thus providing a semiconductor device having a high breakdown strength.

10 Summary of the Invention

[0007]

However, in the conventional semiconductor device 800, due to a demand for a higher switching speed and higher micronizing of cells in recent years, it has become necessary to take into account a gate oscillation phenomenon (see Fig. 30C described later) which occurs at the time of switching off the semiconductor device 800. Conventionally, the gate oscillation phenomenon which occurs at the time of switching off the semiconductor device 800 is suppressed by externally connecting a capacitance and a resistance between the gate and the drain of the semiconductor device 800.

However, the external connecting of the capacitance and the resistance between the gate and the drain of the semiconductor device 800 brings about the increase of externally connected discrete parts and the increase of the number of steps for externally connecting the discrete parts.

[0008]

The present invention has been made in view of the above-mentioned circumstances, and it is an object of the present invention to provide a semiconductor device which can suppress a gate oscillation phenomenon which occurs at the time of switching off the semiconductor device while obviating the external connecting of a capacitance and a resistance between a gate and a drain of the semiconductor device.

[0009]

[1] According to a first aspect of the present invention, there is provided a semiconductor device provided with an active element part and a gate pad part defined on a semiconductor substrate which is formed by laminating a low resistance semiconductor layer of a first conductive type or a second conductive type and a drift layer of a first conductive type to each other, wherein the active element part includes: the low resistance semiconductor layer; the drift layer formed on the low resistance semiconductor layer; a base region of a second conductive type formed on a surface of the drift layer; a high concentration impurity diffusion region of a first conductive type formed on a surface of the base region; a gate electrode layer formed on the base region sandwiched between the

high concentration impurity diffusion region and the drift layer with a gate insulation layer interposed therebetween; and a first electrode layer formed in contact with a surface of the high concentration impurity diffusion region and a surface of the base region in a state where the first electrode layer is insulated from the gate electrode layer with an interlayer insulation layer

5 interposed therebetween, and the gate pad part includes: the low resistance semiconductor layer; the drift layer formed on the low resistance semiconductor layer; a conductor layer formed above the drift layer over the whole area of the gate pad part with a field insulation layer interposed therebetween; and a gate oscillation suppressing structure formed on a surface of the drift layer, wherein the gate oscillation suppressing structure includes: a first impurity diffusion region of a

10 second conductive type which is disposed along an outer peripheral portion of the gate pad part and is electrically connected with the first electrode layer, and a second impurity diffusion region of a second conductive type in a floating state and an impurity non-diffusion region of a second conductive type which are alternately formed in the region surrounded by the first impurity diffusion region of a second conductive type.

15 [0010]

[2] According to a second aspect of the present invention, there is provided a semiconductor device provided with an active element part and a gate pad part defined on a semiconductor substrate which is formed by laminating a low resistance semiconductor layer of a first conductive type or a second conductive type and a drift layer of a first conductive type to each

20 other, wherein the active element part includes: the low resistance semiconductor layer; the drift layer formed on the low resistance semiconductor layer; a base region of a second conductive type formed on a surface of the drift layer; a plurality of trenches formed such that the trenches open at the base region and reach the drift layer; a high concentration impurity diffusion region of a first conductive type arranged within the base region, exposing at least a portion thereof on inner

25 peripheral surfaces of the trenches; a gate insulation layer formed on the inner peripheral surfaces of the trenches; a gate electrode layer embedded into the inside of the trenches with the gate insulation layer interposed therebetween; and a first electrode layer formed in contact with a surface of the high concentration impurity diffusion region and a surface of the base region in a state where the first electrode layer is insulated from the gate electrode layer with an interlayer insulation layer

30 interposed therebetween, and the gate pad part includes: the low resistance semiconductor layer; the drift layer formed on the low resistance semiconductor layer; a conductor layer formed above the drift layer over the whole area of the gate pad part with a field insulation layer interposed therebetween; and a gate oscillation suppressing structure formed on a surface of the drift layer, wherein the gate oscillation suppressing structure includes: a first impurity diffusion region of a

35 second conductive type which is disposed along an outer peripheral portion of the gate pad part and is electrically connected with the first electrode layer and a second impurity diffusion region of a

second conductive type in a floating state and an impurity non-diffusion region of a second conductive type which are alternately formed in the region surrounded by the first impurity diffusion region of a second conductive type.

[0011]

5 [3] In the semiconductor device according to the present invention, it is preferable that the field insulation layer has a larger thickness than the gate insulation layer.

[0012]

[4] In the semiconductor device according to the present invention, it is preferable that the conductor layer is formed of a poly-silicon layer formed between the field insulation layer and a gate pad electrode layer formed over the field insulation layer.

10

[0013]

[5] In the semiconductor device according to the present invention, it is preferable that the conductor layer is a gate pad electrode layer formed over the field insulation layer.

[0014]

15 [6] In the semiconductor device according to the present invention, it is preferable that the conductor layer is electrically connected with the gate electrode layer via a gate finger part which connects the gate pad electrode layer and the gate electrode layer to each other, and no portion of the conductor layer is directly connected with the gate electrode layer without interposing the gate finger part therebetween.

20

[0015]

[7] In the semiconductor device according to the present invention, it is preferable that a cell arranged adjacent to the gate pad part has the structure where the high concentration impurity diffusion region on a gate pad part side is eliminated.

[0016]

25 [8] In the semiconductor device according to the present invention, it is preferable that a trench arranged adjacent to the gate pad part has the structure where the high concentration impurity diffusion region on a gate pad part side is eliminated.

[0017]

[9] In the semiconductor device according to the present invention, it is preferable that the active element part further includes a high concentration projecting diffusion region of a second conductive type which is formed in a downwardly projecting manner from the base region, and the first impurity diffusion region of a second conductive type and the second impurity diffusion region of a second conductive type are formed in the same step for forming the high concentration projecting diffusion region, and the first impurity diffusion region of a second conductive type is formed continuously with the high concentration projecting diffusion region.

35

[0018]

[10] In the semiconductor device according to the present invention, it is preferable that the first impurity diffusion region of a second conductive type and the second impurity diffusion region of a second conductive type are formed in the same step for forming the base region, and the first impurity diffusion region of a second conductive type is formed continuously with the base region.

[0019]

[11] In the semiconductor device according to the present invention, it is preferable that the active element part further includes a low concentration projecting diffusion region of a second conductive type which is formed in a downwardly projecting manner from the base region, and the first impurity diffusion region of a second conductive type and the second impurity diffusion region of a second conductive type are formed in the same step for forming the low concentration projecting diffusion region, and the first impurity diffusion region of a second conductive type is formed continuously with the low concentration projecting diffusion region.

[0020]

[12] In the semiconductor device according to the present invention, it is preferable that the first impurity diffusion region of a second conductive type and the second impurity diffusion region of a second conductive type are formed in the same step for forming a guard ring which is formed around the active element part.

[0021]

[13] In the semiconductor device according to the present invention, it is preferable that the first impurity diffusion region of a second conductive type and the second impurity diffusion region of a second conductive type are formed in the same step for forming the base region, and the first impurity diffusion region of a second conductive type is formed continuously with the base region.

[0022]

[14] In the semiconductor device according to the present invention, it is preferable that the active element part further includes a high concentration projecting diffusion region of a second conductive type which is formed in a downwardly projecting manner from the base region, and the first impurity diffusion region of a second conductive type and the second impurity diffusion region of a second conductive type are formed in the same step for forming the high concentration projecting diffusion region, and the first impurity diffusion region of a second conductive type is formed continuously with the high concentration projecting diffusion region.

[0023]

[15] In the semiconductor device according to the present invention, it is preferable that the second impurity diffusion region of a second conductive type is formed in a region surrounded by the first impurity diffusion region of a second conductive type, and the impurity non-diffusion region of

a second conductive type is formed in a stripe shape or an island shape inside the second impurity diffusion region of a second conductive type.

[0024]

[16] In the semiconductor device according to the present invention, it is preferable that the impurity non-diffusion region of a second conductive type is formed in a region surrounded by the first impurity diffusion region of a second conductive type, and the second impurity diffusion region of a second conductive type is formed in a stripe shape or an island shape inside impurity non-diffusion region of a second conductive type.

[0025]

[17] In the semiconductor device according to the present invention, it is preferable that the first impurity diffusion region of a second conductive type and the second impurity diffusion region of a second conductive type do not have a semiconductor region of a first conductive type therein.

[0026]

[18] In the semiconductor device according to the present invention, it is preferable that a gate finger part which connects the gate pad electrode layer and the gate electrode layer also has a gate oscillation suppressing structure where a third impurity diffusion region of a second conductive type electrically connected with the first electrode layer and a second impurity non-diffusion region of a second conductive type are alternately formed on the surface of the drift layer.

[0027]

In the semiconductor device of the present invention, “one region is continuously formed with another region different from the one region” means that “one region” is formed in a directly connected manner with “another region different from the one region” without interposing other layers therebetween.

Advantage of the Invention

[0028]

In the conventional semiconductor device 800, a gate-drain capacitance takes a value obtained by adding a capacitance of a capacitor C_1 formed in the gate pad part to a capacitance of a capacitor C_0 formed in the active element part (see the semiconductor device 100A shown in Fig. 3B described later). The capacitor C_1 formed in the gate pad part has the structure where “the conductor layer (a poly-silicon layer 136 in Fig. 3B) which constitutes one electrode”, “the field insulation layer 134 which constitutes a dielectric and the p^+ -type diffusion region 158” and “the drift layer 114 which constitutes another electrode” are laminated to each other.

[0029]

On the other hand, also in the semiconductor device of the present invention, a gate-drain capacitance takes a value obtained by adding capacitances of capacitors C_2 , C_3 formed in the gate

pad part to a capacitance of the capacitor C_0 formed in the active element part (see the semiconductor device 100 shown in Fig. 3A described later). In such a constitution, the capacitor C_2 is a capacitor formed in a region where the first impurity diffusion region of a second conductive type and the second impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132a and the p^+ -type diffusion region 132b in Fig. 3A) are formed on a surface of the drift layer. The capacitor C_2 is formed of: “the conductor layer (the poly-silicon layer 136 in Fig. 3A) which constitutes one electrode”; “the field insulation layer (the field insulation layer 134 in Fig. 3A) which constitutes a dielectric and the impurity diffusion region of a second conductive type (the first impurity diffusion region of a second conductive type and the second impurity diffusion region of a second conductive type)(the p^+ -type diffusion region 132a and p^+ -type diffusion region 132b in Fig. 3A)”; and “a drift layer (a drift layer 114 in Fig. 3A) which constitutes another electrode”. The capacitor C_3 is a capacitor formed in the impurity non-diffusion region of a second conductive type (the p-type impurity non-diffusion regions 132c, 132d in Fig. 3A) on a surface of the drift layer. The capacitor C_3 is formed of: “a conductor layer (the poly-silicon layer 136 in Fig. 3A) which constitutes one electrode”; “the field insulation layer (the field insulation layer 134 in Fig. 3A) which constitutes a dielectric”; and “a drift layer (the drift layer 114 in Fig. 3A) which constitutes another electrode”.

[0030]

In the semiconductor device of the present invention, usually, the field insulation layer is formed extremely thin compared with the p region 71 (Fig. 32B) and the p^+ -type diffusion region 158 (see Fig. 3B) in the conventional semiconductor device (field insulation layer: 200nm to 500nm, p region 71, p^+ -type diffusion region 158: 2.4 μ m to 8.0 μ m). Among the capacitors C_1 , C_2 and C_3 , the capacitance of the capacitor C_3 is extremely increased. As a result, the gate-drain capacitance C_{rds} of the semiconductor device of the present invention becomes larger than the gate-drain capacitance C_{rds} of the conventional semiconductor device.

[0031]

In the semiconductor device of the present invention, the narrow region sandwiched by the impurity diffusion regions of a second conductive type which are disposed adjacent to each other on the surface of the drift layer (the region sandwiched between the first impurity non-diffusion region of a second conductive type and the second impurity non-diffusion region of a second conductive type (p^+ -type non-diffusion region 132c sandwiched between the p^+ -type diffusion region 132a and the p^+ -type diffusion region 132b in Fig. 3A) and the narrow region sandwiched by the second impurity diffusion regions of a second conductive type which are disposed adjacent to each other (p^+ -type non-diffusion region 132d sandwiched between the p^+ -type diffusion regions 132d which are arranged adjacent to each other in Fig. 3A) form a current path (see Fig. 3A described later). Further, in the current path, at the time of switching off the semiconductor device, a depletion layer

spreads toward a drift layer side from the impurity diffusion region of a second conductive type (the first impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132a) and the second impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132b)) (see Fig. 4A to Fig. 4E described later) and hence, a resistance having a relatively large resistance value (see a resistance R3 in Fig. 3A described later) is formed in the above-mentioned narrow regions.

[0032]

As a result, in the semiconductor device of the present invention, a large capacitance and a large resistance can be formed between the gate and the drain and hence, it is possible to suppress a gate oscillation phenomenon which occurs at the time of switching off the semiconductor device without externally connecting the capacitance and the resistance between the gate and the drain.

[0033]

The second impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132b in Fig. 3A) is in a floating state and hence, at the time of applying a reverse bias voltage, it is usually considered that a depletion layer does not spread toward a drift layer side from the second impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132b in Fig. 3A). However, as shown in Fig. 4A to Fig. 4C described later, in the semiconductor device of the present invention, at the time of applying a reverse bias voltage, in the course that a depletion layer “d” spreads toward the drift layer side from the first impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132a in Fig. 3A) electrically connected with the first electrode layer (the source electrode layer 128 in Fig. 3A), the depletion layer “d” spreading from the first impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132a in Fig. 3A) is brought into contact with the second impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132b in Fig. 3A). Accordingly, a potential of the second impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132b in Fig. 3A) becomes equal to a potential of the first impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132a in Fig. 3A) and, thereafter, as shown in Fig. 4C to Fig. 4E described later, a depletion layer spreads to the drift layer side also from the second impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132b in Fig. 3A).

[0034]

In the semiconductor device of the present invention, the gate pad part is provided with the gate oscillation suppressing structure which includes: the first impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132a in Fig. 3A) which is disposed along an outer peripheral portion of the gate pad part and electrically connected with the first electrode layer; and the second impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132b in Fig. 3A) in a floating state and the impurity non-diffusion regions of a second conductive type (the

p-type impurity non-diffusion regions 132c, 132d in Fig. 3A) which are alternately formed in a region surrounded by the first impurity diffusion region of a second conductive type. Accordingly, as shown in Fig. 4A to Fig. 4E described later, at the time of applying a reverse bias voltage, the respective depletion layers extend in the lateral direction, and are brought into contact with each other, and extend toward the low resistance semiconductor layer 112 over the whole area of the gate pad part. Accordingly, in the same manner as the conventional semiconductor device 800, the present invention can provide a semiconductor device having a high breakdown strength.

[0035]

In the conventional semiconductor device 800, the p region 71 is formed over the whole area of the gate pad part and hence, a pn junction area is large and a carrier injection amount at the time of switching off the semiconductor device 800 is also increased. Accordingly, the conventional semiconductor device 800 has a drawback that a reverse recovery period t_{rr} extends and also has a drawback that a reverse recovery peak current IPR is increased. To the contrary, in the semiconductor device of the present invention, the gate pad part is provided with the gate oscillation suppressing structure which includes: the first impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132a in Fig. 3A) which is disposed along an outer peripheral portion of the gate pad part and is electrically connected with the first electrode layer; and the second impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132b in Fig. 3A) in a floating state and the impurity non-diffusion region of a second conductive type (the p-type impurity non-diffusion regions 132c, 132d in Fig. 3A) which are alternately formed in the region surrounded by the first impurity diffusion region of a second conductive type. Accordingly, a pn junction area is small and a carrier injection amount at the time of switching off the semiconductor device is also decreased. Accordingly, the semiconductor device of the present invention has an advantage that a reverse recovery period t_{rr} becomes short and also has an advantage that a reverse recovery peak current IPR is decreased. Further, according to the semiconductor device of the present invention, the second impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132b in Fig. 3A) of the gate pad part is in a floating state and hence, compared to the case where the second impurity diffusion region of a second conductive type of the gate pad part is not in a floating state, an area of the impurity diffusion region of a second conductive type where the impurity diffusion region functions as a body diode is decreased, and an amount of injecting carrier at the time of switching off the semiconductor device is also decreased. As a result, a reverse recovery period t_{rr} becomes shorter and hence, a di/dt resistance can be increased.

[0036]

Patent literature 1 discloses the semiconductor device in which a cell formed of a MOSFET is incorporated also in the gate pad part (see Fig. 1A and Fig. 1B in patent literature 1). Assume

such a semiconductor device as a second conventional semiconductor device. It is considered that the second conventional semiconductor device can also provide a semiconductor device having a large gate-drain capacitance compared with the conventional semiconductor device 800.

[0037]

5 However, in the second conventional semiconductor device, usually, a rate of an area of a drift region which faces a gate electrode layer in an opposed manner with a gate insulation layer interposed therebetween is small. Accordingly, a gate-drain capacitance increasing effect which the second conventional semiconductor device possesses is small compared with a gate-drain capacitance increasing effect which the semiconductor device of the present invention possesses.

10 In an actual operation, the second conventional semiconductor device exhibits a small effect of suppressing a gate oscillation phenomenon at the time of switching off the semiconductor device.

[0038]

 Further, in the second conventional semiconductor device, a MOSFET of the gate pad part performs the same operation in parallel as a MOSFET of an active element part and hence, the
15 second conventional semiconductor device cannot acquire an effect of preventing a gate oscillation phenomenon at the time of switching off the semiconductor device.

[0039]

 Further, in the second conventional semiconductor device, when an avalanche breakdown occurs in a region just below the gate pad part, an avalanche current flows a long distance from the
20 region just below the gate pad part to a source electrode layer of the active element part. Accordingly, a parasitic transistor is liable to be operated at a peripheral end of the gate pad part thus giving rise to cause breaking of the MOSFET.

[0040]

 There has been known a semiconductor device where a p well layer is formed in a ring
25 shape in a lower portion of a gate pad part (see JP-A-5-167070, for example). Assume such a semiconductor device as a third conventional semiconductor device 900. Fig. 33 is a cross-sectional view of the third conventional semiconductor device 900.

[0041]

 As shown in Fig. 33, the third conventional semiconductor device 900 is a semiconductor
30 device provided with an active element part and a gate pad part defined on a semiconductor substrate which is formed by laminating an n^+ drain layer (not shown in the drawings) and the n^- drift layer 901 to each other. As shown in Fig. 33, the active element part includes: the n^+ drain layer (not shown in the drawing); the n^- drift layer 901; p base regions 902 formed on a surface of the n^- drift layer 901; n^+ source regions 903 formed on surfaces of the p base regions 902; gate electrodes 905 formed on the
35 p base regions 902 sandwiched between the n^+ source regions 903 and the n^- drift layer 901 with gate insulation films 904 interposed therebetween; and source electrodes 908 formed in contact with

surfaces of the n^+ source regions 903 and the p base regions 902 in a state where the source electrodes 908 are insulated from the gate electrodes 905 with interlayer insulation films 906 interposed therebetween.

[0042]

5 On the other hand, as shown in Fig. 33, the gate pad part includes: the n^+ drain layer (not shown in the drawing), the n^- drift layer 901; a conductor 911 formed of a poly-silicon film formed above the n^- drift layer 901 over the whole area of the gate pad part with a field insulation layer 910 interposed therebetween; gate pad electrodes 907 formed on the conductor 911; and a p well layer 919 formed in the lower portion of the gate pad part in a ring shape.

10 [0043]

 However, in the third conventional semiconductor device 900, to possess a larger breakdown strength than the conventional semiconductor devices (the conventional semiconductor device 800, the semiconductor device described in Fig. 3 of JP-A-5-167070) at the time of switching off the semiconductor device, a capacitance of a parasitic diode below the gate pad part is set small.

15 Further, in the third conventional semiconductor device 900, the p well layer 919 is not formed at the center portion of the gate pad part and hence, a value of a resistance R3 formed at the center portion of the gate pad part becomes small. Accordingly, the third conventional semiconductor device 900, unlike the present invention, cannot suppress a gate oscillation which occurs at the time of switching off the semiconductor device.

20 [0044]

 Further, in the third conventional semiconductor device 900, the p well layer 919 is formed in the lower portion of the gate pad part in a ring shape. That is, the p well layer 919 is not formed at the center portion of the gate pad part (see Fig. 5B described later) and hence, there also arises a drawback that an effect of making the spreading of a depletion layer in the lower portion of the gate pad part at the time of applying a reverse bias voltage stable is decreased.

25 [0045]

 To the contrary, the semiconductor device of the present invention is provided with the gate oscillation suppressing structure (the gate oscillation suppressing structure 132 shown in Fig. 3A) which includes: the first impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132a in Fig. 3A) which is disposed along the outer peripheral portion of the gate pad part and is electrically connected with the first electrode layer; and the second impurity diffusion region of a second conductive type (the p^+ -type diffusion region 132b in Fig. 3A) in a floating state and the impurity non-diffusion region of a second conductive type (the p-type impurity non-diffusion regions 132c, 132d in Fig. 3A) which are alternately formed in the region surrounded

30 by the first impurity diffusion region of a second conductive type. According to the semiconductor

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device of the present invention, the above-mentioned drawback that the third conventional semiconductor device 900 has does not arise.

[0046]

Further, in the third conventional semiconductor device 900, the p well layer 919 formed in the lower portion of the gate pad part is not connected to the source electrode and hence, a depletion layer does not extend in a region where the p well layer 919 is not formed at the time of applying a reverse bias voltage and hence, a field intensity is not decreased whereby a breakdown strength is decreased.

[0047]

To the contrary, the semiconductor device of the present invention is provided with the gate oscillation suppressing structure (the gate oscillation suppressing structure 132 shown in Fig. 3A) which includes: the first impurity diffusion region of a second conductive type (the p⁺-type diffusion region 132a in Fig. 3A) which is disposed along the outer peripheral portion of the gate pad part and is electrically connected with the first electrode layer; and the second impurity diffusion region of a second conductive type (the p-type impurity diffusion region 132b in Fig. 3A) in a floating state and the impurity non-diffusion regions of a second conductive type (the p-type impurity non-diffusion regions 132c, 132d in Fig. 3A) which are alternately formed in the region surrounded by the first impurity diffusion region of a second conductive type. According to the semiconductor device of the present invention, the above-mentioned drawback that the third conventional semiconductor device 900 has does not arise.

Brief Description of Drawings

[0048]

Fig. 1A and Fig. 1B are views for explaining a semiconductor device 100 according to a first embodiment;

Fig. 2A and Fig. 2B are views for explaining the semiconductor device 100 according to the first embodiment;

Fig. 3A and Fig. 3B are views for explaining an advantageous effect acquired by the semiconductor device 100 according to the first embodiment;

Fig. 4A to Fig. 4E are views for explaining an advantageous effect acquired by the semiconductor device 100 according to the first embodiment;

Fig. 5A and Fig. 5B are views for explaining an advantageous effect acquired by the semiconductor device 100 according to the first embodiment;

Fig. 6A to Fig. 6C are views for explaining a method of manufacturing the semiconductor device according to the first embodiment;

Fig. 7A to Fig. 7C are views for explaining the method of manufacturing the semiconductor device according to the first embodiment;

Fig. 8A to Fig. 8C are views for explaining the method of manufacturing the semiconductor device according to the first embodiment;

5 Fig. 9A to Fig. 9C are views for explaining the method of manufacturing the semiconductor device according to the first embodiment;

Fig. 10A to Fig. 10C are views for explaining the method of manufacturing the semiconductor device according to the first embodiment;

10 Fig. 11 is a view for explaining a semiconductor device 100a according to a second embodiment;

Fig. 12 is a view for explaining a semiconductor device 100b according to a third embodiment;

Fig. 13 is a view for explaining a semiconductor device 100c according to a fourth embodiment;

15 Fig. 14 is a view for explaining a semiconductor device 100d according to a fifth embodiment;

Fig. 15 is a cross-sectional view of a semiconductor device 100e according to a sixth embodiment;

20 Fig. 16 is a cross-sectional view of a semiconductor device 100f according to a seventh embodiment;

Fig. 17A and Fig. 17B are views for explaining a semiconductor device 100g according to an eighth embodiment;

Fig. 18 is a cross-sectional view of a semiconductor device 100h according to a ninth embodiment;

25 Fig. 19 is a cross-sectional view of a semiconductor device 100i according to a tenth embodiment;

Fig. 20A and Fig. 20B are cross-sectional views of a semiconductor device 100j according to an eleventh embodiment;

30 Fig. 21A to Fig. 21C are views for explaining a method of manufacturing the semiconductor device according to the eleventh embodiment;

Fig. 22A and Fig. 22B are cross-sectional views of a semiconductor device 100k according to a twelfth embodiment;

Fig. 23 is a cross-sectional view of a semiconductor device 200 according to a thirteenth embodiment;

35 Fig. 24 is a cross-sectional view of a semiconductor device 200a according to a fourteenth embodiment;

Fig. 25 is a cross-sectional view of a semiconductor device 200b according to a fifteenth embodiment;

Fig. 26 is a cross-sectional view of a semiconductor device 300 according to a sixteenth embodiment;

5 Fig. 27A and Fig. 27B are views for explaining a semiconductor device 100l according to a seventeenth embodiment;

Fig. 28A and Fig. 28B are cross-sectional views of the semiconductor devices 100i, 100C used for test examples 1 and 2;

Fig. 29A to Fig. 29C are views for explaining an evaluation result in the test example 1;

10 Fig. 30A to Fig. 30C are views for explaining an evaluation method and an evaluation result in the test example 2;

Fig. 31 is a plan view of a semiconductor device 100m according to a modification;

Fig. 32A and Fig. 32B are views for explaining a conventional semiconductor device 800; and

15 Fig. 33 is a view for explaining a conventional semiconductor device 900.

Description of Preferred Embodiments

[0049]

20 Hereinafter, a semiconductor device according to the present invention is explained in conjunction with embodiments shown in the drawings.

[0050]

[Embodiment 1]

1. Semiconductor device 100 according to the embodiment 1

25 Fig. 1A and Fig. 1B and Fig. 2A and Fig. 2B are views for explaining a semiconductor device 100 according to an embodiment 1. Fig. 1A is a plan view of the semiconductor device 100, and Fig. 1B is a cross-sectional view taken along a line A1-A1 in Fig. 1A. Fig. 2A is a plan view of the semiconductor device 100, and Fig. 2B is a cross-sectional view taken along a line A2-A2 in Fig. 2A. In Fig. 1A, only a profile line (indicated by a chain line) is indicated with respect to p⁺-type projecting diffusion regions 118, p⁺-type diffusion regions 132a, 132b, 162, p-type impurity non-diffusion regions 132c, 132d, a gate oscillation suppressing structure 132 and a source electrode layer 128. In Fig. 2A, only a profile line (indicated by a chain line) is indicated with respect to the poly-silicon layer 136 and the source electrode layer 128. In Fig. 1A, the p⁺-type projecting diffusion regions 118 and the p⁺-type diffusion regions 132a, 132b, 162 are indicated by a dot pattern. In Fig. 1B, the p⁺-type projecting diffusion regions 118 and the p⁺-type diffusion regions 132a, 132b are indicated by an outlined pattern. In Fig. 1B and Fig. 2B, symbol 130 indicates a drain electrode layer.

35

[0051]

As shown in Fig. 1A and Fig. 1B, the semiconductor device 100 according to the embodiment 1 is a semiconductor device (a power MOSFET) which is provided with a MOSFET part (corresponding to an active element part of the present invention), a gate pad part and a gate finger part defined on a semiconductor substrate 110 which is formed by laminating an n⁺-type low resistance semiconductor layer 112 and an n⁻-type drift layer 114 to each other.

[0052]

As shown in Fig. 1B, the MOSFET part includes: the low resistance semiconductor layer 112; the drift layer 114 formed on the low resistance semiconductor layer 112; p-type base regions 116 formed on a surface of the drift layer 114; n⁺-type source regions (high concentration impurity diffusion regions) 120 formed on surfaces of the base regions 116; gate electrode layers 124 formed on the base regions 116 sandwiched between the source regions 120 and the drift layer 114 with a gate insulation layer 122 interposed therebetween; and the source electrode layer 128 (corresponding to a first electrode layer of the present invention) formed in contact with the surfaces of the source regions 120 and the base regions 116 in a state where the source electrode layer 128 is insulated from the gate electrode layers 124 with an interlayer insulation layer 126 interposed therebetween.

[0053]

As shown in Fig. 1B, the gate pad part includes: the low resistance semiconductor layer 112; the drift layer 114 formed on the low resistance semiconductor layer 112; the poly-silicon layer 136 which constitutes a conductor layer and is formed above the drift layer 114 over the whole area of the gate pad part with a field insulation layer 134 interposed therebetween; and the gate oscillation suppressing structure 132 formed on a surface of the drift layer 114, wherein the gate oscillation suppressing structure 132 includes: the p⁺-type diffusion region 132a (corresponding to the first impurity diffusion region of a second conductive type of the present invention) which is disposed along an outer peripheral portion of the gate pad part in an annular manner and is electrically connected with the source electrode layer 128; and the p⁺-type diffusion region 132b (corresponding to the second impurity diffusion region of a second conductive type of the present invention) in a floating state and the p-type impurity non-diffusion regions 132c, 132d (corresponding to the impurity non-diffusion regions of a second conductive type of the present invention) which are alternately formed in the region surrounded by the p⁺-type diffusion region 132a. The p⁺-type diffusion regions 132a are electrically connected with the source electrode layer 128 via the p⁺-type projecting diffusion regions 118.

[0054]

In the embodiment 1 and embodiments 2 to 17 described later, the p⁺-type diffusion regions, the p-type diffusion regions and the p⁻-type diffusion regions correspond to the first or the second conductive type impurity diffusion regions of a second conductive type, and the p-type

impurity non-diffusion regions correspond to the impurity non-diffusion regions of a second conductive type.

[0055]

As shown in Fig. 2B, the gate finger part includes: the low resistance semiconductor layer 112; the drift layer 114 formed on the low resistance semiconductor layer 112; the poly-silicon layer 136 formed above the drift layer 114 over the whole area of the gate finger part with the field insulation layer 134 interposed therebetween; and the p⁺-type diffusion region 162 (corresponding to the third impurity diffusion region of a second conductive type of the present invention) formed on the whole surface of the drift layer 114. The p⁺-type diffusion region 162 is electrically connected with the source electrode layer 128 via the p⁺-type projecting diffusion regions 118.

[0056]

In the semiconductor device 100 according to the embodiment 1, as shown in Fig. 1B, in the gate pad part, the interlayer insulation layer 126 is formed on the poly-silicon layer 136, and a gate pad electrode layer 138 is formed on the interlayer insulation layer 126. The poly-silicon layer 136 and the gate pad electrode layer 138 are electrically connected with each other via a through hole 140 formed in the interlayer insulation layer 126.

[0057]

In the semiconductor device 100 according to the embodiment 1, as shown in Fig. 2B, in the gate finger part, the interlayer insulation layer 126 is formed on the poly-silicon layer 136, and a gate finger line layer 142 is formed on the interlayer insulation layer 126. The poly-silicon layer 136 and the gate finger line layer 142 are electrically connected with each other via the through hole 140 formed in the interlayer insulation layer 126.

[0058]

In the semiconductor device 100 according to the embodiment 1, the poly-silicon layer 136 is electrically connected with the gate electrode layer 124 via the gate finger part which connects the gate pad electrode layer 138 and the gate electrode layer 124 to each other, and no portion of the poly-silicon layer 136 is directly connected with the gate electrode layer 124 without interposing the gate finger part therebetween (see a portion indicated by symbol D in Fig. 2A).

[0059]

In the semiconductor device 100 according to the embodiment 1, the p⁺-type diffusion region 132b is formed in the region surrounded by the p⁺-type diffusion region 132a, and the p-type impurity non-diffusion regions 132d are formed in a stripe shape inside the p⁺-type diffusion region 132b. The p⁺-type diffusion region 132b is formed in a stripe shape such that both ends of the p⁺-type diffusion region 132b are connected to each other so as to surround each p-type impurity non-diffusion region 132d.

[0060]

The semiconductor device 100 according to the embodiment 1 has the structure where the source region 120 (corresponding to the high concentration impurity diffusion region of the first conductive type of the present invention) on a gate pad part side is eliminated in a cell adjacent to the gate pad part (see a portion indicated by symbol B in Fig. 5A and Fig. 5B described later).

5 [0061]

In the semiconductor device 100 according to the embodiment 1, the MOSFET part further includes the p⁺-type projecting diffusion regions 118 formed in a downwardly projecting manner (in the depth direction) from the base regions 116. The p⁺-type diffusion regions 132a, 132b in the gate pad part are formed in the same step for forming the p⁺-type projecting diffusion regions 118 in the MOSFET part and the p⁺-type diffusion regions 162 in the gate finger part, and the p⁺-type diffusion regions 132a in the gate pad part are also formed continuously with the p⁺-type projecting diffusion regions 118 in the MOSFET part and the p⁺-type diffusion region 162 in the gate finger part.

[0062]

In the semiconductor device 100 according to the embodiment 1, the p⁺-type diffusion regions 132a, 132b do not include an n-type semiconductor region therein.

15 [0063]

In the semiconductor device 100 according to the embodiment 1, a ratio of an area of a portion in the gate pad part where the poly-silicon layer 136 which constitutes the conductor layer faces the drift layer 114 in an opposed manner with the field insulation layer 134 interposed therebetween to an area of the whole gate pad part is set larger than a ratio of an area of a portion in the MOSFET part where the gate electrode layer 124 faces the drift layer 114 in an opposed manner with the gate insulation layer 122 interposed therebetween to an area of the whole MOSFET part.

[0064]

A thickness of the low resistance semiconductor layer 112 is set to 100μm to 400μm, and an impurity concentration in the low resistance semiconductor layer 112 is set to $1 \times 10^{19} \text{cm}^{-3}$ to $1 \times 10^{20} \text{cm}^{-3}$. A thickness of the drift layer 114 is set to 5μm to 50μm, and an impurity concentration in the drift layer 114 is set to $1 \times 10^{14} \text{cm}^{-3}$ to $1 \times 10^{16} \text{cm}^{-3}$. A depth of the base region 116 is set to 2μm to 2.5μm, and an impurity concentration in the base region 116 is set to $5 \times 10^{16} \text{cm}^{-3}$ to $1 \times 10^{18} \text{cm}^{-3}$. A depth of the source region 120 is set to 0.2μm to 0.4μm, and an impurity concentration in the source region 120 is set to $5 \times 10^{19} \text{cm}^{-3}$ to $2 \times 10^{20} \text{cm}^{-3}$. A depth of the p⁺-type projecting diffusion region 118 is set to 2.4μm to 8.0μm, and an impurity concentration in the p⁺-type projecting diffusion region 118 is set to $1 \times 10^{17} \text{cm}^{-3}$ to $3 \times 10^{18} \text{cm}^{-3}$. A depth of the p⁺-type diffusion regions 132a, 132b is set to 2.4μm to 8.0μm, and an impurity concentration in the p⁺-type diffusion regions 132a, 132b is set to $1 \times 10^{17} \text{cm}^{-3}$ to $3 \times 10^{18} \text{cm}^{-3}$.

35 [0065]

The base regions 116, the p⁺-type projecting diffusion regions 118, the gate electrode layers 124 and the p⁺-type diffusion region 132b are formed in a stripe shape. Pitches at which the base regions 116, the p⁺-type projecting diffusion regions 118 and the gate electrode layers 124 are formed are set to 15μm, for example, and a pitch at which the p⁺-type diffusion region 132b is formed is set to 15μm, for example. A stripe width of the base region 116 is set to 9μm, for example. A stripe width of the p⁺-type projecting diffusion region 118 is set to 3.75μm, for example. A stripe width of the gate electrode layer 124 is set to 6μm, for example. A stripe width of the p⁺-type diffusion region 132b is set to 8μm, for example.

[0066]

The gate insulation layer 122 is formed of a silicon dioxide film having a thickness of 100nm, for example, and is formed by a thermal oxidation method. The field insulation film 134 is formed of a silicon dioxide film having a thickness of 450nm, for example, and is formed by a thermal oxidation method. The interlayer insulation layer 126 is formed of a PSG film having a thickness of 1000nm and is formed by a CVD method. The gate electrode layer 124 is formed of a low resistance poly-silicon film having a thickness of 500nm, for example, and is formed by a CVD method and an ion implantation method. The poly-silicon layer 136 is formed of a low resistance poly-silicon film having a thickness of 500nm, for example, and is formed by a CVD method and an ion implantation method. The gate electrode layer 124 and the poly-silicon layer 136 are formed in the same step.

[0067]

The source electrode layer 128 is formed of an aluminum film having a thickness of 4μm, for example, and is formed by a sputtering method. The gate pad electrode layer 138 and the gate finger line layer 142 are formed of an aluminum film having a thickness of 4μm, for example, and are formed by a sputtering method. The source electrode layer 128, the gate pad electrode layer 138 and the gate finger line layer 142 are formed in the same step. A drain electrode layer 130 is formed of a multi-layered metal film such as a Ti-Ni-Au film and a thickness of the whole multi-layered metal film is set to 0.5μm, for example.

[0068]

2. Advantageous effects acquired by the semiconductor device 100 according to the embodiment 1

Fig. 3A to Fig. 5B are views for explaining advantageous effects acquired by the semiconductor device 100 according to the embodiment 1. Fig. 3A is a view where parasitic capacitances and parasitic resistances are additionally described in a cross-sectional view of the semiconductor device 100 according to the embodiment 1. Fig. 3B is a view where parasitic capacitances and parasitic resistances are additionally described in a cross-sectional view of the semiconductor device 100A according to a comparison example 1. The semiconductor device

100A according to the comparison example 1 basically corresponds to the conventional semiconductor device 800.

[0069]

Fig. 4A to Fig. 4E are views showing modes where depletion layers d extend at the time of applying a reverse bias voltage. Fig. 4A is a view showing the mode where the depletion layers d extend when a reverse bias voltage is not applied. Fig. 4B is a view showing the mode where the depletion layers d extend when a low reverse bias voltage is applied. Fig. 4C is a view showing the mode where the depletion layers d extend when an intermediate reverse bias voltage is applied. Fig. 4D is a view showing the mode where the depletion layers d extend when a high reverse bias voltage is applied. Fig. 4E is a view showing the mode where the depletion layers d extend when a reverse bias voltage higher than the reverse voltage in the case shown in Fig. 4D is applied. The low resistance semiconductor layer 112, the drain electrode layer 130, the interlayer insulation layer 126 and the source electrode layer 128 are omitted in Fig. 4A to Fig. 4E.

[0070]

Fig. 5A is a view where parasitic capacitances and parasitic resistances are additionally described in the cross-sectional view of the semiconductor device 100 according to the embodiment 1. Fig. 5B is a view where parasitic capacitances and parasitic resistances are additionally described in a cross-sectional view of a semiconductor device 100B of a comparison example 2. The semiconductor device 100B according to the comparison example 2 basically corresponds to the third conventional semiconductor device 900.

[0071]

In the conventional semiconductor device 800 (or the semiconductor device 100A according to the comparison example 1), a gate-drain capacitance takes a value obtained by adding a capacitance of a capacitor C_1 formed in the gate pad part to a capacitance of a capacitor C_0 formed in the MOSFET part (see Fig. 3B). In such a constitution, the capacitor C_1 formed in the gate pad part has the structure where “the poly-silicon layer 136 which constitutes one electrode”, “a field insulation layer 134 which constitutes a dielectric and a p^+ -type diffusion region 158”, and “an n^- -type drift layer 114 which constitutes another electrode” are laminated to each other (see Fig. 3B).

[0072]

On the other hand, as shown in Fig. 3A, in the semiconductor device 100 according to the embodiment 1, a gate-drain capacitance takes a value obtained by adding capacitances of capacitors C_2, C_3 formed in the gate pad part to a capacitance of a capacitor C_0 formed in the MOSFET part. In such a constitution, the capacitor C_2 is a capacitor formed in a region where the p^+ -type diffusion region 132a and the p^+ -type diffusion region 132b are formed on a surface of the drift layer 114. The capacitor C_2 is formed of: “the poly-silicon layer 136 which constitutes one electrode”, “the field

insulation layer 134 which constitutes a dielectric and the p⁺-type diffusion regions (the p⁺-type diffusion region 132a and the p⁺-type diffusion region 132b)", and "the drift layer 114 which constitutes another electrode". The capacitor C₃ is a capacitor formed in the p-type impurity non-diffusion regions 132c, 132d on a surface of the drift layer 114. The capacitor C₃ is formed of

5 "the poly-silicon layer 136 which constitutes one electrode", "the field insulation layer 134 which constitutes a dielectric", and "the drift layer 114 which constitutes another electrode".

[0073]

In the semiconductor device 100 according to the embodiment 1, usually, the field insulation layer 134 is formed extremely thin compared with the p⁺-type diffusion regions 132a,

10 132b (field insulation layer 134: 200nm to 500nm, p⁺-type diffusion regions 132a, 132b: 2.4μm to 8.0μm). Accordingly, among the capacitors C₁, C₂ and C₃, the capacitance of the capacitor C₃ is extremely increased. As a result, the gate-drain capacitance Crss of the semiconductor device 100 according to the embodiment 1 becomes larger than the gate-drain capacitance Crss of the

15 conventional semiconductor device 800 (or the semiconductor device 100A according to the comparison example 1).

[0074]

In the semiconductor device 100 according to the embodiment 1, the narrow regions each of which is sandwiched by the p⁺-type diffusion regions which are disposed adjacent to each other on the surface of the drift layer 114 (the p-type impurity non-diffusion regions 132c each of which is

20 sandwiched by the p⁺-type diffusion region 132a and the p⁺-type diffusion regions 132, and the p-type impurity non-diffusion regions 132d each of which is sandwiched by the p⁺-type diffusion regions 132b which are disposed adjacent to each other) form current paths (see Fig. 3A). Further, in the current paths, at the time of switching off the semiconductor device, a depletion layer spreads toward a drift layer side from the p⁺-type diffusion regions (the p⁺-type diffusion region 132a and the

25 p⁺-type diffusion regions 132b) (see Fig. 4A to Fig. 4E) and hence, a resistance having a relatively large resistance (see a resistance R3 in Fig. 3A) is formed in the above-mentioned narrow regions.

[0075]

As a result, in the semiconductor device 100 according to the embodiment 1, a large capacitance and a large resistance can be formed between the gate and the drain and hence, it is

30 possible to suppress a gate oscillation phenomenon which occurs at the time of switching off the semiconductor device without externally connecting the capacitance and the resistance between the gate and the drain.

[0076]

The p⁺-type diffusion region 132b is in a floating state and hence, at the time of applying a

35 reverse bias voltage, it is usually considered that depletion layers do not spread toward a drift layer side from the p⁺-type diffusion region 132b. However, as shown in Fig. 4A to Fig. 4C, in the

semiconductor device 100 of the embodiment 1, at the time of applying a reverse bias voltage, in the course that the depletion layers “d” spread toward the drift layer side from the p⁺-type diffusion region 132a electrically connected with the source electrode layer 128, the depletion layers “d” spreading from the p⁺-type diffusion region 132a are brought into contact with the p⁺-type diffusion region 132b. Accordingly, a potential of the p⁺-type diffusion region 132b becomes equal to a potential of the p⁺-type diffusion region 132a and, thereafter, as shown in Fig. 4C to Fig. 4E, the depletion layers spread to the drift layer side also from the p⁺-type diffusion region 132b.

[0077]

Further, the semiconductor device 100 according to the embodiment 1 is provided with the gate oscillation suppressing structure 132 which includes the p⁺-type diffusion region 132a which is disposed along an outer peripheral portion of the gate pad part in an annular manner and is electrically connected with the source electrode layer 128 and the p⁺-type diffusion region 132b in a floating state and the p-type impurity non-diffusion regions 132c, 132d which are alternately formed in the region surrounded by the p⁺-type diffusion region 132a. Accordingly, as shown in Fig. 4A to Fig. 4E, at the time of applying a reverse bias voltage, the respective depletion layers extend in the lateral direction, are brought into contact with each other, and extend toward the low resistance semiconductor layer 112 over the whole area of the gate pad part. Accordingly, in the same manner as the conventional semiconductor device 800, the present invention can provide a semiconductor device having a high breakdown strength.

[0078]

In the conventional semiconductor device 800, the p region 71 is formed over the whole area of the gate pad part and hence, a pn junction area is large and hence, a carrier injection amount at the time of switching off the semiconductor device 800 is also increased. Accordingly, the conventional semiconductor device 800 has a drawback that a reverse recovery period t_{rr} extends and also have a drawback that a reverse recovery peak current IPR is increased. To the contrary, the semiconductor device 100 of the embodiment 1 is, in the gate pad part, provided with the gate oscillation suppressing structure 132 which includes the p⁺-type diffusion region 132a which is disposed along an outer peripheral portion of the gate pad part and is electrically connected with the first electrode layer and the p⁺-type diffusion region 132b in a floating state and the p-type impurity non-diffusion regions 132c, 132d which are alternately formed in the region surrounded by the p⁺-type diffusion region 132a. Accordingly, a pn junction area is small and a carrier injection amount at the time of switching off the semiconductor device is also decreased. Accordingly, the semiconductor 100 of the embodiment 1 has an advantage that a reverse recovery period t_{rr} becomes short and also has an advantage that a reverse recovery peak current IPR is decreased. Further, according to the semiconductor 100 of the embodiment 1, the p⁺-type diffusion region 132b of the gate pad part is in a floating state and hence, compared to the case where the p⁺-type diffusion region

132b of the gate pad part is not in a floating state, an area of the p⁺-type diffusion region 132b where the impurity diffusion regions function as a body diode is decreased, and a carrier injection amount at the time of switching off the semiconductor device is also decreased. As a result, a reverse recovery period t_{rr} becomes shorter and hence, a di/dt resistance can be increased.

5 [0079]

As described previously, in the third conventional semiconductor device 900 (or the semiconductor device 100B according to the comparison example 2), the p well layer 919 (132c) is formed in a ring shape in the lower portion of the gate pad part.

[0080]

10 However, in the third conventional semiconductor device 900 (or the semiconductor device 100B according to the comparison example 2), to possess a larger breakdown strength than the conventional semiconductor device (the conventional semiconductor device 800 or a semiconductor device described in Fig. 3 of JP-A-5-167070) at the time of switching off the semiconductor device, a capacitance of a parasitic diode below the gate pad part is set small.

15 Further, in the third conventional semiconductor device 900 (or the semiconductor device 100B according to the comparison example 2), the p well layer 919 (132c) is not formed at the center portion of the gate pad part and hence, a value of a resistance R3 formed at the center portion of the gate pad part becomes small. Accordingly, the third conventional semiconductor device 900, unlike the semiconductor device 100 according to the embodiment 1, cannot suppress a gate
20 oscillation phenomenon which occurs at the time of switching off the semiconductor device.

[0081]

Further, in the third conventional semiconductor device 900 (or the semiconductor device 100B according to the comparison example 2), the p well layer 919 (132c) is formed in the lower portion of the gate pad part in a ring shape. That is, the p well layer 919 (132c) is not formed at the
25 center portion of the gate pad part (see Fig. 33 and Fig. 5B) and hence, there also arises a drawback that an effect of making the spreading of a depletion layer in the lower portion of the gate pad part at the time of applying a reverse bias voltage stable is decreased.

[0082]

To the contrary, the semiconductor device 100 according to the embodiment 1 is provided
30 with the gate oscillation suppressing structure 132 which includes the p⁺-type diffusion region 132a which is disposed along an outer peripheral portion of the gate pad part in an annular manner and is electrically connected with the source electrode layer 128 and the p⁺-type diffusion region 132b in a floating state and the p-type impurity non-diffusion regions 132c, 132d which are alternately formed in the region surrounded by the p⁺-type diffusion region 132a. Accordingly, in the semiconductor
35 device 100 according to the embodiment 1, such a drawback that the third conventional

semiconductor device 900 (or the semiconductor device 100B according to the comparison example 2) has does not arise.

[0083]

Further, in the third conventional semiconductor device 900 (or the semiconductor device 100B according to the comparison example 2), the p well layer 919 (132c) formed in the lower portion of the gate pad part is not connected to the source electrode and hence, a depletion layer does not extend in a region where the p well layer 919 (132c) is not formed at the time of applying a reverse bias voltage and hence, a field intensity is not decreased whereby a breakdown strength is decreased.

[0084]

To the contrary, the semiconductor device 100 according to the embodiment 1 is provided with the gate oscillation suppressing structure 132 which includes the p⁺-type diffusion region 132a which is disposed along an outer peripheral portion of the gate pad part in an annular manner and is electrically connected with the source electrode layer 128 and the p⁺-type diffusion region 132b in a floating state and the p-type impurity non-diffusion regions 132c, 132d which are alternately formed in the region surrounded by the p⁺-type diffusion region 132a. Accordingly, in the semiconductor device 100 according to the embodiment 1, such a drawback that the third conventional semiconductor device 900 (or the semiconductor device 100B according to the comparison example 2) has does not arise.

[0085]

In the semiconductor device 100 according to the embodiment 1, the interlayer insulation layer 126 is formed on the poly-silicon layer 136 which constitutes a conductor layer, and the gate pad electrode layer 138 is formed on the interlayer insulation layer 126. Accordingly, a multi-layer structure formed of the poly-silicon layer 136, the interlayer insulation layer 126 and the gate pad electrode layer 138 functions as a shock absorber when an external terminal is connected to the gate pad electrode layer 138 and hence, the embodiment can provide a highly reliable semiconductor device.

[0086]

In the semiconductor device 100 according to the embodiment 1, as shown in Fig. 2A, the poly-silicon layer 136 is electrically connected with the gate electrode layer 124 via the gate finger part which connects the gate pad electrode layer 138 and the gate electrode layer 124 to each other, and no portion of the poly-silicon layer 136 is directly connected with the gate electrode layer 124 without interposing the gate finger part therebetween (see portions indicated by symbol D in Fig. 2A). Accordingly, a distance between the gate pad electrode layer 138 and the gate electrode layer 124 in the semiconductor device 100 according to the embodiment 1 becomes longer than the semiconductor device 100B according to the comparison example 2 where the gate pad electrode

layer 138 is directly connected with the gate electrode layer 124 (see a portion indicated by symbol C in Fig. 5B). Due to such constitution also, it is also possible to suppress a gate oscillation phenomenon.

[0087]

5 The semiconductor device 100 according to the embodiment 1 has the structure where the source region 120 on a gate pad part side is eliminated in a cell adjacent to the gate pad part (see a portion indicated by symbol B in Fig. 5A). In this manner, the semiconductor device 100 according to the embodiment 1 has the structure where the source region 120 which is the closest region to the gate pad part and where a gate oscillation phenomenon is most likely to occur is eliminated. Also
10 due to such constitution, it is possible to suppress a gate oscillation phenomenon.

[0088]

 In the semiconductor device 100 according to the embodiment 1, the p⁺-type diffusion regions 132a, 132b in the gate pad part are formed in the same step for forming the p⁺-type projecting diffusion regions 118 in the MOSFET part and hence, it is unnecessary to perform an extra step for
15 forming the p⁺-type diffusion regions 132a, 132b in the gate pad part. Further, the p⁺-type diffusion region 132a in the gate pad part is formed continuously with the p⁺-type projecting diffusion region 118 in the MOSFET part and hence, a potential equal to a potential of the p⁺-type projecting diffusion region 118 in the MOSFET part is applied to the p⁺-type diffusion region 132a (and the p⁺-type diffusion region 132b) in the gate pad part. As a result, the depletion layers in the drift layer
20 114 extend toward the drain layer at the time of applying a reverse bias voltage and hence, the embodiment 1 can provide a semiconductor device having a high breakdown strength.

[0089]

 In the semiconductor device 100 according to the embodiment 1, the p-type impurity non-diffusion regions 132d are formed in a stripe shape inside the p⁺-type diffusion region 132b and
25 hence, the p-type impurity non-diffusion regions 132d are easily depleted at the time of applying a reverse bias voltage. Due to such a constitution also, the embodiment 1 can provide a semiconductor device having a high breakdown strength.

[0090]

 In the semiconductor device 100 according to the embodiment 1, the p⁺-type diffusion regions 132a, 132b do not include an n-type semiconductor region therein and hence, a reach through phenomenon does not occur whereby the embodiment 1 can also acquire an advantageous effect that a high breakdown strength can be assured.

[0091]

 In the semiconductor device 100 according to the embodiment 1, the field insulation layer
35 134 which is required to possess a high insulation property because of having a large area has a larger

thickness than the thickness of the gate insulation layer 122 and hence, the embodiment 1 can provide a highly reliable semiconductor device having an excellent insulation property.

[0092]

In the semiconductor device 100 according to the embodiment 1, a ratio of an area of a portion in the gate pad part where the poly-silicon layer 136 which constitutes the conductor layer faces the drift layer 114 in an opposed manner with the field insulation layer 134 interposed therebetween to the whole area of the gate pad part is set larger than a ratio of an area of a portion in the MOSFET part where the gate electrode layer 124 faces the drift layer 114 in an opposed manner with the gate insulation layer 122 interposed therebetween to the whole area of the MOSFET part and hence, it is possible to effectively increase a gate-drain capacitance C_{rss} .

[0093]

3. Method of manufacturing a semiconductor device according to embodiment 1.

The semiconductor device 100 according to the embodiment 1 can be manufactured by a manufacturing method having the following manufacturing steps (method of manufacturing a semiconductor device according to the embodiment 1). Fig. 6A to Fig. 10C are views for explaining the method of manufacturing the semiconductor device according to the embodiment 1. Fig. 6A to Fig. 10C show the respective steps.

[0094]

(1) Preparation of semiconductor substrate

A semiconductor substrate 110 is prepared by forming a silicon layer which constitutes the drift layer 114 on a silicon substrate which constitutes the low resistance semiconductor layer 112 by an epitaxial growth method. A thickness of the low resistance semiconductor layer 112 is set to 100 μ m to 400 μ m, for example, and an impurity concentration in the low resistance semiconductor layer 112 is set to $1 \times 10^{19} \text{ cm}^{-3}$ to $1 \times 10^{20} \text{ cm}^{-3}$. A thickness of the drift layer 114 is set to 5 μ m to 50 μ m, and an impurity concentration in the drift layer 114 is set to $1 \times 10^{14} \text{ cm}^{-3}$ to $1 \times 10^{16} \text{ cm}^{-3}$.

[0095]

(2) Formation of p⁺-type projecting diffusion region, p⁺-type diffusion region and field insulation layer

Then, a p-type impurity is introduced into the regions on a surface of the drift layer 114 corresponding to the p⁺-type projecting diffusion regions 118 and regions corresponding to the p⁺-type diffusion regions 132a, 132b in such a manner that a silicon dioxide thin film M1 which has openings in regions corresponding to the p⁺-type projecting diffusion regions 118 and regions corresponding to the p⁺-type diffusion regions 132a, 132b is formed, and a p-type impurity (boron ion, for example) is injected into the surface of the drift layer 114 through the silicon dioxide thin film M1 by an ion implantation method (see Fig. 6A).

[0096]

Then, a heat treatment is applied to the semiconductor substrate 110 in an oxygen gas containing atmosphere thus forming the p⁺-type projecting diffusion region 118 and the p⁺-type diffusion regions 132a, 132b (see Fig. 6B). A forming depth of the p⁺-type projecting diffusion region 118 and a forming depth of the p⁺-type diffusion regions 132a, 132b are set to 2.4μm to 8.0μm, and an impurity concentration in the p⁺-type projecting diffusion region 118 and an impurity concentration in the p⁺-type diffusion regions 132a, 132b are set to $1 \times 10^{17} \text{ cm}^{-3}$ to $3 \times 10^{18} \text{ cm}^{-3}$. Here, in the gate pad part, the p-type impurity non-diffusion regions 132c, 132d are formed on portions of a surface of the drift layer 114 where the p-type impurity is not diffused. A surface of the drift layer 114 is thermally oxidized so that the field insulation layer 134 is formed. A thickness of the field insulation layer 134 is set to 450nm, for example.

[0097]

(3) Formation of gate insulation layer and gate electrode layer

Then, after a mask (not shown in the drawing) having openings is formed in the MOSFET part, and the field insulation layer 134 is etched so as to expose the drift layer 114 in the MOSFET part (see Fig. 6C). Then, a heat treatment is applied to the semiconductor substrate 110 in an oxygen gas containing atmosphere so that a surface of the drift layer 114 is thermally oxidized whereby a gate insulation layer 122 is formed in the MOSFET part (see Fig. 7A). A thickness of the gate insulation layer 122 is set to 100nm, for example.

[0098]

Then, a low resistance poly-silicon layer 123 is formed by a CVD method on a surface of the field insulation layer 134 and a surface of the gate insulation layer 122 (see Fig. 7B). A thickness of the poly-silicon layer 123 is set to 500nm, for example. Then, a mask (not shown in the drawing) is formed on regions corresponding to the poly-silicon layer 136 and regions corresponding to the gate electrode layers 124 to be formed and, thereafter, the poly-silicon layer 123 is etched thus forming the gate electrode layers 124 in the MOSFET part and the poly-silicon layer 136 in the gate pad part (see Fig. 7C).

[0099]

(4) Formation of base region

Then, a p-type impurity is introduced into the regions on a surface of the drift layer 114 corresponding to the base regions 116 to be formed by injecting a p-type impurity (boron ion, for example) into the surface of the drift layer 114 with the gate insulation layer 122 interposed therebetween by an ion implantation method using the field insulation layer 134 and the gate electrode layers 124 as masks (see Fig. 8A).

Then, an annealing treatment for activating a p-type impurity is performed by applying a heat treatment to the semiconductor substrate 110 thus forming the base regions 116 (see Fig. 8B).

A depth of the base region 116 is set to $2\mu\text{m}$ to $2.5\mu\text{m}$, and an impurity concentration in the base region 116 is set to $5\times 10^{16}\text{cm}^{-3}$ to $1\times 10^{18}\text{cm}^{-3}$.

[0100]

(5) Formation of source regions

5 Then, a mask M2 is formed on regions on the gate insulation layers 122 except for regions where the source regions 120 are to be formed. An n-type impurity is introduced into the regions on a surface of the drift layer 114 corresponding to the source regions 120 by injecting an n-type impurity (phosphorous ion, for example) into the surface of the drift layer 114 with the gate insulation layer 122 interposed therebetween by an ion implantation method using the mask M2, the gate electrode layer 124 and the field insulation layer 134 as masks (see Fig. 8C).

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[0101]

Then, the mask M2 is removed and, thereafter, the interlayer insulation layer 126 formed of PSG and having a thickness of 1000nm , for example, is formed over the whole area of the semiconductor substrate 110 on a first main surface side by a CVD method (see Fig. 9A). Then, an annealing treatment for activating the n-type impurity is performed by applying a heat treatment to the semiconductor substrate 110 thus forming the source regions 120 (see Fig. 9B). A depth of the source region 120 is set to $0.2\mu\text{m}$ to $0.4\mu\text{m}$, and an impurity concentration in the source region 120 is set to $5\times 10^{19}\text{cm}^{-3}$ to $2\times 10^{20}\text{cm}^{-3}$.

15

[0102]

20 (6) Formation of source electrode layer, gate pad electrode layer and drain electrode layer

Then, the interlayer insulation layer 126 formed on a portion (through holes 140) where the gate pad electrode layer 138 to be formed is brought into contact with the poly-silicon layer 136 and portions (contact holes 141) where the source electrode layer 128 is brought into contact with the source regions 120 and the base regions 116 is selectively removed respectively (see Fig. 9C) and, thereafter, a metal layer 127 made of aluminum is formed from above the interlayer insulation layer 126 by a sputtering method (see Fig. 10A). Then, the metal layer 127 is divided into the source electrode layer 128 and the gate pad electrode layer 138 by removing predetermined regions of the metal layer 127 by etching thus forming the source electrode layer 128 and the gate pad electrode layer 138 (see Fig. 10B). A thickness of the source electrode layer 128 and a thickness of the gate pad electrode layer 138 are set to $4\mu\text{m}$, for example.

25

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[0103]

Then, a metal film formed of a multi-layered metal film such as a Ti-Ni-Au film is formed on a surface of the semiconductor substrate 110 on a second main surface side (surface of the low resistance semiconductor layer 112) thus forming the drain electrode layer 130 (see Fig. 10C). A thickness of the drain electrode layer 130 is set to $0.5\mu\text{m}$, for example, over the whole multi-layered metal film.

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[0104]

The semiconductor device 100 according to the embodiment 1 can be manufactured through the above-mentioned steps.

[0105]

5 [Embodiments 2 to 5]

Fig. 11 is a plan view of a semiconductor device 100a of an embodiment 2. Fig. 12 is a plan view of a semiconductor device 100b of an embodiment 3. Fig. 13 is a plan view of a semiconductor device 100c of an embodiment 4. Fig. 14 is a plan view of a semiconductor device 100d of an embodiment 5. In Fig. 11, Fig. 12, Fig. 13 and Fig. 14, only a profile line (indicated by a chain line) is indicated with respect to p⁺-type projecting diffusion regions 118, p⁺-type diffusion regions 132a, 132b, 162, p-type impurity non-diffusion regions 132c, 132d, a gate oscillation suppressing structure 132 and a source electrode layer 128.

[0106]

Although the semiconductor devices 100a to 100d according to the embodiments 2 to 5 basically have the substantially same constitution as the semiconductor device 100 according to the embodiment 1, the semiconductor devices 100a to 100d according to the embodiments 2 to 5 differ from the semiconductor device 100 according to the embodiment 1 in the planar structure of the gate oscillation suppressing structure 132. That is, as shown in Fig. 11, in the semiconductor device 100a according to the embodiment 2, unlike the case of the semiconductor device 100 according to the embodiment 1, the direction of the stripe of p⁺-type diffusion region 132a and the direction of the stripe of the p-type impurity non-diffusion regions 132d are orthogonal to the direction of the stripe of the p⁺-type projecting diffusion regions 118. As shown in Fig. 12, in the semiconductor device 100b according to the embodiment 3, p-type impurity non-diffusion regions 132d are formed in an island-like shape inside the p⁺-type diffusion region 132b. As shown in Fig. 13, in the semiconductor device 100c according to the embodiment 4, a p-type impurity non-diffusion region 132c is formed in a region surrounded by the p⁺-type diffusion region 132a, and the p⁺-type diffusion regions 132b and the p-type impurity non-diffusion regions 132d are formed in a stripe shape inside the p-type impurity non-diffusion region 132c. As shown in Fig. 14, in the semiconductor device 100d according to the embodiment 5, a p-type impurity non-diffusion region 132c is formed in a region surrounded by the p⁺-type diffusion region 132a, p⁺-type diffusion regions 132b are formed in an island shape inside the p-type impurity non-diffusion region 132c, and a p-type impurity non-diffusion region 132d is formed in a grid shape inside the p-type impurity non-diffusion region 132c.

[0107]

35 [Embodiments 6 and 7]

Fig. 15 is a cross-sectional view of a semiconductor device 100e according to an embodiment 6. Fig. 16 is a cross-sectional view of a semiconductor device 100f according to an embodiment 7.

[0108]

5 Although the semiconductor devices 100e, 100f according to the embodiments 6 and 7 basically have the substantially same constitution as the semiconductor device 100 according to the embodiment 1, the semiconductor devices 100e, 100f according to the embodiments 6 and 7 differ from the semiconductor device 100 according to the embodiment 1 in the electrode lamination structure in a gate pad part. That is, as shown in Fig. 15, in the semiconductor device 100e
10 according to the embodiment 6, a gate pad electrode layer 138 is directly formed over the substantially whole surface of a poly-silicon layer 136 which constitutes a conductor layer without interposing an interlayer insulation layer 126 therebetween. On the other hand, as shown in Fig. 16, in the semiconductor device 100f according to the embodiment 7, a gate pad electrode layer 138 which constitutes a conductor layer is directly formed over the substantially whole surface of a field
15 insulation layer 134 without interposing a poly-silicon layer therebetween.

[0109]

[Embodiment 8]

Fig. 17A and Fig. 17B are views for explaining a semiconductor device 100g according to an embodiment 8. Fig. 17A is a plan view of the semiconductor device 100g, and Fig. 17B is a
20 cross-sectional view taken along a line A1-A1 in Fig. 17A. In Fig. 17B, symbol 130 indicates a drain electrode layer. In Fig. 17A, only a profile line (indicated by a chain line) is indicated with respect to base regions 116, p-type diffusion regions (corresponding to the second conductive type impurity diffusion regions of the present invention) 133a, 163, a p-type impurity non-diffusion region (corresponding to the impurity non-diffusion region of a second conductive type of the
25 present invention) 133b, a gate oscillation suppressing structure 133 and a source electrode layer 128.

[0110]

Although the semiconductor device 100g according to the embodiment 8 basically has the substantially same constitution as the semiconductor device 100 according to the embodiment 1, the
30 semiconductor device 100g according to the embodiment 8 differs from the semiconductor device 100 according to the embodiment 1 in a step of forming the second conductive type impurity diffusion region. That is, as shown in Fig. 17A and Fig. 17B, in the semiconductor device 100g according to the embodiment 8, p⁺-type contact regions 144 are formed in place of the p⁺-type projecting diffusion regions in a MOSFET part, and the p-type diffusion region 133a which
35 constitutes the second conductive type impurity diffusion region is formed in the same step for

forming the base regions 116 in place of being formed in the same step for forming p⁺-type projecting diffusion regions.

[0111]

[Embodiments 9 to 11]

5 Fig. 18 is a cross-sectional view of a semiconductor device 100h according to an embodiment 9. Fig. 19 is a cross-sectional view of a semiconductor device 100i according to an embodiment 10. Fig. 20A and Fig. 20B are views for explaining a semiconductor device 100j according to an embodiment 11. Fig. 20A is a cross-sectional view of a gate pad part and a MOSFET part in the semiconductor device 100j, and Fig. 20B is a cross-sectional view of the
10 MOSFET part, a gate finger part and a guard ring part in the semiconductor device 100j. In Fig. 18 to Fig. 20A, symbols 150c, 150d indicate p-type impurity non-diffusion regions (corresponding to the impurity non-diffusion region of a second conductive type in the present invention), and symbol 150 indicates a gate oscillation suppressing structure.

[0112]

15 Although the semiconductor devices 100h to 100j according to the embodiments 9 to 11 basically have the substantially same constitution as the semiconductor device 100 according to the embodiment 1, the semiconductor device 100h to 100j according to the embodiments 9 to 11 differ from the semiconductor device 100 according to the embodiment 1 in a point that a p⁻-type diffusion region 150a which contains a p-type impurity having a lower concentration than base regions 116 is
20 formed in place of a p⁺-type diffusion region 132a which contains a p-type impurity having a higher concentration than the base regions 116. That is, as shown in Fig. 18 to Fig. 20B, in the semiconductor devices 100h to 100j according to the embodiments 9 to 11, an n-type reference concentration semiconductor layer 146 is formed in the MOSFET part in a state where the n-type reference concentration semiconductor layer 146 which is shallower than the base region 116 is
25 formed between the base regions 116 arranged adjacent to each other and the n-type reference concentration semiconductor layer 146 contains an n-type impurity having a higher concentration than a drift layer 114 and a lower concentration than source regions 120. p⁻-type projecting diffusion regions 148 which contain a p-type impurity having a lower concentration than the base regions 116 are formed in the MOSFET part in place of the p⁺-type projecting diffusion regions 118
30 which contain a p-type impurity having a higher concentration than the base regions 116. Further, the p⁻-type diffusion regions 150a, 150b which contain a p-type impurity having a lower concentration than the base regions 116 are formed in the gate pad part in place of the p⁺-type diffusion regions 132a, 132b which contain a p-type impurity having a higher concentration than the base regions 116. The technique for forming the n-type reference concentration semiconductor
35 layers 146 and the p⁻-type projecting diffusion regions 148 in the MOSFET part is a technique

developed by the applicant of the present invention, and this technique is disclosed in detail in JP-A-2011-228643.

[0113]

Among the semiconductor devices 100h to 100j according to the embodiments 9 to 11, in the semiconductor device 100h according to the embodiment 9, the n-type reference concentration semiconductor layer 146 extends into the gate pad part (see Fig. 18). In the semiconductor device 100i according to the embodiment 10, the n-type reference concentration semiconductor layer 146 is formed only in the MOSFET part (see Fig. 19). In the semiconductor device 100j according to the embodiment 11, n⁺-type semiconductor layers 152 are formed in the MOSFET part in a state where the n⁺-type semiconductor layers 152 which are shallower than the n-type reference concentration semiconductor layer 146 are formed on a surface of the n-type reference concentration semiconductor layer 146, and the n⁺-type semiconductor layers 152 contain an n-type impurity having a higher concentration than the n-type reference concentration semiconductor layer 146 and a lower concentration than the source region 120 (see Fig. 20A and Fig. 20B).

[0114]

In the semiconductor devices 100h to 100j according to the embodiments 9 to 11, the p⁻-type diffusion regions 150a, 150b of the gate pad part are formed in the same step for forming the p⁻-type projecting diffusion regions 148 in the MOSFET part. Further, the p⁻-type diffusion region 150a of the gate pad part is formed continuously with the p⁻-type projecting diffusion region 148 in the MOSFET part (see Fig. 18 to Fig. 20B). In the semiconductor device 100j according to the embodiment 11, the p⁻-type diffusion regions 150a, 150b in the gate pad part and the p⁻-type diffusion region 164 in the gate finger part are formed in the same step for forming a guard ring 154 in a guard ring part formed around the MOSFET part (see Fig. 20A and Fig. 20B).

[0115]

The semiconductor device 100i according to the embodiment 10 can be manufactured by a method of manufacturing a semiconductor device described hereinafter. Fig. 21A to Fig. 21C are views for explaining a method of manufacturing a semiconductor device according to the embodiment 10. Fig. 21A to Fig. 21C are views showing respective steps.

[0116]

Although the method of manufacturing the semiconductor device according to the embodiment 10 basically includes the substantially same steps as the method of manufacturing the semiconductor device according to the embodiment 1, the method of manufacturing the semiconductor device according to the embodiment 10 differs from the method of manufacturing the semiconductor device according to the embodiment 1 in the contents of steps of forming the n-type reference concentration semiconductor layer 146, the p⁻-type projecting diffusion regions 148 and the p-type impurity diffusion regions 150a, 150b. Accordingly, the method of manufacturing the

semiconductor device according to the embodiment 10 is explained by mainly focusing on the steps for forming the n-type reference concentration semiconductor layer 146, the p⁻-type projecting diffusion regions 148 and the p-type impurity diffusion regions 150a, 150b.

[0117]

5 (1) Formation of n-type reference concentration semiconductor layer

After performing “preparation of semiconductor substrate (step)” in the same manner as the method of manufacturing the semiconductor device according to the embodiment 1, a silicon dioxide thin film M3 which has openings in regions corresponding to the n-type reference concentration semiconductor layer 146 is formed. An n-type impurity (phosphorous ion, for example) is introduced into the regions on a surface of a drift layer 114 corresponding to the n-type reference concentration semiconductor layer 146 by injecting an n-type impurity into the surface of the drift layer 114 through the silicon dioxide thin film M3 by an ion implantation method (see Fig. 21A).

[0118]

15 (2) Formation of p⁻-type projecting diffusion region, p⁻-type diffusion region and field insulation layer

The silicon dioxide thin film M3 is removed and, thereafter, a silicon dioxide thin film M4 which has openings in regions corresponding to the p⁻-type projecting diffusion regions 148 and the p⁻-type diffusion regions 150a, 150b is formed. A p-type impurity (boron ion, for example) is introduced into the regions on a surface of the drift layer 114 corresponding to the p⁻-type projecting diffusion regions 148 and the regions corresponding to the p⁻-type diffusion regions 150a, 150b by injecting a p-type impurity into the surface of the drift layer 114 through the silicon dioxide thin film M4 by an ion implantation method (see Fig. 21B).

[0119]

25 Then, a heat treatment is applied to the semiconductor substrate 110 in an oxygen gas containing atmosphere thus forming the n-type reference concentration semiconductor layer 146, the p⁻-type projecting diffusion regions 148 and the p⁻-type diffusion regions 150a, 150b (see Fig. 21C). A forming depth of the p⁻-type projecting diffusion region 148 and a forming depth of the p⁻-type diffusion regions 150a, 150b are set to 6.0μm to 8.0μm, and an impurity concentration in the p⁻-type projecting diffusion region 148 and an impurity concentration in the p⁻-type diffusion regions 150a, 150b are set to $1 \times 10^{17} \text{ cm}^{-3}$ to $3 \times 10^{18} \text{ cm}^{-3}$ respectively. At this stage of operation, a surface of the drift layer 114 is thermally oxidized so that a field insulation layer 134 is formed. A thickness of the field insulation layer 134 is set to 450nm, for example.

[0120]

35 Then, in the substantially same manner as the method of manufacturing the semiconductor device according to the embodiment 1, the respective succeeding steps, that is, “formation of gate

insulation layer and gate electrode layer”, “formation of base regions”, “formation of source regions”, “formation of source electrode layer, gate pad electrode layer and drain electrode layer” are performed. In accordance with such steps, the semiconductor device 100i according to the embodiment 11 can be manufactured.

5 [0121]

In manufacturing the semiconductor device 100h according to the embodiment 9, at the time of performing the step “formation of n-type reference concentration semiconductor layer”, an n-type impurity (phosphorous ion, for example) is injected into the surface of the drift layer 114 also in the gate pad part by an ion implantation method.

10 [0122]

In manufacturing the semiconductor device 100j according to the embodiment 11, after performing the above-mentioned step “formation of p⁻-type projecting diffusion region, p⁻-type diffusion region and field insulation layer”, an n-type impurity (phosphorous ion, for example) is introduced into the regions on a surface of the drift layer 114 where the n⁺-type semiconductor layer 152 is formed by injecting an n-type impurity into the surface of the drift layer 114 only in the region where the n⁺-type semiconductor layer 152 is to be formed by an ion implantation method. Then, an annealing treatment for activating an n-type impurity is performed by applying a heat treatment to the semiconductor substrate 110 thus forming the n⁺-type semiconductor layer 152.

[0123]

20 [Embodiment 12]

Fig. 22A and Fig. 22B are views for explaining a semiconductor device 100k according to an embodiment 12. Fig. 22A is a cross-sectional view of a gate pad part and a MOSFET part in the semiconductor device 100k, and Fig. 22B is a cross-sectional view of the MOSFET part, a gate finger part and a guard ring part in the semiconductor device 100k.

25 [0124]

Although the semiconductor device 100k according to the embodiment 12 basically has the substantially same constitution as the semiconductor device 100 according to the embodiment 1, the semiconductor device 100k according to the embodiment 12 differs from the semiconductor device 100 according to the embodiment 1 in a step of forming p⁺-type diffusion regions. That is, in the semiconductor device 100k according to the embodiment 12, p⁺-type contact regions 144 are formed in a MOSFET part in place of the p⁺-type projecting diffusion regions 118, and p⁺-type diffusion regions 132a, 132b are formed in the same step for forming a p⁺-type diffusion region 162 and guard rings 154 which are formed around the MOSFET part (see Fig. 22A and Fig. 22B).

[0125]

35 [Embodiments 13 to 15]

Fig. 23 is a cross-sectional view of a semiconductor device 200 according to an embodiment 13. Fig. 24 is a cross-sectional view of a semiconductor device 200a according to an embodiment 14. Fig. 25 is a cross-sectional view of a semiconductor device 200b according to an embodiment 15.

5 [0126]

Although the semiconductor devices 200 to 200b according to the embodiments 13 to 15 basically have the substantially same constitution as the semiconductor device 100 according to the embodiment 1, the semiconductor devices 200 to 200b according to the embodiments 13 to 15 differ from the semiconductor device 100 according to the embodiment 1 in a point that a MOSFET part
10 does not have the planar structure but the trench structure.

[0127]

That is, as shown in Fig. 23 and Fig. 25, the semiconductor devices 200 to 200b according to the embodiments 13 to 15 are semiconductor devices 200 provided with a MOSFET part and a gate pad part defined on a semiconductor substrate 210 which is formed by laminating an n⁺-type low resistance semiconductor layer 212 and an n⁻-type drift layer 214 to each other. The MOSFET part includes: the low resistance semiconductor layer 212; the drift layer 214 formed on the low resistance semiconductor layer 212; a p-type base region 216 formed on a surface of the drift layer 214; a plurality of trenches 217 formed in the base region 216 in a state where the trenches 217 reach the drift layer 214; n⁺-type source regions 220 formed such that the n⁺-type source region 220 is
15 disposed in the inside of the base region 216 and at least a portion of the n⁺-type source region 220 is exposed on an inner peripheral surface of the trench 217; gate insulation layers 222 formed on the inner peripheral surface of the trenches 217; gate electrode layers 224 embedded in the inside of the trenches 217 with the gate insulation layers 222 interposed therebetween; and a source electrode layer 228 formed in contact with the surfaces of the source regions 220 and the base region 216 in a state where the source electrode layer 228 is insulated from the gate electrode layers 224 with an interlayer insulation film 226 interposed therebetween. The gate pad part includes: the low resistance semiconductor layer 212; the drift layer 214 formed on the low resistance semiconductor layer 212; a poly-silicon layer 236 constituting a conductor layer and formed above the drift layer 214 over the whole area of the gate pad part with a field insulation layer 234 interposed
20 therebetween; and a gate oscillation suppressing structure (the gate oscillation suppressing structure 233 in the embodiment 13, and the gate oscillation suppressing structure 232 in the embodiments 14 and 15) formed on the surface of the drift layer 214.

30 [0128]

The gate oscillation suppressing structure 233, 232 includes: a first diffusion region of a second conductive type (a p-type diffusion region 233a in the embodiment 13, a p⁺-type diffusion region 232a in the embodiments 14 and 15) which is disposed along an outer peripheral portion of
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the gate pad part in an annular manner and is electrically connected with the source electrode layer 228; and a first impurity diffusion region of a second conductive type (a p-type diffusion region 233b in the embodiment 13, a p⁺-type diffusion regions 232b in the embodiments 14 and 15) in a floating state and non-diffusion regions of a second conductive type (p-type impurity non-diffusion regions 233c, 233d in the embodiment 13, p-type impurity non-diffusion regions 232c, 232d in the embodiments 14, 15). The gate electrode layers 224 and the source regions 220 are insulated from each other with the gate insulation layer 222 interposed therebetween.

[0129]

In the semiconductor device 200 according to the embodiment 13, the p-type diffusion regions 233a, 233b are formed in the same step for forming the base region 216. The p-type diffusion regions 233a are formed continuously with the base region 216 (see Fig. 23). In the semiconductor device 200a according to the embodiment 14, the p⁺-type diffusion regions 232a, 232b are formed in the same step for forming the p⁺-type projecting diffusion regions 218. The p⁺-type diffusion regions 232a are formed continuously with the p⁺-type projecting diffusion regions 218 (see Fig. 24). In the semiconductor device 200b according to the embodiment 15, the p⁺-type diffusion regions 232a, 232b are formed in the same step for forming a guard ring not shown in the drawing which is mounted at a position surrounding the MOSFET part (see Fig. 25).

[0130]

[Embodiment 16]

Fig. 26 is a cross-sectional view of a semiconductor device 300 according to the embodiment 16.

Although the semiconductor device 300 according to the embodiment 16 basically has the substantially same constitution as the semiconductor device 100 according to the embodiment 1, the semiconductor device 300 according to the embodiment 16 differs from the semiconductor device 100 according to the embodiment 1 in a point that the semiconductor device is not a power MOSFET but an IGBT. That is, as shown in Fig. 26, the semiconductor device 300 according to the embodiment 16 is an IGBT, and includes a p⁺-type low resistance semiconductor layer in place of the n⁺-type low resistance semiconductor layer as a low resistance semiconductor layer.

[0131]

[Embodiment 17]

Fig. 27A and Fig. 27B are views for explaining a semiconductor device 100l according to an embodiment 17. Fig. 27A is a plan view of the semiconductor device 100l, and Fig. 27B is a cross-sectional view taken along a line A1-A1 in Fig. 27A. In Fig. 27B, symbol 130 indicates a drain electrode layer. In Fig. 27A, only a profile line (indicated by a chain line) is indicated with respect to p⁺-type projecting diffusion regions 118, p⁺-type diffusion regions 132a, 132b, a p-type impurity non-diffusion region 132c, 132d, a gate oscillation suppressing structure 132 and a source

electrode layer 128. In Fig. 27A, the p⁺-type projecting diffusion regions 118 and the p⁺-type diffusion regions 132a, 132b are indicated by a dot pattern, and in Fig. 27B, the p⁺-type projecting diffusion regions 118 and the p⁺-type diffusion regions 132a, 132b are indicated by an outlined pattern.

5 [0132]

Although the semiconductor device 100l according to the embodiment 17 basically has the substantially same constitution as the semiconductor device 100 according to the embodiment 1, the semiconductor device 100l according to the embodiment 17 differs from the semiconductor device 100 according to the embodiment 1 in a point that a plurality of p⁺-type diffusion regions (corresponding to the third impurity diffusion region of a second conductive type of the present invention) are formed such that the p⁺-type diffusion regions are formed in a spaced-apart manner from each other also in a gate finger part which connects a gate pad electrode layer 138 and a gate electrode layer 124 to each other. That is, as shown in Fig. 27A and Fig. 27B, in the semiconductor device 100l according to the embodiment 17, the plurality of p⁺-type diffusion regions 132e are formed in a spaced-apart manner from each other on a surface of a drift layer 114 also in the gate finger part which connects the gate pad electrode layer 138 and the gate electrode layer 124 to each other. A field insulation layer 134 is formed on a surface of the drift layer 114 in the gate finger part, and a poly-silicon layer 136 is formed on the field insulation layer 134 such that the poly-silicon layer 136 extends from the poly-silicon layer 136 just below the gate pad electrode layer 138. As shown in Fig. 27A, the plurality of p⁺-type diffusion regions 132e may be formed in a stripe shape along a long side of the gate finger part. The plurality of p⁺-type diffusion regions 132e may be formed in a stripe shape along a short side of the gate finger part. The plurality of p⁺-type diffusion regions 132e may be also formed in an island shape in a region of the gate finger part.

[0133]

25 [Advantageous effects according to the embodiments 2 to 17]

As has been explained heretofore, the semiconductor devices 100a to 300 according to the embodiments 2 to 17 differ from the semiconductor device 100 according to the embodiment 1 in the above-mentioned respective points (the embodiments 2 to 5: the planar structure of the gate oscillation suppressing structure 132, the embodiments 6 and 7: the electrode lamination structure in the gate pad part, the embodiment 8: the step of forming impurity diffusion regions of a second conductive type, the embodiments 9 to 11: the provision of the p⁻-type diffusion region in place of the p⁺-type diffusion region, the embodiment 12: the step of forming the p⁺-type diffusion region, the embodiments 13 to 15: the MOSFET part including the trench structure, the embodiment 16: the semiconductor device being an IGBT, the embodiment 17: a plurality of p⁺-type diffusion regions being formed in a spaced-apart manner from each other also in the gate finger part). However, in the semiconductor devices 100a to 300, the gate pad part includes: the poly-silicon layer 136 which

constitutes a conductor layer and is formed above a drift layer 114 over the whole area of a gate pad part with the field insulation layer 134 interposed therebetween; and the gate oscillation suppressing structure which includes a first impurity diffusion region of a second conductive type which is disposed along an outer peripheral portion of the gate pad part in an annular manner and is electrically connected with a first electrode layer (a source electrode layer or an emitter electrode layer), a second impurity diffusion region of a second conductive type in a floating state and an impurity non-diffusion region of a second conductive type which are alternately formed in the region surrounded by the first impurity diffusion region of a second conductive type. Accordingly, a gate-drain capacitance C_{rss} in the semiconductor devices 100a to 300 according to the embodiments 2 to 17 becomes larger than the gate-drain capacitance C_{rss} of the conventional semiconductor device.

[0134]

A narrow region (impurity non-diffusion region of a second conductive type) sandwiched by the impurity diffusion regions of a second conductive type which are disposed adjacent to each other on the surface of the drift layer 114 (the first impurity diffusion region of a second conductive type and the second impurity diffusion region of a second conductive type) forms a current path. Further, in the current path, at the time of switching off the semiconductor device, a depletion layer spreads toward a drift layer side from the impurity diffusion regions of a second conductive type (the first impurity diffusion region of a second conductive type and the second impurity diffusion region of a second conductive type) and hence, a resistance having a relatively large resistance value is formed in the above-mentioned narrow region. As a result, in the substantially same manner as the semiconductor device 100 according to the embodiment 1, a large capacitance and a large resistance can be formed between the gate and the drain and hence, it is possible to suppress a gate oscillation phenomenon which occurs at the time of switching off the semiconductor device without externally connecting the capacitance and the resistance between the gate and the drain.

[0135]

The semiconductor devices 100a to 300 according to the embodiments 2 to 17 are, in the gate pad part, provided with the gate oscillation suppressing structure which includes the first impurity diffusion region of a second conductive type which is disposed along an outer peripheral portion of the gate pad part and is electrically connected with the first electrode layer and the second impurity diffusion region of a second conductive type in a floating state and the impurity non-diffusion region of a second conductive type which are alternately formed in the region surrounded by the first impurity diffusion region of a second conductive type. Accordingly, a pn junction area is small and a carrier injection amount at the time of switching off the semiconductor device is also decreased. Accordingly, the semiconductor devices 100a to 300 according to the embodiments 2 to 17 have an advantage that a reverse recovery period t_{rr} becomes short and an

advantage that a reverse recovery peak current IPR is decreased. Further, according to the semiconductor devices 100a to 300 according to the embodiments 2 to 17, the second impurity diffusion region of a second conductive type in the gate pad part is in a floating state and hence, compared to the case where the second impurity diffusion region of a second conductive type in the gate pad part is not in a floating state, an area of the second conductive type impurity diffusion region where the impurity diffusion region functions as a body diode is decreased, and a carrier injection amount at the time of switching off the semiconductor device is also decreased. As a result, a reverse recovery period t_{rr} becomes shorter and hence, a di/dt resistance can be increased.

[0136]

In addition to the above-mentioned advantageous effects, the semiconductor devices 100h to 100j according to the embodiments 9 to 11 and the semiconductor device 100l according to the embodiment 17 have the following advantageous effects.

[0137]

That is, in the semiconductor devices 100h to 100j according to the embodiments 9 to 11, the n-type reference concentration semiconductor layer 146 is formed in the MOSFET part in a state where the n-type reference concentration semiconductor layer 146 which is shallower than the base region 116 is disposed between the base regions 116 arranged adjacent to each other and contains an n-type impurity having a higher concentration than the drift layer 114 and a lower concentration than the source region 120. Accordingly, the semiconductor device can be micronized by making a distance between the base regions narrower than the conventional semiconductor device. Even when the distance between the base regions is made narrower than the conventional semiconductor device, there is no possibility that the ON resistance of the semiconductor device is increased. Accordingly, the semiconductor devices 100h to 100j according to the embodiments 9 to 11 become semiconductor devices which can be micronized without increasing an ON resistance of the semiconductor device and have a favorable high breakdown strength.

[0138]

In the semiconductor device 100j according to the embodiment 11, the n⁺-type semiconductor layer 152 is formed in the MOSFET part in a state where the n⁺-type semiconductor layer 152 which is shallower than the n-type reference concentration semiconductor layers 146 is formed over a surface of the n-type reference concentration semiconductor layer 146 and contains an n-type impurity having a higher concentration than the n-type reference concentration semiconductor layers 146 and a lower concentration than the source region 120. Accordingly, an ON resistance of the semiconductor device can be decreased, and a gate oscillation phenomenon at the time of switching off the semiconductor device can be suppressed more effectively.

[0139]

In the semiconductor device 100i according to the embodiment 10, the n-type reference concentration semiconductor layer 146 is not formed in the gate pad part and hence, there is no possibility that a resistance value of a resistance of the p^- -type non-diffusion regions 150c, 150d is excessively decreased.

5 [0140]

In the semiconductor device 100l according to the embodiment 17, also in the gate finger part which connects the gate pad electrode layer 138 and the gate electrode layer 124 to each other, the poly-silicon layer 136 which constitutes a conductor layer is formed above the drift layer 114 with the field insulation layer 134 interposed therebetween, and the plurality of p^+ -type diffusion regions 132a which are formed in a spaced-apart manner from each other are formed on a surface of the drift layer 114. Accordingly, the semiconductor devices 100l according to the embodiment 17 can acquire an advantageous effect that a gate-drain capacitance C_{rss} of the semiconductor device 100l according to the embodiment 17 becomes larger than the gate-drain capacitance C_{rss} of the semiconductor device 100 according to the embodiment 1.

15 [0141]

[Test examples]

In realizing the semiconductor devices 100 to 300 according to the embodiments 1 to 17 having the above-mentioned constitutions respectively, results obtained by following test examples 1 and 2 are used as references.

20 [0142]

[Test example 1]

The test example 1 is a test example which is performed so as to clarify that a large capacitance is formed between the gate and the drain in the semiconductor device of the present invention.

25 Fig. 28A and Fig. 28B are cross-sectional views of semiconductor devices 100i, 100C which are used in the test examples 1 and 2. Fig. 29A to Fig. 29C are views for explaining an evaluation result of the test example 1. Fig. 29A is a view showing an equivalent circuit of the semiconductor device 100i. Fig. 29B is a view showing an equivalent circuit of the semiconductor device 100C. Fig. 29C is a view showing measurement results of the semiconductor device 100i and the semiconductor device 100C. Although the semiconductor devices 100i, 100C shown in Fig. 28A and Fig. 28B have the slightly different constitution from the constitution of the semiconductor device 100 shown in Fig. 2A and Fig. 2B or the semiconductor device 100A shown in Fig. 3A and Fig. 3B, corresponding resistances and capacitances are indicated by the same symbols (C_0 , C_1 , C_2 , C_3 , R_0 , R_1 , R_2 , R_3) to facilitate the understanding of the test examples 1, 2.

35 [0143]

1. Constitutional conditions on semiconductor device

(1) Semiconductor device according to embodiment

A semiconductor device having the substantially same constitution as the semiconductor device 100i according to the embodiment 10 is employed without modification as the semiconductor device 100i according to the embodiment (see Fig. 28A).

5 [0144]

(2) Semiconductor device according to comparison example

A semiconductor device which has the substantially same constitution as the semiconductor device 100i according to the embodiment 10 but includes a well-like p⁻-type diffusion region 160 formed on a surface of the drift layer 114 over the whole area of the gate pad part in place of the above-mentioned gate oscillation suppressing structure 150 is employed as the semiconductor device 100C of a comparison example 3 (see Fig. 28B).

[0145]

2. Method of test

A test is performed with respect to the above-mentioned semiconductor device 100i according to the above-mentioned embodiment and the semiconductor device 100C according to the comparison example 3 by measuring a gate-drain capacitance Crss using a capacitance measurement device while changing a drain-source voltage V_{DS}.

[0146]

3. Result of test

The measurement result is shown in Fig. 29C. It is clearly understood from Fig. 29C that a larger gate-drain capacitance Crss is formed in the semiconductor device of the present invention (the semiconductor device 100i according to the embodiment) than the conventional semiconductor device (semiconductor device 100C according to the comparison example 3).

[0147]

25 [Test example 2]

The test example 2 is a test example which is performed so as to clarify that a gate oscillation phenomenon at the time of switching off the semiconductor device can be suppressed more efficiently in the semiconductor device of the present invention than in the conventional semiconductor device.

30 [0148]

1. Constitutional condition of semiconductor device

(1) Semiconductor device according to embodiment

“the semiconductor device 100i according to embodiment” which is used in the test example 1 is also used as the semiconductor device 100i according to embodiment in the test example 2 as it is.

35

[0149]

(2) Semiconductor device according to comparison example

“the semiconductor device 100C according to the comparison example 3” which is used in the test example 1 is also used as “the semiconductor device 100C according to the comparison example 3” in the test example 2 as it is.

[0150]

2. Method of test

Fig. 30A to Fig. 30C are views for explaining an evaluation method and an evaluation result in the test example 2. Fig. 30A is a view showing a measurement system used in the test example 2, Fig. 30B is a view showing a response waveform at the time of switching off the semiconductor device in the semiconductor device 100i according to the embodiment, and Fig. 30C is a view showing a response waveform at the time of switching off the semiconductor device in the semiconductor device 100C according to the comparison example 3.

[0151]

The test is performed by measuring a gate-source voltage V_{GS} and a drain current I_D at the time of switching off the semiconductor device using the measurement system shown in Fig. 30A.

[0152]

3. Result of test

The result of the test is shown in Fig. 30B and Fig. 30C. It is clearly understood from Fig. 30B and Fig. 30C that a gate oscillation phenomenon at the time of switching off the semiconductor device can be suppressed more efficiently in the semiconductor device of the present invention (semiconductor device 100i according to the embodiment) than in the third conventional semiconductor device 900 (semiconductor device 100C according to the comparison example 3).

[0153]

Although the present invention has been explained based on the above-mentioned embodiments heretofore, the present invention is not limited to the above-mentioned embodiments. The present invention can be carried out in various modes without departing from the gist of the present invention, and the following modifications are conceivable, for example.

[0154]

(1) In the above-mentioned respective embodiments, the present invention is explained by taking the case where the n type is the first conductive type and the p type is the second conductive type. However, the present invention is not limited to such a case. For example, the present invention is also applicable to the case where the p type is the first conductive type and the n type is the second conductive type.

[0155]

(2) The present invention is not limited to the layout or the arrangement of the parts shown in Fig. 2A provided that the conductor layer (the poly-silicon layer 136) is electrically connected with the gate electrode layer 124 via the gate finger part and no portion of the conductor layer is directly connected with the gate electrode layer 124 without interposing the gate finger part. Fig. 31 is a plan view of a semiconductor device 100m according to a modification. In Fig. 31, in the same manner as in the Fig. 2A, only a profile line (indicated by a chain line) is indicated with respect to a poly-silicon layer 136 and a source electrode layer 128. The conductor layer (the poly-silicon layer 136) may be arranged as shown in Fig. 31, for example.

Description of symbols

- 10 [0156]
- 100, 100A, 100B, 100C, 100a, 100b, 100c, 100d, 100e, 100f, 100g, 100h, 100i, 100j, 100k, 100l, 100m, 200, 200a, 200b, 300, 800, 900: semiconductor device
- 112, 212, 312: low resistance semiconductor layer
- 114, 214, 314: drift layer
- 15 116, 216, 316: base region
- 118, 218, 318: p⁺-type projecting diffusion region
- 120, 220: source region
- 122, 222, 322: gate insulation layer
- 124, 224, 324: gate electrode layer
- 20 126, 226, 326: interlayer insulation layer
- 127: metal layer
- 128, 228, 328: source electrode layer
- 130, 230, 320: drain electrode layer
- 132, 133, 150, 232, 233, 332: gate oscillation suppressing structure
- 25 132a, 132b, 158, 162, 232a, 232b, 332a, 332b: p⁺-type diffusion region
- 132c, 132d, 133c, 133d, 150c, 150d, 232c, 232d, 233c, 233d, 332c, 332d: p-type impurity non-diffusion region
- 133a, 133b, 163, 233a, 233b: p-type diffusion region
- 134, 234, 334: field insulation layer
- 30 136, 137, 236, 336: poly-silicon layer
- 138, 238, 338: gate pad electrode layer
- 140, 240, 340: through hole
- 141: contact hole
- 142: gate finger line layer
- 35 144: contact region
- 146: n-type reference concentration semiconductor layer

148: p⁻-type projecting diffusion region

150a, 150b, 160, 164: p⁻-type diffusion region

152: n⁺-type semiconductor region

154: guard ring

5 156: channel stopper

217: trench

320: emitter region

328: emitter electrode layer

330: collector electrode layer

10

Conclusies

1. Halfgeleiderinrichting, die is voorzien van een actief-elementdeel en een gate-pad-deel, die zijn gedefinieerd op een halfgeleidersubstraat, dat is gevormd door het aan elkaar lamineren van een
 - 5 lage-weerstand-halfgeleiderlaag van een eerste geleidend type of een tweede geleidend type en een driftlaag van het eerste geleidende type, waarbij het actieve-elementdeel omvat:
 - de lage-weerstand-halfgeleiderlaag;
 - de op de lage-weerstand-halfgeleiderlaag gevormde driftlaag;
 - 10 een basisgebied van het tweede geleidende type, dat is gevormd op een oppervlak van de driftlaag; een hoge-concentratie-onzuiverheid-diffusiegebied van het eerste geleidende type, dat is gevormd op een oppervlak van het basisgebied;
 - een gate-elektrodelaa, die is gevormd op het basisgebied en is aangebracht tussen het hoge-concentratie-onzuiverheid-diffusiegebied en de driftlaag met een daartussen opgestelde
 - 15 gate-isolatielaag; en
 - een eerste elektrodelaa, die in contact met een oppervlak van het hoge-concentratie-onzuiverheid-diffusiegebied en het oppervlak van het basisgebied is gevormd in een toestand waarin de eerste elektrodelaa is geïsoleerd van de gate-elektrodelaa met een daartussen opgestelde tussenlaagisolatielaag, en
 - 20 het gate-pad-deel omvat:
 - de lage-weerstand-halfgeleiderlaag;
 - de op de lage-weerstand-halfgeleiderlaag gevormde driftlaag;
 - een geleiderlaag, die boven de driftlaag is gevormd over het gehele gebied van het gate-pad-deel met een daartussen opgestelde veld-isolatielaag; en
 - 25 een gate-trilling onderdrukkende structuur, die is gevormd op het oppervlak van de driftlaag, waarbij de gate-trilling onderdrukkende structuur omvat:
 - een eerste onzuiverheid-diffusiegebied van het tweede geleidende type, dat is aangebracht langs een buitenste omtreksdeel van het gate-pad-deel en dat elektrisch is verbonden met de eerste elektrodelaa, en een tweede onzuiverheid-diffusiegebied van het tweede geleidende type in een
 - 30 zwevende toestand en een onzuiverheid-non-diffusiegebied van het tweede geleidende type, die afwisselend zijn gevormd in een gebied, dat wordt omgeven door het eerste onzuiverheid-diffusiegebied van het tweede geleidende type.
2. Halfgeleiderinrichting, die is voorzien van een actief-elementdeel en een gate-pad-deel, die zijn
 - 35 gedefinieerd op een halfgeleidersubstraat, dat is gevormd door het aan elkaar lamineren van een lage-weerstand-halfgeleiderlaag van een eerste geleidend type of een tweede geleidend type en een

driftlaag van het eerste geleidende type, waarbij

het actieve-elementdeel omvat:

de lage-weerstand-halfgeleiderlaag;

de driftlaag, die op de lage-weerstand-halfgeleiderlaag is gevormd;

- 5 een basisgebied van het tweede geleidende type, dat is gevormd op een oppervlak van de driftlaag; een aantal sleuven, dat zodanig is gevormd, dat de sleuven openen aan het basisgebied en de driftlaag bereiken;

een hoge-concentratie-onzuiverheid-diffusiegebied van het eerste geleidende type, dat is aangebracht in het basisgebied, waarvan ten minste een deel wordt blootgesteld aan binnenste

- 10 omtreksoppervlakken van de sleuven;

een gate-isolatielaag, die is gevormd op de binnenste omtreksoppervlakken van de sleuven;

een gate-elektrodelaa, die is ingebed in de binnenzijde van de sleuven met de gate-isolatielaag daartussen opgesteld; en

een eerste elektrodelaa, die in contact met een oppervlak van het

- 15 hoge-concentratie-onzuiverheid-diffusiegebied en een oppervlak van het basisgebied is gevormd in een toestand waarin de eerste elektrodelaa is geïsoleerd van de gate-elektrodelaa met een daartussen opgestelde tussenlaagisolatielaag, en

het gate-pad-deel omvat:

de lage-weerstand-halfgeleiderlaag;

- 20 de driftlaag, die op de lage-weerstand-halfgeleiderlaag is gevormd;

een geleiderlaag, die boven de driftlaag is gevormd over een geheel gebied van het gate-pad-deel met een daartussen opgestelde veld-isolatielaag; en

een gate-trilling onderdrukkende structuur, die is gevormd op het oppervlak van de driftlaag, waarbij de gate-trilling onderdrukkende structuur omvat:

- 25 een eerste onzuiverheid-diffusiegebied van het tweede geleidende type, dat is aangebracht langs een buitenste omtreksdeel van het gate-pad-deel en dat elektrisch is verbonden met de eerste elektrodelaa, en een tweede onzuiverheid-diffusiegebied van het tweede geleidende type in een zwevende toestand en een onzuiverheid-non-diffusiegebied van het tweede geleidende type, die afwisselend zijn gevormd in een gebied, dat wordt omgeven door het eerste
- 30 onzuiverheid-diffusiegebied van het tweede geleidende type.

3. Halfgeleiderinrichting volgens conclusie 1 of 2, waarbij de veld-isolatielaag een grotere dikte heeft dan de gate-isolatielaag.

- 35 4. Halfgeleiderinrichting volgens een der conclusies 1 - 3, waarbij de geleiderlaag is gevormd van een poly-siliciumlaag, die is gevormd tussen de veld-isolatielaag en een gate-pad-elektrodelaa, die

is gevormd over de veldisolatielaag.

5. Halfgeleiderinrichting volgens een der conclusies 1 - 3, waarbij de geleiderlaag een gate-pad-elektrodelaa is, die is gevormd over de veldisolatielaag.

5

6. Halfgeleiderinrichting volgens conclusie 4 of 5, waarbij de geleiderlaag elektrisch is verbonden met de gate-elektrodelaa via een gate-vingerdeel, dat de gate-pad-elektrodelaa en de gate-elektrodelaa aan elkaar verbindt, en waarbij geen deel van de geleiderlaag direct is verbonden met de gate-elektrodelaa zonder tussenplaatsing van het gate-vingerdeel daartussen.

10

7. Halfgeleiderinrichting volgens conclusie 1, waarbij een cel, die aangrenzend aan het gate-pad-deel is opgesteld de structuur heeft waar het hoge-concentratie-onzuiverheid-diffusiegebied op een gat-pad-deelzijde is geëlimineerd.

15 8. Halfgeleiderinrichting volgens conclusie 2, waarbij een sleuf, die aangrenzend aan het gate-pad-deel is opgesteld een structuur heeft waar het hoge-concentratie-onzuiverheid-diffusiegebied op een gat-pad-deelzijde is geëlimineerd.

9. Halfgeleiderinrichting volgens conclusie 1, waarbij het actieve-elementdeel verder een
20 hoge-concentratie-uitstekend-diffusiegebied van het tweede geleidende type omvat, dat is gevormd op een neerwaarts uitstekende manier vanaf het basisgebied, en het eerste onzuiverheid-diffusiegebied van het tweede geleidende type en het tweede onzuiverheid-diffusiegebied van het tweede geleidende type zijn gevormd in eenzelfde stap van het vormen van het hoge-concentratie-uitstekend-diffusiegebied, en waarbij het eerste
25 onzuiverheid-diffusiegebied van het tweede geleidende type continu met het hoge-concentratie-uitstekend-diffusiegebied is gevormd.

10. Halfgeleiderinrichting volgens conclusie 1, waarbij het eerste onzuiverheid-diffusiegebied van het tweede geleidende type en het tweede onzuiverheid-diffusiegebied van het tweede geleidende
30 type zijn gevormd in eenzelfde stap van het vormen van het basisgebied, en waarbij het eerste onzuiverheid-diffusiegebied van het tweede geleidende type continu met het basisgebied is gevormd.

11. Halfgeleiderinrichting volgens conclusie 1, waarbij het actieve-elementdeel verder een
35 lage-concentratie-uitstekend-diffusiegebied van het tweede geleidende type omvat, dat is gevormd op een neerwaarts uitstekende manier vanaf het basisgebied, en

het eerste onzuiverheid-diffusiegebied van het tweede geleidende type en het tweede onzuiverheid-diffusiegebied van het tweede geleidende type zijn gevormd in eenzelfde stap van het vormen van het lage-concentratie-uitstekend-diffusiegebied, en waarbij het eerste onzuiverheid-diffusiegebied van het tweede geleidende type continu met het

5 lage-concentratie-uitstekend-diffusiegebied is gevormd.

12. Halfgeleiderinrichting volgens conclusie 1, waarbij het eerste onzuiverheid-diffusiegebied van het tweede geleidende type en het tweede onzuiverheid-diffusiegebied van het tweede geleidende type zijn gevormd zijn gevormd in eenzelfde stap van het vormen van een bewakingsring, die is

10 gevormd om het actieve-elementdeel.

13. Halfgeleiderinrichting volgens conclusie 2, waarbij het eerste onzuiverheid-diffusiegebied van het tweede geleidende type en het tweede onzuiverheid-diffusiegebied van het tweede geleidende type zijn gevormd in eenzelfde stap van het vormen van het basisgebied, en waarbij het eerste

15 onzuiverheid-diffusiegebied van het tweede geleidende type continu met het basisgebied is gevormd.

14. Halfgeleiderinrichting volgens conclusie 2, waarbij het actieve-elementdeel verder een hoge-concentratie-uitstekend-diffusiegebied van het tweede geleidende type omvat, dat is gevormd

20 op een neerwaarts uitstekende manier vanaf het basisgebied, en het eerste onzuiverheid-diffusiegebied van het tweede geleidende type en het tweede onzuiverheid-diffusiegebied van het tweede geleidende type zijn gevormd in eenzelfde stap van het vormen van het hoge-concentratie-uitstekend-diffusiegebied, en waarbij het eerste onzuiverheid-diffusiegebied van het tweede geleidende type continu met het

25 hoge-concentratie-uitstekend-diffusiegebied is gevormd.

15. Halfgeleiderinrichting volgens een der conclusies 1 - 14, waarbij het tweede onzuiverheid-diffusiegebied van het tweede geleidende type is gevormd in een gebied, dat wordt omgeven door het eerste onzuiverheid-diffusiegebied van het tweede geleidende type, en

30 het onzuiverheid-non-diffusiegebied van het tweede geleidende type is gevormd in een streepvorm of een eilandvorm in het tweede onzuiverheid-diffusiegebied van het tweede geleidende type.

16. Halfgeleiderinrichting volgens een der conclusies 1 - 14, waarbij het onzuiverheid-non-diffusiegebied van het tweede geleidende type is gevormd in een gebied, dat

35 wordt omgeven door het eerste onzuiverheid-diffusiegebied van het tweede geleidende type, en het tweede onzuiverheid-diffusiegebied van het tweede geleidende type is gevormd in een

streepvorm of een eilandvorm in het onzuiverheid-non-diffusiegebied van het tweede geleidende type

17. Halfgeleiderinrichting volgens een der conclusies 1 - 16, waarbij het eerste
- 5 onzuiverheid-diffusiegebied van het tweede geleidende type en het tweede onzuiverheid-diffusiegebied van het tweede geleidende type geen halfgeleidergebied van het eerste geleidende type daarin hebben.
18. Halfgeleiderinrichting volgens een der conclusies 4 tot 6, waarbij een gate-vingerdeel, dat de
- 10 gate-pad-elektrodelaaag en de gate-elektrodelaaag verbindt, ook een gate-trilling onderdrukkende structuur heeft waarin een derde onzuiverheid-diffusiegebied van het tweede geleidende type, dat elektrisch is verbonden met de eerste elektrodelaaag en een tweede onzuiverheid-non-diffusiegebied van het tweede geleidende type afwisselend zijn gevormd op het oppervlak van de driftlaag.

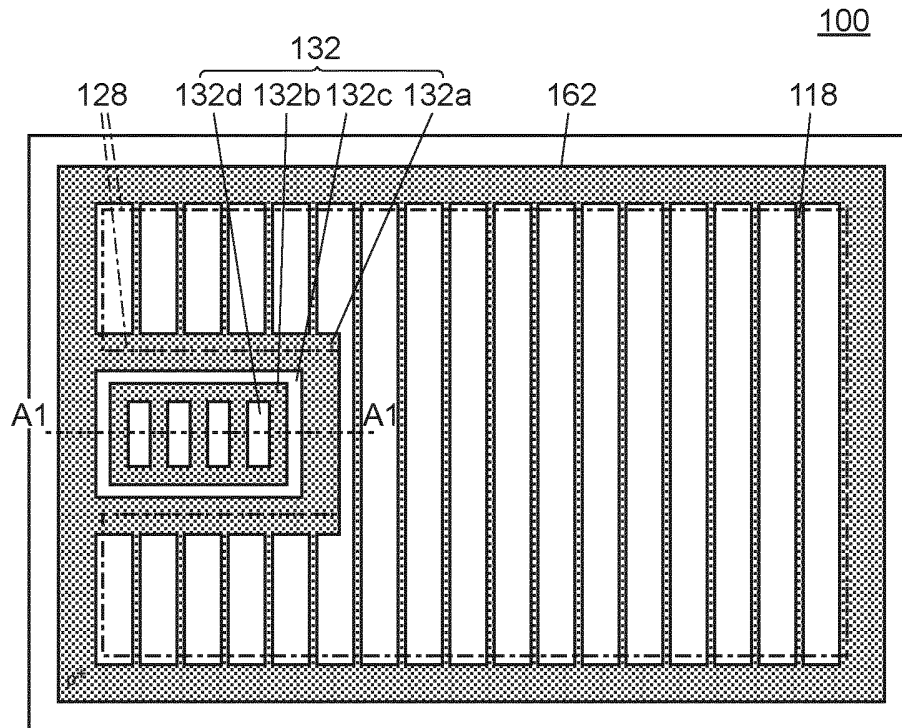


FIG. 1A

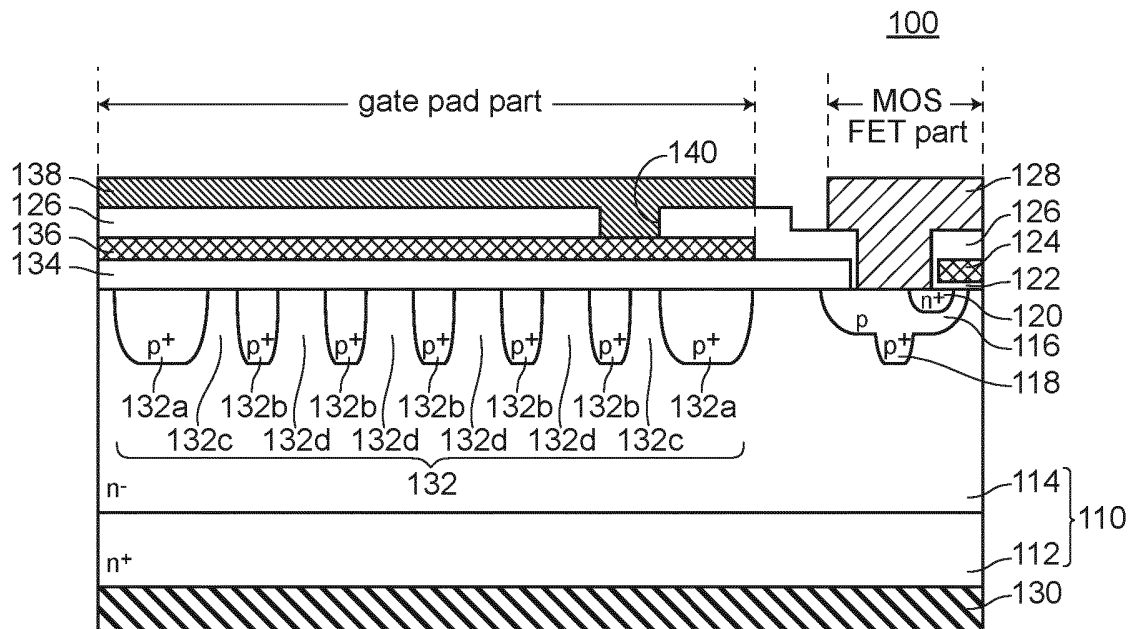


FIG. 1B

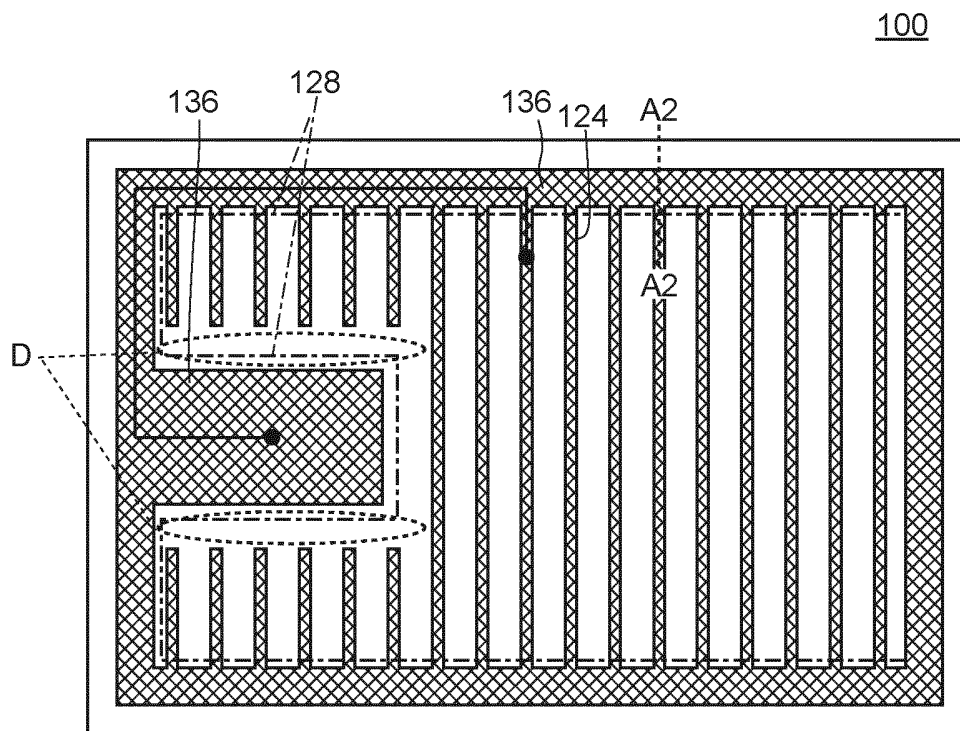


FIG.2A

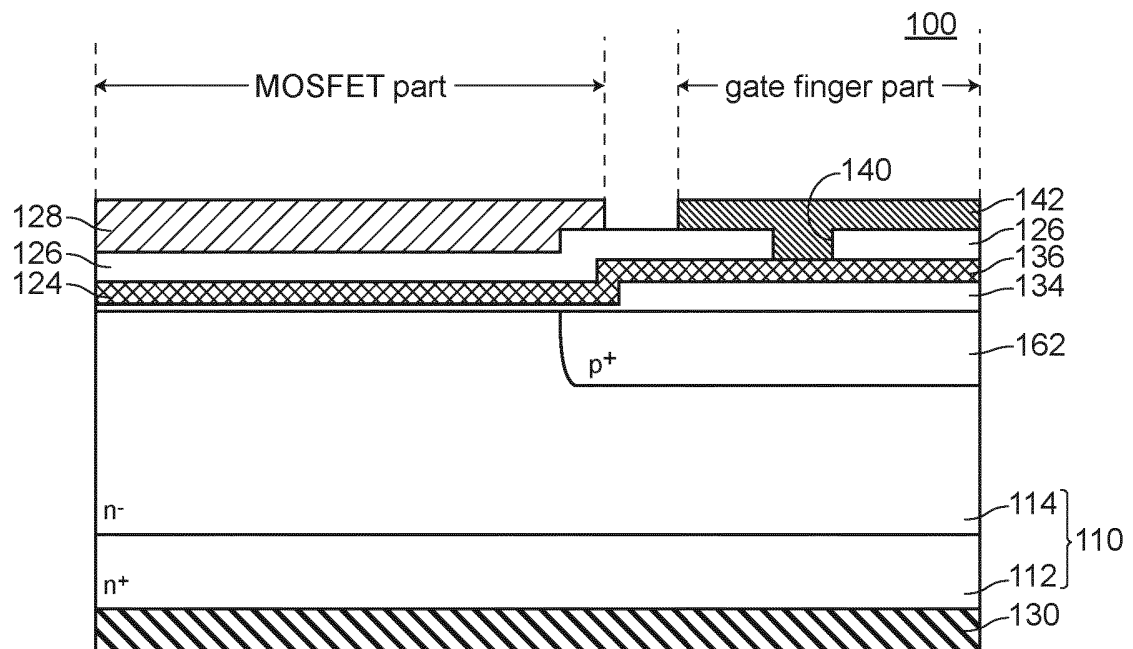


FIG.2B

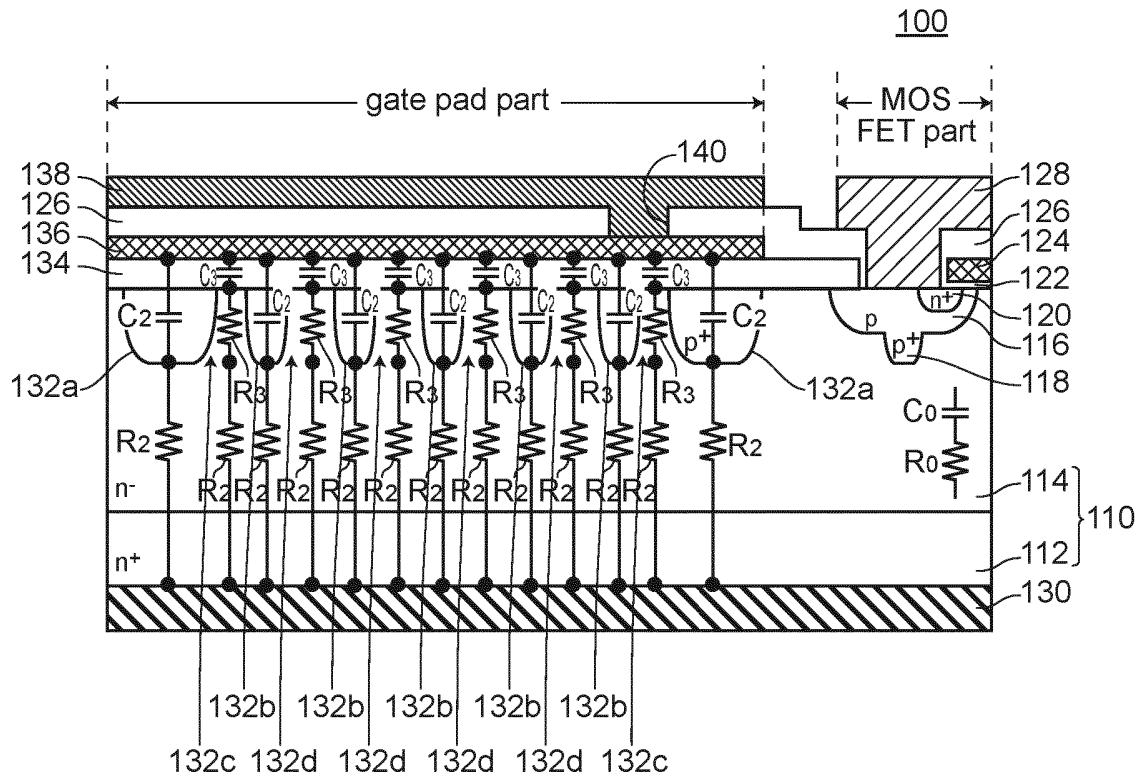


FIG.3A

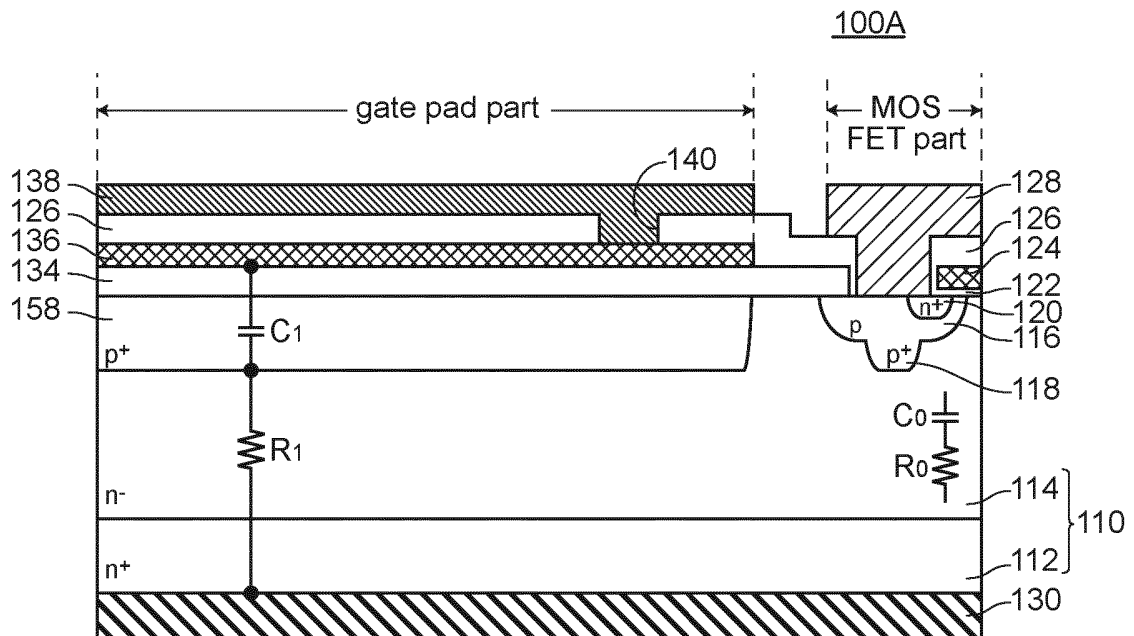


FIG.3B

FIG.4A

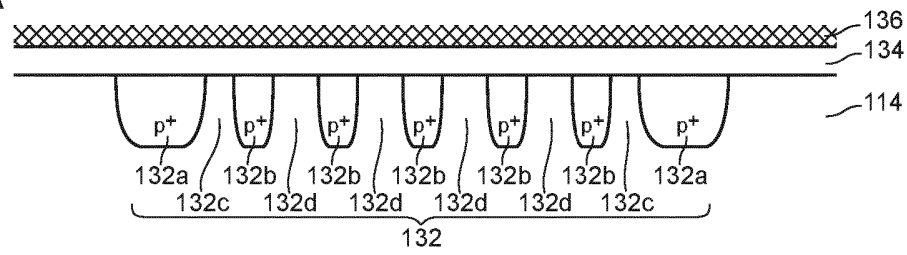


FIG.4B

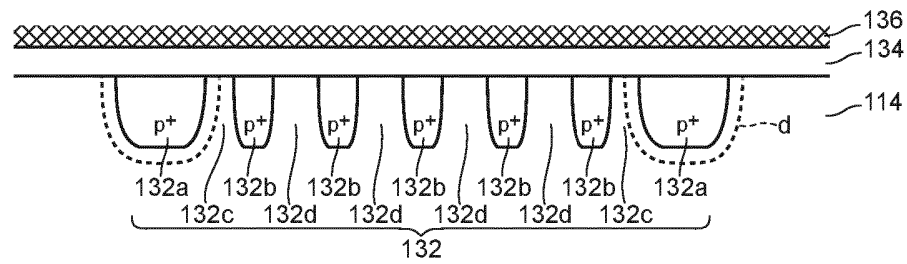


FIG.4C

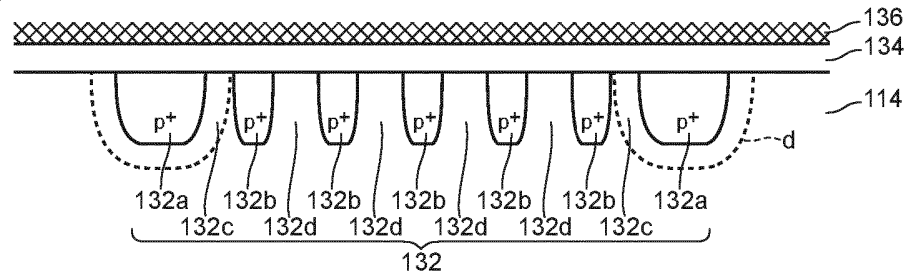


FIG.4D

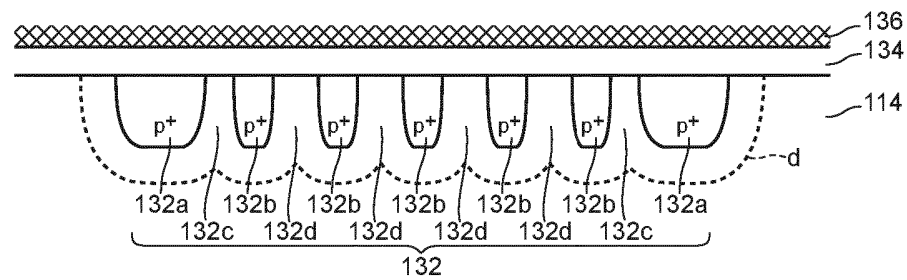
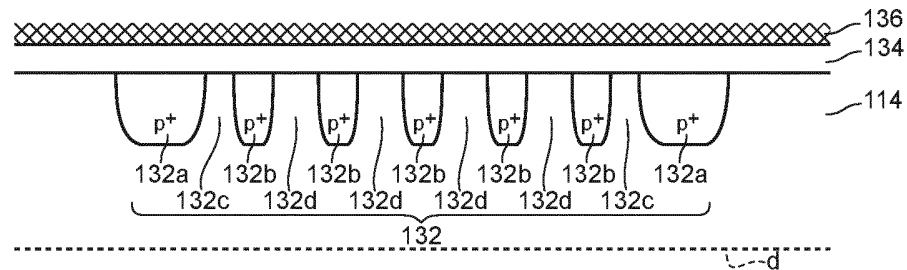


FIG.4E



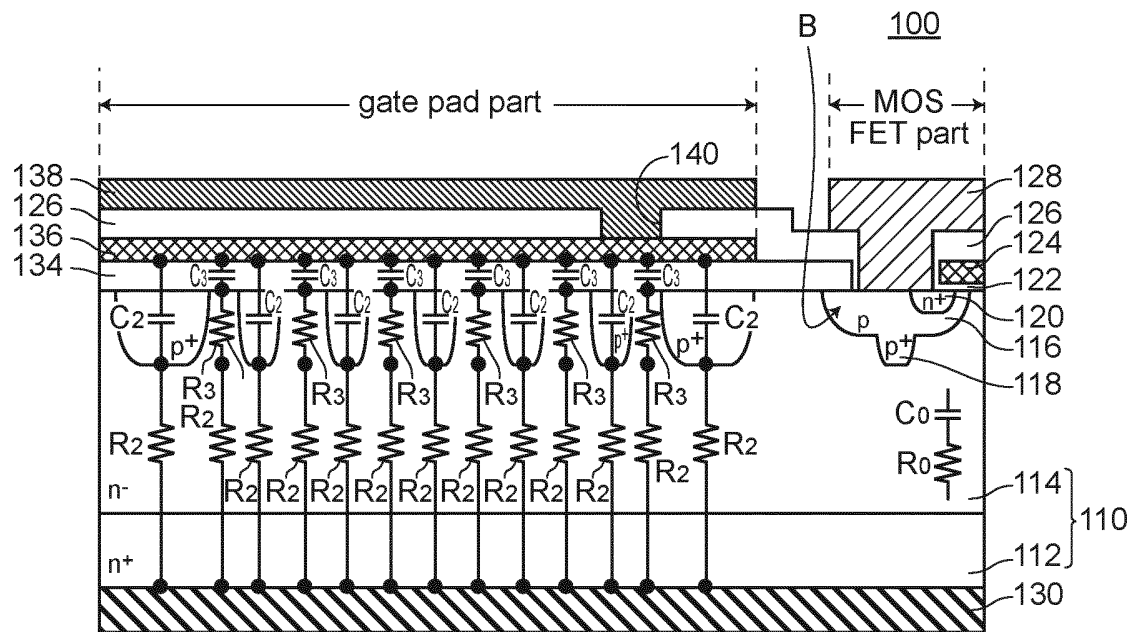


FIG. 5A

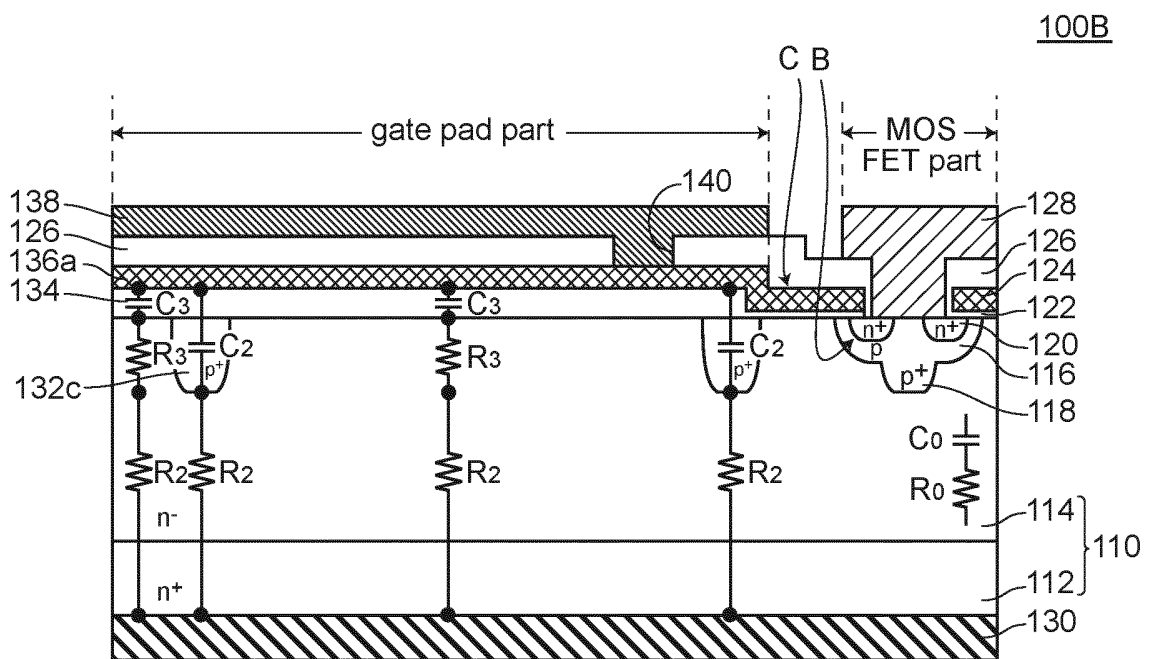


FIG. 5B

FIG.6A

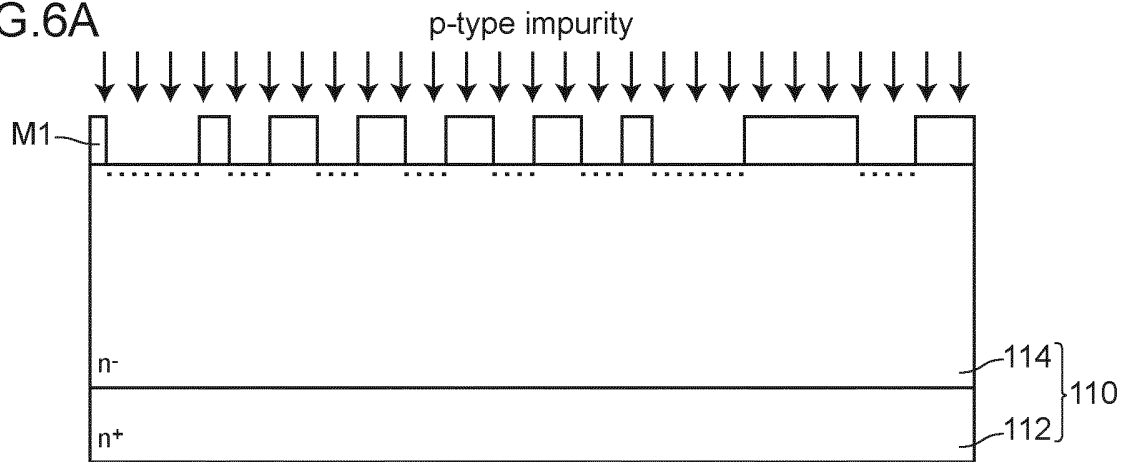


FIG.6B

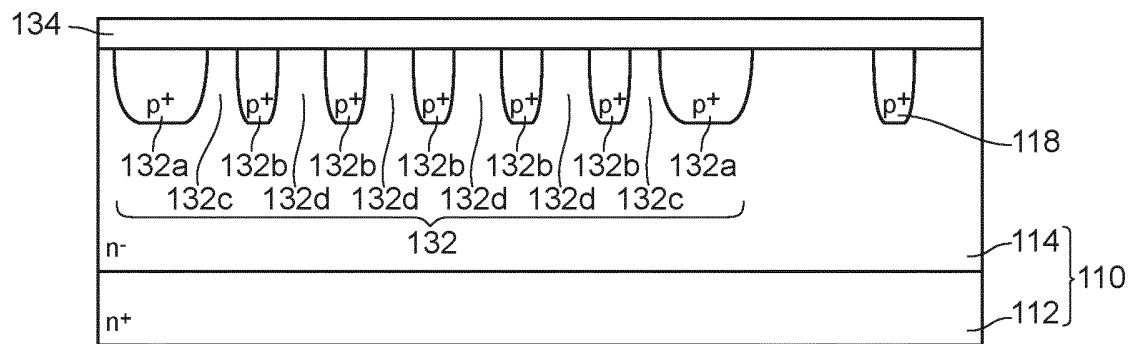


FIG.6C

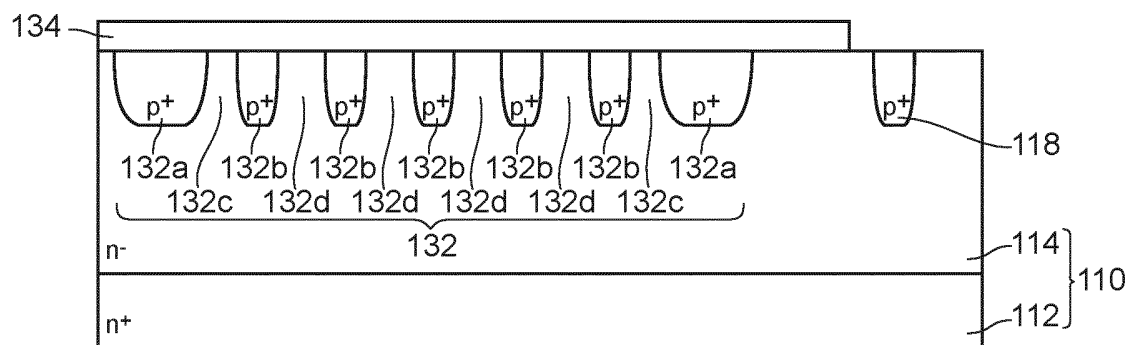


FIG.7A

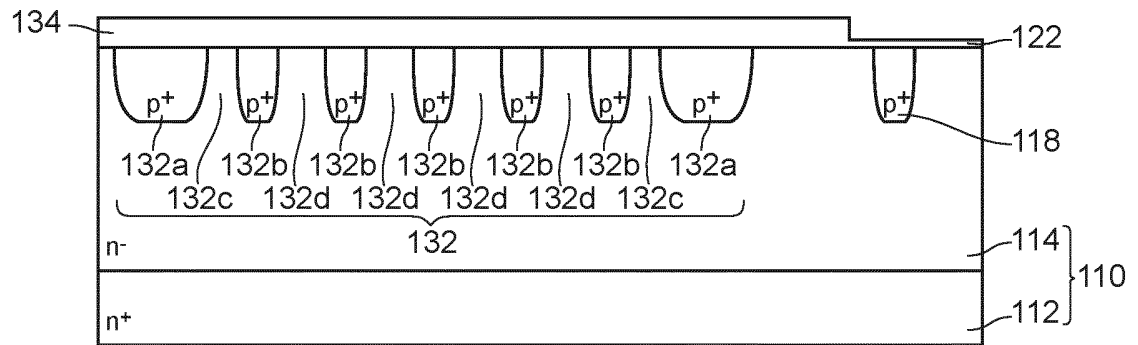


FIG.7B

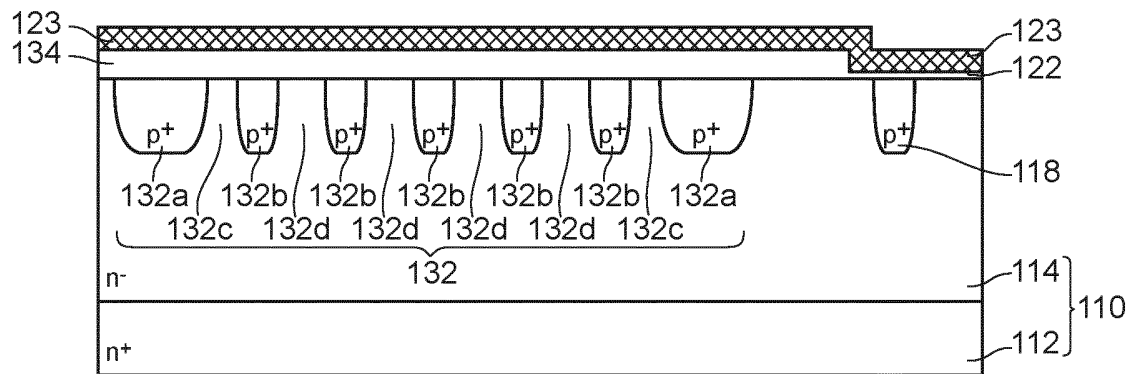


FIG.7C

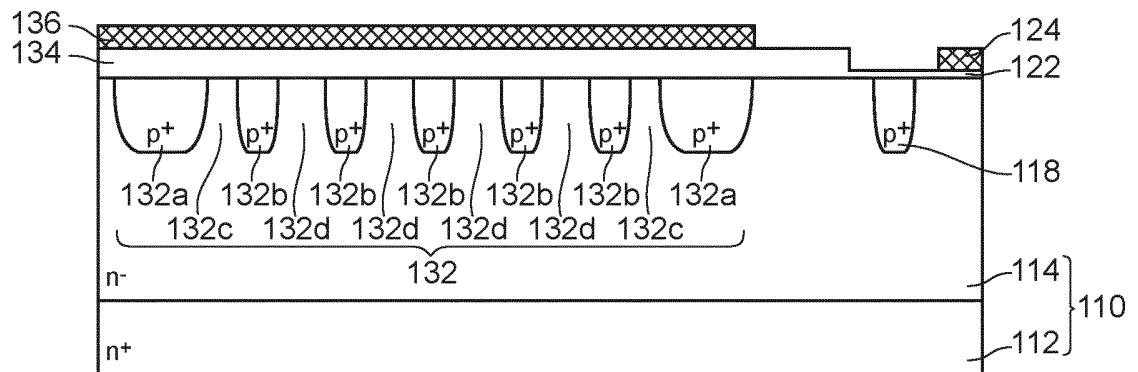


FIG.7A

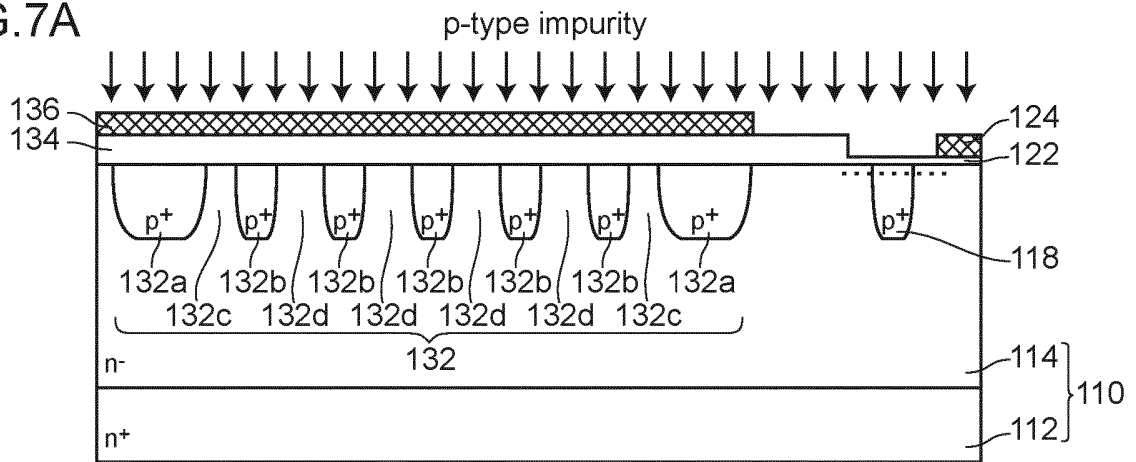


FIG.7B

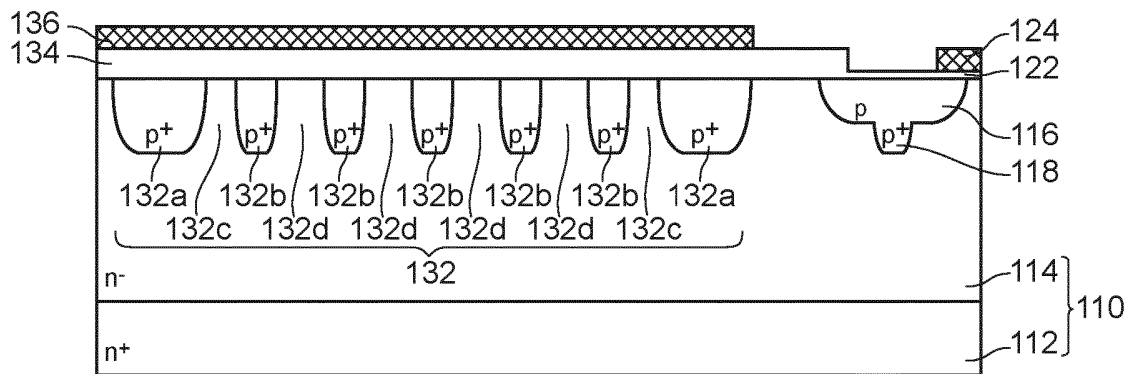


FIG.7C

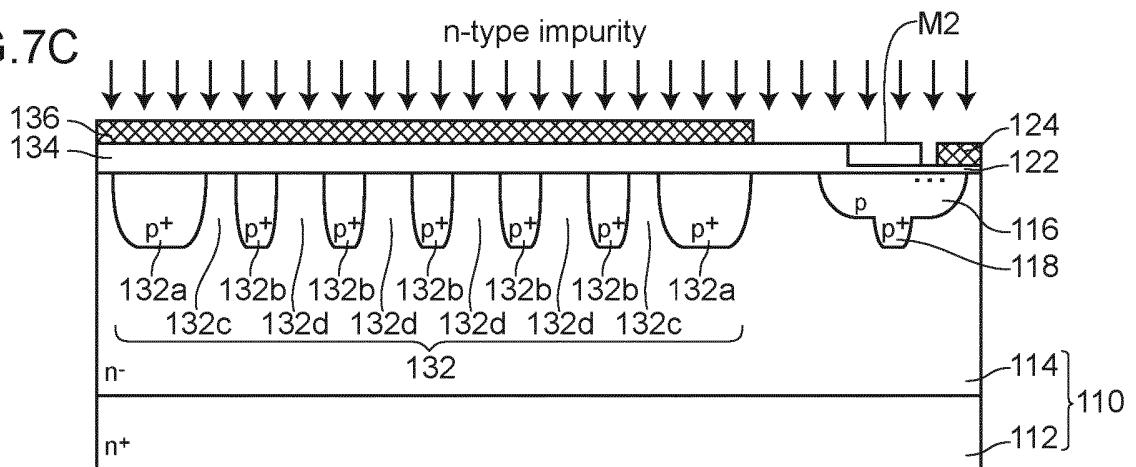


FIG.9A

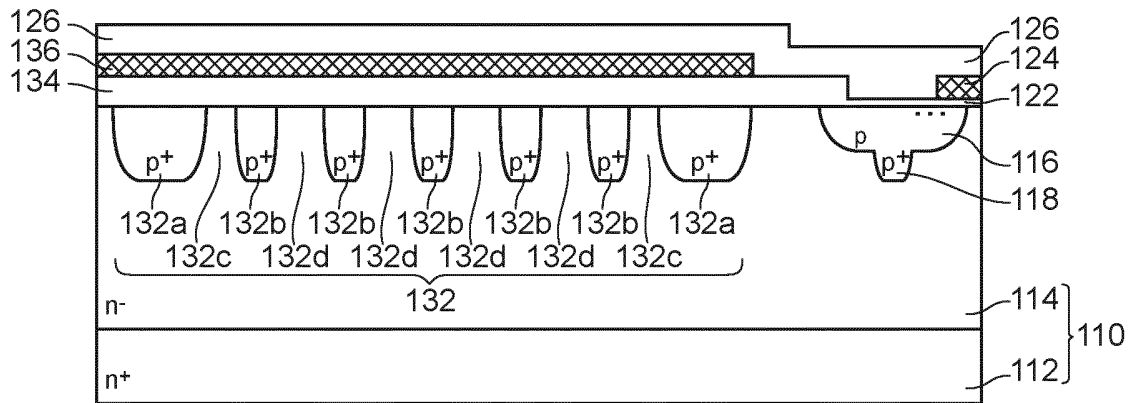


FIG.9B

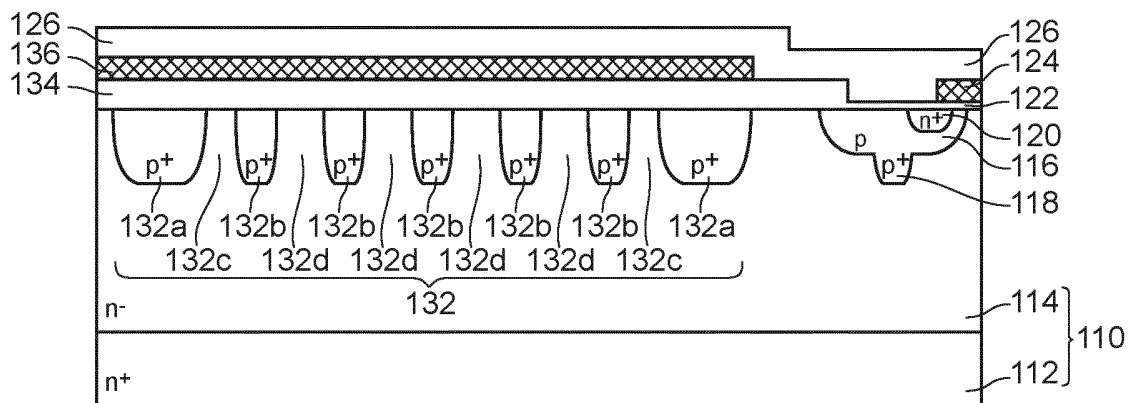


FIG.9C

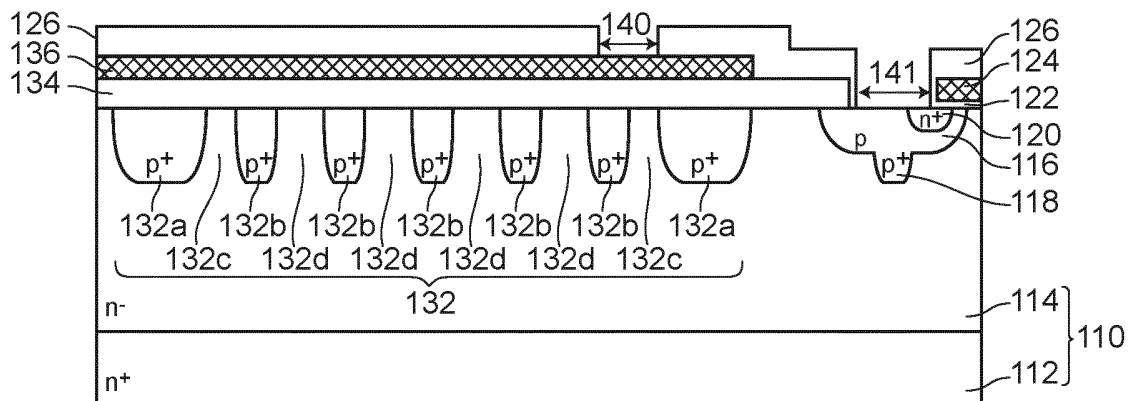


FIG.10A

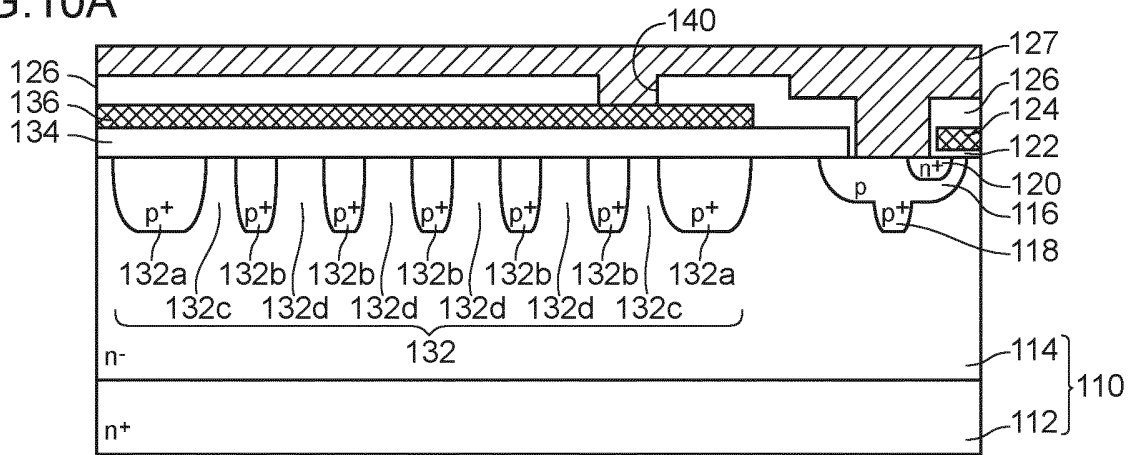


FIG.10B

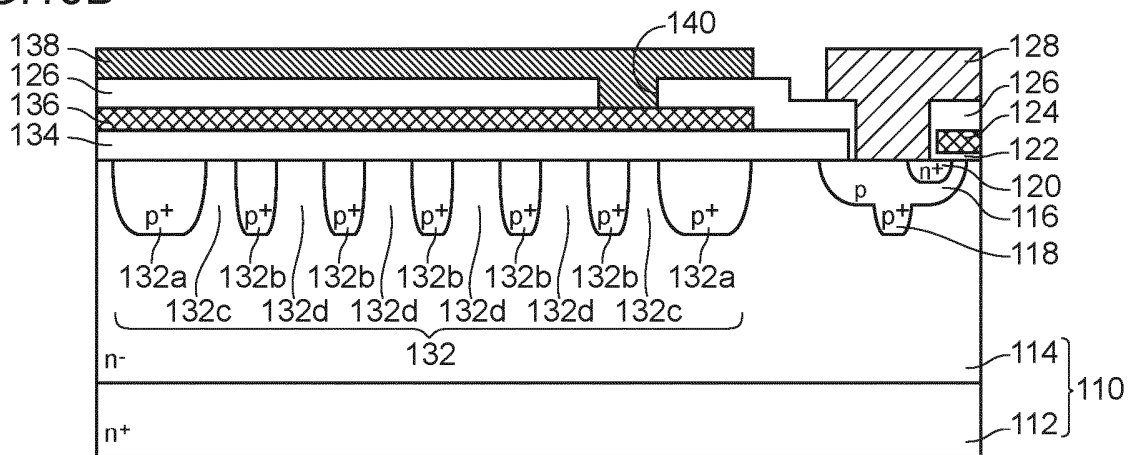
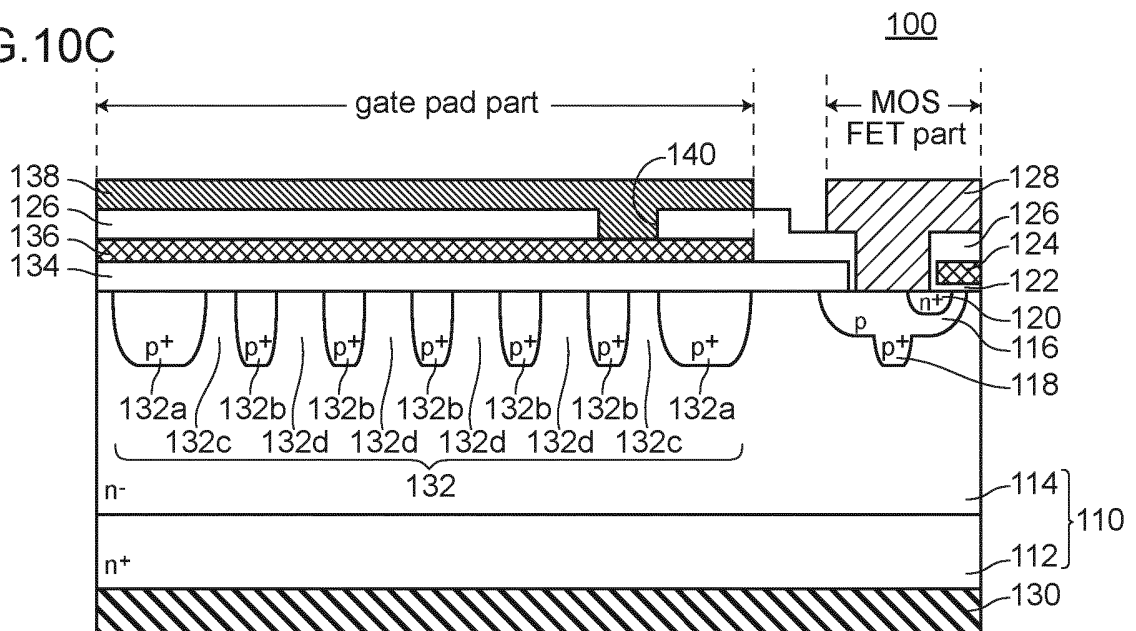


FIG.10C



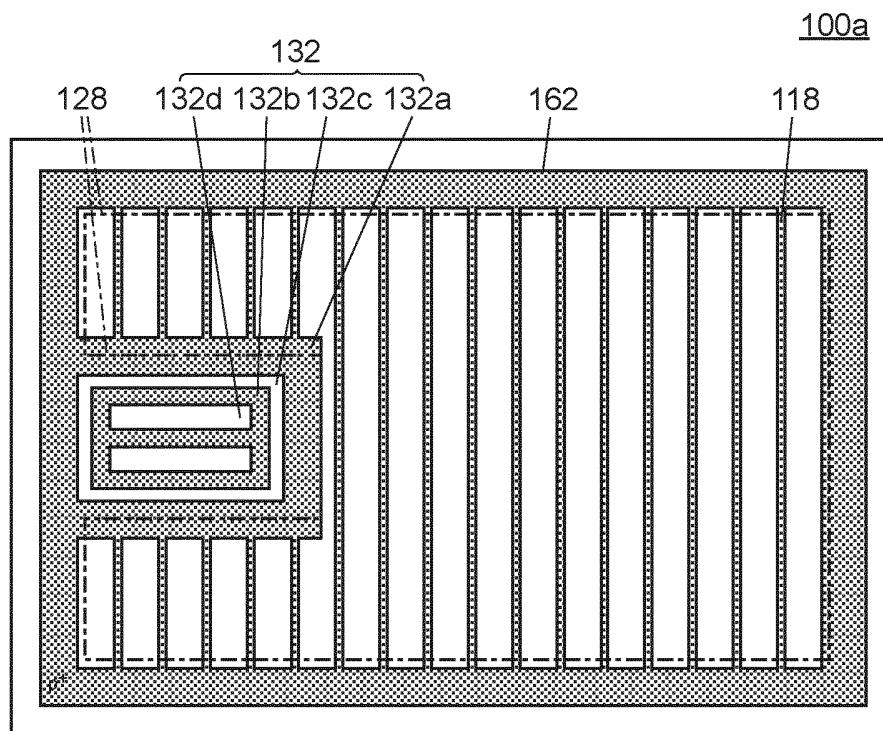


FIG.11

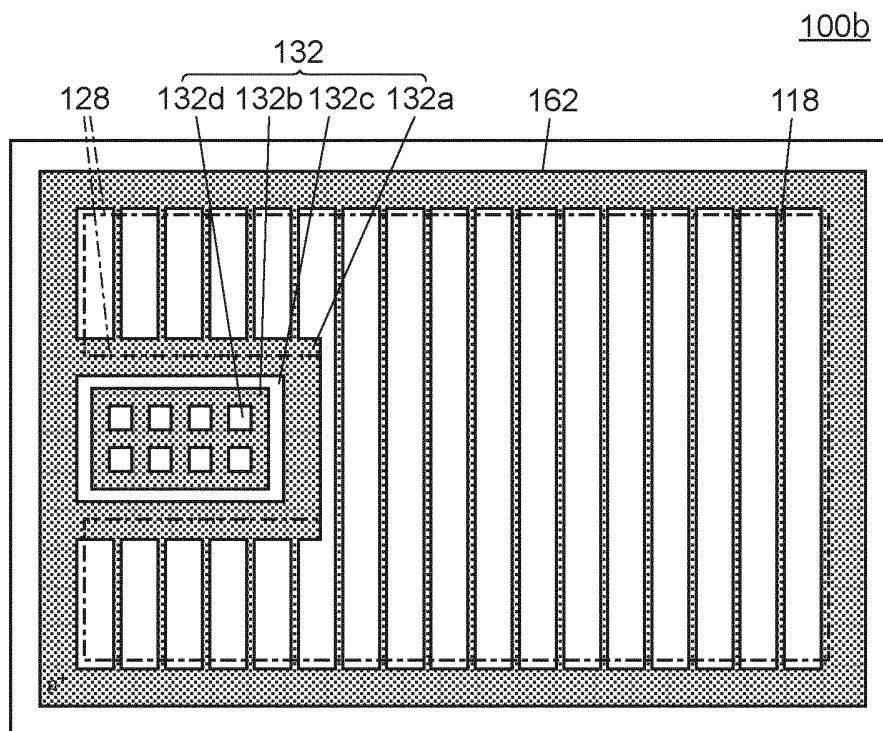


FIG.12

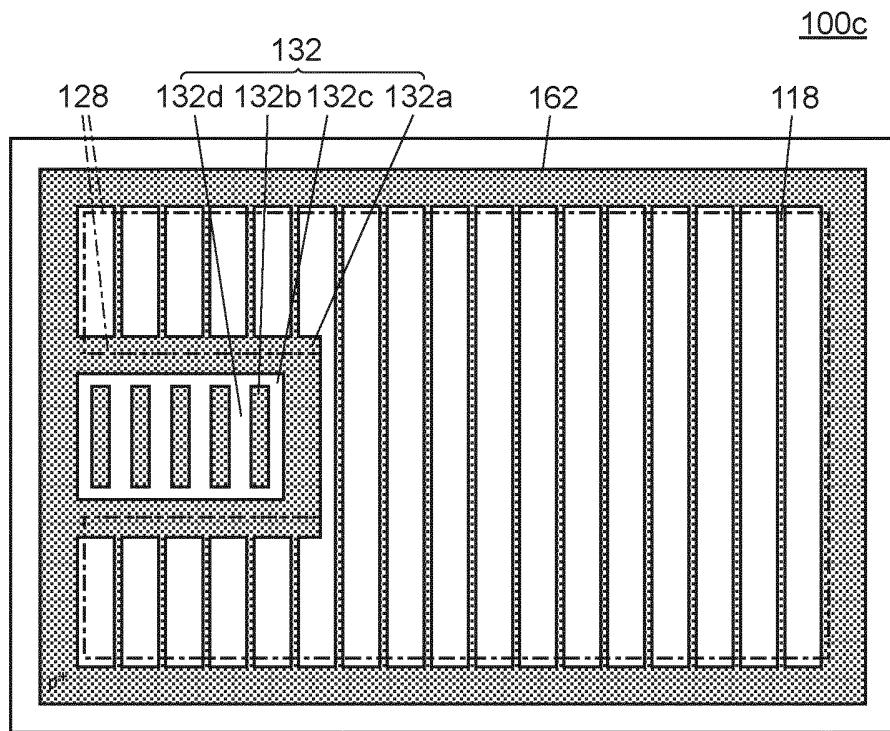


FIG. 13

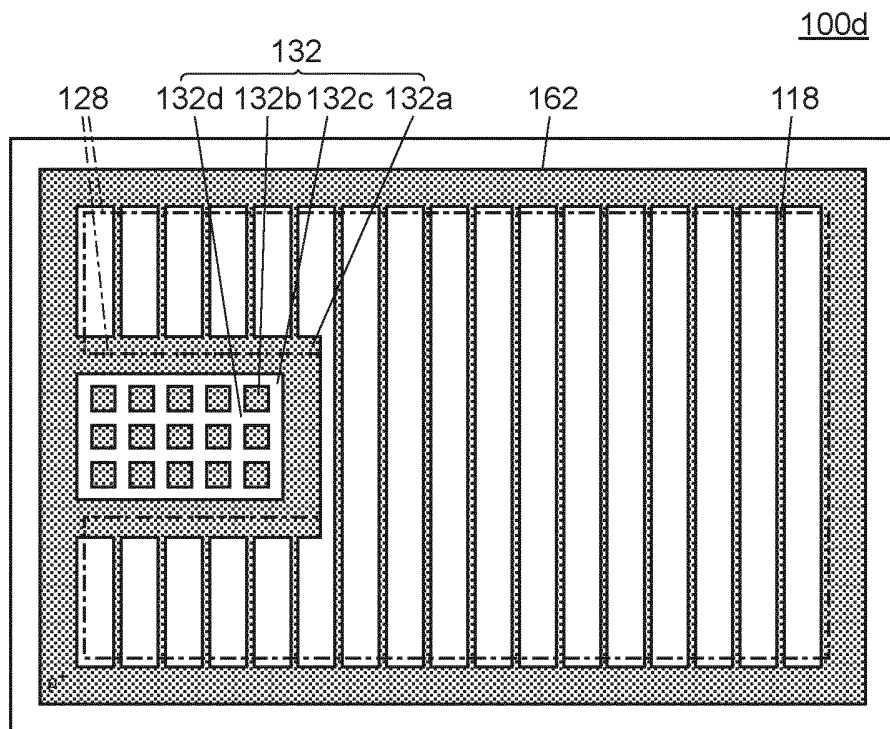


FIG. 14

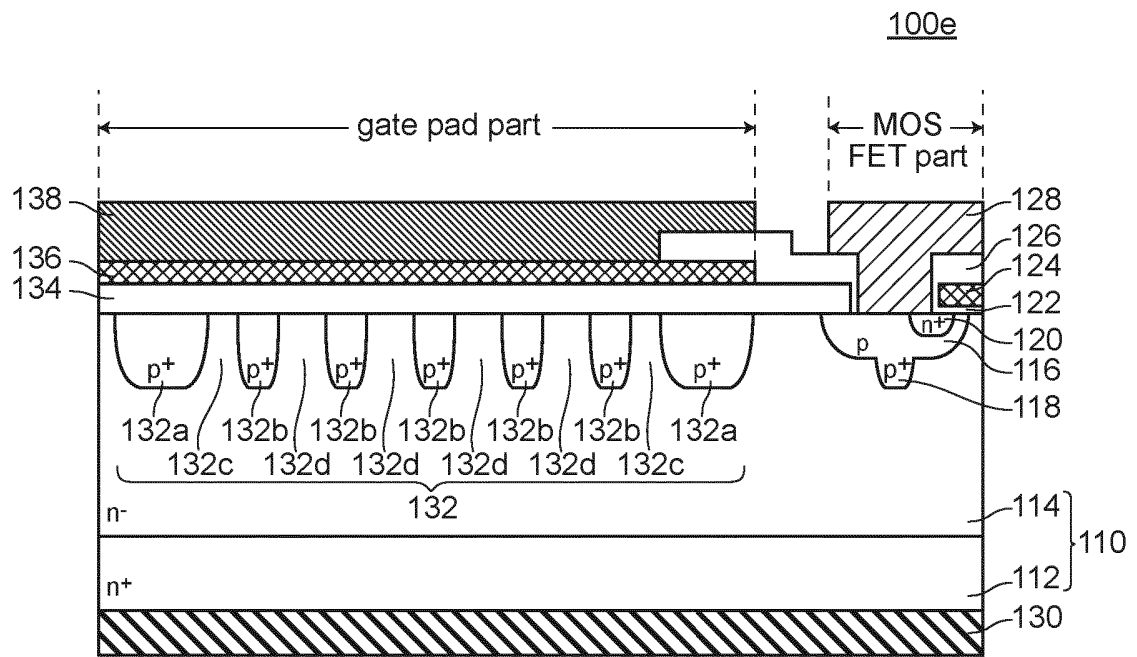


FIG.15

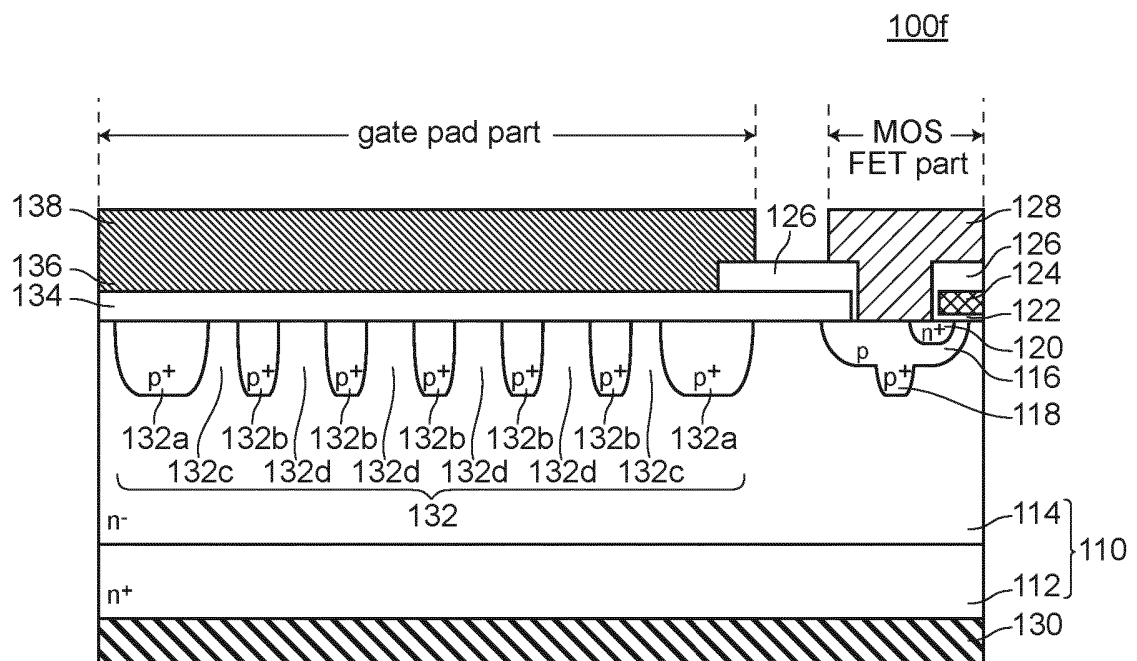


FIG.16

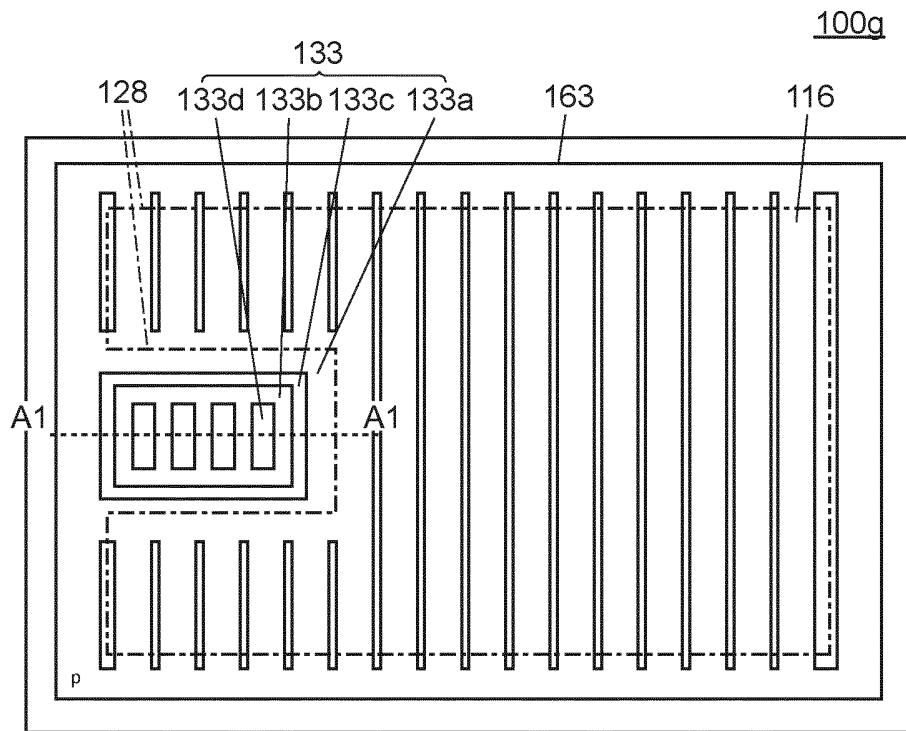


FIG. 17A

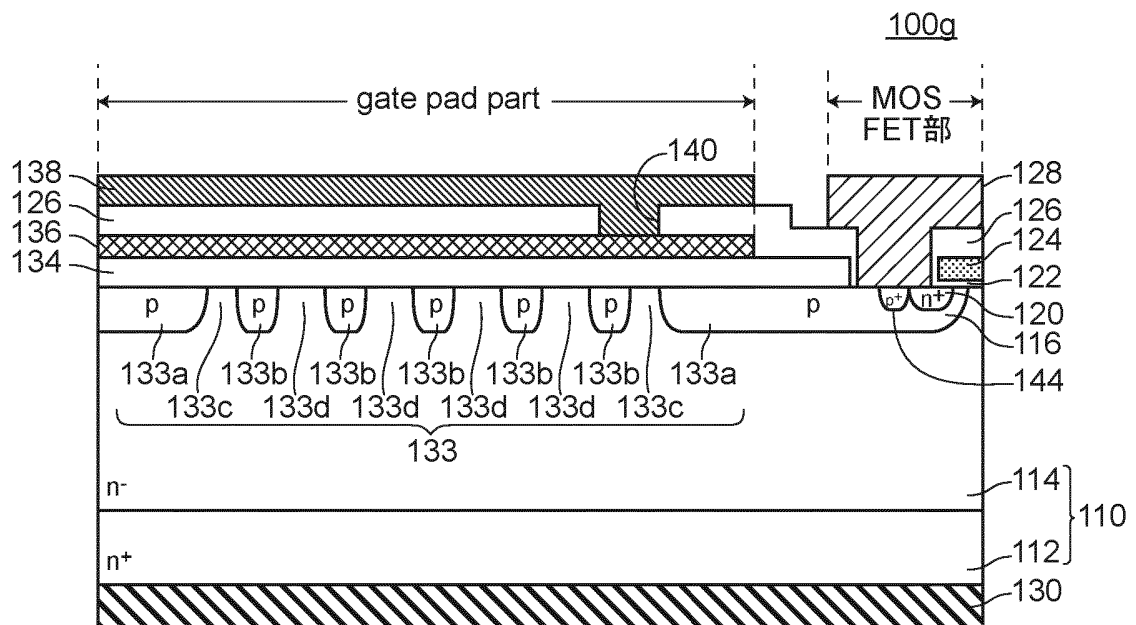


FIG. 17B

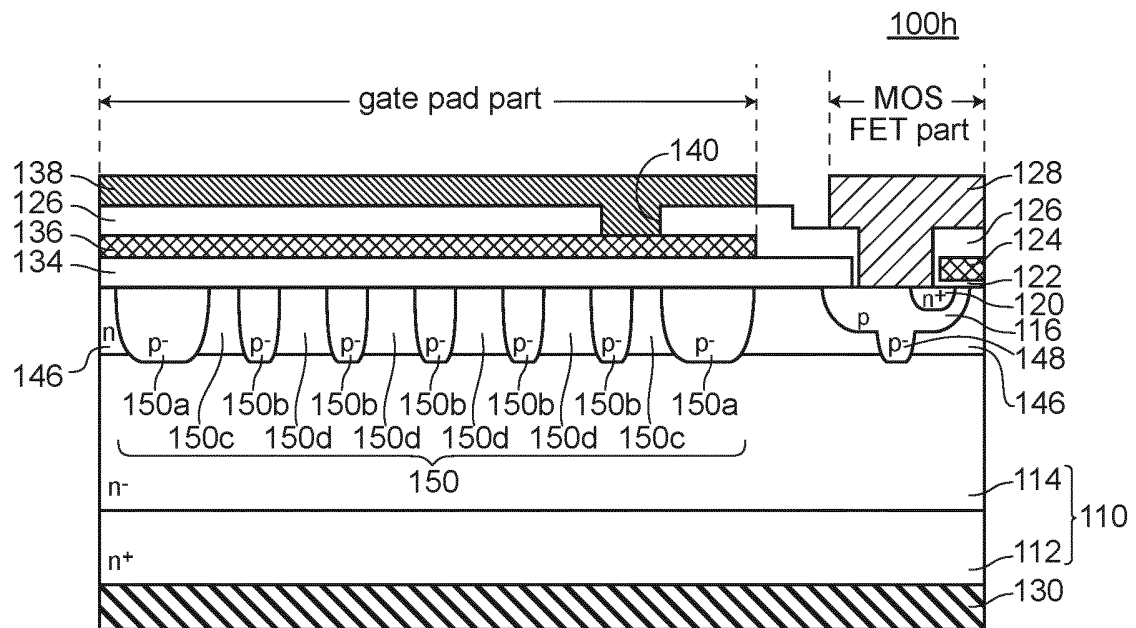


FIG.18

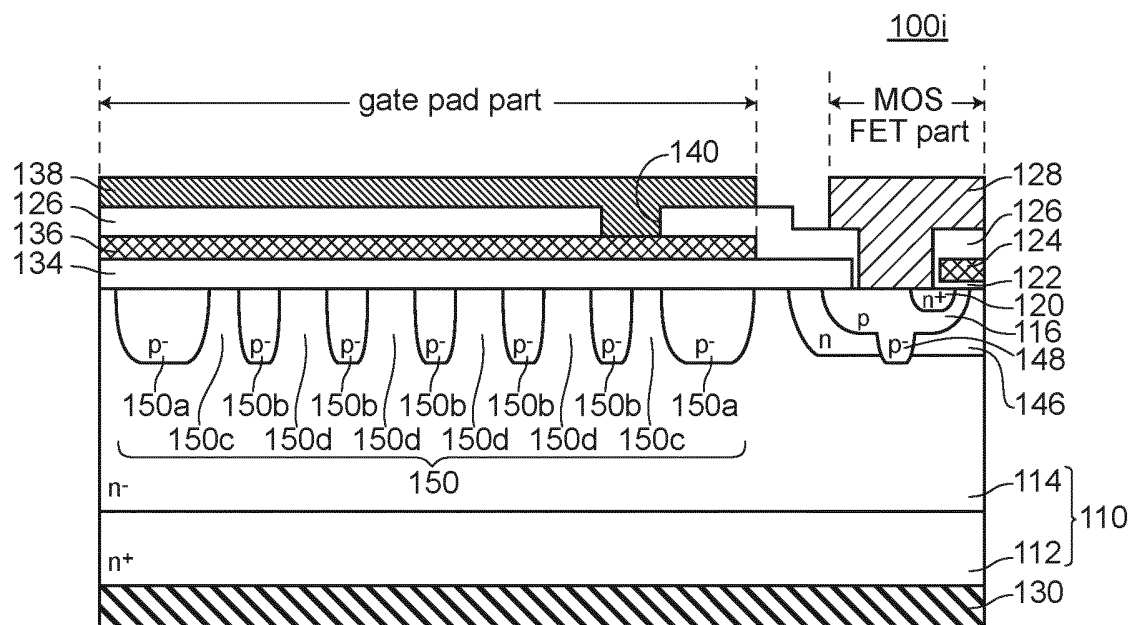


FIG.19

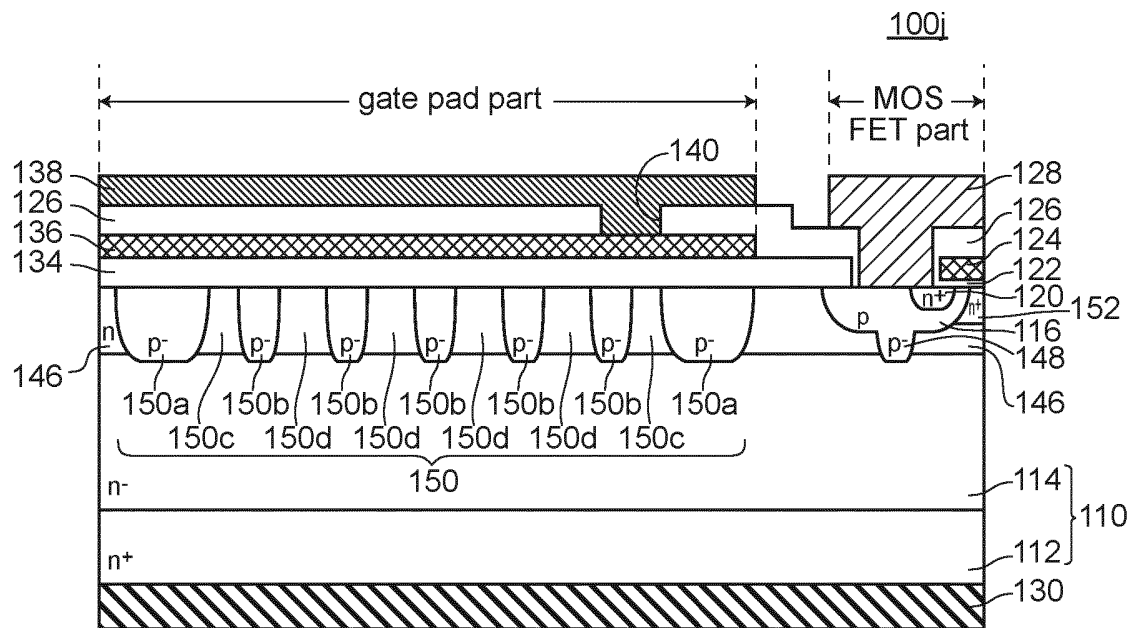


FIG.20A

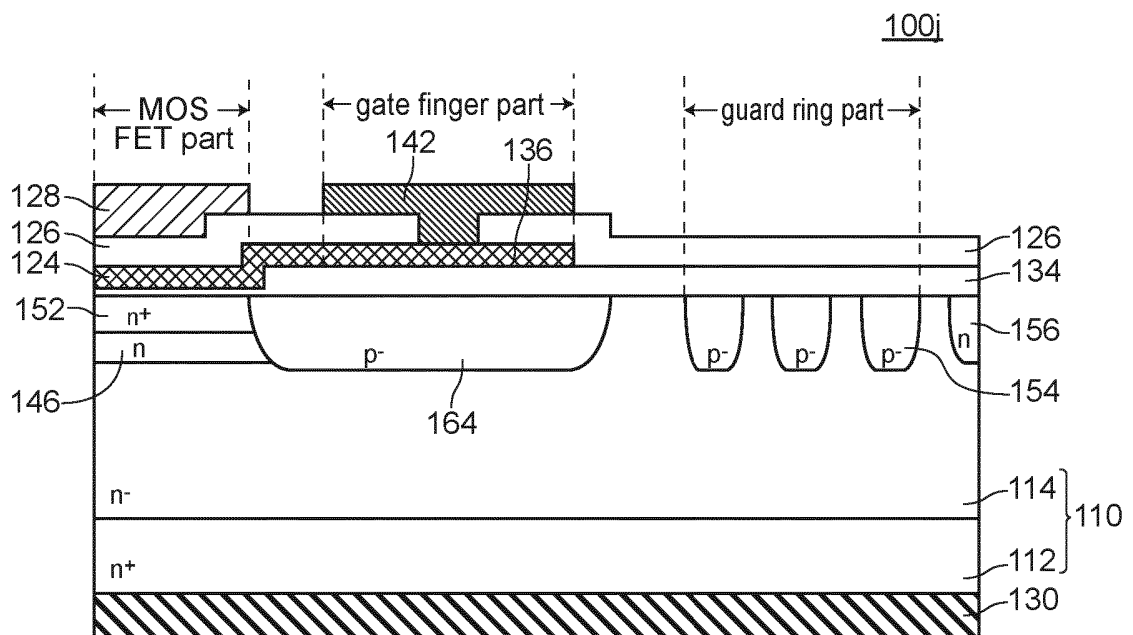


FIG.20B

FIG.21A

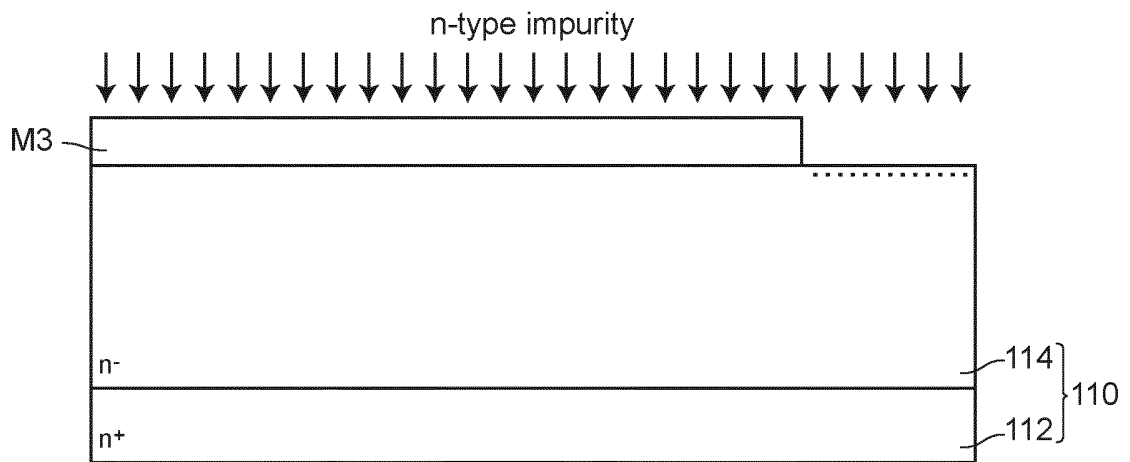


FIG.21B

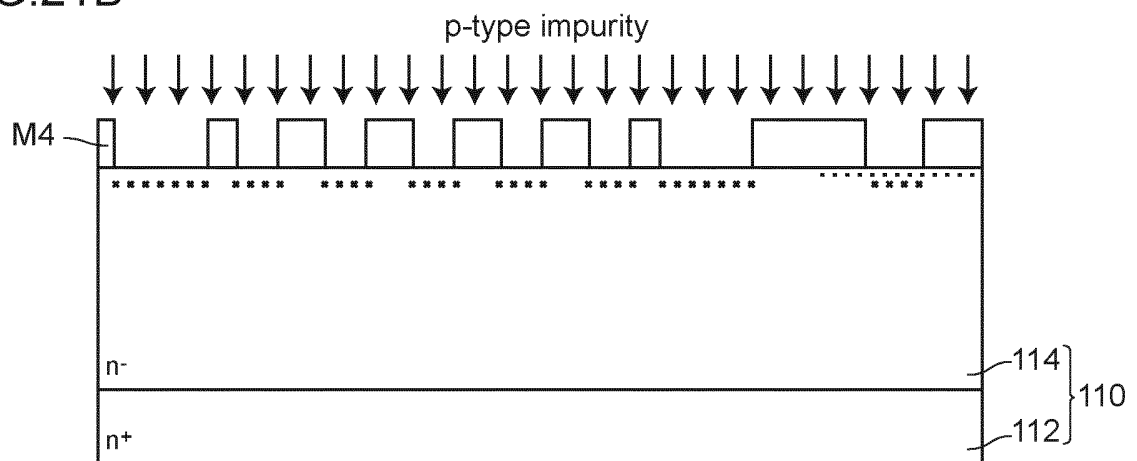
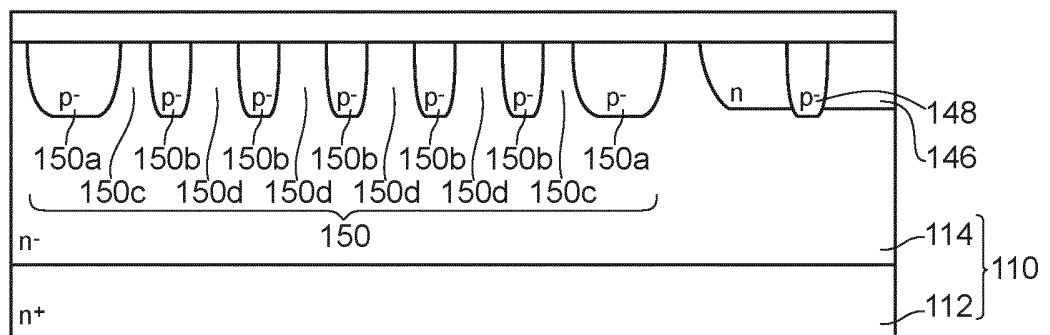


FIG.21C



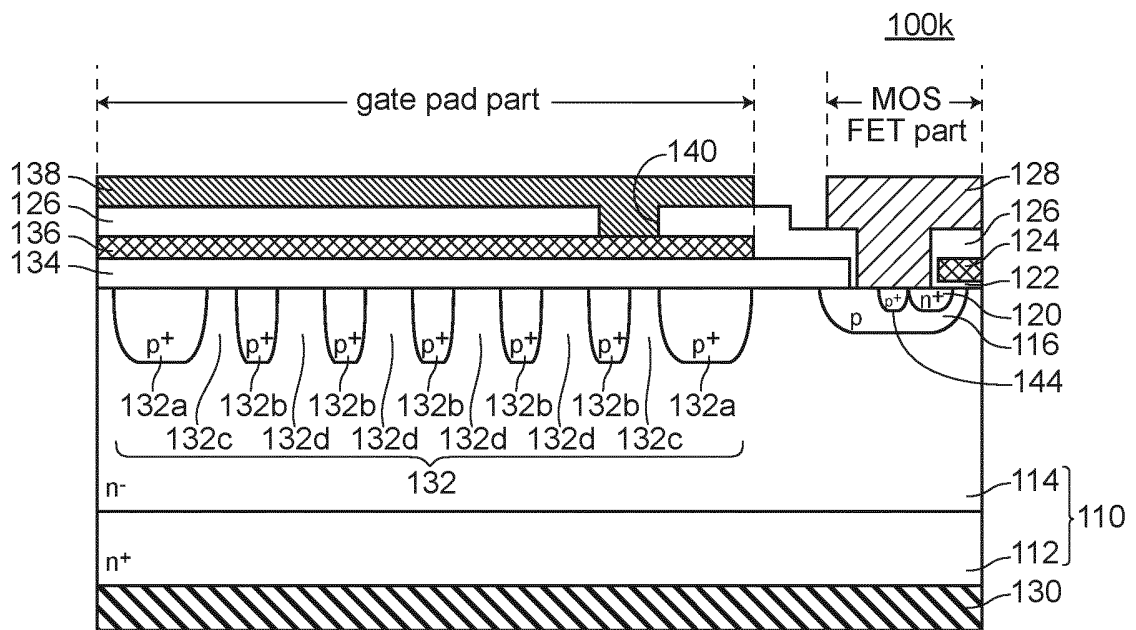


FIG.22A

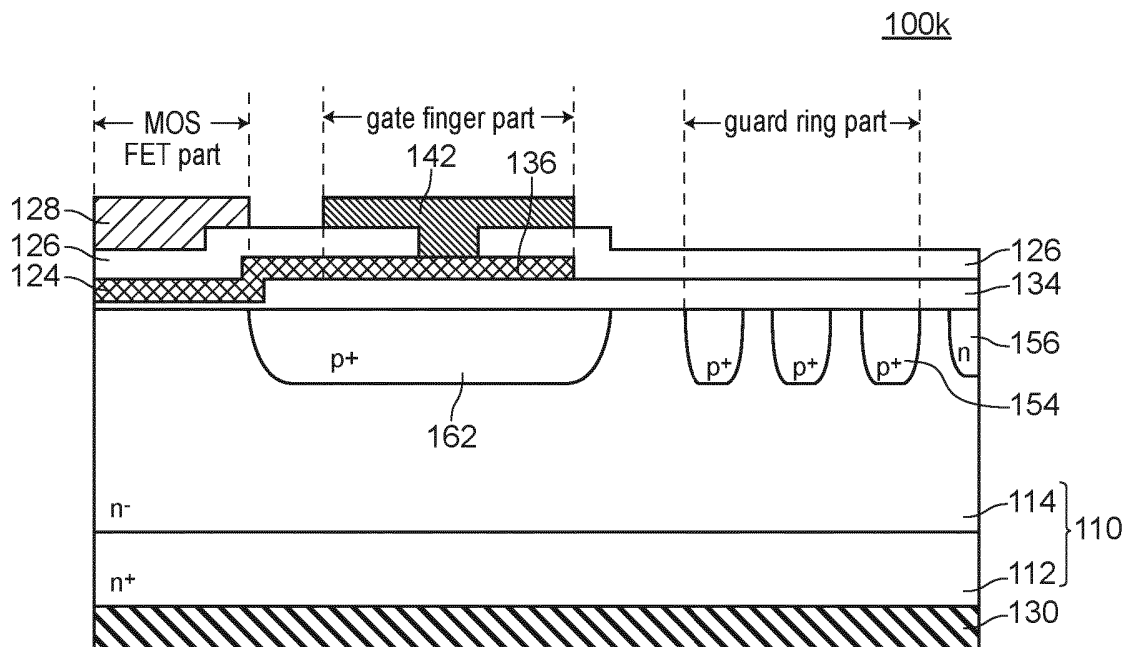


FIG.22B

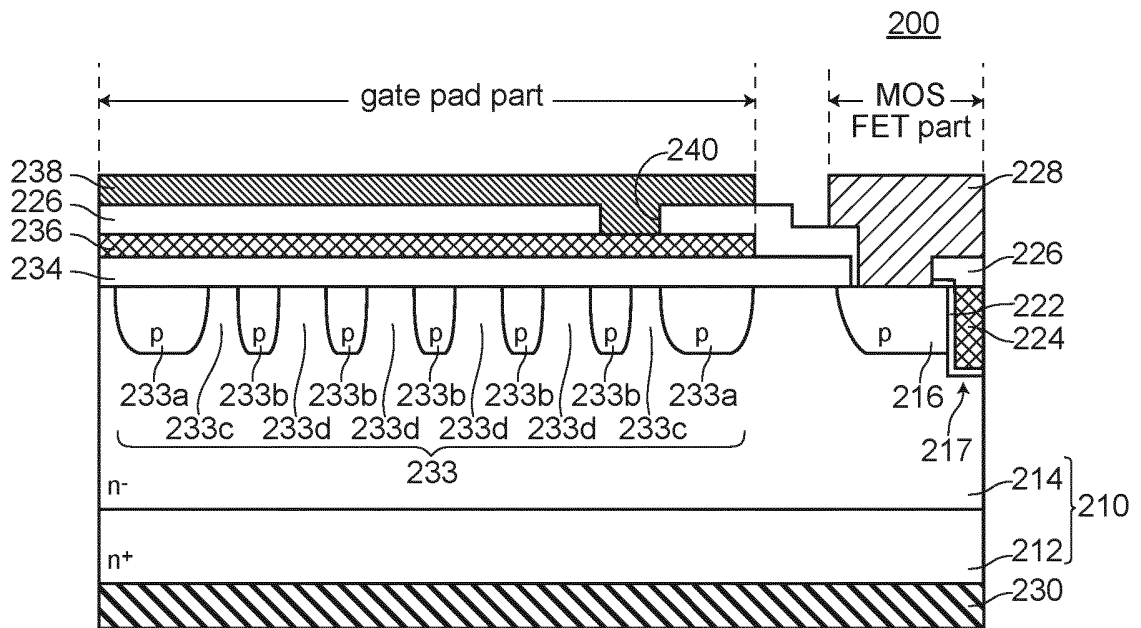


FIG.23

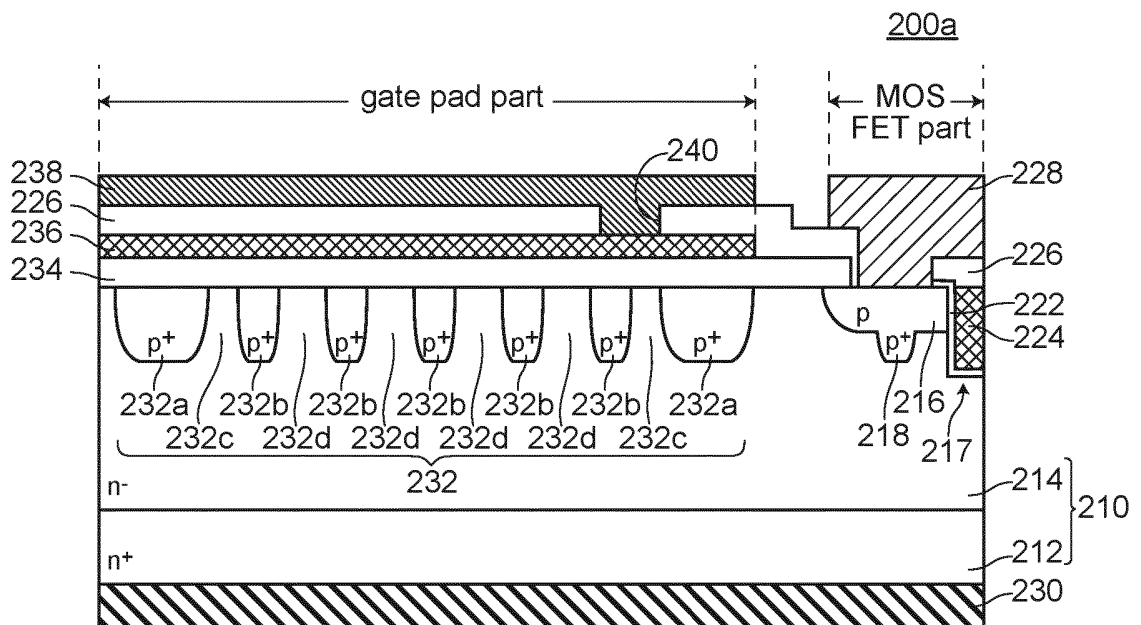


FIG.24

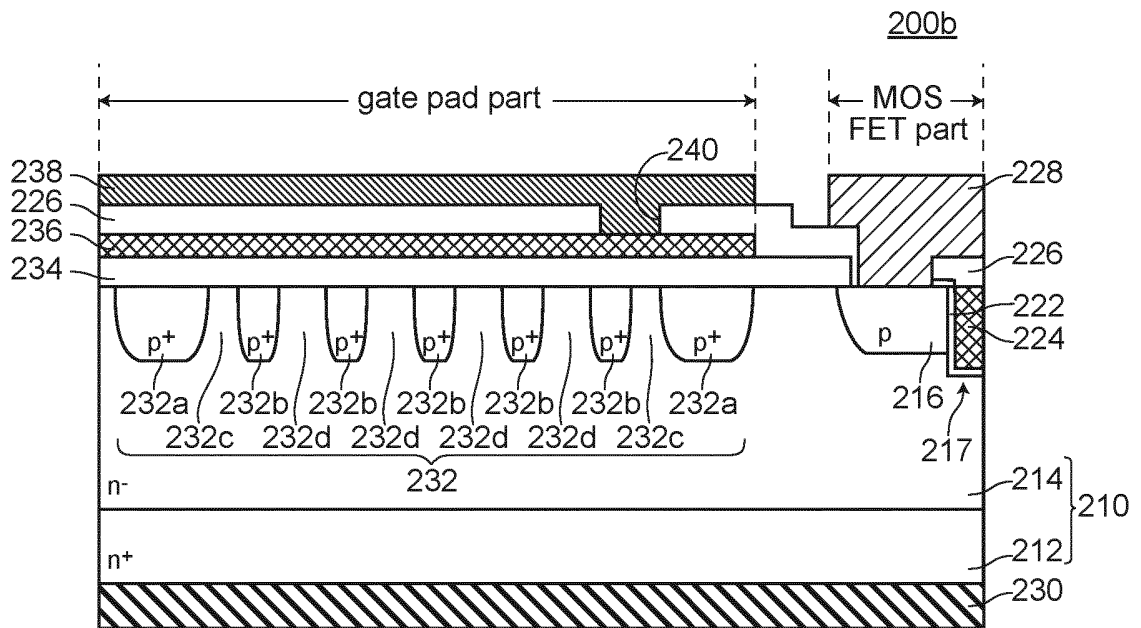


FIG.25

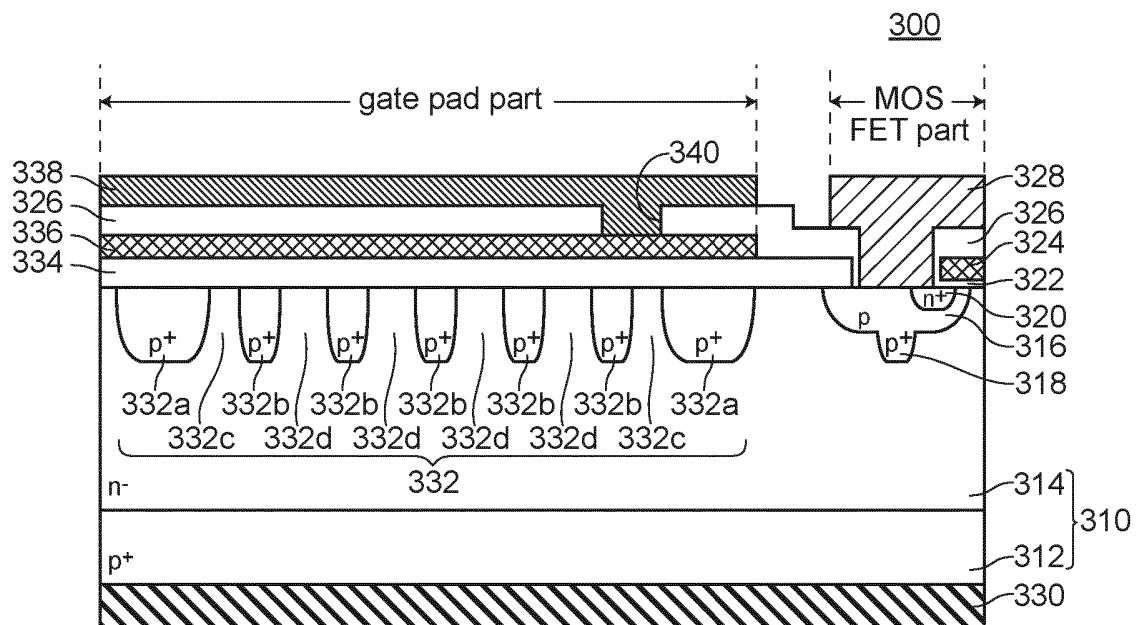


FIG.26

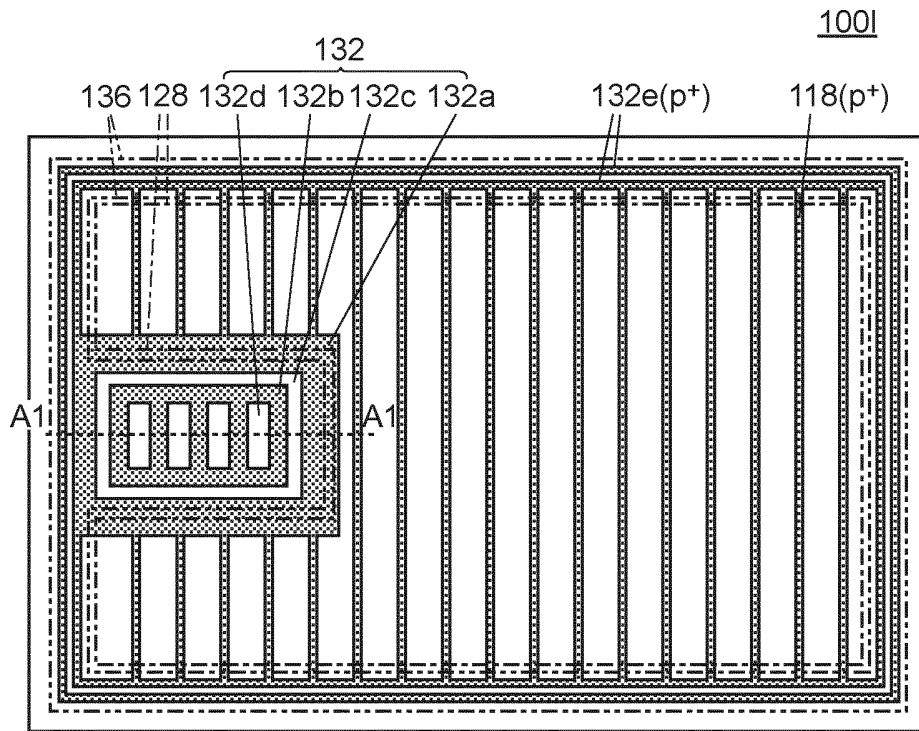


FIG. 27A

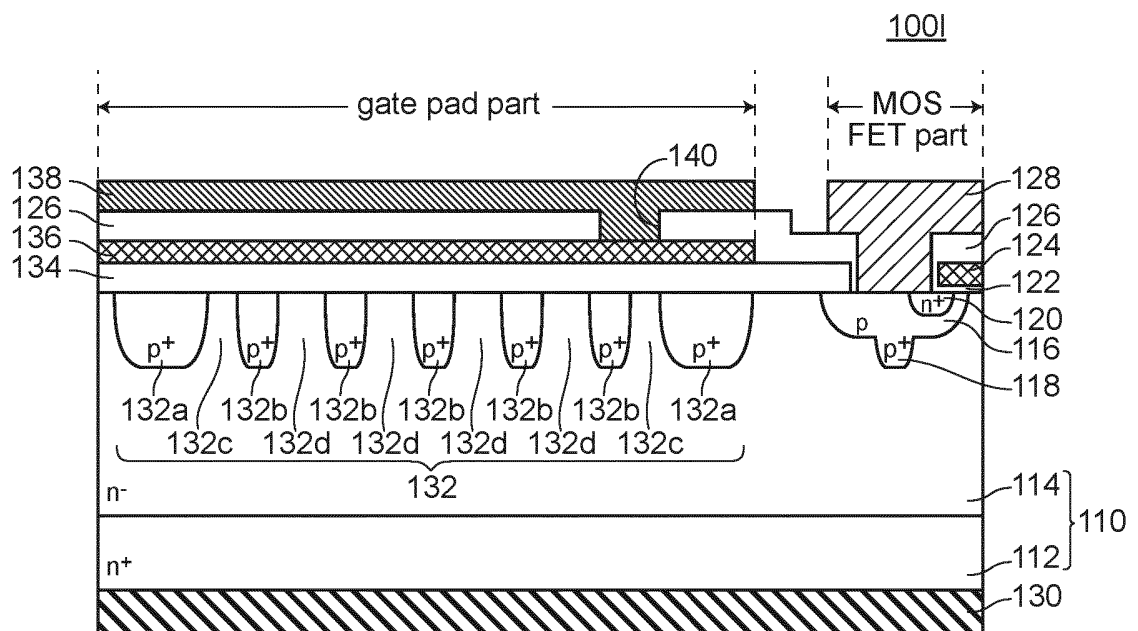


FIG. 27B

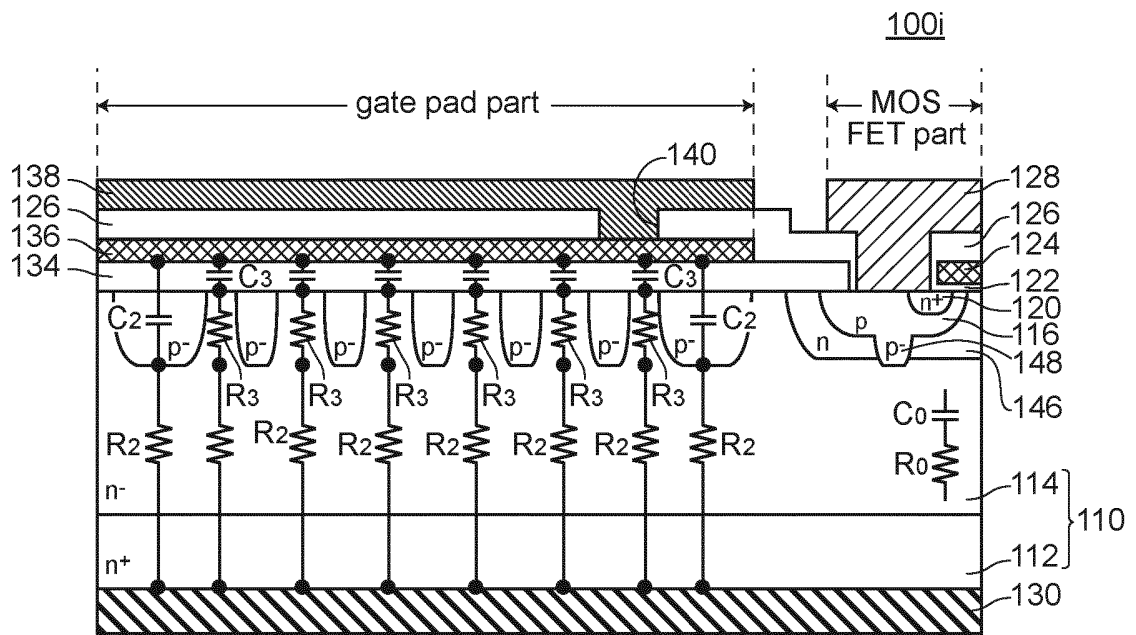


FIG.28A

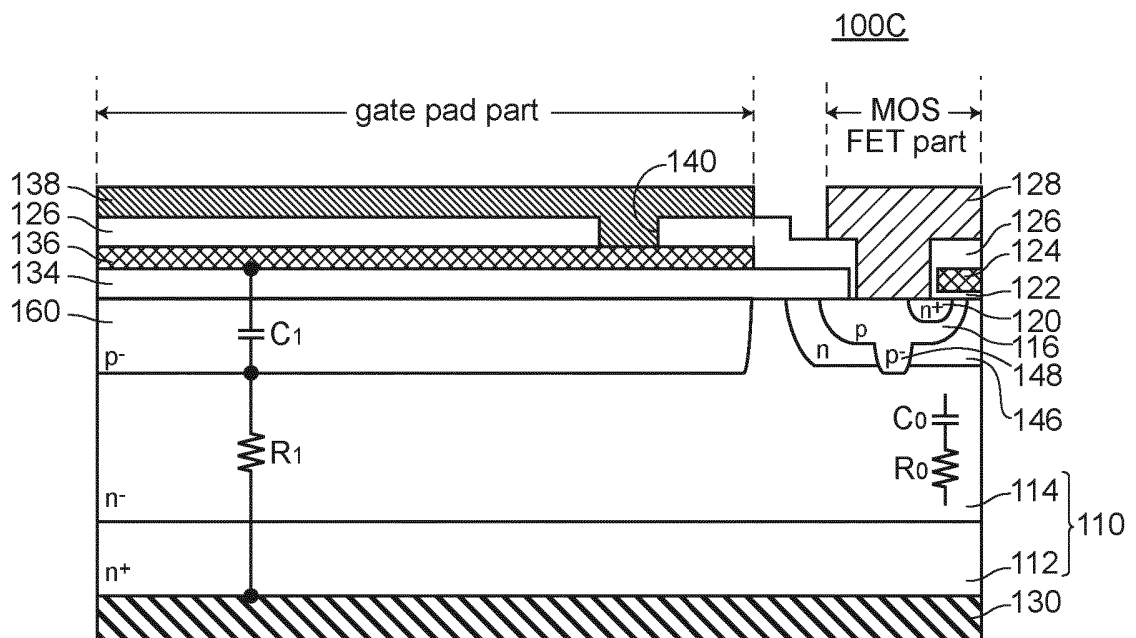


FIG.28B

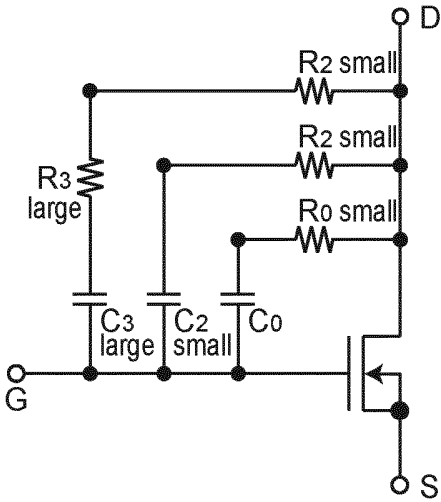


FIG.29A

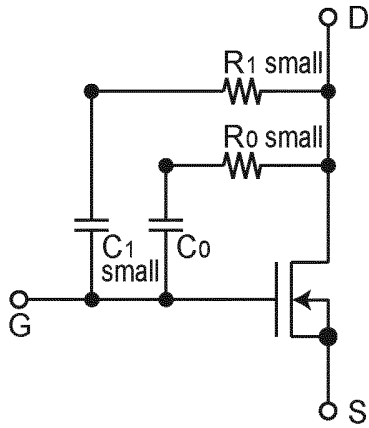


FIG.29B

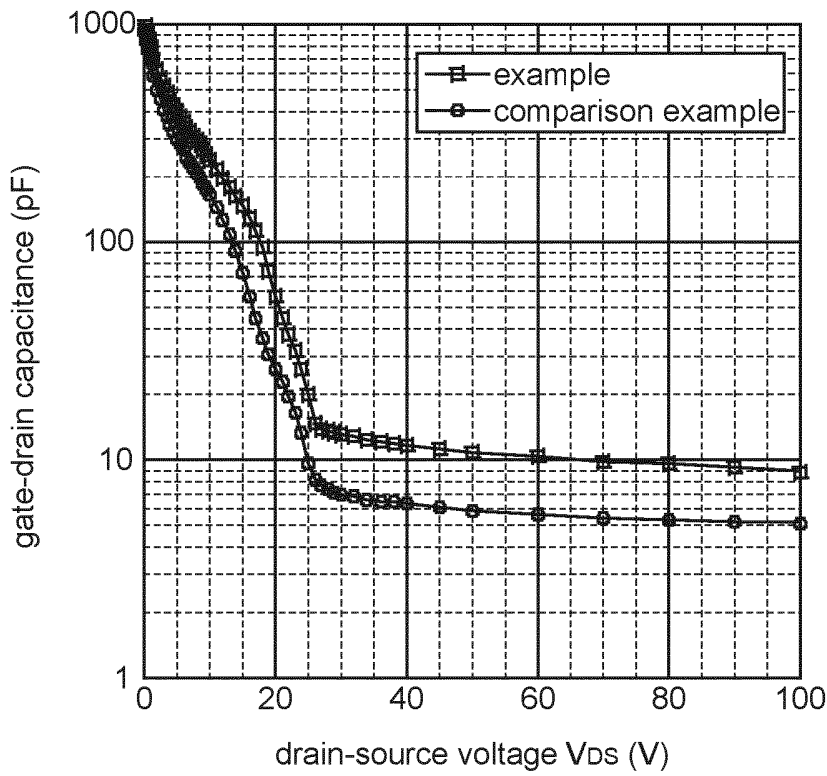


FIG.29C

【図 30】

FIG.30A

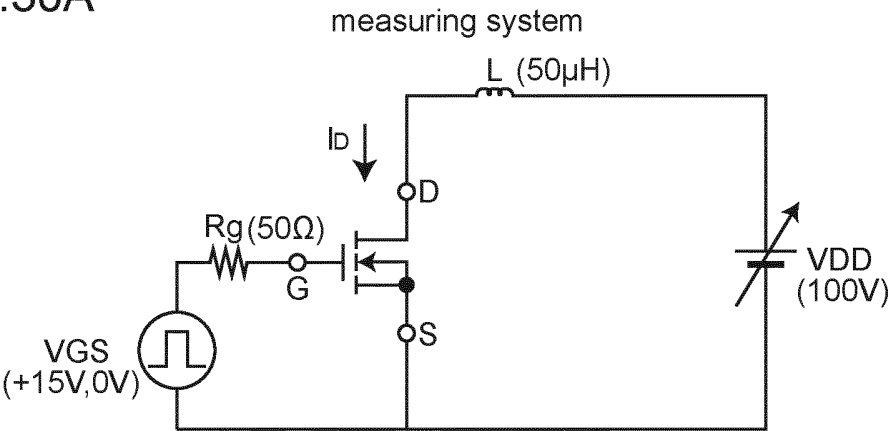


FIG.30B

example

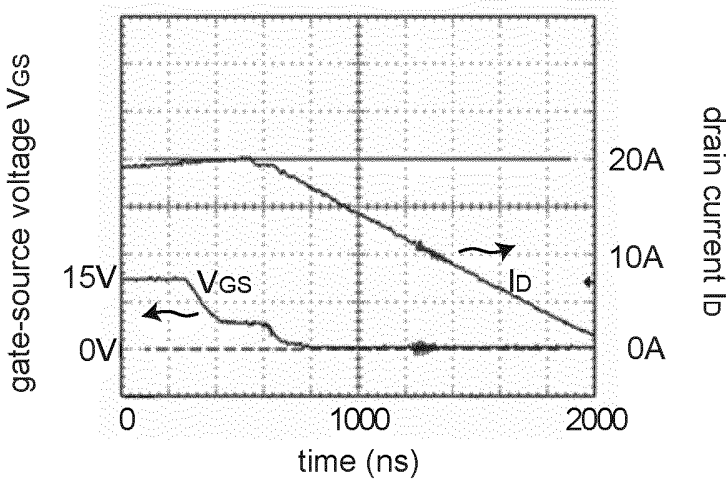
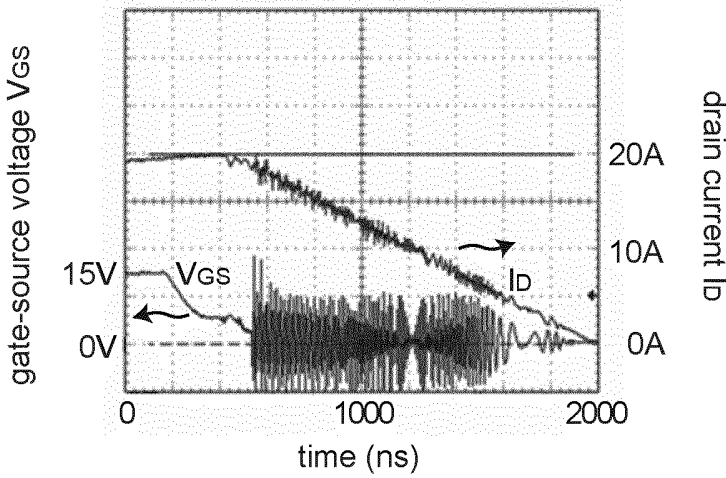


FIG.30C

comparison example



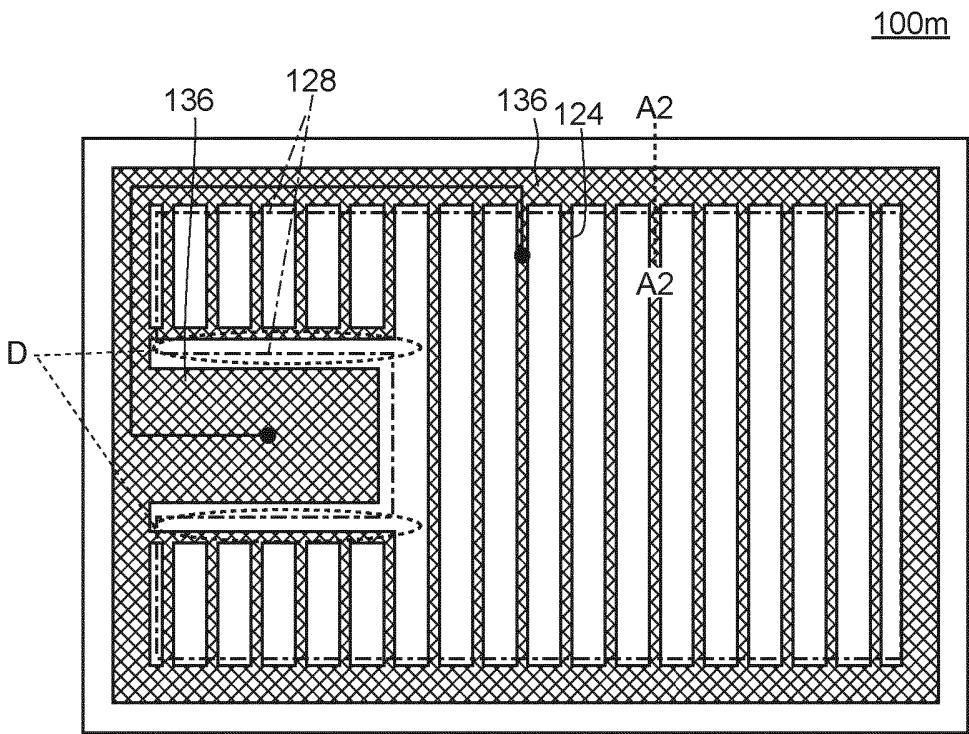


FIG.31

FIG.32A

800

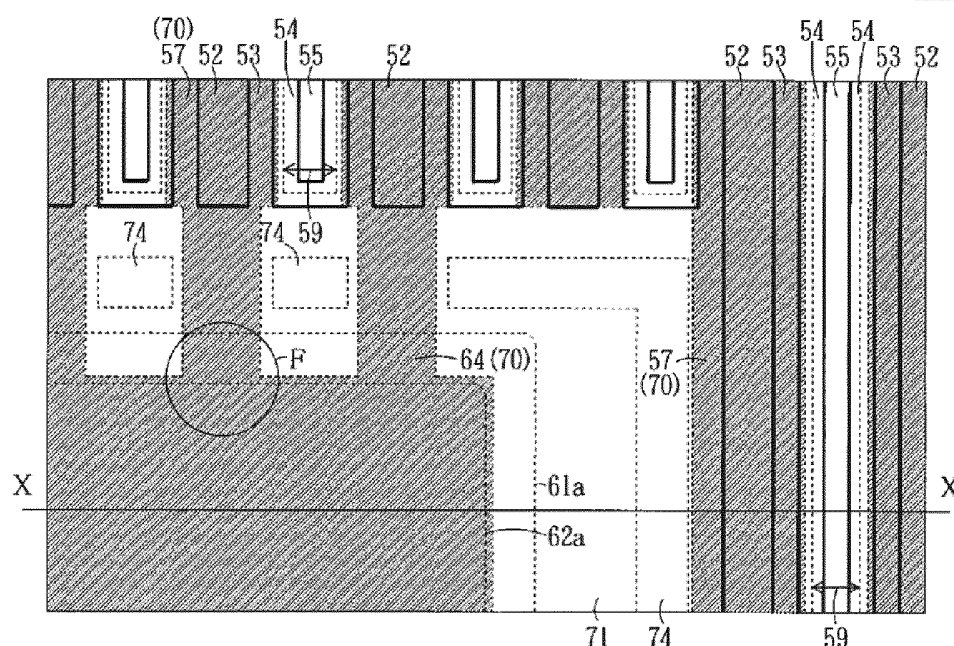
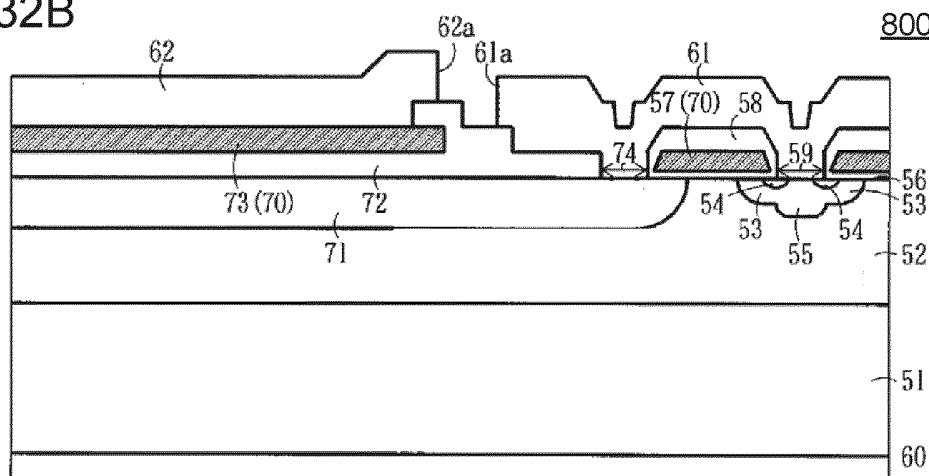


FIG.32B

800



- | | |
|---------------------------------------|-------------------------------------|
| 51 . . . n ⁺ drain layer | 61 . . . source electrode |
| 52 . . . n ⁻ drift layer | 61a . . . source electrode end |
| 53 . . . p base region | 62 . . . gate pad electrode |
| 54 . . . n ⁺ source region | 62a . . . gate pad electrode end |
| 55 . . . p ⁺ well region | 70 . . . poly-silicon film |
| 56 . . . gate insulation film | 71 . . . p region |
| 57 . . . gate electrode | 72 . . . interlayer insulation film |
| 58 . . . interlayer insulation film | 73 . . . conductor |
| 59 . . . source contact hole | 74 . . . p region contact hole |
| 60 . . . drain electrode | |

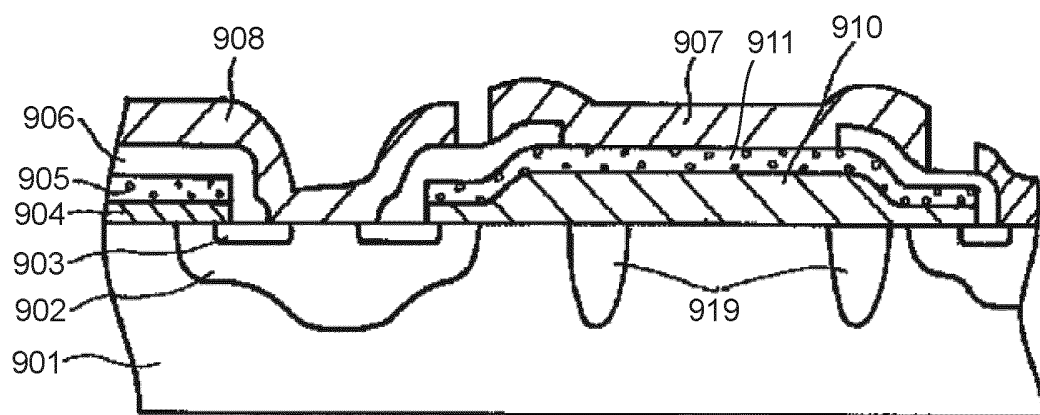
900

FIG.33

Abstract of Disclosure

Provided is a semiconductor device which can suppress a gate oscillation phenomenon which occurs at the time of switching off the semiconductor device while obviating the external connecting of a capacitance and a resistance between a gate and a drain of the semiconductor device.

5 In a semiconductor device provided with a MOSFET part and a gate pad part, the gate pad part includes: a low resistance semiconductor layer 112; a drift layer 114; a poly-silicon layer 136 constituting a conductor layer and a gate pad electrode 138 formed above the drift layer 114 over the whole area of the gate pad part with a field insulation layer 134 interposed therebetween; and a gate

10 oscillation suppressing structure 132, wherein the gate oscillation suppressing structure 132 includes a p⁺-type diffusion region 132a which is disposed along an outer peripheral portion of the gate pad part and is electrically connected with the a source electrode layer 128, and a p⁺-type diffusion region 132b in a floating state and the p-type impurity non-diffusion regions 132c, 132d which are alternately formed in the region surrounded by the p⁺-type diffusion region 132a.

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Rijksdienst voor Ondernemend
Nederland

OCTROOIAANVRAAG NR.
NO 139412
NL 2014503

ONDERZOEKSRAPPORT

BETREFFENDE HET RESULTAAT VAN HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK

RELEVANTE LITERATUUR			
Categorie	Literatuur met, voor zover nodig, aanduiding van specifiek van belang zijnde tekstgedeelten of figuren	Van belang voor conclusie nr.	Classificatie (IPC)
Y	EP 2 421 046 A1 (NXP BV [NL]) 22 februari 2012 (2012-02-22)	1-11, 13-17 12,18	INV. H01L29/06 H01L29/423 H01L29/739 H01L29/78
A	* alinea [0006] * * alinea [0014] - alinea [0023] * * figuren 2,3 *		
Y	US 2012/217555 A1 (SAITO WATARU [JP] ET AL) 30 augustus 2012 (2012-08-30)	1-11, 13-17 12,18	
A	* alinea [0003] - alinea [0005] * * alinea [0059] * * alinea [0062] - alinea [0069] * * alinea [0094] - alinea [0096] * * alinea [0134] - alinea [0137] * * alinea [0144] * * figuren 4-5C,12,19 *		
A	US 2012/205669 A1 (MIURA NARUHISA [JP] ET AL) 16 augustus 2012 (2012-08-16)	1-18	
	* alinea [0030] - alinea [0065] * * figuren 1-6 *		
A	FR 2 768 858 A1 (SGS THOMSON MICROELECTRONICS [FR]) 26 maart 1999 (1999-03-26)	1-18	Onderzochte gebieden van de techniek H01L
	* bladzijde 1, regel 5 - bladzijde 3, regel 5 * * figuren 1A,1B *		
A	US 2008/079078 A1 (NOGUCHI YASUNARI [JP] ET AL) 3 april 2008 (2008-04-03)	1-18	
	* het gehele document *		
Indien gewijzigde conclusies zijn ingediend, heeft dit rapport betrekking op de conclusies ingediend op:			
Plaats van onderzoek:		Datum waarop het onderzoek werd voltooid:	Bevoegd ambtenaar:
München		9 maart 2016	Kostrzewa, Marek
CATEGORIE VAN DE VERMELDE LITERATUUR			
X: de conclusie wordt als niet nieuw of niet inventief beschouwd ten opzichte van deze literatuur Y: de conclusie wordt als niet inventief beschouwd ten opzichte van de combinatie van deze literatuur met andere geïsoleerde literatuur van dezelfde categorie, waarbij de combinatie voor de vakman voor de hand liggend wordt geacht A: niet tot de categorie X of Y behorende literatuur die de stand van de techniek beschrijft C: niet-schriftelijke stand van de techniek P: tussen de voormiddelen en de indieningsdatum gepubliceerde literatuur T: na de indieningsdatum of de voormiddelen gepubliceerde literatuur die niet bezwaarlijk is voor de octrooiaanvraag, maar wordt vermeld ter verheldering van de theorie of het principe dat ten grondslag ligt aan de uitvinding E: eerdere octrooiaanvragen, gepubliceerd op of na de indieningsdatum, waarin dezelfde uitvinding wordt beschreven D: in de octrooiaanvraag vermeld L: om andere redenen vermelde literatuur B: na de indieningsdatum of voormiddelen gepubliceerde literatuur			

**AANHANGSEL BEHORENDE BIJ HET RAPPORT BETREFFENDE
HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK,
UITGEVOERD IN DE OCTROOIAANVRAGE NR.**

NO 139412
NL 2014503

Het aanhangsel bevat een opgave van elders gepubliceerde octrooiaanvragen of octrooien (zogenaamde leden van dezelfde octroofamilie), die overeenkomen met octrooschriften genoemd in het rapport.

De opgave is samengesteld aan de hand van gegevens uit het computerbestand van het Europees Octrooibureau per

De juistheid en volledigheid van deze opgave wordt noch door het Europees Octrooibureau, noch door het Bureau voor de Industriële eigendom gegarandeerd; de gegevens worden verstrekt voor informatiedoeleinden.

09-03-2016

In het rapport genoemd octrooigecchrift		Datum van publicatie	Overeenkomst(e) geschrift(en)	Datum van publicatie
EP 2421046	A1	22-02-2012	GEEN	
US 2012217555	A1	30-08-2012	CN 102623499 A	01-08-2012
			JP 5665567 B2	04-02-2015
			JP 2012156333 A	16-08-2012
			US 2012217555 A1	30-08-2012
			US 2014319599 A1	30-10-2014
			US 2016043213 A1	11-02-2016
US 2012205669	A1	16-08-2012	CN 102576728 A	11-07-2012
			DE 112009005320 T5	22-11-2012
			JP 4962664 B2	27-06-2012
			KR 20120051774 A	22-05-2012
			US 2012205669 A1	16-08-2012
			WO 2011045834 A1	21-04-2011
FR 2768858	A1	26-03-1999	GEEN	
US 2008079078	A1	03-04-2008	CN 101154664 A	02-04-2008
			JP 5511124 B2	04-06-2014
			JP 2008085189 A	10-04-2008
			US 2008079078 A1	03-04-2008
			US 2010148268 A1	17-06-2010

SCHRIFTELIJKE OPINIE

DOSSIER NUMMER NO139412	INDIENINGSDATUM 23.03.2015	VOORRANGSDATUM 31.03.2014	AANVRAAGNUMMER NL2014503
CLASSIFICATIE INV. H01L29/06 H01L29/423 H01L29/739 H01L29/78			
AANVRAGER Shindengen Electric Manufacturing Co., Ltd.			

Deze schriftelijke opinie bevat een toelichting op de volgende onderdelen:

- ☒ Onderdeel I Basis van de schriftelijke opinie
- ☐ Onderdeel II Voorrang
- ☐ Onderdeel III Vaststelling nieuwheid, inventiviteit en industriële toepasbaarheid niet mogelijk
- ☐ Onderdeel IV De aanvraag heeft betrekking op meer dan één uitvinding
- ☒ Onderdeel V Gemotiveerde verklaring ten aanzien van nieuwheid, inventiviteit en industriële toepasbaarheid
- ☐ Onderdeel VI Andere geciteerde documenten
- ☒ Onderdeel VII Overige gebreken
- ☐ Onderdeel VIII Overige opmerkingen

	DE BEVOEGDE AMBTENAAR Kostrzewa, Marek
--	---

SCHRIFTELIJKE OPINIE

Aanvraag nr.
NL2014503

Onderdeel I Basis van de Schriftelijke Opinie

1. Deze schriftelijke opinie is opgesteld op basis van de meest recente conclusies ingediend voor aanvang van het onderzoek.
2. Met betrekking tot **nucleotide en/of aminozuur sequenties** die genoemd worden in de aanvraag en relevant zijn voor de uitvinding zoals beschreven in de conclusies, is dit onderzoek gedaan op basis van:
 - a. type materiaal:
 - ☐ sequentie opsomming
 - ☐ tabel met betrekking tot de sequentie lijst
 - b. vorm van het materiaal:
 - ☐ op papier
 - ☐ in elektronische vorm
 - c. moment van indiening/aanlevering:
 - ☐ opgenomen in de aanvraag zoals ingediend
 - ☐ samen met de aanvraag elektronisch ingediend
 - ☐ later aangeleverd voor het onderzoek
3. ☐ In geval er meer dan één versie of kopie van een sequentie opsomming of tabel met betrekking op een sequentie is ingediend of aangeleverd, zijn de benodigde verklaringen ingediend dat de informatie in de latere of additionele kopieën identiek is aan de aanvraag zoals ingediend of niet meer informatie bevatten dan de aanvraag zoals oorspronkelijk werd ingediend.
4. Overige opmerkingen:

SCHRIFTELIJKE OPINIE

Aanvraag nr.
NL2014503

Onderdeel V Gemotiveerde verklaring ten aanzien van nieuwheid, inventiviteit en industriële toepasbaarheid

1. Verklaring

Nieuwheid	Ja: Conclusies 1-18 Nee: Conclusies
Inventiviteit	Ja: Conclusies 12, 18 Nee: Conclusies 1-11, 13-17
Industriële toepasbaarheid	Ja: Conclusies 1-18 Nee: Conclusies

2. Citaties en toelichting:

Zie aparte bladzijde

Onderdeel VII Overige gebreken

De volgende gebreken in de vorm of inhoud van de aanvraag zijn opgemerkt:

Zie aparte bladzijde

Item V

1 Reference is made to the following document:

D1 EP 2 421 046 A1 (NXP BV [NL]) 22 februari 2012 (2012-02-22)

D2 US 2012/217555 A1 (SAITO WATARU [JP] ET AL) 30 augustus 2012
(2012-08-30)

2 The present application does not meet the criteria of patentability, because the subject-matter of independent claims 1 and 2 does not involve an inventive step.

2.1 Regarding claim 1, document D1 is regarded as being the prior art closest to its subject-matter and discloses (D1: alinea [0014] - alinea [0023]; figuren 2,3):

"Halfgeleiderinrichting, die is voorzien van een actief-elementdeel (2) en een gate-pad-deel (8), die zijn gedefinieerd op een halfgeleidersubstraat (1, 22, 38), dat is gevormd door het aan elkaar lamineren van een lage-weerstand-halfgeleiderlaag van een eerste geleidend type (1) of een tweede geleidend type en een driftlaag van een eerste geleidend type (38), waarbij het actievelementdeel omvat:

de lage-weerstand-halfgeleiderlaag (1);

de op de lage-weerstand-halfgeleiderlaag gevormde driftlaag (38);

een basisgebied van een tweede geleidend type (36), dat is gevormd op een oppervlak van de driftlaag;

een hoge-concentratie-onzuiverheid-diffusiegebied van een eerste geleidend type (31), dat is gevormd op een oppervlak van het basisgebied;

een gate-elektrodelaa (32), die is gevormd op het basisgebied en is aangebracht tussen het hoge-concentratie-onzuiverheid-diffusiegebied en de driftlaag met een daartussen opgestelde gate-isolatielaag (34); en

een eerste elektrodelaa, die in contact met een oppervlak van het hoge-concentratie-onzuiverheid-diffusiegebied en een oppervlak van het basisgebied is gevormd in een toestand waarin de eerste elektrodelaa is geïsoleerd van de gate-elektrodelaa met een daartussen opgestelde tussenlaagisolatielaag (D1: impliciete openbaarmaking, paragraaf 16),

en het gate-pad-deel omvat:

de lage-weerstand-halfgeleiderlaag (1); de op de lage-weerstand-halfgeleiderlaag gevormde driftlaag (22, 38); een geleiderlaag (8), die boven de driftlaag is gevormd over het gehele gebied van het gate-pad-deel met een daartussen opgestelde veld-isolatielaag (9); en een gate-trilling onderdrukkende structuur, die is gevormd op een oppervlak van de driftlaag, waarbij de gate-trilling onderdrukkende structuur omvat:

een eerste onzuiverheid-diffusiegebied van een tweede geleidend type (24), dat is aangebracht langs een buitenste omtreksdeel van het gate-pad-deel en dat elektrisch is verbonden met de eerste elektrodelaaag (D1: paragraaf 23), en een onzuiverheid-non-diffusiegebied van een tweede geleidend type."

- 2.2 The subject-matter of claim 1 therefore differs from this known from D1 in that a device is further provided with a second impurity diffusion region of a second conductive type in a floating state wherein an impurity non-diffusion region of a second conductive type is alternately formed in the region surrounded by the first impurity diffusion region of a second conductive type.
- 2.3 The technical effect of the aforementioned difference is that the gate oscillations at the time of switching are minimized.
- 2.4 The technical problem to be solved by the present invention may be regarded as improving the switching characteristics of a power device.
- 2.5 The solution proposed in claim 1 of the present application cannot be considered as involving an inventive step for the following reasons:

Document D1 addresses the problem of the gate oscillation (see paragraph 6). The aforementioned problem is solved by providing a structure beneath a gate pad wherein p-type regions (diffusion region and polysilicon regions) are provided alternately. The diffusion regions 24 (see figure 3) are either in floating state (see paragraph 22) or connected to a source potential (see paragraph 23).

The person skilled in the art is therefore aware of the problem as defined in paragraph 2.4 and would always try to further optimize the switching characteristics of a power device.

The skilled person would inevitably consider the disclosure of the document D2. Indeed, document D2 addresses, in the same technical context, the problem of switching (D2: see paragraphs 3 - 5).

Document D2 teaches (D2: paragraphs 134 - 137, figure 19) a structure provided with p-type regions (D2: figure 19, elements 12p, 15p) wherein the regions formed at the periphery of a gate pad region are connected to a source potential and the regions disposed within the area surrounded by the aforementioned regions are in floating state.

According to D2, it allows to further lower the drain-source capacitance and therefore improve the switching characteristics.

The skilled person would recognise that the solution proposed in D2 solves the underlying objective technical problem as presented above (see paragraph 2.4). The indications provided in D2 (as discussed above) are sufficient to prompt the skilled person to further improve the device known from D1 by forming a structure as taught in D2 thus arriving at the device exactly as defined in claim 1 without involving an inventive step.

- 2.6 The subject-matter of the independent claim 2 corresponds in substance to the subject-matter of claim 1 and relates to a device provided with trench gates. These additional features are also disclosed in D1, see figure 3 and the corresponding text. Hence, the subject-matter of claim 2 does not involve an inventive step for the same reasons as given above for claim 1.
- 2.7 Dependent claim 3 - 18 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of inventive step. The additional features of claims 3 - 18 are known from ~~D1~~ **D3**, see the search report and the corresponding citations, in particular:
- claim 3 (obvious modification, see also D2: paragraphs 94 - 96, figure 12, element 40A, see in particular paragraph 95),
 - claims 4 and 6 (D2: paragraph 59 and paragraphs 62 - 69, figures 4 - 5C),
 - claim 5 (D1: figure 3, D2: figure 19),
 - claim 7 (D2: figure 19, element 12a),
 - claim 8 (D2: figure 19, element 12a, see also paragraph 144),
 - claims 9 - 11 and 14 (D2: figure 19, see projections from element 12),
 - claim 13 (D1: figure 3, elements 24, 36),
 - claims 15 - 17 (obvious modification).
- 3 The combination of the features of any of the dependent claims 12 or 18 is neither known from, nor rendered obvious by, the available prior art. The reasons are as follows: the provision of the guard ring as defined in claim 12 and/or the arrangement as defined in claim 18 further improves the switching characteristics by suppressing the gate oscillations.

Item VII

- 1 Independent claims 1 and 2 are not in the two-part form, which in the present case would be appropriate, with those features known in combination from the prior art being placed in the preamble and the remaining features being included in the characterising part.

- 2 The features of claims are not provided with reference signs placed in parentheses.
- 3 The relevant background art disclosed in D1 and D2 is not mentioned in the description, nor are these documents identified therein.