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(54) Title: PARTIAL ENERGY PROCESSING CONVERTERS FOR A HIGH EFFICIENCY AND FULL MPPT RANGE PV MODULE INTEGRATED CONVERTER MIC

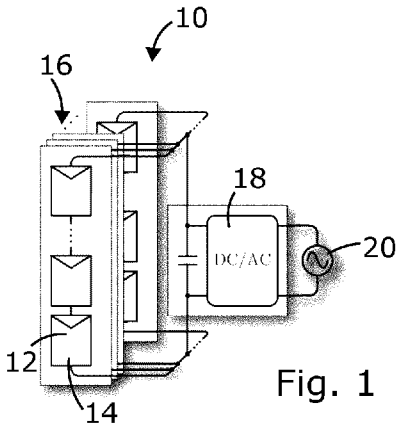

Fig. 1

(57) Abstract: In this patent document, the partial energy processing (PEP) concept is developed to achieve a high-efficiency and full MPPT range PV MIC. For PEP the energy is flown from the source to the load through multiple paths. The total energy then is divided into arbitrary portions in power-time plane and each portion is transferred through a different path to achieve the best conversion performance. A three path PEP structure that is specifically suitable for PV MIC application is proposed and realized in component level. A 220 W prototype converter is implemented to justify the converter principal of operation and analyses. Using the proposed PV MIC, MPPT is achieved for the full range of the PV power generation while 99.6% to 96.5% efficiency is achieved for the power mismatches in the PV module ranging from 0 to 50% of the maximum module power generation capability, respectively. The efficiency drop is shown to be linear with power mismatch level without any abrupt reductions that is commonly observed in conventional PV module integrated converters.

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PARTIAL ENERGY PROCESSING CONVERTERS FOR A HIGH EFFICIENCY AND FULL MPPT RANGE PV MODULE INTEGRATED CONVERTER MIC

TECHNICAL FIELD

Power converters.

BACKGROUND

[0001] Photovoltaic (PV) solar energy is one of the promising renewable energy resources for which the solar energy is directly converted to electricity. PV modules generate dc voltage in the range of several tens of volts and require both voltage elevation and dc-ac conversion before they can be connected to the ac utility grid.

[0002] Efficiency and power density of Power Electronics converters has been constantly increased for decades and is projected to further improve. As an example, the efficiency at rated power for converters used in telecommunication and PV applications has increased from around 90% in 1990s to about 98% in recent years which has also contributed to the increase of converter power density. Specifically, for PV converters, not only the rated power efficiency must be increased but also converters must perform Maximum Power Point Tracking (MPPT) at module level to increase the energy yield in presence of module level power mismatches. Therefore, module level converters may be adopted for PV systems where the converter efficiency for the whole MPPT range becomes an important design factor. Furthermore, to fit the module level PV converters in the panel's junction box and to reduce the manufacturing costs module level converters must have a high power density.

[0003] Photovoltaic (PV) Module Integrated Converters (MICs) perform maximum power point tracking (MPPT) for individual PV panels and improve the system energy capture efficiency. The efficiency of the MIC and its MPPT range are key factors that determine the suitability of MICs for PV systems. Conventional PV MICs are either full power converters (FPC) or partial power converters (PPC) which suffer from low efficiency and small MPPT range, respectively.

[0004] Furthermore, the power generation of a PV module is dependent on the electrical characteristic of its load and maximum power which is called maximum power point (MPP) is obtained for one specific load characteristic. The MPP of PV modules changes with temperature and irradiation changes, thus maximum power point tracking (MPPT) may be applied on PV modules to extract the maximum energy.

[0005] In a PV system, power converters are employed to perform the dc-ac conversion and MPPT. The voltage elevation can be obtained either through the series connection of the PV modules or by means of power converters. Various PV system configurations are presented in the literature based on the series connection of the PV modules or voltage elevation through power converters.

[0006] Figs. 1-4 show some of the most common PV system configurations 10. In the basic PV system configuration, shown in Fig. 1, multiple PV modules 12 are connected in series to build up a string 16 with a high dc voltage that is suitable for the dc-ac converter 18 which in the example shown produces an overall AC output 20. It would also be possible for a PV system to generate an overall DC output. In the examples shown in Figs. 1-3, each PV module 12 may substantially comprise a solar panel 14, with no converter at the module level. Then, parallel combination of some of these high dc voltage strings 16 is connected to a central inverter to perform the dc-ac conversion. This configuration has the lowest power processed by the conversion stage, however, has poor energy capture performance. As a result of series connections, all PV modules 12 in each string 16 have equal currents. However, due to the power mismatch, each module may have a different maximum power point (MPP) and consequently a different MPP current. Therefore, in the presence of power mismatch, some of the modules will operate away from their MPP in this configuration resulting in the reduction of captured energy. Power mismatch between modules is the difference between their MPPs which is caused by multiple factors including nonuniform shading, soiling, aging, temperature gradients, etc. In the central inverter configuration shown in Fig. 1, the loss of extractable power may be caused by the power mismatch between different PV strings 16 as well, in which the overall voltage of each string is required to be the same due to the parallel connections, but at any single voltage the resulting currents differ from the overall optimal current for at least some string 16. Depending on the extent of power mismatch in a PV system, up to 30% of the annual extractable energy can be lost in string/central inverter configurations as shown in Fig. 1. To overcome the string level power mismatch other configurations are also presented as shown in Fig. 2 and Fig. 3. In the configuration shown in Fig. 2, each string 16 is connected to a string inverter 22 to perform the dc-ac conversion separately and in the configuration shown in Fig. 3 which is called multistring or two-stage PV system configuration, the strings 16 are equipped with string-level dc-dc converters 24 and multiple strings are then paralleled to increase the power level while only one dc-ac stage is used with overall DC-AC

converter 18. Despite its usefulness in addressing string level power mismatches using the string level dc-dc converters 24 or per string dc/ac inversion with string inverters 22, these configurations are not able to address the module level power mismatches.

[0007] There is also another configuration for which the voltage control, here in the form of elevation, is obtained by means of power electronic converters. This category includes paralleled PV modules 12 equipped with the high step-up dc-dc converters 26 and microinverters 28 which is shown in Fig. 4. This configuration can overcome the module level power mismatch however it requires a dc-dc converter with a high voltage conversion ratio. High voltage gain converters usually suffer from high component stresses and low efficiencies. PV system configurations that adopt microinverters and paralleled PV modules equipped with the high step-up dc-dc converters 26 are from this category, and these kind of system configurations normally provide lower efficiencies compared to the rest of PV system configurations.

[0008] For the configurations with series stack of PV modules the energy loss due to power mismatch can be prevented by equipping each PV module 12 with a dc-dc converter as shown in Figs. 5-7. These dc-dc converters are known as dc-dc module integrated converters (MICs).

[0009] dc-dc MICs in the literature are used with the PV panels series stack configuration which require voltage gains close to unity and are divided into two categories of full and partial power converters (FPC and PPC). Figs. 5-7 shows different PV system configurations 10 with these MICs. FPCs 30, as shown in Fig. 5, process all the power of their PV panels 14 regardless of mismatch condition in the system, thus they have significant losses and a power rating equal to the PV panels rated power. Furthermore, FPC efficiencies drop significantly when the voltage gain deviates from unity. For a commercialized example it is shown that efficiency decreases from 98% to 96% when the voltage gain is reduced form unity to 0.75. Decreased power efficiency decreases the portion of MPP power that is available at PV MIC output after performing MPPT, thus it decreases the energy capture. The energy capture is integration of power over time and for most of the time FPCs operate away from unity gain where the power efficiency is decreased. Therefore, the FPCs efficiency drop with voltage gain deviations causes a significant loss in energy capture. PPCs comprise of two subcategories of parallel-PPC, shown in Fig. 6, and series-PPC, shown in Fig. 7. The parallel-PPCs 32 shown in Fig. 6 are connected in parallel with the PV panels and perform MPPT by shuffling currents among them. Parallel-PPCs are widely referred to as Differential Power Processing (DPP) converters in the literature and are implemented using

various configurations and topologies. DPP converters improve system efficiency by processing only part of the nominal power and can have smaller rated power than their PV panels. However, there are disadvantages for the DPP converters that have limited their commercial application. Due to the shuffling of currents among converters, the total power processed by converters in some of DPP configurations increases significantly with the increase of the number of panels in a string which diminishes the merits of partial power processing. DPP configurations normally require an extra high-current DC wiring between panels or between panels and the dc bus which increases the cost and adversely affects reliability and efficiency. In most DPP configurations, every string only has one MPP voltage and paralleling strings is not possible without an extra converter. Furthermore, as DPP converters are connected in parallel with the PV panels they normally operate with rated PV voltage and low current for which power converters exhibit low efficiency due to the power independent losses. The other subcategory of the PPC is series-PPC, shown in Fig. 7, for which a controlled voltage is added in series with the PV voltage to perform MPPT. The series-PPC 34 processes part of the PV panels power and as such preserves all the merits of DPP, while it does not have DPP disadvantages. In a series-PPC configuration, every panel's voltage can be controlled regardless of other MICs, as with an FPC configuration. A series-PPC 34 can comprise a converter 62 arranged with an IPOS arrangement (left) or with an ISOP arrangement (right). The power processed by each MIC only depends on its associated panels power mismatch. Therefore, unlike DPP, in the series-PPC configuration, total power processed by each of the converters does not increase with the increase of the number of panels in the string. No extra wiring among panels or DC bus is added in this configuration because all connections are connected within the converter. Parallel operation of the strings without extra converters is feasible as the series-PPCs can equalize string voltages while performing MPPT for every panel. For maintaining efficiency when MPPT for all panels changes (for example in dim light) the DC-AC inverter 18 may adjust the overall bus voltage and the series PPC MICs will adjust themselves to accommodate whatever bus voltage is applied. The inverter can do maximum efficiency tracking by finding the bus voltage that is best in terms of output power as this bus voltage will change the operating point and efficiency of the system. Since the series-PPC 34 is in series with the PV panel 14 it operates with low voltage and rated PV current most of the times and as such it can be optimized to have good partial load efficiency. Also, the power processed by series-PPC is zero if a unity voltage gain is required for the MPPT, and it is increased if the deviation of the voltage gain from unity is

increased. Therefore, merits of the partial power processing for a series-PPC become negligible if extreme power mismatches are considered. As an example, it is possible in a PV system for a panel to have zero power generation while the rest of the panels operate at their rated power. In such conditions, output voltage for the series-PPC 34 of the shaded panel 14 must be zero. Therefore, series-PPCs 34 must be designed for a wide range of voltage gains including the zero which results in a converter rating equal to an FPC 30.

[0010] MICs perform maximum power point tracking (MPPT) for each PV module and increase the system energy capture. However, as the components used in MICs are not ideal, some energy is dissipated in the MICs. The energy loss of the MICs is added to the PV system losses and compromises part of the energy capture gain obtained using the module level MPPT. Thus, to justify the inclusion of the MICs from the energy capture point of view, it is crucially important to improve the efficiency of the MICs. Efficiency of the MICs in turn depends on their configuration and topology. Most of the existing literature adopt conventional configurations (such as FPC and PPC) and topologies for MIC implementation which suffer from low efficiency and limited MPPT range.

SUMMARY

[0011] In this patent document, the various voltage conversion ratio operations of module integrated dc-dc converters are analyzed. For this analysis, the common PV system dc-ac converters i.e., constant and variable dc bus voltage inverters, are considered. It has been shown that step-down series-PPCs are beneficial for both constant voltage and variable voltage dc bus PV systems.

[0012] In this patent document, the partial power processing concept is extended to the partial energy processing (PEP) concept in some embodiments to attempt to solve the challenges of the series-PPCs. According to the PEP concept, the energy flows from the source to the load through multiple paths. The total energy then is divided into arbitrary portions in the power-time plane and each portion is transferred through a different path to achieve the best conversion performance. Not all the paths need to be real power converters and a dummy bypassed converter which is simply a direct wired connection of the input and output terminals can be used as one of the paths to improve the efficiency. Furthermore, in some embodiments, some components can be shared among the converters to achieve a low-cost implementation.

[0013] Using the PEP concept, in some embodiments, a novel structure is proposed for a PV MIC application which consists of three energy paths. One of the paths is a dummy bypassed converter which transfers the largest portion of the energy and results in improved MIC efficiency. The other two paths are power converters that share all their components to reduce the component count. Each converter is operated with the dummy bypassed converter in pair. The two resulting pairs are optimized for efficiency and have fixed conversion ratios. The conversion ratio of the overall PEP structure is controlled by adjusting the time duration that each pair is operating. The conversion ratios of the pairs are designed to cover the wide range of the voltage gains required for PV MIC. Lower voltage gains are obtained by one of the pairs while the larger gains are obtained using the other pair. Therefore, voltage and current ratings of the converters are kept small, and their efficiencies are improved while the MIC performs the MPPT for the full range of PV panel power from zero to the rated power. The PEP-based PV MIC is designed to cover the voltage gains in the range of zero to unity while it achieves high efficiencies.

[0014] A soft-switching and high-frequency topology which has a simple structure and can provide zero voltage conversion ratio is adopted in some embodiments to realize the PEP-based MIC in component level. A special gating scheme is used for the converter to achieve soft switching operations. Furthermore, the effects of switch output capacitances have been investigated in this patent document. It is shown that switch capacitances resonate with the leakage inductance when the switch is turned off and causes voltage spikes and oscillations on switches, which may reduce the efficiency specifically in high frequency applications. Two clamp diodes are employed to effectively suppress the voltage spikes, and to restore the energy of the leakage inductance once the switch capacitances are charged to the desired voltage. A 1 MHz prototype MIC was built, and magnetic design bottle necks were identified and optimized using a novel modelling approach for the transformer.

[0015] Embodiments of the method described herein differ from conventional partial power processing because of the presence of multiple energy paths between the source and the load. Another difference is in the way the method controls the power converter to obtain the desired conversion ratio. In embodiments of the proposed method, the conversion ratio for each of the paths is constant to optimize efficiency while obtaining various conversion ratios through two different means:

1. Utilizing the flexibility that various possible configurations provide in a multiple path partial energy processing converter.

2. Time control of the operation of converter using each of the constant conversion ratio paths.

[0016] In conventional partial power processing techniques, there are generally only two possible configurations which are commonly referred to as IPOS and ISOP. By contrast, using multiple path partial energy processing there are several possible configurations which are shown in Figs. 13A-13F for a three-path example. In the conventional partial power processing, each of the two possible configurations have a total conversion ratio that relates to the real power converter conversion ratio as follows:

$$M_{IPOS} = 1 \pm M_{conv}$$
$$M_{ISOP} = 1 \pm \frac{1}{M_{conv}}$$

[0017] As can be seen, once the configuration is chosen for conventional partial power processing there is usually no way other than converter conversion ratio control to adjust the total conversion ratio. However, in multiple-path PEP there are multiple real converters, and their conversion ratios contribute to the total conversion ratio. The way that the total conversion ratio is related to the conversion ratio of the real converters depends on the combination of the converters that are used at the same time and depends on the configuration. As an example, each of the real converters may be used in pair with the dummy converter in a three-path PEP. Accordingly, there are six possible configurations and for each configuration there are two conversion ratios available. For example, in configuration C1, shown in Fig. 13A and Fig. 14, the two conversion ratios are:

$$M_{pair1}(C1) = 1 \pm M_{conv1} \; and \; M_{pair2}(C1) = 1 \pm M_{conv2}$$

[0018] While, configuration C2, shown in Fig. 13B, has the following conversion ratios:

$$M_{pair1}(C2) = 1 \pm \frac{1}{M_{conv1}} \; and \; M_{pair2}(C2) = 1 \pm M_{conv2}$$

[0019] The total conversion ratio depends on the pairs' conversion ratios and the pairs' conversion ratios themselves depend on the real converter conversion ratio. As an example, regarding configuration C1, it can be seen that by selecting two different values for the conversion ratio of real converter 1 and 2, one can have two different conversion ratios for the pairs. Also, one can

get different pair conversion ratios even using the same real converter conversion ratio as can be seen from the configuration C2 conversion ratios. This way part of total conversion ratio control is done by selecting the appropriate configuration and the constant conversion ratios for each of the used real power converters.

[0020] The other part of the conversion ratio control is done by time controlling the converter operation using each of the pairs. Assume that for configuration C1, $M_{conv1} = 0.5$ and $M_{conv2} = 1$ are chosen. Then using the positive output polarity converters, the conversion ratio of the pairs are:

$M_{pair1} = 0.5$ and $M_{pair2} = 0$.

[0021] An obvious operating mode on top of pair 1 and pair 2 operation is the no real power converter mode operation which means only using the dummy converter that results in M=1. Now having these three conversion ratios any conversion ratio between 0.5 and 1 is obtained by operating the converter in pair 1 mode, which may be referred to as process mode, and in the mode using the dummy converter, referred to as pass-through mode. Also, any conversion ratio between 0 and 0.5 is obtained by operating the converter in pair 2 (which may be referred to as bypass mode) and pair 1 (pass-through) modes. Appropriately allocating the time for each of the mentioned modes of operation gives the ability of sweeping the conversion ratio between 0 and 1.

[0022] Notably, in the above example, only the operation of the real converters in pair with the bypass path were used however there are other feasible modes that also could be used. For example, operating all energy paths together is another feasible operating mode which may give even more options for modes of operation to better adjust the total conversion ratio of the PEP structure.

BRIEF DESCRIPTION OF THE FIGURES

[0023] Fig. 1 is a schematic diagram of a prior art PV system configuration with a central inverter.

[0024] Fig. 2 is a schematic diagram of a prior art PV system configuration with string inverters.

[0025] Fig. 3 is a schematic diagram of a prior art PV system configuration with a two-stage inverter.

[0026] Fig. 4 is a schematic diagram of a prior art PV system configuration with micro-inverters.

[0027] Fig. 5 is a schematic diagram of a prior art PV system configuration with full power converters (FPC)

[0028] Fig. 6 is a schematic diagram of a prior art PV system configuration with parallel partial power converters.

[0029] Fig. 7 is a schematic diagram of a prior art PV system configuration with series partial power converters, with the series partial power converters shown in additional detail at lower left with an IPOS arrangement and at lower right with an ISOP arrangement.

[0030] Fig. 8 is a graph showing a triangular allocation of the total transferred energy in a Partial Energy Processing (PEP) configuration with two paths.

[0031] Fig. 9 is a schematic diagram showing a PEP configuration with three energy flow paths..

[0032] Fig. 10 is a graph showing an example energy allocation of the total transferred energy in the PEP configuration of Fig. 9.

[0033] Fig. 11 is a schematic diagram showing a PEP configuration including a dummy converter.

[0034] Fig. 12A is a schematic diagram showing an invalid wire connection for the configuration of Fig. 11, where converter 1 and the dummy converter are in a PIPO configuration when converter 2 is off.

[0035] Fig. 12B is a schematic diagram showing an invalid wire connection for the configuration of Fig. 11, where converter 1 and the dummy converter are in a SISO configuration when converter 2 is off.

[0036] Fig. 13A-13F are schematic diagrams showing practically valid configurations of the PEP configuration of Fig. 11.

[0037] Fig. 14 is a schematic diagram showing the configuration of Fig. 13A with positive ground.

[0038] Fig. 15 is a schematic diagram showing a string of PV panels along with their converters which have inductive output filters in series, the inductive filters represented using a single inductive filter.

[0039] Fig. 16A is a circuit diagram showing a realization of the converter 1 and dummy converter of Fig. 14.

[0040] Fig. 16B is a circuit diagram showing a realization of the converter 2 and dummy converter of Fig. 14.

[0041] Fig. 17 is a circuit diagram showing a combination of the circuits of Fig. 16A and Fig. 16B to provide a realization of the configuration of Fig. 14.

[0042] Fig. 18 is a circuit diagram showing a simplified version of the realization shown in Fig. 17.

[0043] Fig. 19A is a schematic diagram showing the converter of Fig. 18 operating in a pass-through mode.

[0044] Fig. 19B is a schematic diagram showing the converter of Fig. 18 operating in a bypass mode.

[0045] Fig. 19C is a schematic diagram showing the converter of Fig. 18 operating in a process mode.

[0046] Fig. 20 is a circuit diagram showing the converter of Fig. 18 operating in the pass-through mode.

[0047] Fig. 21 is a circuit diagram showing the converter of Fig. 18 operating in the bypass mode.

[0048] Fig. 22 is a chart showing switching schemes, intervals and waveforms for the converter of Fig. 18 operating in process mode.

[0049] Figs. 23A-23F are circuit diagrams showing the operation of the converter of Fig. 18 in intervals M1-M6 respectively, as shown in Fig. 22.

[0050] Fig. 24 is a picture of an experimental prototype of a converter.

[0051] Fig. 25 is graph showing zero voltage switching waveforms for a switch corresponding to Q_1 of the converter of Fig. 18 in the prototype shown in Fig. 18.

[0052] Fig. 27A is a graph showing switching waveforms for Q_1 of the prototype when operating with $N_{pdm} = 20$.

[0053] Fig. 27B is a graph showing switching waveforms and input current ripple for Q_3 of the prototype when operating with $N_{pdm} = 20$.

[0054] Fig. 28A is a graph showing switching waveforms for Q_1 of the prototype when operating with $N_{pdm} = 12$.

[0055] Fig. 28B is a graph showing switching waveforms and input current ripple for Q_3 of the prototype when operating with $N_{pdm} = 12$.

[0056] Fig. 29 is a graph showing efficiency of the prototype in relation to different mismatches between panels, for different nominal input voltages

DETAILED DESCRIPTION

Partial Energy Processing (PEP) Concept

[0057] Extension of Partial Power Processing to Partial Energy Processing Concept

[0058] The concept of partial power processing is based on providing two or more power flow paths from the source to the load and transferring each part of the total power through one of the paths. In this concept, power flow path is a two-port network and can be considered as a general power converter. One of the power flow paths is normally more efficient than the other and is used to transfer the largest part of the power. Much of the existing art for the partial power processing is based on simultaneous operation of the two converters where the instantaneous power of each converter is equal to its average power, all the time. To improve the overall efficiency, one of the converters is normally realized as an ultra-efficient converter with fixed conversion ratio, while the other converter regulates the output by processing smaller power compared to a full power converter. In the most common configurations, one of the power flow paths is realized as a dummy bypassed converter with 100% efficiency to obtain the maximum overall efficiency when operating close to unity conversion ratios. By using the dummy converter as one of the converters for partial power processing, there are only two feasible structures of input parallel output series (IPOS) or input series output parallel (ISOP). In some embodiments described herein, the concept of partial power processing is extended to partial energy processing (PEP). A single source single load configuration is qualified as PEP if:

- There is more than one path for energy flow from the source to the load,
- The energy flow between the source and the load is divided into at least two portions and each portion is transferred through a different path.

[0059] It is important to note that the energy that flows from the source to the load equals to the area enclosed between source/load instantaneous power and the time axis as it is shown in Fig. 8 for example. The allocation of this area to each of the converters can be done in many ways to serve different optimization goals. As an example, consider a PEP configuration with two paths. If the energy flow is divided into two triangular areas as shown in Fig. 8, the configuration can resemble two interleaved PWM converters with reduced filter requirements which operate at DCM boundary to achieve soft switching. Another example is to divide the energy flow into two rectangles which resembles the basic partial power processing concept under which one of the rectangular portions of energy can be transferred through a dummy converter. A PEP configuration can also have three energy flow paths, as shown in Fig. 9, where any shape of three energy portions serves as an example. As shown in Fig. 9, a PEP configuration connects a source 40 to a load 42

through three converters 48 which provide the three energy flow paths. The converters are connected to the source through input side wire connections 44 and to the load by output side wire connections 46. The input and output side wire connections can be connected via wires in the converters 48, which is particularly of note in the case of one of the converter being a dummy converter 50 (as shown in Fig. 11) with direct wire links between the input side wire connections and output side wire connections.

[0060] One useful example would be dividing the energy flow into rectangular portions as shown in Fig. 10 and using a dummy converter to transfer the largest portion (e.g. the portion labeled E_3). On top of the loss free energy transfer through the dummy converter, this PEP configuration allows converters to operate in pairs. Each pair consists of only one of the converters and the dummy converter. Then each of the converters are operated at two power levels only and can be optimized to have the best operation and efficiency at these power levels. Therefore, using embodiments of this PEP structure, the efficiency of the basic partial power processing can be further improved. Leveraging the PEP concept and substituting one of the converters 48 by a dummy converter 50 as shown in Fig. 11, a new structure is invented for PV converters which can be considered an extension of the series-PPC. Therefore, the source 40 would be a dc voltage source representing the PV panel and the load 42 can be either a dc voltage or a current source representing the rest of the converters in the string and the dc-ac inversion stage. In case of using the invented MIC the rest of the PVs and converters, represented along with the load seen by a string as a whole as load 42, act as a current source since it uses an inductive filter at string side. According to Fig. 11, efficient converter pairs that can be used for energy transfer are: pair1 consisting of a first converter 52 and the dummy converter 50, and pair 2 consisting of a second converter 54 and the dummy converter 50. When one pair is operating, the remaining converters terminals should be either a short or open circuit depending on the wire connections among converter terminals. In general, terminals of the three converters can be connected in parallel or series and there are several wire connections possible for the PEP configuration shown in Fig. 11. However, some of the connections have no practical value because they may lead to parallel input and parallel output (PIPO) or series input and series output (SISO) connection between one of the converters and the dummy converter. The only converter that can be in a PIPO or SISO configuration with a dummy converter is another dummy converter, resulting in a direct connection from source to load. Therefore, the wire connections leading to PIPO and SISO with the dummy converter are

considered practically invalid. Fig. 12A and Fig. 12B show two examples of invalid wire connections. The pair of first converter 52 and dummy converter 50 which is used with second converter 54 in the OFF state has PIPO and SISO connections in Fig. 12A and Fig. 12B respectively. If the invalid connections and replicas are removed, there are 6 practically valid configurations for the PEP structure shown in Fig. 11. These 6 configurations can be categorized into two groups where the first group configurations have at least one IPOS pair and the second group configurations have at least one ISOP pair. Figs. 13A-13F show these 6 configurations. The configurations are referred to using labels C1-C6 as follows: Fig. 13A shows configuration C1, with pair 1 and pair 2 as IPOS; Fig. 13B shows configuration C2, with pair 1 as ISOP and pair 2 as IPOS; Fig. 13C shows configuration C3, with pair 1 and 2 as IPOS; Fig. 13D shows configuration C4, with pair 1 and 2 as ISOP; Fig. 13E shows configuration C5, with with pair 1 as IPOS and pair 2 as ISOP; and Fig. 13F shows configuration C6, with pair 1 and 2 as ISOP. Configurations C1 to C3 have at least one IPOS pair and configurations C4 to C6 have at least one ISOP pair. The difference between these 6 configurations is the ISOP or IPOS connection of their pairs and the way that the remaining converter is operating at its OFF state. For example, C1 and C2 each have different IPOS or ISOP connection in their pairs. As another example, C1 and C3 have the same IPOS connections in their pairs, however they have different OFF state converter operation.

[0061] In C1, both the input and output terminals are open circuit when the converters are in their OFF state, but in C3 the input terminal is open circuit and the output terminal is short circuit when the converters are in their OFF state. The IPOS or ISOP connection of the pairs plays a vital role in the converter realization. The preferred state of the converter terminals when it is off depends on the application specifications. For example, if the efficiency is of crucial importance, the open circuit terminal would be more beneficial as the converter does not have any losses for an open circuit terminal, while the short circuit terminal has conduction losses associated with the current passing through the short circuited terminal. On the other hand, for applications in which the terminal voltage stress is critical, the short circuit terminals for the converter OFF state is more beneficial.

PEP Based Converter for PV MIC

[0062] In this section, the PEP concept is leveraged in some embodiments to develop a power converter that can replace existing PV MICs. This PEP-based converter preserves all the benefits of series-PPCs and tackles the drawbacks that were associated with the wide MPPT range operation. A voltage step-down type converter is preferred in some embodiments as it reduces the overall system cost by accommodating more panels per string compared to a voltage step-up type converter. Also, a converter with both step-up and step-down is not considered suitable in some embodiments as it is less efficient and operates away from its unity gain to keep the inverter dc bus voltage constant. As a result, a significant portion of the captured energy is processed with low conversion efficiencies offsetting any gain obtained from employing the constant voltage inverter.

[0063] For a voltage step-down PV MIC, the voltage gain (M) range required to cover all extreme mismatch cases that can occur in PV systems is:

[0064] $0 \leq M \leq 1.$ (3.1)

[0065] However, most of the captured energy in a PV system is processed with a close to unity voltage gain (M) as suggested by field studies. Also, the range of the converter voltage gain for which the greatest portion of the energy is processed depends on the mismatch conditions in the PV system. For applications with light mismatch conditions, the voltage gains for which the large portion of the captured energy is processed are in a narrow range around M = 1. Whereas, for the heavy mismatch conditions, this range is relatively large around M = 1. Voltage gain range also needs to include small values and even M = 0 as they might happen in PV systems with mismatch but with lower probability. Therefore, a suitable converter for the step-down PV MIC must be able to cover $0 \leq M \leq 1$ while it ideally provides the greatest efficiency for voltage gains close to unity. Also, the range at which converter has the most efficient operation may be flexible to be changed based on application. This flexibility in the high-efficiency operation range renders an extra degree of freedom to further improve the converter efficiency in the desired range. In this section, embodiments of an appropriate configuration of the three path PEP structure to realize the PV MIC with the discussed voltage gain capabilities is described. As shown in Figs. 13A-13F, various PEP configurations are all composed of ISOP and IPOS pairs only. Thus, the pros and cons of realizing the PV MIC using each of ISOP and IPOS connections is addressed first to facilitate the selection of the appropriate PEP configuration. In a PV MIC, the source is a PV panel operating at its MPP and as such has relatively constant voltage equal to the rated MPP voltage (V_{MPP}). However, the panel current may vary from zero to the rated MPP current (I_{MPP}). The load current is equal to the

string current which is normally set to I_{MPP} by means of inverter voltage adjustment. Setting the string current to I_{MPP} makes most of the MICs to operate with unity gain and have higher efficiency. The load voltage for each panel can vary between zero and V_{MPP} to cover the voltage gain range from zero to 1. By using the IPOS connection between the PV panel and the string, the PV side would be the voltage sourced terminal of the converter and the string side would be the current sourced terminal of the converter. Thus, the converter used for IPOS has a constant voltage at the voltage terminal and a constant current at the current sourced terminal. The ISOP connection on the other hand yields to a converter with the voltage of voltage sourced terminal varying from 0 to V_{MPP} and the current of current sourced terminal varying from 0 to I_{MPP}. Operating a voltage sourced terminal with zero voltage and current sourced terminal with zero current causes realization challenges such as unwanted DCM operation and EMI problems. Furthermore, the current sourced terminal of the IPOS is on the string side of the converter, which is in series with other converters, while the current sourced terminal of the ISOP is on the PV side and each current source is only connected to its own PV panel. Therefore, the IPOS configuration gives the opportunity to reduce the inductive filter requirements by sharing the inductance of the converters with a possible inductance used in the dc bus side for other purposes. Also, interleaved operation of the converters is feasible in the IPOS configuration which further reduces the inductive filter size. It can be concluded that from a converter realization point of view, the IPOS connection better suites the PV panel and string configuration requirements.

[0066] Among the valid configurations of a three path PEP structure with a dummy converter, C1 and C3 are composed of IPOS connections only and are therefore considered especially suitable for the PV MIC realization for the above reasons. For the off-state operation of the converter in C1, both input and output terminals are open circuit which helps to reduce conduction losses. However, for the off-state operation of the converter in C3, output terminals must be short circuit which causes extra conduction losses compared to C1. In C1, both input and output terminals of the converters are in parallel, while the output terminals of converters in C3 are connected in series. Thus, the first converter 52 and second converter 54 in C1 can share switching components and energy storage elements in both input and output terminals. However, for C3 the reference potential of the output switching components and energy storage elements are different in the first converter 52 and second converter 54. As a result, in C3, the first converter 52 and second converter 54 cannot share as many components as they can in C1. Therefore, the most appropriate

configuration for the PV application is considered to be C1 which is used to realize the PV MIC in the next section.

[0067] Realization of the PEP Based PV MIC

[0068] In this section, C1 is adopted to build the voltage step-down PV MIC. In the version of C1 shown in Fig. 13A, the negative terminals of the source and the load are connected together as the common ground. The order of converters in C1 can be swapped to make the structure a positive ground configuration where the positive terminals of the load and the source are connected together. The positive ground connection of C1 is shown in Fig. 14 which can eliminate the switch gate isolation requirements and is used to realize the voltage step-down PV MIC. It is important to note that in Fig.14 the source 40 shown in Fig. 13A is replaced with a PV panel 14 and its capacitive filter 56, and the load 42 is replaced with a current source 58 representing the string behavior. In C1, the current-sourced output terminals of the converters, which are realized using inductive filters, are connected in series with the load. Thus, the combination of all inductive filters of the converters is seen from load terminal, resulting in a large inductive filter. As shown in Fig. 15, this combination of inductors can be realized using a single inductor 60 on the string, and the string behavior can be modeled by a current source (58, shown in Fig. 14). In component level, this configuration can be realized in various ways; however, all the realizations of C1 must have the following features:

- At least one of the first and second converters must have galvanic isolation to avoid short circuit problems and to avoid loss of partial energy processing merits at the component level.
- The first and second converters must each have a current sourced terminal at the string side and a voltage sourced terminal at the PV side.

[0069] The above specifications and limitations depend on the converter topology and the selected configuration. In general if a configuration creates a short circuit in the topology that converter should be isolated.

[0070] Figs. 16A and 16B shows one realization for pair 1 (shown in Fig. 16A) and pair 2, (shown in Fig. 16B) where all windings are wound on the same magnetic core. This realization uses the positive ground C1 configuration in a three converter PEP structure as shown schematically in Fig. 14 As can be seen in Figs. 16A and 16B, the output voltage is equal to the input voltage plus the extra voltage generated at the bottom by the converter. The dummy converter is realized in the

wiring arrangement, and has the effect of the input voltage appearing at the output directly and providing power to the output, and the converter output provides extra voltage, where needed, by processing some power taken from the input and passing to the output which can be achieved in several different intervals and states as described below, for example in Figs. 23A-23F.

[0071] As can be seen from Fig. 16A and Fig. 16B, pair 1 and pair 2 have the inductive filter L_f, the windings with n_1 number of turns and switches Q_3 and Q_4 in common. Thus, they can be collected into one converter as shown in Fig. 17.

[0072] Soft-Switching High-Frequency Realization of the proposed MIC

[0073] The general realization of a particular example of the PV MIC would be as shown in Fig. 17, however some simplifications are still possible. The inductor L_f can be removed from converters and be replaced by a larger single inductor on the inverter dc bus. The turns ratio used for the transformer are as $n_2 = N_2/N_1$ and $n_3 = N_3/N_1$ which can be designed based on the converter operating mode requirements. For a specific operating mode, diodes D_1 and D_2 are used to clamp the voltages across the switches Q_3 and Q_4. For this operating mode, n_3 is selected as $N_3 = 2N_1 - N_2$ to be able to clamp the OFF state voltages of Q_3 and Q_4 to the PV voltage. If $n_2 = 2$ for this operation, then n_3 becomes zero and two windings can be saved in realization. Therefore, using these turn ratios, MIC realization is simplified as shown in Fig. 18. It is important to note that all the switches are on the same ground and there is no need for power isolation for gate driving of the proposed converter. Furthermore, the inductor can be integrated with the transformer in some embodiments to reduce the size and cost and improve the efficiency. To perform MPPT, normally MICs are controlled using the duty cycle and/or frequency control which is not efficient for the entire load/voltage range. Using the PEP concept can improve the efficiency of the MICs and their MPPT range. The two pairs of the PEP based MIC can be operated using ON and OFF control mode (i.e., burst mode) to implement the PEP concept and optimize the efficiencies of the converters. Pair 1 and 2 can be designed to have their lowest voltage gain in ON mode and their largest voltage gain in their OFF mode. Then, a range of voltage gains are obtained by combining the ON and OFF mode operation of pairs 1 and 2 while the larger voltage gains are achieved through mostly OFF mode operation of the converters which improves the efficiency, referred to below as “pass-through mode”.

[0074] The ON and OFF mode operation of the pairs are determined by the on and off state of the switches on the PV and string side. Both pair 1 and pair 2 OFF mode operation leads to short

circuit on the string side terminal and open circuit on the PV side terminal, as shown in Fig. 20, referred to as "pass-through mode". Then, string side switches Q_3 and Q_4 must be turned on and PV side switches Q_1 and Q_2 must be turned off for OFF mode operation of the pairs. As pair 1 and pair 2 have the string side switches Q_3 and Q_4 in common, the same switches would turn on for both the pair 1 and pair 2 OFF modes while the rest of the switches Q_1 and Q_2 are turned off. Therefore, the pair 1 and 2 OFF modes results in the same circuit. The ON modes however are different for pair 1 and pair 2 leading to three different modes of operation for the PEP based PV MIC in total. The PEP-based PV MIC operates in one of these three modes for each switching period. Also, it ensures the PV panel is operating at its maximum power point (MPP) by regulating the time duration for each of these modes per a sequence of switching periods. The three modes of operation for the proposed MIC are shown in Fig. 19A, Fig. 19B and Fig. 19C in the MIC's high-level representation. In this representation, the MIC is shown as having a positive input terminal 64, negative input terminal 66, positive output terminal 68, and negative output terminal 70. The first mode, shown in Fig. 19A, is obtained by imposing pair 1 and pair 2 to their OFF states where the energy flow from the PV to the string is through the dummy converter. Therefore, this mode is called pass-through mode which simply connects the PV module to the output as if there is no conversion at all. The conversion ratio of the pass-through mode is 1. The second mode, shown in Fig. 19B, is obtained by imposing pair 1 and pair 2 to their OFF and ON states, respectively, which is called bypass mode. The bypass mode bypasses the output terminal while leaving the PV module open-circuit, thus results in a conversion ratio of 0. The third operating mode, shown in Fig. 19C is obtained by imposing pair 1 and pair 2 to their ON and OFF states, respectively, which is called process mode. As pair 1 is a soft-switching converter at constant conversion ratio, the MIC in the process mode acts as a DC transformer with constant conversion ratio $0 < M < 1$. Then, any conversion ratio between M and 1 can be obtained by proper allocation of the time to pass-through and process modes while conversion ratios between 0 and M are obtained by time allocation between bypass and process modes.

[0075] Converter operation in each of these modes is described as follows:

[0076] Pass-through Mode

[0077] Fig. 20 shows the converter circuit in Pass-through mode. In this mode, switches Q_1 and Q_2 are turned-off and switches Q_3 and Q_4 are turned-on causing clamp diodes D_1 and D_2 to be reverse-biased. In this mode, the capacitive filter is discharged by $-(I_{str} - I_{PV})$ current whereas, the

inductive filter is charged by $V_{PV} - V_{out}$ voltage. If the converter stays in this mode for an adequately long time, filters let $I_{str} = I_{PV}$ and $V_{out} = V_{PV}$, thus MIC voltage gain becomes 1.

[0078] Bypass Mode

[0079] In Bypass mode, all switches (Q_1,Q_2,Q_3, and Q_4) are turned-off and clamp diodes D_1 and D_2 are forced to conduct the string current I_{str}. The MIC equivalent circuit for Bypass mode is shown in Fig. 21. In this mode, the capacitive filter is charged by the PV current I_{PV} whereas, the inductive filter is discharged by $-V_{out}$ voltage across it. The converter terminals act as short-circuit if the converter stays in this mode for a long time and the voltage gain becomes zero.

[0080] Process Mode

[0081] In this mode, switches are turned ON and OFF periodically in every switching cycle to process the power using the high frequency transformer. The leakage inductance of the transformer and switch output capacitance are used in this mode to obtain soft-switching operation for the converter. Furthermore, the diodes D_1 and D_2 which are normally used for bypass mode realization are used as clamp diodes in Process mode operation. Using a specific switching scheme, energy stored in the switch capacitances is restored by the clamp diodes.

[0082] The switching scheme of the converter, its components voltage and current waveforms, and switching intervals during each switching period in this mode in an embodiment are shown in Fig. 22. The waveforms are obtained for the following assumptions. Capacitor C_f is large enough to keep the voltage constant during the switching cycle. Transformer magnetizing inductance is large enough to be ignored. Total transformer leakage inductance reflected to the string side is denoted by L_{lkg} which is shown on both of the string side windings with an inductance value of $0.5L_{lkg}$. Gate pulses for Q_3 and Q_4 are phase shifted by 180^o and have duty cycles $D > 0.5$ to avoid disruption of inductive filter's current. Gate pulses for Q_1 and Q_2 have 50% duty cycle with a deadtime inserted at the rising edge. Gate pulses for Q_1 and Q_2 are phase shifted by $(D - 0.5) \times 180^o$ with respect to Q_4 and Q_3, respectively. The MOSFETs are modeled as an ideal switch with a parallel capacitor representing the output capacitance. Diodes are modeled as ideal diodes in series with a forward voltage drop. In this figure, v_{gs} refers to gate source voltage and v_{ds} refers to drain source voltage. Based on the assumptions, there are 12 switching intervals from which 6 switching intervals $M7$ to $M12$ are the complement of $M1$ to $M6$. Converter operation in each of the switching intervals $M1$ to $M6$ is described below:

*M*1 ($t_0 < t \leq t_1$)**, shown in Fig. 23A:** This switching interval begins right after the dead time between Q_1 and Q_2. At the end of the dead time, voltage across Q_2's output capacitance, i.e. C_{oss2}, has reached zero and the anti-parallel diode of Q_2 conducts the current through top left winding. Also, switch Q_3 was conducting prior to this interval, thus the string current, I_{str}, was passing through Q_3 mainly. A small portion of I_{str} was passing through the clamp diode D_2 because of turning off the switch Q_4. This interval begins with the turn ON of Q_2 which turns on with zero voltage switching (ZVS). When Q_2 is on, V_{PV} is applied on the top left winding resulting in a reflected voltage equal to $0.5V_{PV}$ on each of the bottom side windings. The major part of I_{str} passes through the switch Q_3 and bottom left winding in this interval which loads the high-frequency transformer with a power of $0.5V_{PV}I_{str}$, i.e. half of the rated power of PV. Also, the small portion of I_{str} which passes through the clamp diode D_2 discharges the leakage inductance L_{lkg} using the loop composed of PV, Q_3, leakage inductance, bottom side windings and the clamp diode D_2. Current of D_2 decays over the time due to the voltage drop of the diode and reaches to zero during the interval M1 ($t_0 < t \leq t_1$). In this interval, switches Q_1 and Q_4 are turned OFF and tolerate $2V_{PV}$ and V_{PV} voltage stresses, respectively. The capacitive filter is charged by $I_{PV} - 0.5I_{str}$ current whereas, the inductive filter is discharged by $-(V_{out} - 0.5V_{PV})$ voltage. This interval ends at t_1 when the switch Q_4 turns ON and I_{str} starts to commutate to Q_4.

*M*2 ($t_1 < t \leq t_2$)**, shown in Fig. 23B:** Switch Q_4 turns ON at the beginning of this interval and the overlap of the Q_3 and Q_4 is started to ensure that the inductive filter L_f current is not disrupted. Furthermore, switch Q_2 is ON and applies $+V_{PV}$ on the top left winding of the transformer. The reflected voltage to the combination of bottom side windings of transformer is $+V_{PV}$ that is applied on the leakage inductance as the switches Q_3 and Q_4 are ON and create a short circuit path for these windings. The voltage applied on the leakage inductance decreases the Q_3 current and increases the Q_4 current, thus it shifts the current from Q_3 to Q_4 with a slope determined by the value of leakage inductance. As can be seen, Q_4 turns ON with zero current switching (ZCS) and leakage inductance acts as a snubber for it to further reduce the switching losses. To balance the MMF within the core $i_{Q2} = 0.5(i_{Q4} - i_{Q3})$. Thus, when half of the overlap time is elapsed, Q_3 current equals the Q_4 current and the Q_2 current becomes zero. This is the end of *M*2 interval when Q_2 turns OFF with ZCS.

*M*3 ($t_2 < t \leq t_3$)**, shown in Fig. 23C:** Switch Q_2 turns OFF at the beginning of this interval and the dead-time between Q_1 and Q_2 is started. Switch output capacitance (C_{oss}) for Q_1 and Q_2

start to resonate with the leakage inductance which discharges C_{oss1} and charges C_{oss2}. Until C_{oss1} is not discharged to 0 or equivalently C_{oss2} is not charged to V_{PV}, the resonance mode continues and causes the Q_3 current to become negative and Q_4 current to slightly go beyond I_{str}. This interval ends at t_3 when Q_3 turns off with a negative current, thus its current diverts to the body diode and it turns OFF with zero voltage switching (ZVS).

*M*4 ($t_3 < t \leq t_4$)**, shown in Fig. 23D:** In this interval, the leakage inductance current passes through Q_2 and the body diode of Q_3. The resonance between output capacitances of Q_1 and Q_2 continues in this interval. As C_{oss1} is charged towards $+2V_{PV}$ and C_{oss2} is discharged towards zero, Q_3 current rises to zero and Q_4 current falls to I_{str}. This relatively short interval ends at t_4 when the current of the body diode of Q_3 becomes zero.

*M*5 ($t_4 < t \leq t_5$)**, shown in Fig.23E:** In this interval, the body diode of Q_3 is turned off and its output capacitance C_{oss3} along with C_{oss1} and C_{oss2} form a resonant circuit with leakage inductance. As C_{oss3} charges towards V_{PV}, the leakage inductance current reaches its peak value in the resonance cycle. In order to avoid voltage ringing on Q_3, which deteriorates the converter efficiency and may cause converter failure due to voltage spikes, the clamp diode D_1 is added to clamp the Q_3 voltage to V_{PV} and recover the energy stored in the leakage inductance. This interval ends when the Q_3 voltage reaches V_{PV} and clamp diode D_1 turns ON.

*M*6 ($t_5 < t \leq t_6$)**, shown in Fig. 23F:** Clamp diode D_1 starts conducting at the beginning of this interval and the leakage inductance current flows to the capacitive filter through D_1. As C_{oss2} is not yet discharged to zero and C_{oss1} is not fully charged to $+2V_{PV}$, the voltage across the PV side winding (combined top side windings) is less than $+2V_{PV}$. Thus, reflected voltage on the string side (bottom side windings) is less than $+V_{PV}$ while the capacitive filter voltage is $+V_{PV}$. Then the difference of these two values is applied to the leakage inductance along with the voltage drop of diode D_1. This voltage drop decreases the current though the leakage inductance and diode. This interval ends at t_6 when the C_{oss2} is discharged to zero and Q_2 turns ON with the zero voltage switching (ZVS).

[0083] The intervals *M*7 to *M*12 are complements of the intervals *M*1 to *M*6 and the converter operation in these intervals operates in the same manner as described above, substituting right and left components, e.g. Q_3 <-> Q_4, Q_1 <-> Q_2, D_1 <-> D_2.

[0084] According to the principle of operation discussed in the embodiments above, converter switches always turn ON and OFF with soft switching in Process mode which results in higher

efficiency and allows higher power densities. The converter operation here is described for $n_2 = 2$ and $n_3 = 0$ while other turns ratios are feasible. The only requirement on the turns ratio with the clamping capability described here is $n_3 = 2 - n_2$, and any N_1, N_2, and N_3 that satisfies this constraint can be used.

[0085] The operation of the ISOP counterpart of the MIC is similar to the IPOS configuration that has been discussed here while the voltage and current stress of the switches might be different as a result of swapping the ports of the MIC from PV side to string side in the ISOP configuration.

[0086] Control Implementation of the PEP-based MIC Using Pulse Density Modulation

[0087] Embodiments of the control method optimize the PV power generation and perform MPPT by regulating the output voltage V_{out}. MIC sets the V_{out} between zero and V_{PV} to respond to the changes in PV power generation. If the converter operates in Bypass mode for a long time the output voltage V_{out} becomes zero and the PV power generation is zero. If the converter operates in Pass-through mode for a long time, the output voltage V_{out} becomes equal to the PV voltage V_{PV} and the PV power generation becomes $I_{str}V_{PV}$. Assuming that $n_2 = n$, if the converter operates in Process mode for a long time $V_{out} = V_{PV}(1 - \frac{1}{n})$ (i.e., voltage gain is $1 - \frac{1}{n}$), and PV power generation is $I_{str}V_{PV}(1 - \frac{1}{n})$. For any PV power generation between zero and $I_{str}V_{PV}(1 - \frac{1}{n})$, the controller allocates a time duration to the converters operation in each of the Process mode and Bypass modes so that desired voltage gain is obtained. Within the controller, time allocation between two modes can be implemented through a periodic signal with discrete controllable ON and OFF times which is also called pulse density modulation (PDM). If the duration of Process mode to the total duration of PDM cycle is denoted by D_{pdm}, then:

$$V_{out} = D_{pdm}(1 - \frac{1}{n})V_{PV}. \tag{3.2}$$

[0088] Similarly, for any PV power generation between $I_{str}V_{PV}(1 - \frac{1}{n})$ and $I_{str}V_{PV}$, the controller sets the duration of the converter's operation in each of the Pass-through and Process modes using PDM. If the duration of Process mode to the total duration of PDM cycle is denoted by D_{pdm}, then:

$$V_{out} = (1 - D_{pdm}/n)V_{PV}. \tag{3.3}$$

[0089] In fact, using the proposed PV MIC, the converter only processes the power difference between $I_{str}V_{PV}$ and the current power generation of the PV panel.

Design and Experimental Verification of the Proposed MIC

[0090] In this section, the component selection for the IPOS step-down MIC is done for a sample PV application. It is important to note that the MIC component ratings and the conversion ratio of the Process mode are imposed by the transformer turns ratio. As discussed in the Process mode section, $n_3 = 2-n_2$ is imposed by converter operation and transformer turns ratio is determined by selection of $n_2 = N_2/N_1$. As N_2/N_1 approaches to 1 : 1 converter rating approaches the PV panel maximum power P_{PV}. However, for N_2/N_1 equal to n : 1, the converter power rating becomes P_{PV}/n. Increasing n, the converter power rating decreases while the power deviation that can be compensated using Process mode also decreases to $I_{str}V_{PV}/n$. The reduction of the power rating results in higher efficiency, power density, and lower cost for the PV MIC. However, it is important to note that Process mode is the most efficient operating mode of the MIC and selecting larger transformer turns ratio may reduce the energy capture of the PV system. Therefore, turns ratio is selected based on the statistical probability of the power mismatch on PV modules of a PV system. It is assumed for a PV system exposed to uneven shading that 50% power mismatch statistically covers the majority of the PV system operating points. Therefore, $n_2 = 2$ can be chosen to both save two windings in the MIC realization and cover the statistically important operating points of a PV system. Assuming a PV module open circuit voltage of 50 V, the maximum voltage on the Q_3 and Q_4 would be 100 V and assuming a power level of 200 W, the transformer can be designed to withstand the core and conduction losses using natural convection according to the design process given in [8]. Using these assumptions, A PV MIC is built with components details as given in Table 3.1.

[0091] Table 3.1: Components and part numbers used in the prototyped high frequency and efficient partial power PV MIC

Components	Part Number and description
Switches Q_1, Q_2, Q_3 and Q_4	GS61008T, 100V Enhancement Mode GaN Transistor, $R_{ds(ON)} = 7m\Omega$
Diodes D_1 and D_2	CDBB5100-HF, Schottky Diode 100V & 5A
Magnetic Core	E32/6/20/R-3F4 + PLT32/20/3.2/R-3F4

Capacitive filter C_f	16 × GRM188R61H225ME11D, 2.2μF 50V

Experimental Verification

[0092] In this section, the proposed operation of an embodiment of the converter is experimentally verified using the prototyped MIC. The prototype MIC is built using the components listed in Table 3.1 and its picture is shown in Fig. 24. The ZVS operation of the switches Q_1 and Q_2 is experimentally verified according to Fig. 25. In this figure, the gate source voltage and drain source voltage of the switch Q_1 are shown. It can be seen that the drain source voltage of the switch reaches zero before the gate source voltage crosses the threshold voltage and allows the switch Q_1 to turn on with ZVS. The same scenario occurs for switch Q_2 and it operates with ZVS as well. As discussed earlier, switches Q_3 and Q_4 turn ON with ZCS and turn OFF with ZVS. Fig. 26 shows the switching waveforms for switch Q_3 and verifies its soft-switching operation. As can be seen, the gate source voltage of the switch has reached below the threshold voltage before the drain source voltage rise, therefore ZVS turn OFF is achieved for these switches. Also, at turn ON, there is no Miller plateau which indicates that there is not significant amount of current in the MOSFET channel when turning it ON and this confirms the ZCS turn ON for the switches Q_3 and Q_4. It is important to note that due to the high frequency operation switch currents cannot be directly measured.

[0093] As discussed earlier, PDM method is used for the MIC to perform the MPPT. The PDM has been implemented through a 32 pulse train system, where the PDM duty cycle can be defined as:

$$D_{pdm} = \frac{N_{pdm}}{32}, \qquad N_{pdm} \in \{0, 1, 2, \cdots, 32\}. \tag{3.4}$$

[0094] Switching waveforms of the switches $Q_1$and Q_3 and input current ripple for Q_3 are shown for N_{pdm}= 20 in Fig. 27A (Q_1) and Fig. 27B (Q_3), and for N_{pdm}= 12 for Fig. 28A (Q_1) and Fig. 28B (Q_3). As can be seen the soft-switching operation of the switches is preserved under PDM operation and input current ripple is negligible. Also, it can be seen that the voltage across Q_1 drops to V_{PV} when both Q_1 and Q_2 are OFF while it is switched between zero and $2V_{PV}$ during the process mode. As the amplitude of the positive voltage across Q_1 does not change during the PDM cycle, it can be concluded that the voltage ripple is negligible.

[0095] MIC efficiency for various power mismatch levels is also measured for the prototyped setup. In this test, PV rated power generation is assumed to be 220 W. To measure the efficiency the string current is maintained at the rated current and per unit power mismatch has been swept between 0 and 50%. The test has been repeated for three PV voltage levels of 25 V, 30 V, and 35 V, and the results are shown in Fig. 29. As can be seen, the efficiency is greater than or equal to 96% for all operating conditions and the slope of efficiency reduction with power mismatch is consistent for the whole range. The above observation can be more appreciated if it is compared to the regular PWM dc-dc MICs where efficiencies are normally below 95% and there is a huge step in efficiency when the MIC is operated slightly away from zero power mismatch.

[0096] In this patent document, embodiments of the partial energy processing (PEP) concept are presented as an extension to the existing partial power processing concept. Embodiments of the PEP concept allow more flexibility in the configuration to design high efficiency converters while the converter can be realized with almost the same components as basic partial power processing. The PEP is used to derive a voltage step-down PV MIC for the series connected PV panels. The PEP-based PV MIC achieves high efficiencies by operating converters in pairs and controlling their ON and OFF times rather than continuous duty cycle or frequency control. Compared to full power converters used as PV MICs, embodiments of the proposed converter gives higher efficiency all over the MPPT range and specially for close to unity voltage gains. Compared to DPP PV MICs, the proposed MICs process less power for ad large number of panels and do not need extra connections. Compared to common partial power PV MICs, embodiments of the proposed converter allows full range MPPT for the PV panel while it is still highly efficient. An experimental prototype of the PEP based PV MIC is built which achieves 97.6% to 99.8% efficiency and 12.4 kW/liter power density.

[0097] In this patent document, various PV system configurations have also been studied to exhibit the analysis and design requirements for dc-dc PV converters. It has been also concluded that the PV systems equipped with dc-dc MICs offer the best energy capture in the presence of power mismatch. Different dc-dc MIC categories are studied in this research considering both constant and variable dc bus voltage PV systems. It has been shown that for most of the applications, step-down MICs offer better performance such as larger string size, less processed power and component stress, lower number of MIC required in system level, etc.

[0098] In some embodiments, a new topology is developed for the MIC that renders soft-switching and offers high frequency operation and high efficiency. Rather than conventional duty cycle or frequency control for soft-switching converters, PEP is adopted to perform MPPT using the proposed MIC. This PEP method regulates the MIC conversion ratio by time modulation of the converter operation in three modes of operation which are called Pass-through, Bypass and Process modes. Using the proposed technique, MIC efficiency drop with conversion ratio reduction can be kept linear unlike the conventional PV MICs where a huge drop is observed around unity conversion ratio. Furthermore, the efficient operating modes of Pass-through and Process are used for high power and the statistically most probable range of the PV power generation, while full MPPT range is obtained using Bypass mode. Due to independence of these three modes, the MIC can be optimized for any PV power generation range that is statistically valuable while it is still able to cover the full MPPT range. A prototype MIC was built and tested to experimentally validate the operation and efficiency improvements.

[0099] Immaterial modifications may be made to the embodiments described here without departing from what is covered by the claims.

[0100] In the claims, the word “comprising” is used in its inclusive sense and does not exclude other elements being present. The indefinite articles “a” and “an” before a claim feature do not exclude more than one of the features being present. Each one of the individual features described here may be used in one or more embodiments and is not, by virtue only of being described here, to be construed as essential to all embodiments as defined by the claims.

CLAIMS

1. A module integrated converter (MIC) comprising:

a positive input terminal;

a negative input terminal;

a positive output terminal;

a negative output terminal;

plural converters connecting the positive and negative input terminals to the positive and negative output terminals; and

the MIC being arranged to alter an allocation of power through the plural converters over time to control an overall voltage conversion ratio of the MIC.

2. The MIC of claim 1 in which the plural converters each have respective constant voltage conversion ratios.

3. The MIC of claim 1 or claim 2 in which the plural converters include a first converter, a second converter, and a dummy converter.

4. The MIC of claim 3 in which the first converter, a second converter, and a dummy converter are wired so that the first converter considered as a pair with the dummy converter is arranged either input parallel output series (IPOS) or input series output parallel (ISOP), and the second converter considered as a pair with the dummy converter is arranged either IPOS or ISOP.

5. The MIC of claim 4 in which both the first converter and the second converter are arranged IPOS with the dummy converter.

6. The MIC of claim 5 in which the positive output terminal and positive input terminal are ground.

7. The MIC of claim 5 or claim 6 in which the first converter and the second converter are wired so that the input and output terminals of the MIC are open circuit when the first converter and the second converter are both in respective OFF states.

8. The MIC of any one of claims 4-7 in which the pair of the first converter with the dummy converter includes a connection of an input of the pair to supply a voltage directly to an output of the pair, the first converter also being configured to process power from the input to alter the voltage at the output of the pair.

9. The MIC of any one of claims 4-8 in which the pair of the first converter with the dummy converter operates as a DC-DC transformer.

10. The MIC of claim 9 in which the DC-DC transformer includes:

a first switch;

a second switch;

a third switch;

a fourth switch;

a first inductor arranged in series with the first switch;

a second inductor arranged in series with the second switch;

a third inductor arranged in series with the third switch;

a fourth inductor arranged in series with the fourth switch;

the first inductor, second inductor, third inductor and fourth inductor being arranged on a common core;

the first switch and the second switch arranged in parallel connecting the positive input terminal to the negative input terminal;

the third switch and the fourth switch arranged in parallel connecting the negative output terminal to the negative input terminal or the positive output terminal to the positive input terminal.

11. The MIC of claim 10 in which the first switch and second switch are arranged to switch on at zero voltage.

12. The MIC of claim 10 or claim 11 in which the third switch and the fourth switch are arranged to switch on at zero current.

13. The MIC of any one of claims 10-12 further comprising clamp diodes linking each of the third inductor and the fourth inductor to the positive output terminal, where the third switch and the fourth switch connect the negative output terminal to the negative input terminal, or to the negative output terminal, where the third switch and the fourth switch connect the positive output terminal to the positive input terminal, the clamp diodes being arranged in conjunction with the first, second, third and fourth inductors to clamp voltage across the third switch and the fourth switch.

14. The MIC of claim 13 further comprising additional inductors in series with the diodes, and in which the clamp diodes arranged to clamp voltage across the third switch and the fourth switch in conjunction with the first, second, third and fourth inductors and the additional inductors.

15. The MIC of any one of claims 4-14 in which the pair of the second converter with the dummy converter includes one or more diodes arranged to allow current to pass between the negative output terminal and the positive output terminal.

16. The MIC of claim 15 as dependent on claim 13 or claim 14 in which the one or more diodes are the clamp diodes.

17. The MIC of any one of claims 1-16 in combination with a solar panel, and arranged to control the overall voltage conversion ratio to achieve maximum power point tracking (MPPT) for the solar panel.

18. A DC-DC transformer comprising:

a positive input terminal;

a negative input terminal;

a positive output terminal;

a negative output terminal;

a first switch;

a second switch;

a third switch;

a fourth switch;

a first inductor arranged in series with the first switch;

a second inductor arranged in series with the second switch;

a third inductor arranged in series with the third switch;

a fourth inductor arranged in series with the fourth switch;

the first inductor, second inductor, third inductor and fourth inductor being arranged on a common core;

the first switch and the second switch arranged in parallel connecting the positive input terminal to the negative input terminal;

the third switch and the fourth switch arranged in parallel connecting the negative output terminal to the negative input terminal or the positive output terminal to the positive input terminal.

19. The DC-DC transformer of claim 18 in which the first switch and second switch are arranged to switch on at zero voltage.

20. The DC-DC transformer of claim 18 or claim 19 in which the third switch and the fourth switch are arranged to switch on at zero current.

21. The DC-DC transformer of any one of claims 18-20 further comprising clamp diodes linking each of the third inductor and the fourth inductor to the positive output terminal, where the third switch and the fourth switch connect the negative output terminal to the negative input terminal, or to the negative output terminal, where the third switch and the fourth switch connect the positive output terminal to the positive input terminal, the clamp diodes being arranged in conjunction with the first, second, third and fourth inductors to clamp voltage across the third switch and the fourth switch.

22. The DC-DC transformer of claim 21 further comprising additional inductors in series with the diodes, and in which the clamp diodes arranged to clamp voltage across the third switch and the fourth switch in conjunction with the first, second, third and fourth inductors and the additional inductors.

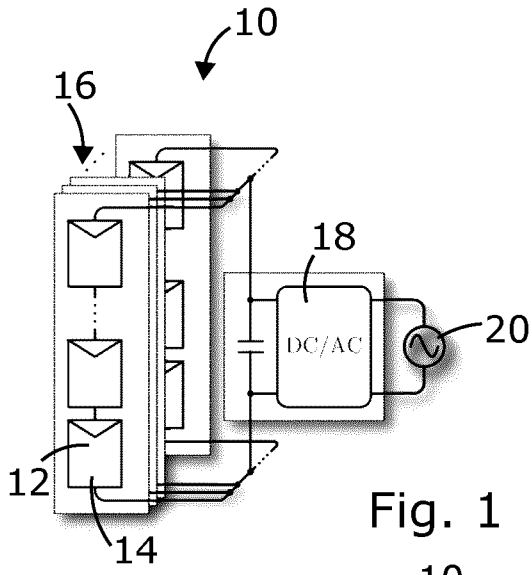


Fig. 1

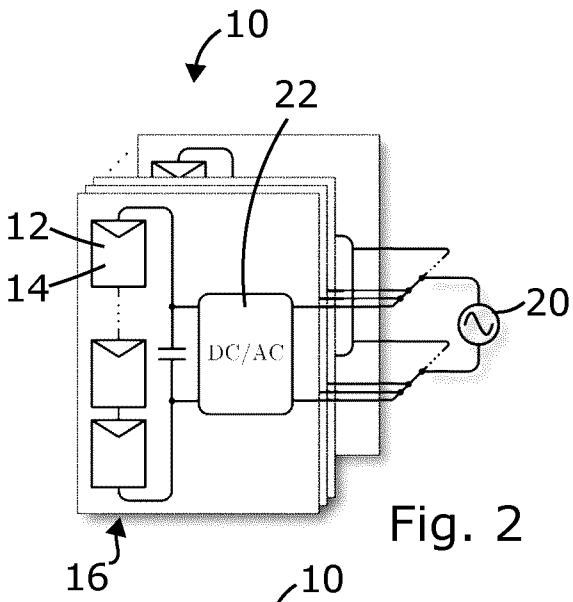


Fig. 2

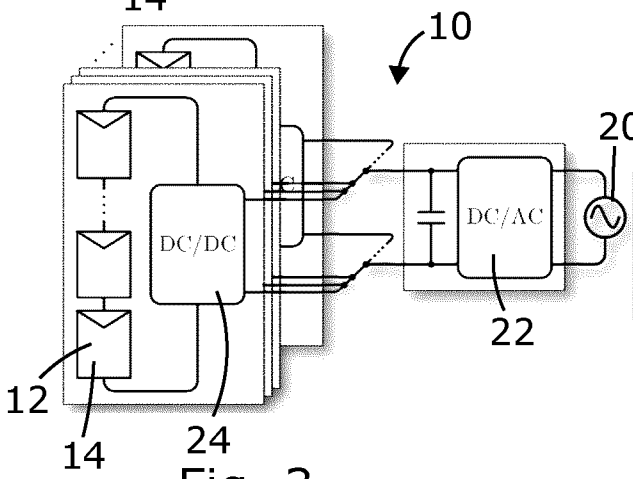


Fig. 3

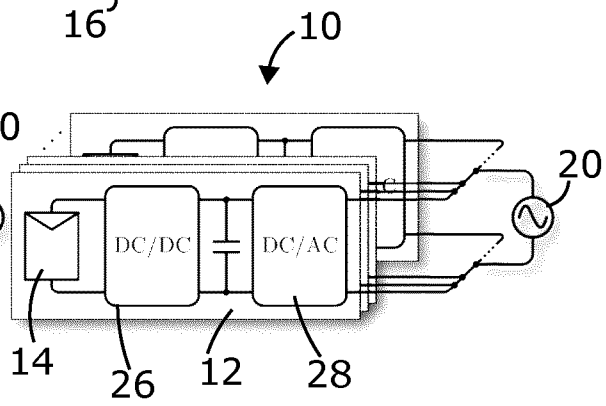


Fig. 4

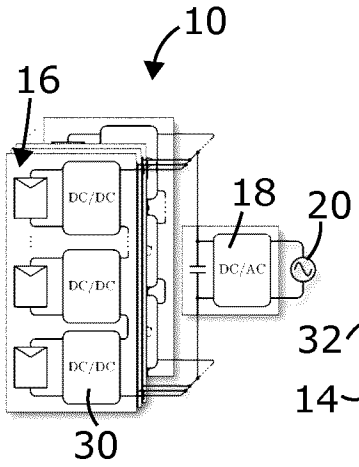


Fig. 5

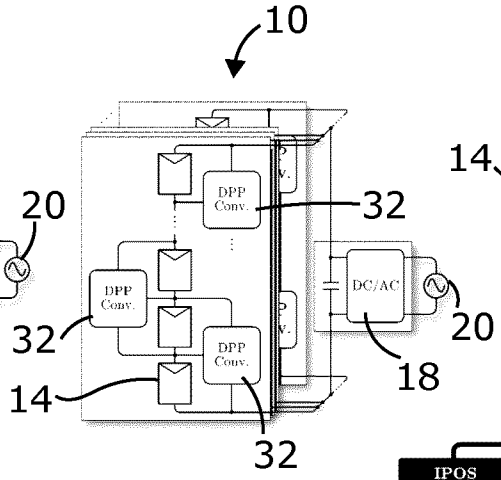


Fig. 6

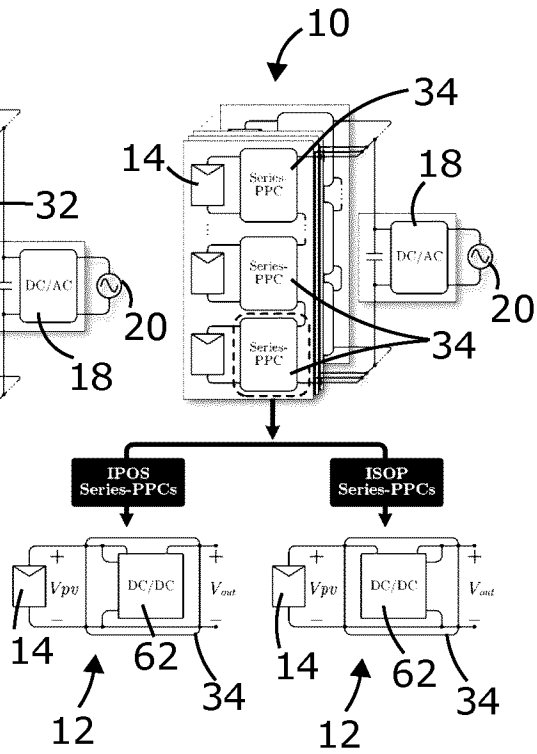


Fig. 7

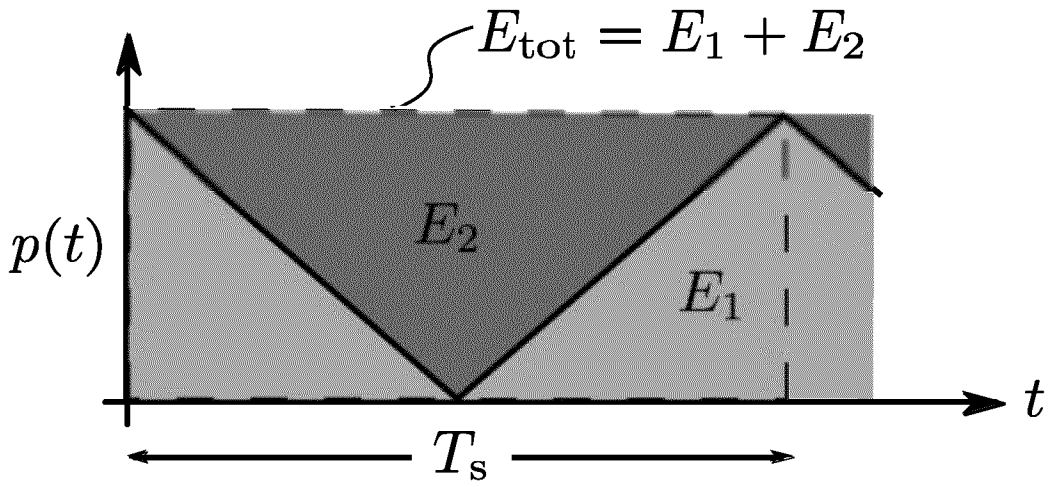


Fig. 8

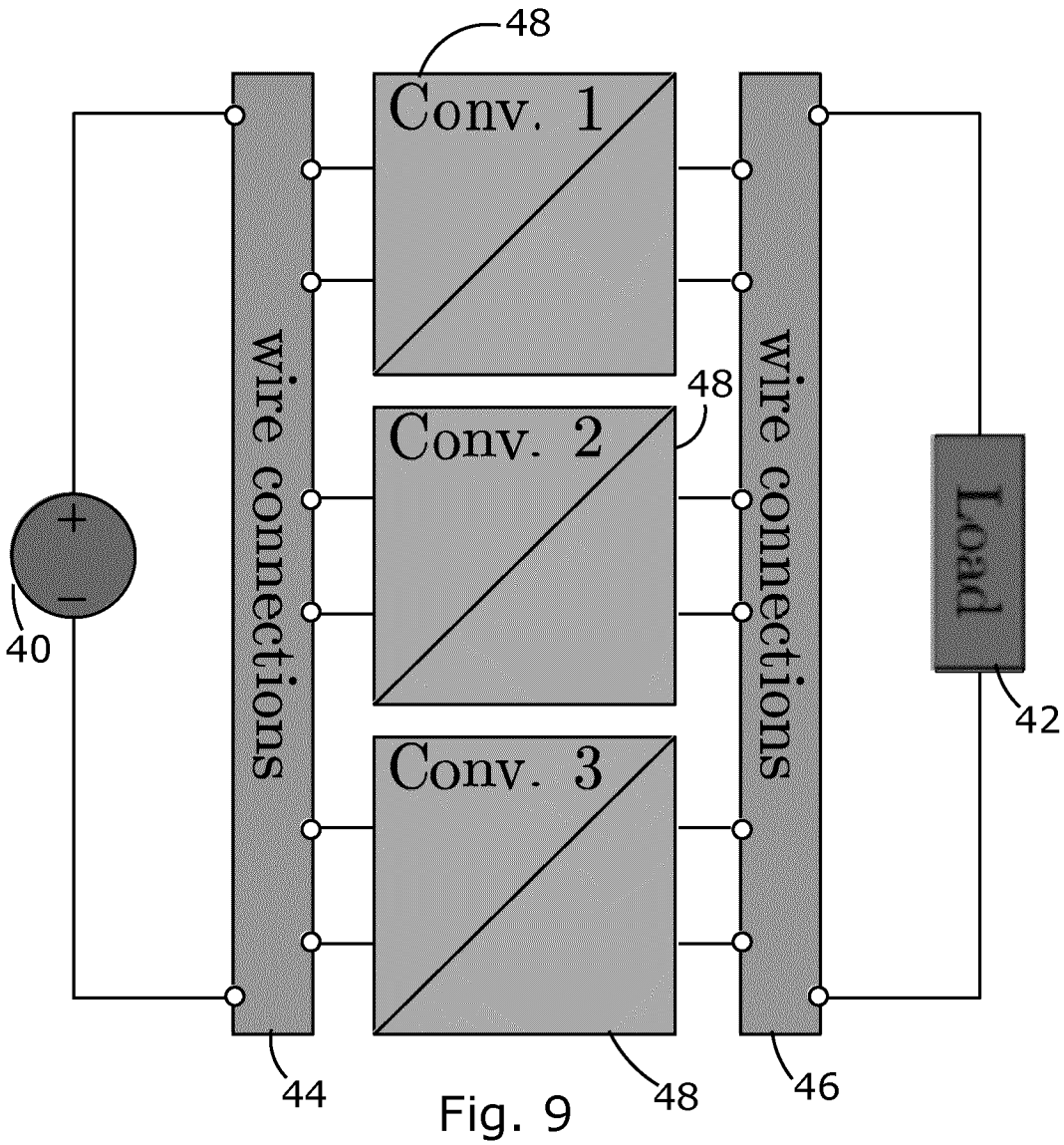

48
Conv. 1
48
Conv. 2
Conv. 3
wire connections
wire connections
Load
+
–
40
42
44
48
46

Fig. 9

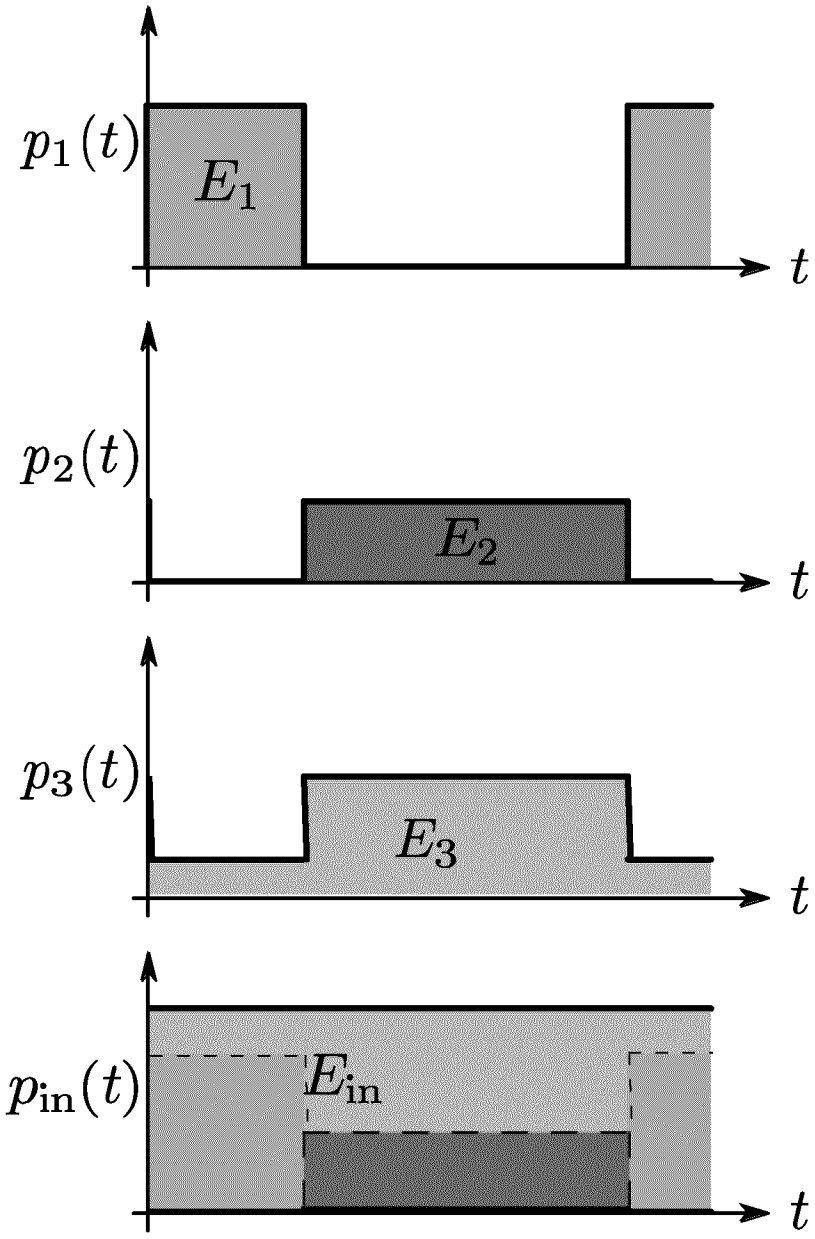


Fig. 10

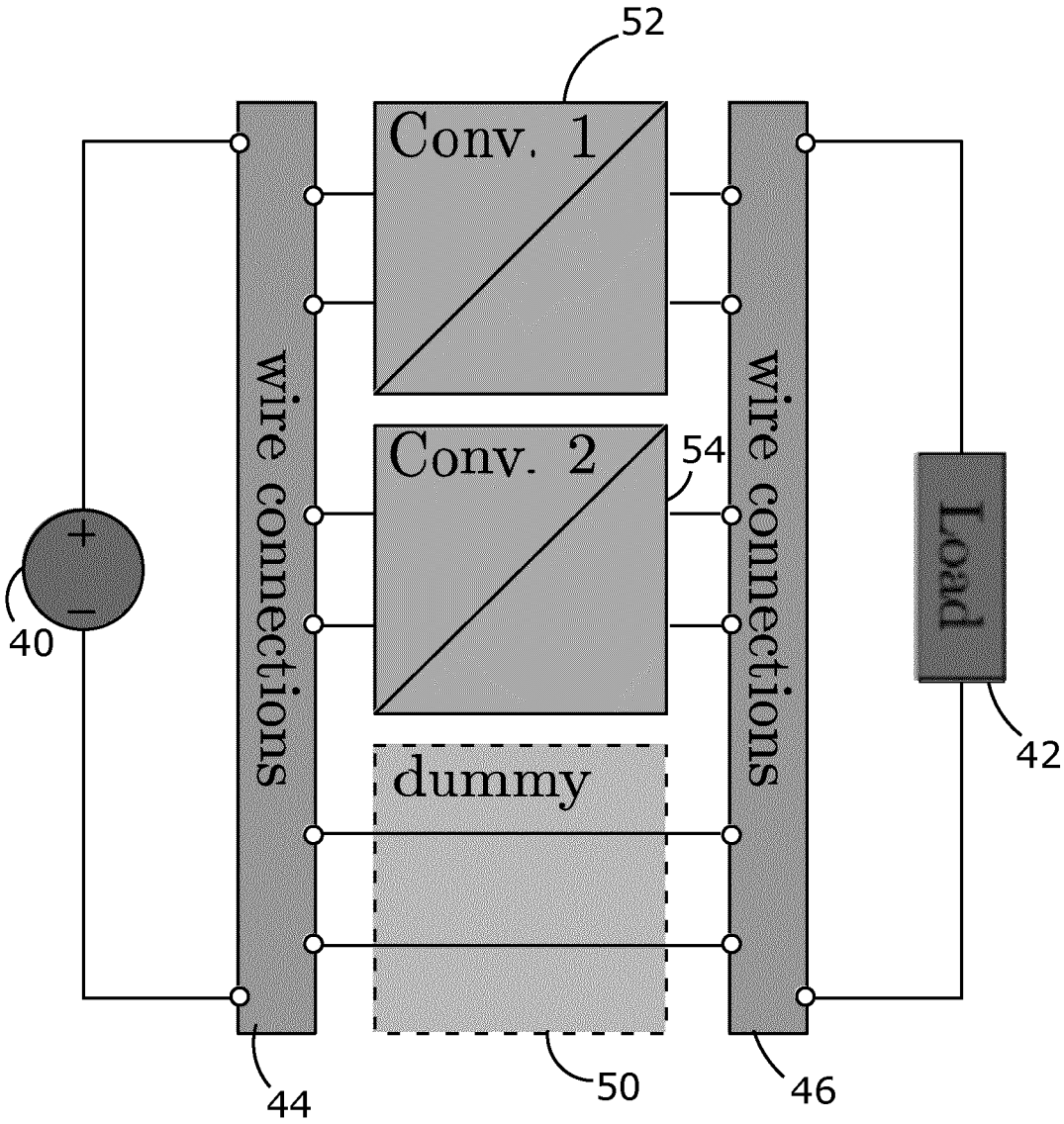

52
Conv. 1
Conv. 2
54
dummy
wire connections
wire connections
Load
+
−
40
42
44
50
46

Fig. 11

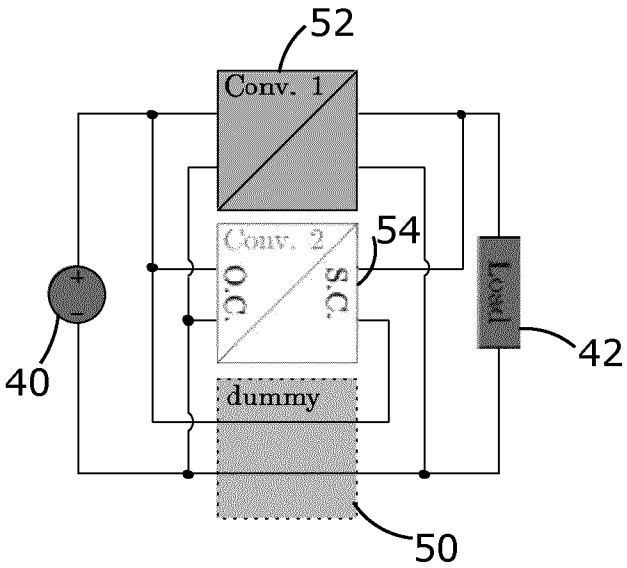


Fig. 12A

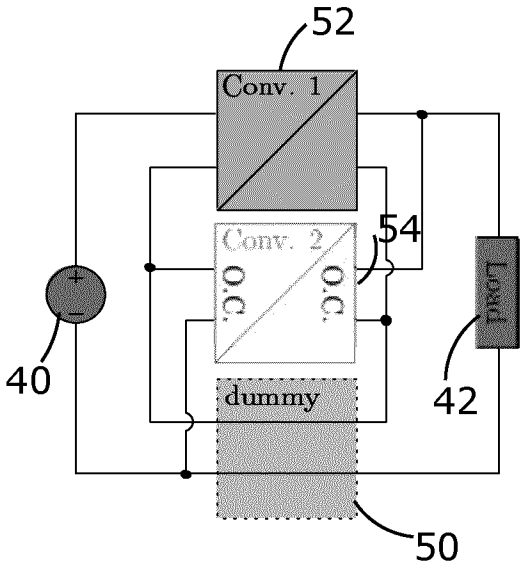


Fig. 12B

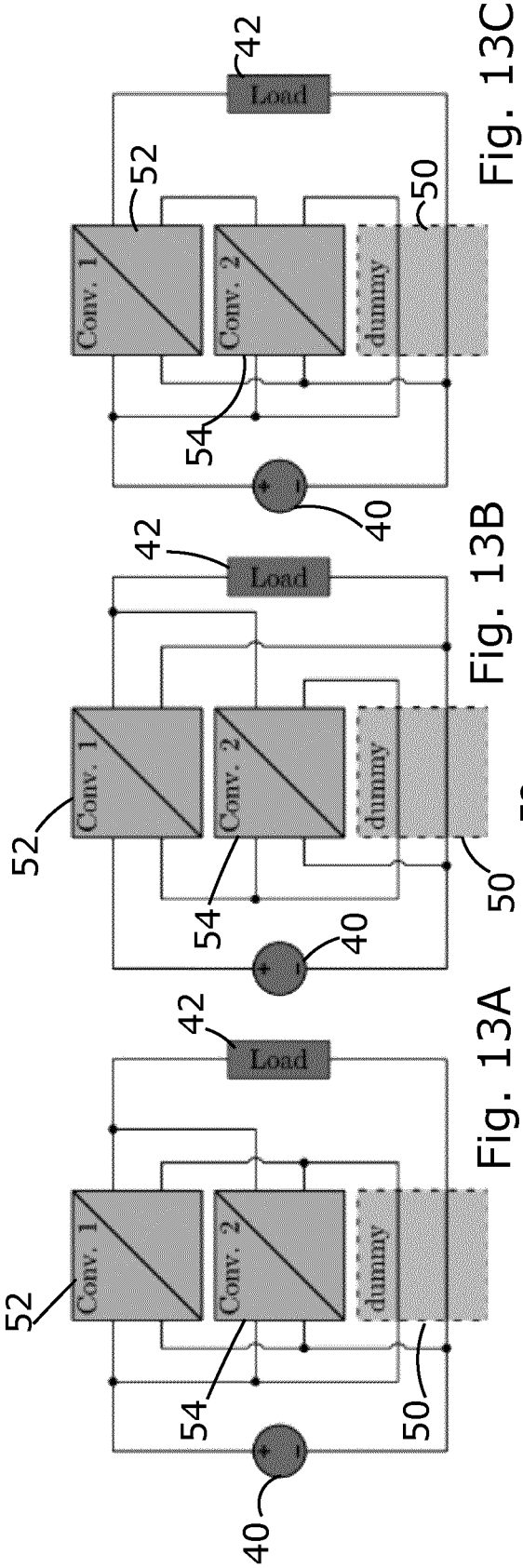


Fig. 13A

Fig. 13B

Fig. 13C

Fig. 13D

Fig. 13E

Fig. 13F

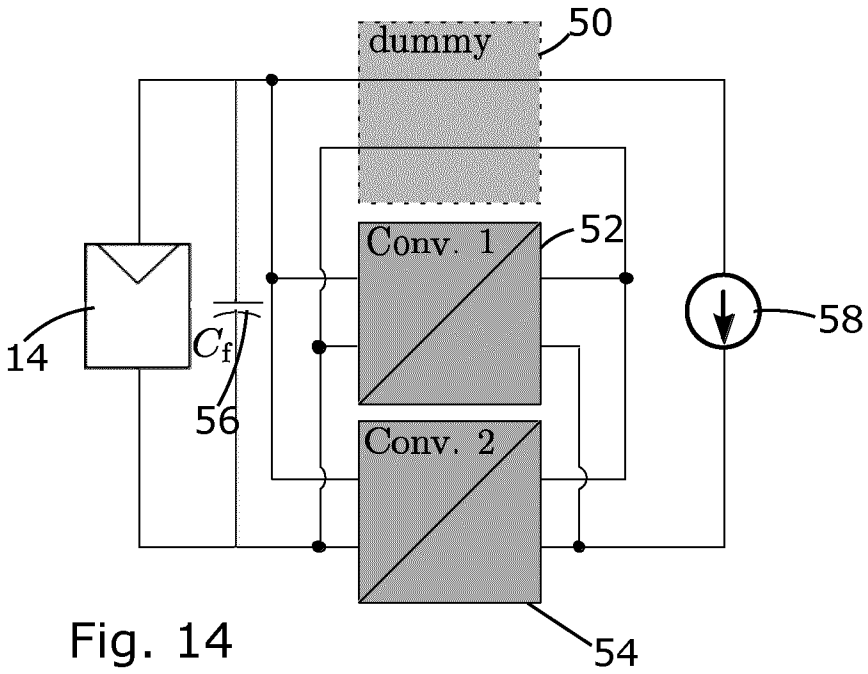


Fig. 14

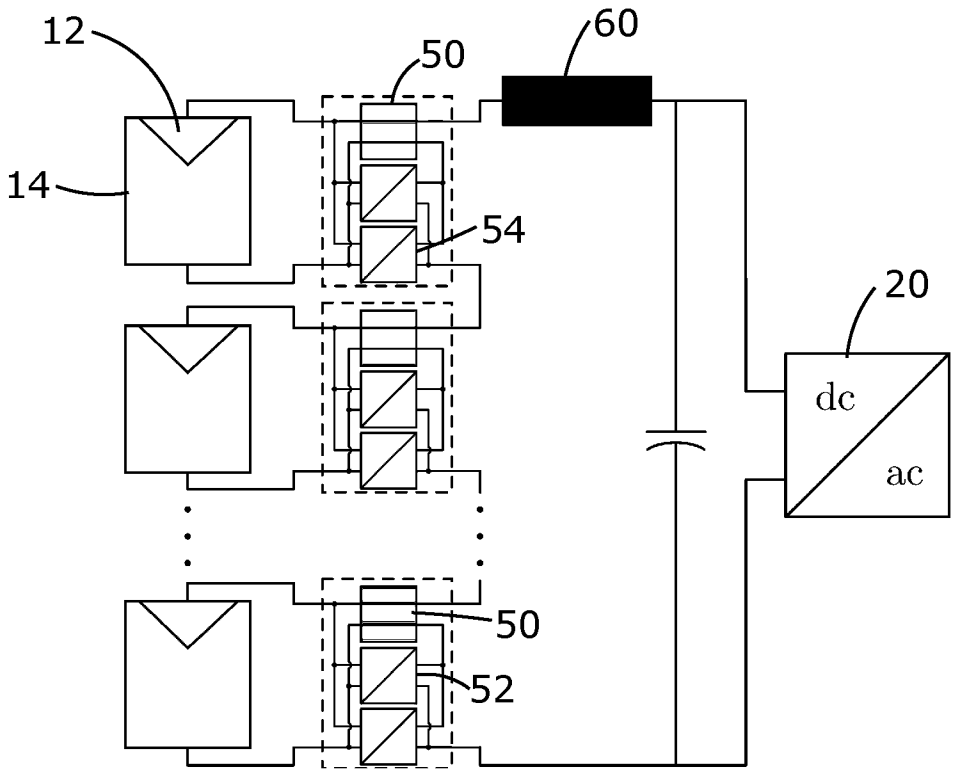


Fig. 15

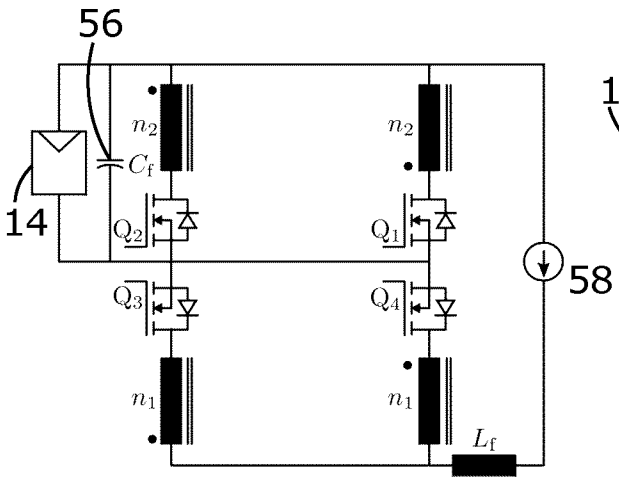


Fig. 16A

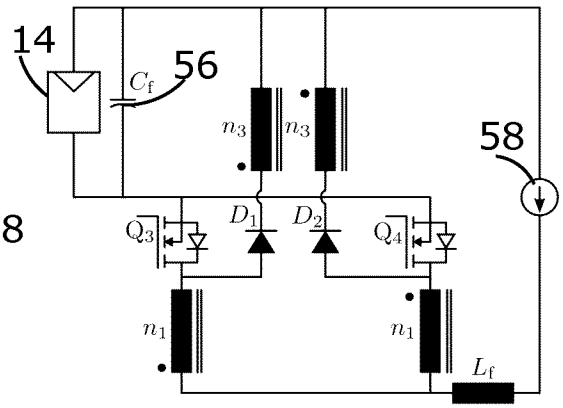


Fig. 16B

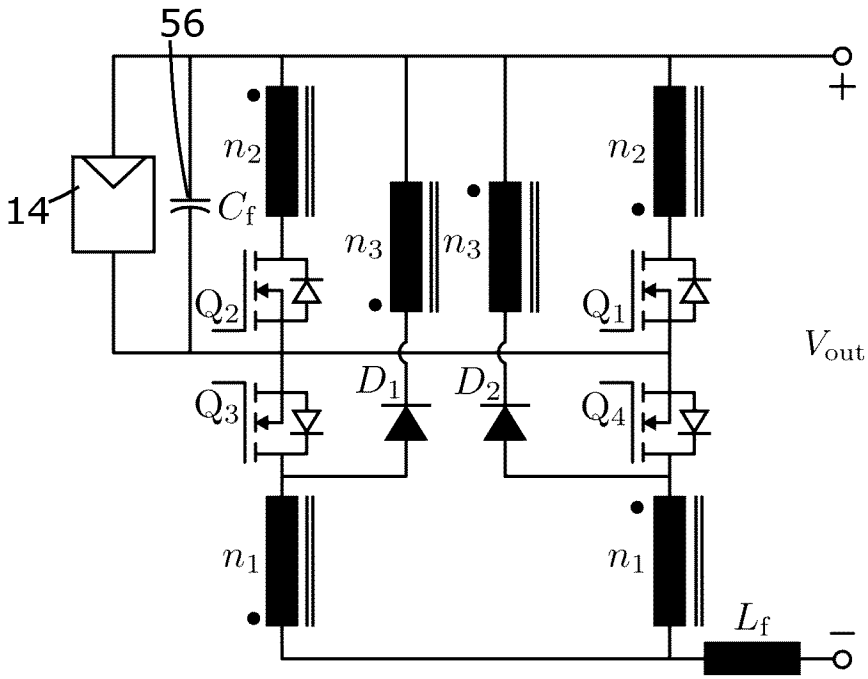


Fig. 17

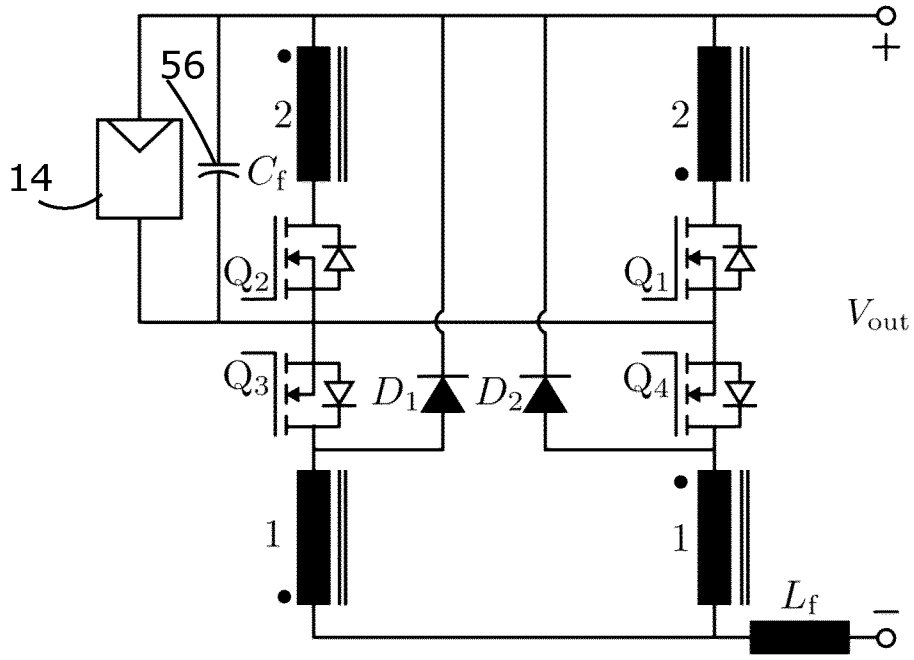


Fig. 18

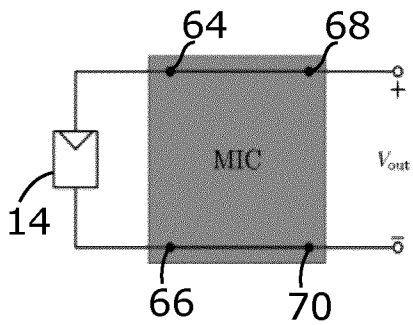


Fig. 19A

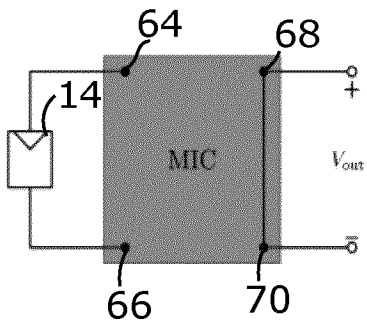


Fig. 19B

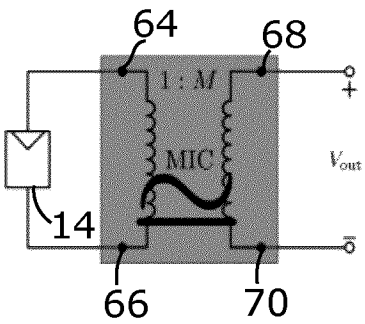
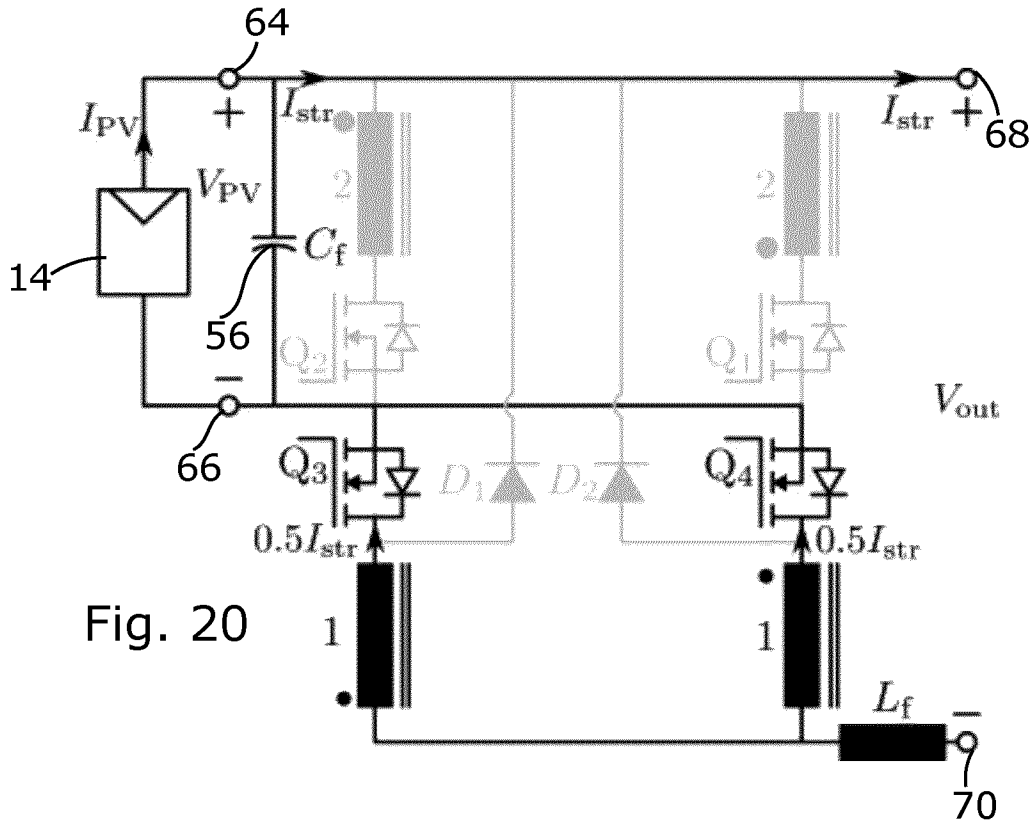


Fig. 19C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I_{PV}
+
I_{str}
I_{str}
+
68
V_{PV}
C_f
14
56
2
2
Q_2
Q_1
−
V_{out}
66
Q_3
D_1
D_2
Q_4
$0.5I_{str}$
$0.5I_{str}$
1
1
L_f
−
70

Fig. 20

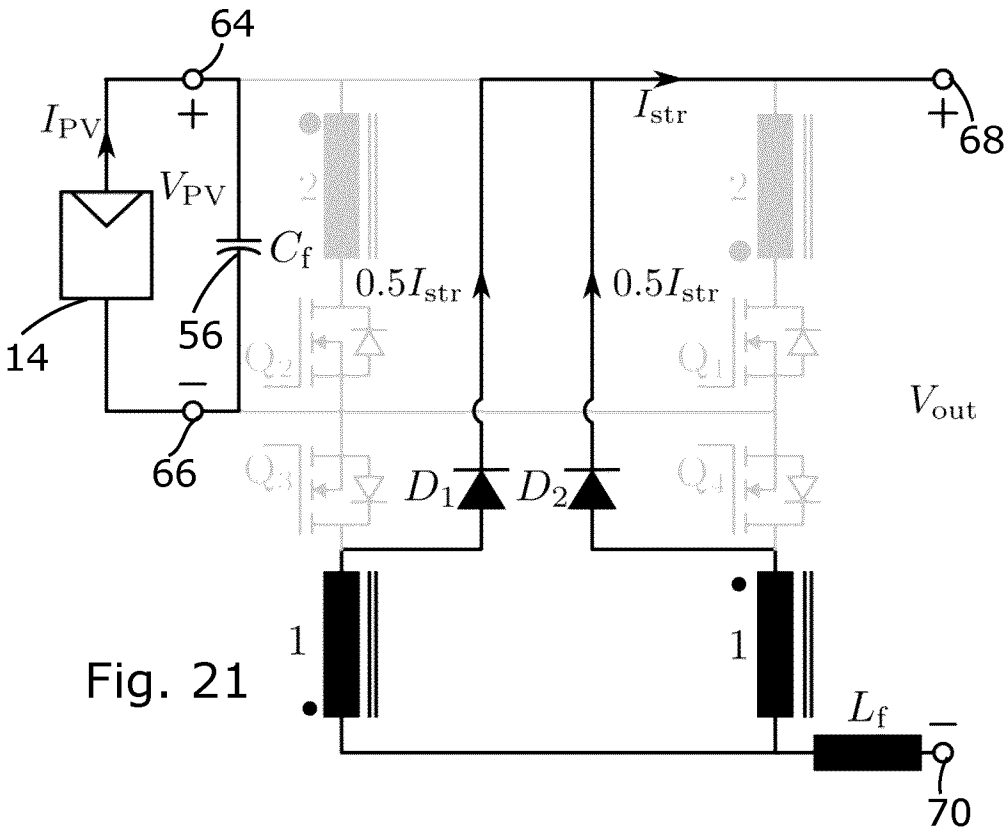
64
I_{PV}
+
I_{str}
+
68
V_{PV}
C_f
2
2
$0.5I_{str}$
$0.5I_{str}$
14
56
Q_2
Q_1
−
V_{out}
66
Q_3
D_1
D_2
Q_4
1
1
L_f
−
70

Fig. 21

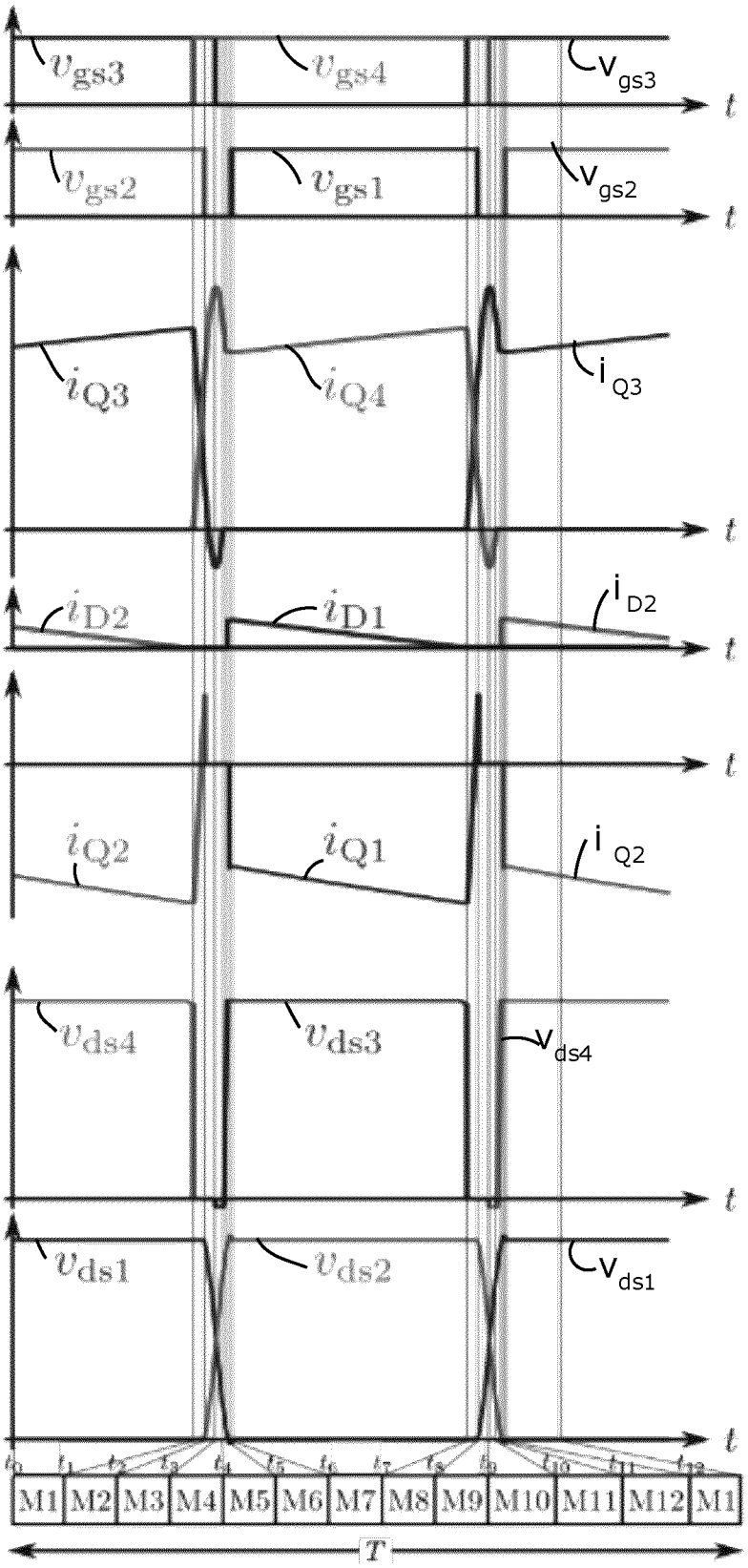
v_{gs3}
v_{gs4}
v_{gs3}
t
v_{gs2}
v_{gs1}
v_{gs2}
t
i_{Q3}
i_{Q4}
i_{Q3}
t
i_{D2}
i_{D1}
i_{D2}
t
t
i_{Q2}
i_{Q1}
i_{Q2}
v_{ds4}
v_{ds3}
v_{ds4}
t
v_{ds1}
v_{ds2}
v_{ds1}
t
t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8 t_9 t_{10} t_{11} t_{12}
M1 M2 M3 M4 M5 M6 M7 M8 M9 M10 M11 M12 M1
T

Fig. 22

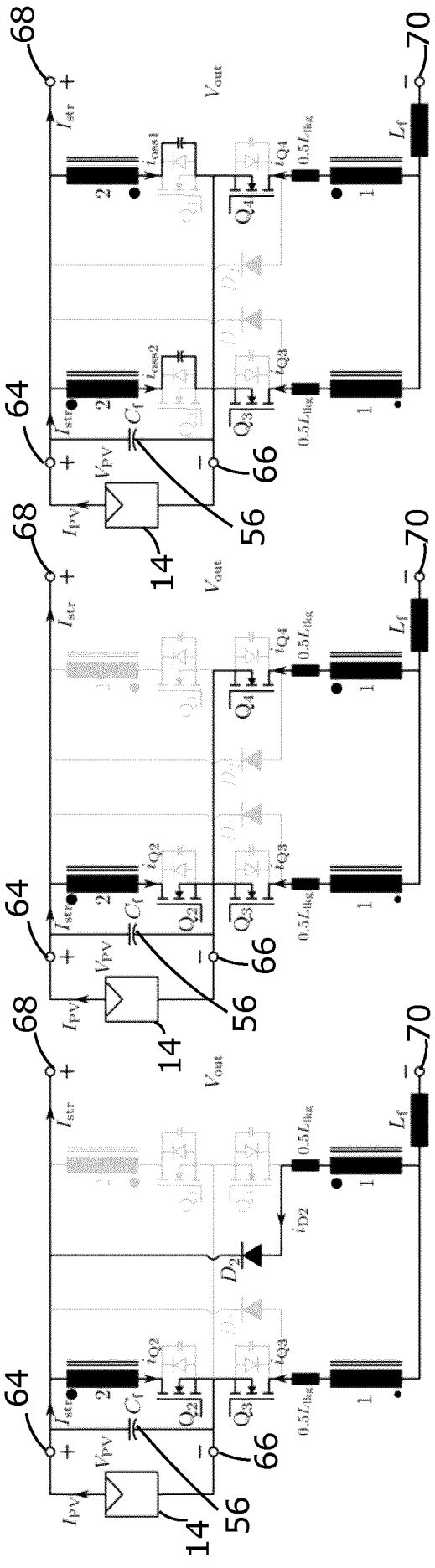

Fig. 23A

Fig. 23B

Fig. 23C

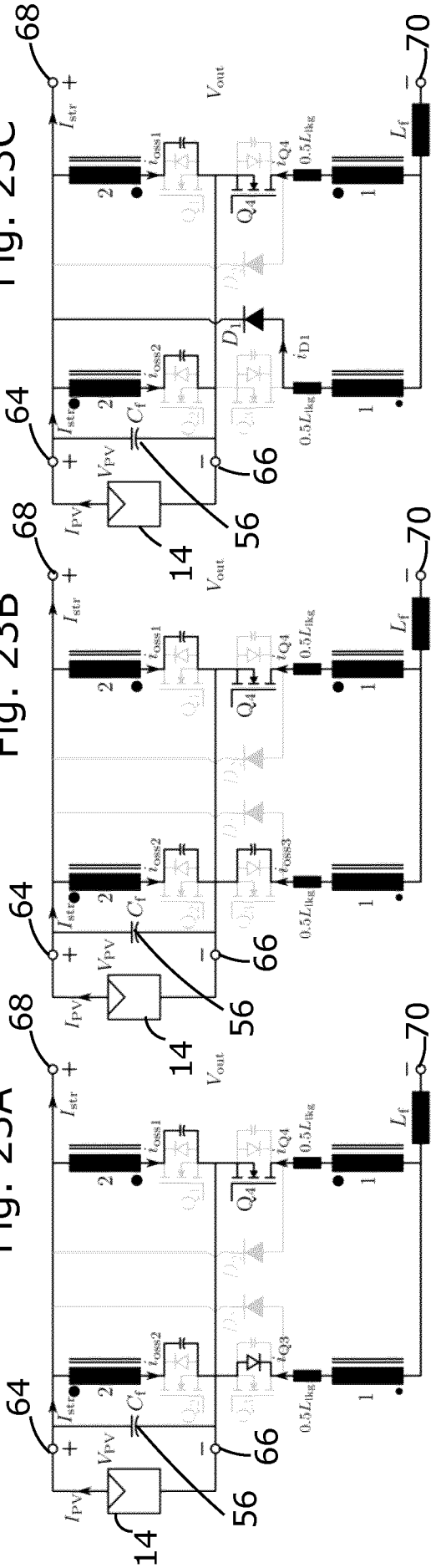

Fig. 23D

Fig. 23E

Fig. 23F

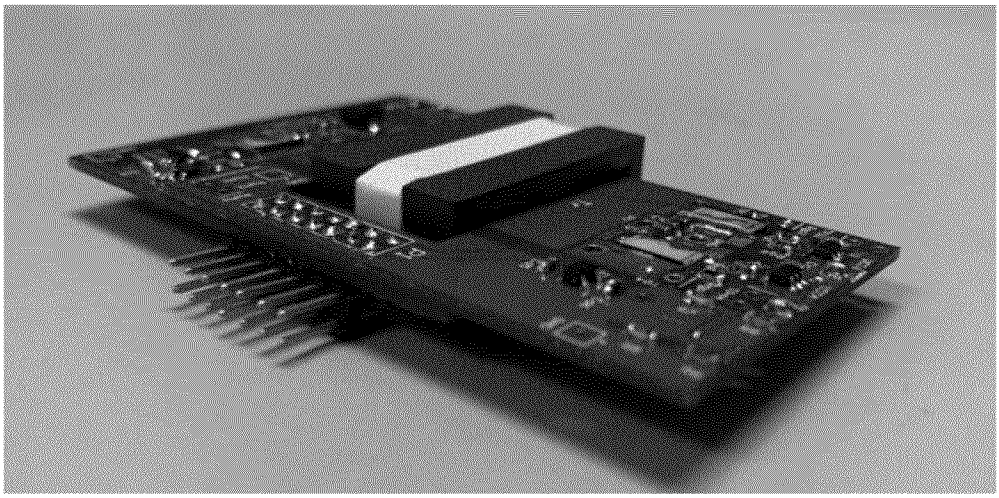

Fig. 24

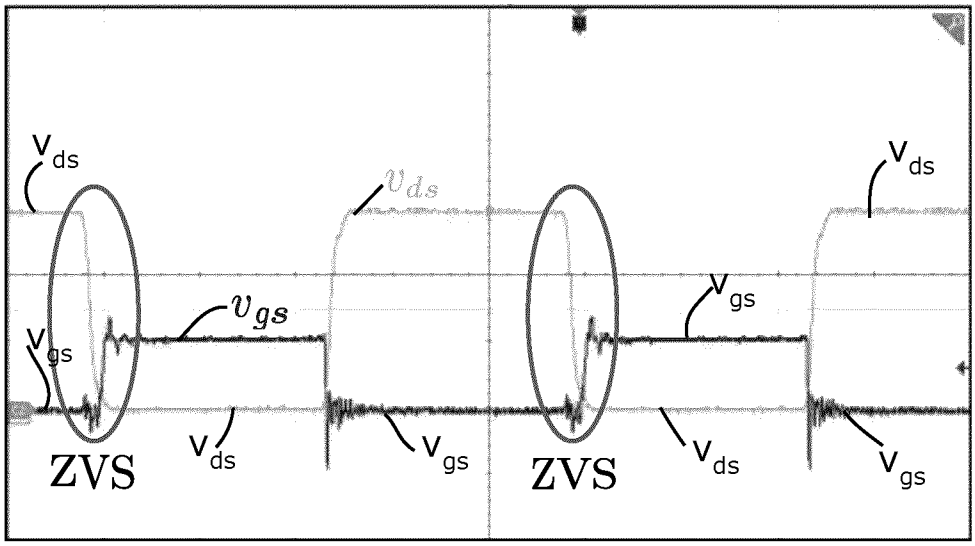

Fig. 25

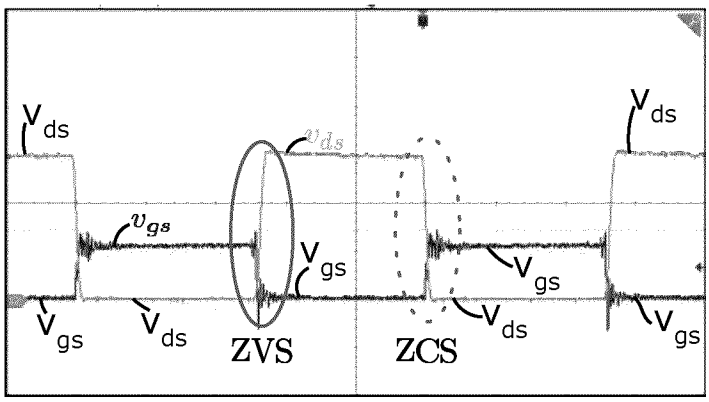

Fig. 26

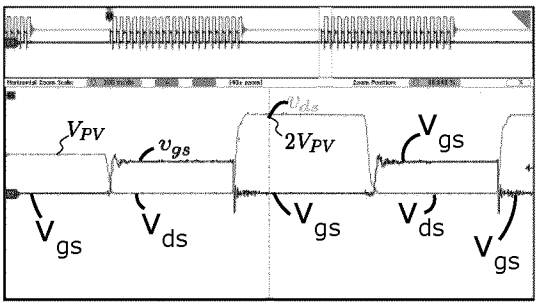

Fig. 27A

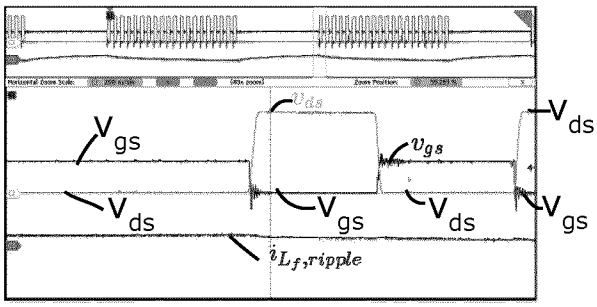

Fig. 27B

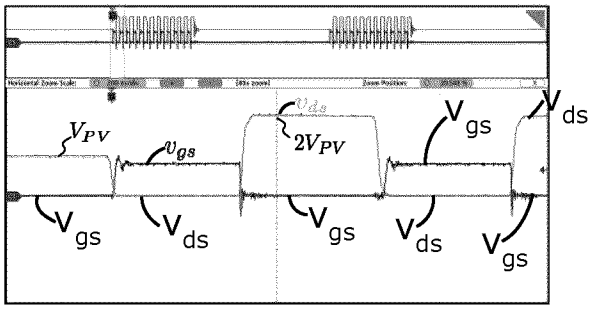

Fig. 28A

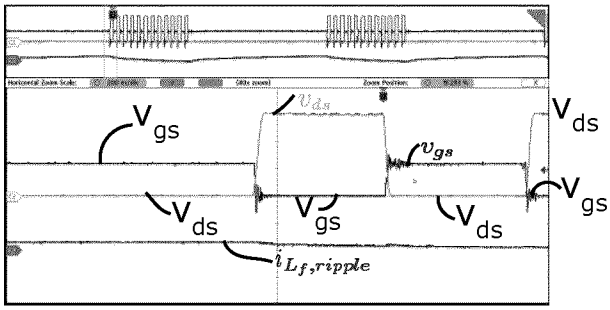

Fig. 28B

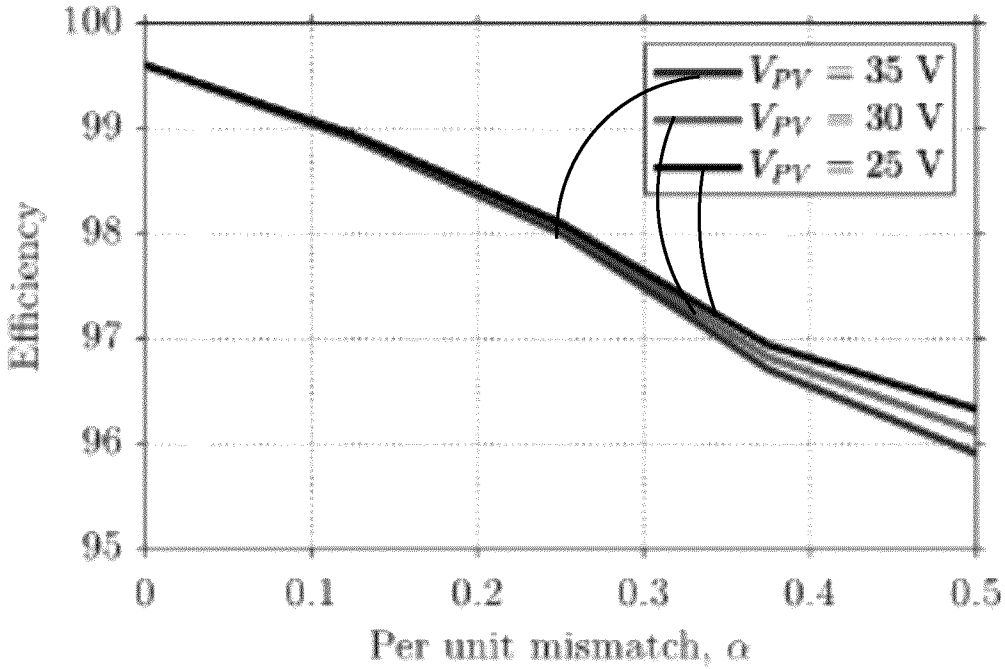
100
99
98
97
96
95
Efficiency
0
0.1
0.2
0.3
0.4
0.5
Per unit mismatch, α
V_{PV} = 35 V
V_{PV} = 30 V
V_{PV} = 25 V

Fig. 29

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2023/051271

A. CLASSIFICATION OF SUBJECT MATTER

IPC: ***H02M 1/00*** (2007.10) , ***H02M 3/00*** (2006.01) , ***H02S 40/32*** (2014.01)

CPC: **H02M 1/0067** (2021.05) , H02M 1/0074 (2021.05) , H02M 1/0077 (2021.05) , H02M 3/00 (2023.05) , H02S 40/32 (2020.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC: H02M 1/00, H02M 3/00, H02S 40/32

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)
Databases: Questel-Orbit (FamPat)
Keywords: voltage, module, converter, integrated, MIC, photovoltaic, PV, DC_DC, transformer, inductor, ISOP, IPOS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO2022102857A1 (KANG, G. et al.) 19 May 2022 (19-05-2022) *Par. [0002]-[0035]; [0045]; Figure 2*	1-22
Y	US20140167513A1 (CHANG, A. et al.) 19 June 2014 (19-06-2014) * Abstract; Par. [0003]-[0012]; [0070]-[0073]; [0095]; Figure 1*	1-22
A	US20200307393A1 (SLEPCHENKOV, M. et al.) 01 October 2020 (01-10-2020) *entire document*	1-22
A	CN112421945 (WEI, M. et al.) 26 February 2021 (26-02-2021) *entire document*	1-22

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"D"	document cited by the applicant in the international application	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"E"	earlier application or patent but published on or after the international filing date	"&"	document member of the same patent family
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)		
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 20 November 2023 (20-11-2023)	Date of mailing of the international search report 23 November 2023 (23-11-2023)
Name and mailing address of the ISA/CA Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 819-953-2476	Authorized officer Maria Salazar (873) 353-0489

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2023/051271

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of the first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claim Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claim Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claim Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

The claims are directed to a plurality of inventive concepts as follows:

Group A - Claims 1-17 are directed to a module integrated converter (MIC) arranged to alter allocation of power through a plurality of converters in order to control the MIC's overall voltage conversion ratio; and

Group B - Claims 18-22 are directed to a DC-DC transformer comprising an arrangement of inductors and switches.

Continued on extra sheet.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claim Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

Continuation of: Box III

The claims cannot be considered to be one invention in the sense of being so linked to form a single general inventive concept because each of the groups possess different special technical features and these features do not share any technical relationship.

The claims must be limited to one inventive concept as set out in PCT Rule 13.

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CA2023/051271

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
WO2022102857A1	19 May 2022 (19-05-2022)	KR20220063516A	17 May 2022 (17-05-2022)
US2014167513A1	19 June 2014 (19-06-2014)	US9407164B2	02 August 2016 (02-08-2016)
		US2014313781A1	23 October 2014 (23-10-2014)
		US9374020B2	21 June 2016 (21-06-2016)
		US2014339918A1	20 November 2014 (20-11-2014)
		US9762145B2	12 September 2017 (12-09-2017)
		US2014355322A1	04 December 2014 (04-12-2014)
		US10218289B2	26 February 2019 (26-02-2019)
		WO2013109719A1	25 July 2013 (25-07-2013)
		WO2013109743A2	25 July 2013 (25-07-2013)
		WO2013109743A3	19 September 2013 (19-09-2013)
		WO2013109797A1	25 July 2013 (25-07-2013)
		WO2013116814A1	08 August 2013 (08-08-2013)
US2020307393A1	01 October 2020 (01-10-2020)	US10807481B1	20 October 2020 (20-10-2020)
		AU2020253330A1	21 October 2021 (21-10-2021)
		AU2020254497A1	21 October 2021 (21-10-2021)
		CA3134697A1	08 October 2020 (08-10-2020)
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		CL2021002529A1	17 June 2022 (17-06-2022)
		CL2021002530A1	17 June 2022 (17-06-2022)
		CN113853719A	28 December 2021 (28-12-2021)
		CN113906645A	07 January 2022 (07-01-2022)
		EP3949063A1	09 February 2022 (09-02-2022)
		EP3949063A4	01 March 2023 (01-03-2023)
		EP3949067A1	09 February 2022 (09-02-2022)
		EP3949067A4	11 January 2023 (11-01-2023)
		IL286764A	31 October 2021 (31-10-2021)
		IL286765A	31 October 2021 (31-10-2021)
		JP2022527301A	01 June 2022 (01-06-2022)
		JP2022527472A	02 June 2022 (02-06-2022)
		KR20210141716A	23 November 2021 (23-11-2021)
		KR20210145228A	01 December 2021 (01-12-2021)
		MX2021011929A	31 January 2022 (31-01-2022)
		MX2021011935A	11 March 2022 (11-03-2022)
		PE20212007A1	18 October 2021 (18-10-2021)
		PE20212032A1	20 October 2021 (20-10-2021)
		SG11202110821RA	28 October 2021 (28-10-2021)
		SG11202110832UA	28 October 2021 (28-10-2021)
		US2020307395A1	01 October 2020 (01-10-2020)
		US10807482B1	20 October 2020 (20-10-2020)
		US2020313445A1	01 October 2020 (01-10-2020)
		US11135923B2	05 October 2021 (05-10-2021)
		US2022161668A1	26 May 2022 (26-05-2022)
		US11597284B2	07 March 2023 (07-03-2023)
		US2022379741A1	01 December 2022 (01-12-2022)
		US11603001B2	14 March 2023 (14-03-2023)
		US2021170886A1	10 June 2021 (10-06-2021)
		US2021170887A1	10 June 2021 (10-06-2021)
		US2023010566A1	12 January 2023 (12-01-2023)
		WO2020205511A1	08 October 2020 (08-10-2020)
		WO2020205574A1	08 October 2020 (08-10-2020)
CN112421945A	26 February 2021 (26-02-2021)	CN112421945B	05 November 2021 (05-11-2021)