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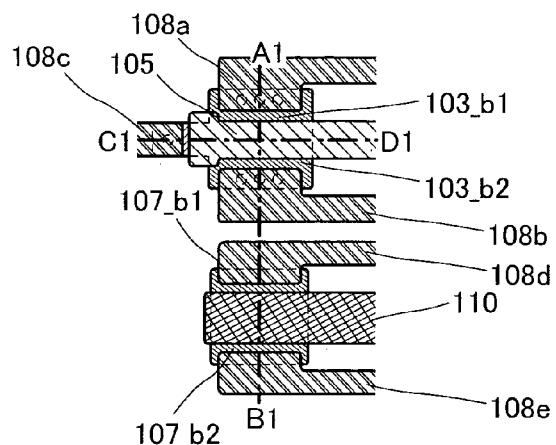
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**(54) Title:** SEMICONDUCTOR DEVICE

FIG. 1A



**(57) Abstract:** A first field-effect transistor provided over a substrate in which an insulating region is provided over a first semiconductor region and a second semiconductor region is provided over the insulating region; an insulating layer provided over the substrate; a second field-effect transistor that is provided one flat surface of the insulating layer and includes an oxide semiconductor layer; and a control terminal are provided. The control terminal is formed in the same step as a source and a drain of the second field-effect transistor, and a voltage for controlling a threshold voltage of the first field-effect transistor is supplied to the control terminal.

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## DESCRIPTION

## SEMICONDUCTOR DEVICE

## 5 TECHNICAL FIELD

[0001]

One embodiment of the present invention relates to a semiconductor device.

## BACKGROUND ART

10 [0002]

In recent years, the information society has been increasingly developed, and the demand for higher speed, higher capacity, smaller size, lighter weight, or the like of, for example, a personal computer, a cellular phone, or the like has been increased. Therefore, semiconductor devices such as a large-scale integrated circuit (also referred 15 to as a large scale integration (LSI)) and a central processing unit (CPU) need higher integration, higher operation speed, and lower power consumption.

[0003]

Power consumption of the semiconductor device is substantially equal to the total of a power consumption generated in an operation state and a power consumption 20 generated in a stop state (hereinafter referred to as a standby power) of the semiconductor device.

[0004]

The standby power can be classified into static standby power and dynamic standby power. The static standby power is power consumed by generation of leakage 25 current between a source and a drain, between a gate and the source, and between the gate and the drain in a state where voltage is not applied between the electrodes of a transistor in the semiconductor device, that is, in a state where a voltage between the gate and the source is approximately 0 V. On the other hand, the dynamic standby power is power which is consumed when voltages of various signals such as a clock 30 signal or a power supply voltage continues to be supplied to a circuit in standby state.

[0005]

Although a microfabrication technique has been developed to obtain higher

operation speed of a semiconductor device, when microfabrication is advanced, a channel of a transistor becomes smaller in length and an insulating layer typified by a gate insulating layer has a smaller thickness. Therefore, leakage current of the transistor is increased and the dynamic standby power tends to be increased. As a 5 method for obtaining higher operation speed of a semiconductor device without microfabrication, a method is given in which a transistor is formed using a substrate in which an insulating region is provided over a first semiconductor region, and a second semiconductor region is provided over the insulating region (also referred to as an SOI substrate) (e.g., Patent Document 1).

10 [Reference]

[Patent Document]

[0006]

[Patent Document 1] Japanese Published Patent Application No. H6-291291

15 DISCLOSURE OF INVENTION

[0007]

The standby power is increased as microfabrication advances and the integration degree is increased. Accordingly, in order to reduce the power consumption, it is important to reduce the standby power.

20 [0008]

In the transistor using the SOI substrate, the first semiconductor region under the insulating region serves as a gate and a threshold voltage is shifted, that is, a back gate effect is caused. Therefore, even when a voltage applied between the gate and the source of the transistor is 0 V, there is a possibility that the amount of current flowing 25 between the source and the drain of the transistor is increased and the power consumption of the semiconductor device is increased.

[0009]

One object of one embodiment of the present invention is to suppress a reduction in operation speed and reduce power consumption.

30 [0010]

In one embodiment of the present invention, a field-effect transistor provided on an SOI substrate and a field-effect transistor which includes an oxide semiconductor

layer and has a low off-state current are provided in a semiconductor device, so that the operation speed is improved and the power consumption is reduced.

[0011]

Further, in one embodiment of the present invention, a control terminal for controlling a threshold voltage of the field-effect transistor provided on the SOI substrate is provided, so that the threshold voltage of the field-effect transistor provided on the SOI substrate is controlled and the power consumption is reduced. At this time, the control terminal is formed in the same step as a source and a drain of the field-effect transistor including the oxide semiconductor layer, whereby an increase in the number of steps is suppressed.

[0012]

Further, the control terminal is electrically connected to an impurity region formed in the second semiconductor region of the SOI substrate. The impurity region has a conductivity type opposite to that of a source region and a drain region of the field-effect transistor provided on the SOI substrate, and a voltage applied to a channel formation region is controlled in accordance with a voltage input via the control terminal. At this time, the impurity region may overlap with a channel formation region of the field-effect transistor including the oxide semiconductor layer, thereby functioning as a terminal (e.g., a back gate) for controlling a threshold voltage of the field-effect transistor including the oxide semiconductor layer. Accordingly, the threshold voltages of the field-effect transistor provided on the SOI substrate and the field-effect transistor including the oxide semiconductor layer can be controlled by the same control voltage so that power consumption is further reduced.

[0013]

In addition, the control terminal may be electrically connected to an impurity region formed in the first semiconductor region of the SOI substrate. The impurity region overlaps with the channel formation region of the field-effect transistor provided on the SOI substrate with the insulating region provided therebetween, and thus, the voltage applied to the channel formation region is controlled by the voltage input via the control terminal.

[0014]

One embodiment of the present invention is a semiconductor device including

a bus interface, a control unit, a cache memory,  $N$  ( $N$  is a natural number greater than or equal to 3) registers, an instruction decoder, and an arithmetic logic unit. At this time, the field-effect transistor provided on the SOI substrate and the field-effect transistor including the oxide semiconductor layer are provided in a unit memory device in the 5 register, and a data signal is input to one of the source and the drain of the field-effect transistor including the oxide semiconductor layer.

[0015]

According to one embodiment of the present invention, a reduction in operation speed can be suppressed and the amount of current flowing between a source 10 and a drain of a transistor which is in an off state can be reduced, which results in a reduction in power consumption.

#### BRIEF DESCRIPTION OF DRAWINGS

[0016]

15 In the accompanying drawings:

FIGS. 1A to 1C illustrate an example of the structure of a semiconductor device in Embodiment 1;

FIGS. 2A1 to 2C2 illustrate an example of a method for manufacturing a semiconductor device in Embodiment 1;

20 FIGS. 3A1 to 3C2 illustrate the example of a method for manufacturing a semiconductor device in Embodiment 1;

FIGS. 4A1 to 4B2 illustrate the example of a method for manufacturing a semiconductor device in Embodiment 1;

25 FIGS. 5A1 to 5B2, illustrate the example of a method for manufacturing a semiconductor device in Embodiment 1;

FIGS. 6A1 to 6B2 illustrate the example of a method for manufacturing a semiconductor device in Embodiment 1;

FIGS. 7A to 7C illustrate an example of the structure of a semiconductor device in Embodiment 2;

30 FIGS. 8A to 8D illustrate an example of the structure of a semiconductor device in Embodiment 3;

FIG. 9 illustrates an example of an arithmetic processing unit in Embodiment

4;

FIGS. 10A and 10B illustrate an example of the structure of a unit memory device;

5 FIGS. 11A to 11C illustrate an example of the structure of a unit memory device;

FIGS. 12A to 12D are schematic views illustrating examples of electronic devices in Embodiment 8.

FIGS. 13A to 13E illustrate structures of oxide materials;

FIGS. 14A to 14C illustrate the structure of an oxide material;

10 FIGS. 15A to 15C illustrate the structure of an oxide material;

FIG. 16 is a graph showing gate voltage dependence of mobility obtained by calculation;

FIGS. 17A to 17C are each a graph showing gate voltage dependence of drain current and mobility obtained by calculation;

15 FIGS. 18A to 18C are each a graph showing gate voltage dependence of drain current and mobility obtained by calculation;

FIGS. 19A to 19C are each a graph showing gate voltage dependence of drain current and mobility obtained by calculation;

20 FIGS. 20A and 20B illustrate cross-sectional structures of transistors used for calculation;

FIGS. 21A to 21C are each a graphs showing characteristics of a transistor;

FIGS. 22A and 22B each show characteristics of a transistor;

FIGS. 23A and 23B each show characteristics of a transistor;

FIG. 24 shows characteristics of a transistor;

25 FIGS. 25A and 25B show characteristics of a transistor;

FIG. 26 shows XRD spectra of oxide materials;

FIG. 27 shows characteristics of a transistor;

FIGS. 28A and 28B are a plan view and a cross-sectional view of a semiconductor device; and

30 FIGS. 29A and 29B are a plan view and a cross-sectional view of a semiconductor device.

## BEST MODE FOR CARRYING OUT THE INVENTION

[0017]

Examples of embodiments describing the present invention will be described with reference to the drawings below. Note that it is easy for those skilled in the art to change contents in an embodiment without departing from the spirit and the scope of the present invention. Thus, the present invention should not be limited to the description of the following embodiments.

[0018]

Note that the contents in different embodiments can be combined with one another as appropriate. In addition, the contents in different embodiments can be interchanged one another.

[0019]

Further, ordinal numbers such as "first" and "second" are added for avoiding confusion between components and the number of components is not limited to the number of ordinal numbers.

[0020]

Note that the components illustrated in the drawings may include those having sizes different from the actual sizes for convenience.

[0021]

20 (Embodiment 1)

In this embodiment, an example of a semiconductor device including a transistor which is provided on an SOI substrate and a transistor including an oxide semiconductor layer will be described.

[0022]

25 A structure example of the semiconductor device in this embodiment is described with reference to FIGS. 1A to 1C. FIG. 1A is a schematic top view, FIG. 1B is a schematic cross-sectional view taken along line A1-B1 of FIG. 1A, and FIG. 1C is a schematic cross-sectional view taken along line C1-D1 of FIG. 1A.

[0023]

30 The semiconductor device illustrated in FIGS. 1A to 1C includes a semiconductor layer 101, an insulating layer 102, a semiconductor layer 103, an insulating layer 104, a conductive layer 105, an insulating layer 106, a semiconductor

layer 107, conductive layers 108a to 108e, an insulating layer 109, and a conductive layer 110. A transistor 100a and a transistor 100b are formed using the above structure.

[0024]

5 Note that, in the semiconductor device, a field-effect transistor can be used as the transistor, for example.

[0025]

Depending on a structure or operation conditions of a transistor, a source and a drain of the transistor are interchanged in some cases.

10 [0026]

Voltage generally refers to a difference between potentials at two points (also referred to as a potential difference). However, values of both a voltage and a potential are represented using volt (V) in a circuit diagram or the like in some cases, so that it is difficult to discriminate between them. This is why in this specification, a 15 potential difference between a potential at one point and a potential to be the reference (also referred to as the reference potential) is used as a voltage at the point in some cases.

[0027]

When a period in which two or more components are electrically connected to 20 each other exists, it can be said that the two or more components are electrically connected to each other.

[0028]

The transistor 100a is formed using a signal crystal semiconductor layer of silicon or the like, for example. The transistor 100a is used as a transistor of a logic 25 circuit in the semiconductor device, for example.

[0029]

The transistor 100b is a transistor including an oxide semiconductor layer whose off-state current is lower than that of a conventional transistor including a semiconductor layer of silicon or the like. The oxide semiconductor layer has a wider 30 bandgap than silicon and is an intrinsic (i-type) or substantially intrinsic semiconductor layer. The off-state current per micrometer of the channel width of the transistor including the oxide semiconductor layer is lower than or equal to 10 aA ( $1 \times 10^{-17}$  A),

preferably lower than or equal to 1 aA ( $1 \times 10^{-18}$  A), further preferably lower than or equal to 10 zA ( $1 \times 10^{-20}$  A), further preferably lower than or equal to 1 zA ( $1 \times 10^{-21}$  A), much further preferably lower than or equal to 100 yA ( $1 \times 10^{-22}$  A). The transistor 100b is used as a transistor of a memory circuit, for example. Data is input 5 to a portion where a source or a drain of the transistor 100b is electrically connected to another circuit or element, and then the transistor 100b is turned off, whereby the data can be retained for a long time. However, this embodiment is not limited thereto, and the transistor 100b can also be used for a logic circuit or the like.

[0030]

10 The semiconductor layer 101 is a first semiconductor region in the SOI substrate. The semiconductor layer 101 is formed using a semiconductor substrate, for example. As the semiconductor substrate, for example, a silicon substrate or the like can be used.

[0031]

15 The insulating layer 102 is provided over the semiconductor layer 101.

[0032]

The insulating layer 102 is an insulating region in the SOI substrate. As the insulating layer 102, for example, a layer of a material such as silicon oxide can be used.

20 [0033]

The semiconductor layer 103 is provided over the insulating layer 102.

[0034]

The semiconductor layer 103 includes a region 103\_a, a region 103\_b1, a region 103\_b2, and a region 103\_c.

25 [0035]

The region 103\_a is a region between the region 103\_b1 and the region 103\_b2. The region 103\_a is a region where a channel is formed (also referred to as a channel formation region).

[0036]

30 The region 103\_b1 and the region 103\_b2 are apart from each other. The region 103\_b1 is a region serving as one of a source region and a drain region of the

transistor 100a, and the region 103\_b2 is a region serving as the other of the source region and the drain region of the transistor 100a. The region 103\_b1 and the region 103\_b2 include an impurity element imparting n-type or p-type conductivity type. As the impurity element imparting n-type or p-type conductivity type, for example, 5 phosphorus, boron, or the like can be used.

[0037]

Further, the region 103\_c is in contact with the region 103\_a where the channel is formed and includes an impurity element imparting a conductivity type opposite to that of the region 103\_b1 and the region 103\_b2. At this time, the region 103\_c has a 10 conductivity type opposite to that of the region 103\_b1 and the region 103\_b2. A voltage is applied to the region 103\_a via the region 103\_c. Further, the concentration of the impurity element added to the region 103\_c is set higher than the concentration of the impurity element added to the region 103\_a, whereby contact resistance with the region 103\_a can be reduced.

15 [0038]

The semiconductor layer 103 is at least part of a second semiconductor region in the SOI substrate. Note that the transistor 100a can also be formed in such a manner that a semiconductor region surrounded by an insulating region is used instead of the semiconductor layer 103.

20 [0039]

The semiconductor layer 103 can be formed using, for example, a single crystal semiconductor layer, e.g., a layer of a material such as single crystal silicon.

[0040]

25 The insulating layer 104 is provided over one flat surface of the semiconductor layer 103.

[0041]

As the insulating layer 104, a silicon oxide layer, a silicon nitride layer, a 30 silicon oxynitride layer, a silicon nitride oxide layer, an aluminum oxide layer, an aluminum nitride layer, an aluminum oxynitride layer, an aluminum nitride oxide layer, or a hafnium oxide layer can be used, for example. The insulating layer 104 can also be formed by stacking layers of materials which can be applied to the insulating layer

104.

[0042]

The insulating layer 104 functions as a gate insulating layer in the transistor 100a.

5 [0043]

The conductive layer 105 overlaps with part of the semiconductor layer 103 (the region 103\_a) with the insulating layer 104 provided therebetween.

[0044]

10 As the conductive layer 105, a layer of a metal material such as aluminum, chromium, copper, tantalum, titanium, molybdenum, or tungsten; or an alloy material which contains any of the above metal materials as a main component can be used, for example. The conductive layer 105 can also be formed by stacking layers of materials which can be applied to the conductive layer 105.

[0045]

15 The conductive layer 105 functions as a gate in the transistor 100a.

[0046]

The insulating layer 106 is provided over the insulating layer 104 and the conductive layer 105.

[0047]

20 As the insulating layer 106, a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, an aluminum oxide layer, an aluminum nitride layer, an aluminum oxynitride layer, an aluminum nitride oxide layer, or a hafnium oxide layer can be used, for example. The insulating layer 106 can also be formed by stacking layers of materials which can be applied to the insulating layer

25 106.

[0048]

The insulating layer 106 functions as a planarization insulating layer.

[0049]

30 The semiconductor layer 107 is provided over one flat surface of the insulating layer 106.

[0050]

The semiconductor layer 107 includes a region 107\_a. Further, a region 107\_b1 and a region 107\_b2 are provided in the semiconductor layer 107 as illustrated in FIGS. 1A and 1B but are not necessarily provided.

[0051]

5 The region 107\_a is a region between the region 107\_b1 and the region 107\_b2. The region 107\_a is a channel formation region of the transistor 100b.

[0052]

The region 107\_b1 and the region 107\_b2 are apart from each other and include an element serving as a dopant. As the dopant, for example, one or more of 10 elements of Group 15 in the periodic table (e.g., one or more of nitrogen, phosphorus, arsenic) and one or more of rare gas elements (e.g., one or more of helium, argon, xenon) can be used. When the dopants are added to form regions functioning as a source region and a drain region, even in the case where the area of the transistor is 15 small, a resistance value between the source or drain and the channel formation region of the transistor can be reduced. Thus, the area of a circuit of the semiconductor device can be reduced.

[0053]

As the semiconductor layer 107, an oxide semiconductor layer containing a four-component metal oxide, a three-component metal oxide, a two-component metal 20 oxide, a single-component metal oxide, or the like can be used, for example.

[0054]

An oxide semiconductor to be used preferably contains at least indium (In) or zinc (Zn). In particular, In and Zn are preferably contained. As a stabilizer for 25 reducing variation in electric characteristics of a transistor using the oxide semiconductor, gallium (Ga) is preferably additionally contained. Tin (Sn) is preferably contained as a stabilizer. Hafnium (Hf) is preferably contained as a stabilizer. Aluminum (Al) is preferably contained as a stabilizer.

[0055]

As another stabilizer, one or plural kinds of lanthanoid such as lanthanum (La), 30 cerium (Ce), praseodymium (Pr), neodymium (Nd), samarium (Sm), europium (Eu), gadolinium (Gd), terbium (Tb), dysprosium (Dy), holmium (Ho), erbium (Er), thulium

(Tm), ytterbium (Yb), or lutetium (Lu) may be contained.

[0056]

For example, as the four-component metal oxide, an In-Sn-Ga-Zn-O-based metal oxide, an In-Hf-Ga-Zn-O-based metal oxide, an In-Al-Ga-Zn-O-based metal oxide, an In-Sn-Al-Zn-O-based metal oxide, an In-Sn-Hf-Zn-O-based metal oxide, an In-Hf-Al-Zn-O-based metal oxide, or the like can be used.

[0057]

As the oxide of three metal elements, an In-Ga-Zn-O-based metal oxide, an In-Sn-Zn-O-based metal oxide, an In-Al-Zn-O-based metal oxide, a Sn-Ga-Zn-O-based metal oxide, an Al-Ga-Zn-O-based metal oxide, a Sn-Al-Zn-O-based metal oxide, an In-Hf-Zn-O-based metal oxide, an In-La-Zn-O-based metal oxide, an In-Ce-Zn-O-based metal oxide, an In-Pr-Zn-O-based metal oxide, an In-Nd-Zn-O-based metal oxide, an In-Sm-Zn-O-based metal oxide, an In-Eu-Zn-O-based metal oxide, an In-Gd-Zn-O-based metal oxide, an In-Tb-Zn-O-based metal oxide, an In-Dy-Zn-O-based metal oxide, an In-Ho-Zn-O-based metal oxide, an In-Er-Zn-O-based metal oxide, an In-Tm-Zn-O-based metal oxide, an In-Yb-Zn-O-based metal oxide, or an In-Lu-Zn-O-based metal oxide can be used, for example.

[0058]

As the two-component metal oxide, an In-Zn-O-based metal oxide, a Sn-Zn-O-based metal oxide, an Al-Zn-O-based metal oxide, a Zn-Mg-O-based metal oxide, a Sn-Mg-O-based metal oxide, an In-Mg-O-based metal oxide, an In-Sn-O-based metal oxide, or an In-Ga-O-based metal oxide can be used, for example.

[0059]

Note that an In-Ga-Zn-O-based metal oxide, refers to a metal oxide whose main components are In, Ga, and Zn, and there is no particular limitation on the ratio of In: Ga: Zn. The In-Ga-Zn-O-based oxide may contain a metal element other than the In, Ga, and Zn.

[0060]

In the case of using an In-Zn-O-based metal oxide, for example, an oxide target which has a composition ratio of In:Zn = 50:1 to 1:2 in an atomic ratio (In<sub>2</sub>O<sub>3</sub>:ZnO =

25:1 to 1:4 in a molar ratio), preferably In:Zn = 20:1 to 1:1 in an atomic ratio (In<sub>2</sub>O<sub>3</sub>:ZnO = 10:1 to 1:2 in a molar ratio), further preferably In:Zn = 15:1 to 1.5:1 (In<sub>2</sub>O<sub>3</sub>:ZnO = 15:2 to 3:4 in a molar ratio) can be used for formation. For example, when the atomic ratio of the target used for the deposition of the In-Zn-O-based oxide 5 semiconductor is expressed by In:Zn:O = P:Q:R, R > 1.5P + Q. An increase in the amount of indium enables mobility of the transistor to increase.

[0061]

Further, in the case of an In-Sn-Zn-O-based metal oxide, an oxide target having a composition ratio of In:Sn:Zn = 1:2:2, In:Sn:Zn = 2:1:3, In:Sn:Zn = 1:1:1, In:Sn:Zn = 10 20:45:35, or the like is used.

[0062]

Alternatively, as the semiconductor layer 107, a layer of an I-O-based metal oxide, a Sn-O-based metal oxide, a Zn-O-based metal oxide, or the like can be used, for example. Further, the metal oxide that can be used as the oxide semiconductor may 15 contain silicon oxide. Alternatively, the metal oxide that can be used as the oxide semiconductor may contain nitrogen.

[0063]

Alternatively, as the semiconductor layer 107, a layer of a material represented by In<sub>LO<sub>3</sub></sub>(ZnO)<sub>l</sub> (l is larger than 0 and is not an integer) can be used. Here, L in 20 In<sub>LO<sub>3</sub></sub>(ZnO)<sub>l</sub> represents one or more metal elements selected from Ga, Fe, Al, Mn, or Co. As the oxide semiconductor, a layer of a material represented by In<sub>3</sub>SnO<sub>5</sub>(ZnO)<sub>n</sub> (n is larger than 0 and is an integer) can also be used.

[0064]

For example, an In-Ga-Zn-O-based metal oxide with an atomic ratio of 25 In:Ga:Zn = 1:1:1 (= 1/3:1/3:1/3) or In:Ga:Zn = 2:2:1 (= 2/5:2/5:1/5), or an oxide with an atomic ratio close to the above atomic ratios can be used. Alternatively, an In-Sn-Zn-O-based oxide with an atomic ratio of In:Sn:Zn = 1:1:1 (= 1/3:1/3:1/3), In:Sn:Zn = 2:1:3 (= 1/3:1/6:1/2), or In:Sn:Zn = 2:1:5 (= 1/4:1/8:5/8), or an oxide with an atomic ratio close to the above atomic ratios may be used.

30 [0065]

However, without limitation to the materials given above, a material with an

appropriate composition may be used depending on desired semiconductor characteristics (e.g., mobility, threshold voltage, and variation). In order to obtain the needed semiconductor characteristics, it is preferable that the carrier concentration, the impurity concentration, the defect density, the atomic ratio of a metal element to oxygen, 5 the interatomic distance, the density, and the like be set to be appropriate.

[0066]

For example, high mobility can be obtained relatively easily in the case where the In-Sn-Zn-O-based metal oxide is used. However, the mobility can be increased by reducing the defect density in the bulk also in the case where the In-Ga-Zn-O-based 10 metal oxide is used.

[0067]

Note that for example, the expression "the composition of an oxide including In, Ga, and Zn at the atomic ratio,  $\text{In:Ga:Zn} = a:b:c$  ( $a + b + c = 1$ ), is in the neighborhood of the composition of an oxide including In, Ga, and Zn at the atomic ratio,  $\text{In:Ga:Zn} = 15 \text{A:B:C}$  ( $\text{A} + \text{B} + \text{C} = 1$ )" means that  $a$ ,  $b$ , and  $c$  satisfy the following relation:  $(a-\text{A})^2 + (b-\text{B})^2 + (c-\text{C})^2 \leq r^2$ , and  $r$  may be 0.05, for example. The same applies to other oxides.

[0068]

The oxide semiconductor may be either single crystal or non-single-crystal. 20 In the latter case, the oxide semiconductor may be either amorphous or polycrystal. Further, the oxide semiconductor may have either an amorphous structure including a portion having crystallinity or a non-amorphous structure.

[0069]

In an oxide semiconductor in an amorphous state, a flat surface can be obtained 25 with relative ease, so that when a transistor is manufactured with the use of the oxide semiconductor, interface scattering can be reduced, and relatively high mobility can be obtained with relative ease.

[0070]

In an oxide semiconductor having crystallinity, defects in the bulk can be 30 further reduced and when a surface flatness is improved, mobility higher than that of an oxide semiconductor layer in an amorphous state can be obtained. In order to improve

the surface flatness, the oxide semiconductor is preferably formed over a flat surface. Specifically, the oxide semiconductor may be formed over a surface with the average surface roughness ( $R_a$ ) of less than or equal to 1 nm, preferably less than or equal to 0.3 nm, more preferably less than or equal to 0.1 nm.

5 [0071]

Note that,  $R_a$  is obtained by three-dimension expansion of center line average roughness that is defined by JIS B 0601 so as to be applied to a plane. The  $R_a$  can be expressed as an "average value of the absolute values of deviations from a reference surface to a specific surface" and is defined by the formula below.

10 [0072]

[Formula 1]

$$R_a = \frac{1}{S_0} \int_{y_1}^{y_2} \int_{x_1}^{x_2} |f(x, y) - Z_0| dx dy$$

[0073]

In the above formula,  $S_0$  represents an area of a plane to be measured (a rectangular region which is defined by four points represented by coordinates  $(x_1, y_1)$ ,  $(x_1, y_2)$ ,  $(x_2, y_1)$ , and  $(x_2, y_2)$ ), and  $Z_0$  represents an average height of the plane to be measured.  $R_a$  can be measured using an atomic force microscope (AFM). Note that the measurement plane is a plane which is shown by all the measurement data, and the measurement data consists of three parameters  $(x, y, z)$  and is represented by  $z = f(x, y)$ .

20 The range of  $x$  (and  $y$ ) is from 0 to  $x_{\max}$  (and  $y_{\max}$ ), and the range of  $z$  is from  $z_{\min}$  to  $z_{\max}$ .

[0074]

At least the region of the semiconductor layer 107 where the channel is formed may be non-single-crystal and includes a phase which has a triangular, hexagonal, regular triangular, or regular hexagonal atomic arrangement when seen from the 25 direction perpendicular to the a-b plane and in which metal atoms are arranged in a layered manner when seen from the direction perpendicular to the c-axis direction or metal atoms and oxygen atoms are arranged in a layered manner when seen from the direction perpendicular to the c-axis direction. The formation of the above phase makes it possible to suppress degradation of the transistor due to light. Note that the 30 material having the phase is also referred to as a c-axis aligned crystal or CAAC.

[0075]

The conductive layer 108a is electrically connected to the region 103\_b1 via a first opening which penetrates the insulating layer 104 and the insulating layer 106.

[0076]

5 The conductive layer 108a functions as one of the source and the drain of the transistor 100a.

[0077]

The conductive layer 108b is electrically connected to the region 103\_b2 via a second opening which penetrates the insulating layer 104 and the insulating layer 106.

10 [0078]

The conductive layer 108b functions as the other of the source and the drain of the transistor 100a.

[0079]

15 The conductive layer 108c is electrically connected to the region 103\_c via a third opening which penetrates the insulating layer 104 and the insulating layer 106.

[0080]

The conductive layer 108c functions as a control terminal for controlling a voltage applied to the region 103\_a of the transistor 100a.

[0081]

20 The conductive layer 108d is electrically connected to the semiconductor layer 107.

[0082]

The conductive layer 108d functions as one of a source and a drain of the transistor 100b.

25 [0083]

The conductive layer 108e is electrically connected to the semiconductor layer 107.

[0084]

30 The conductive layer 108e functions as the other of the source and the drain of the transistor 100b.

[0085]

Note that although the conductive layer 108d and the conductive layer 108e are provided over the semiconductor layer 107 as illustrated in FIGS. 1A and 1B, this embodiment is not limited thereto, and the semiconductor layer 107 may be provided over the conductive layer 108d and the conductive layer 108e.

5 [0086]

The conductive layer 108c is formed in the same step as the conductive layer 108d and the conductive layer 108e. In addition, the conductive layer 108a and the conductive layer 108b may be formed in the same step as the conductive layer 108c to the conductive layer 108e. Each of the conductive layers 108a to 108e can be formed using, for example, a layer of a metal material such as aluminum, chromium, copper, tantalum, titanium, molybdenum, or tungsten; or an alloy material which contains any of the above metal materials as a main component. As the layer of the alloy material, for example, a layer of a Cu-Mg-Al alloy material can be used.

[0087]

15 Further, a layer including a conductive metal oxide can be used as each of the conductive layers 108a to 108e. Note that the conductive metal oxide which can be used for each of the conductive layers 108a to 108e may include silicon oxide.

[0088]

20 The conductive layers 108a to 108e can also be formed by stacking layers of materials which can be applied to the conductive layers 108a to 108e. For example, the conductive layers 108a to 108e are each formed with a stack in which a copper layer is provided over a layer of a Cu-Mg-Al alloy material, whereby adhesion between the conductive layers 108a to 108e and other layers in contact with the conductive layers 108a to 108e can be increased.

25 [0089]

The insulating layer 109 is provided over the insulating layer 106, the semiconductor layer 107, and the conductive layers 108a to 108e.

[0090]

30 A silicon oxide layer can be used as the insulating layer 109, for example. Alternatively, the insulating layer 109 can be formed using a stack of a silicon oxide layer and another layer.

[0091]

The conductive layer 110 overlaps with the semiconductor layer 107 with the insulating layer 109 provided therebetween.

[0092]

The conductive layer 110 can be, for example, a layer of a metal material such 5 as aluminum, chromium, copper, tantalum, titanium, molybdenum, or tungsten; or an alloy material which contains any of the above metal materials as a main component.

[0093]

In the semiconductor device illustrated in FIGS. 1A to 1C, a control voltage is applied via the conductive layer 108c serving as the control terminal. Then, a voltage 10 of the region 103\_a can be controlled to be a level in accordance with the control voltage. For example, in the case where the transistor 100a is a p-channel transistor, when the level of the control voltage is increased, a threshold voltage of the transistor 100a is negatively shifted. Thus, even in the case where the threshold voltage of the transistor 100a varies owing to the semiconductor layer 101, when the control voltage is 15 input via the conductive layer 108c to control the voltage of the region 103\_a and the threshold voltage of the transistor 100a, whereby the amount of current flowing between the source and the drain of the transistor 100a which is in an off state can be reduced. The threshold voltage of the transistor 100a is preferably controlled so that the transistor 100a becomes an enhancement type transistor, for example.

20 [0094]

Note that when the transistor 100a and the transistor 100b have the same conductivity type, the region 103\_c may overlap with the channel formation region of the transistor 100b, so that threshold voltage of the transistor 100a and a threshold voltage of the transistor 100b may be controlled by a common control voltage. In that 25 case, the number of signals can be reduced, whereby the number of wirings can be reduced.

[0095]

Further, another transistor having a different conductivity type from the transistor 100a may be provided on the SOI substrate. At this time, the transistor 30 having the different conductivity type from the transistor 100a can have the same structure as the transistor 100a except that a conductivity type of an impurity region is

different from that of the transistor 100a. Accordingly, the transistor having the different conductivity type can be formed while an increase in the number of manufacturing steps is suppressed.

[0096]

5 This is the example of the semiconductor device in this embodiment.

[0097]

In the example of the semiconductor device in this embodiment, a field-effect transistor provided on an SOI substrate and a field-effect transistor including an oxide semiconductor layer are used. The use of the transistors enables an improvement in 10 operation speed and a reduction in unnecessary current, thereby reducing power consumption.

[0098]

Further, in the example of the semiconductor device in this embodiment, a control terminal for controlling a threshold voltage of the field-effect transistor provided 15 on the SOI substrate is provided, and the threshold voltage of the field-effect transistor provided on the SOI substrate is controlled. As a result, it is possible to reduce the amount of current flowing between a source and a drain of the field-effect transistor which is provided on the SOI substrate and is in an off state, so that the power consumption of the semiconductor device can be reduced. Further, the threshold 20 voltages of n-channel transistors or p-channel transistors which are provided on the SOI substrate and have the above structure can be each controlled.

[0099]

Further, in the example of the semiconductor device in this embodiment, a conductive layer functioning as the control terminal can be formed in the same step as 25 the source and the drain of the field-effect transistor including an oxide semiconductor layer. As a result, an increase in the number of manufacturing steps can be suppressed.

[0100]

An example of a method for manufacturing the semiconductor device illustrated in FIGS. 1A to 1C is described as an example of a method for manufacturing 30 the semiconductor device in this embodiment with reference to FIGS. 2A1 to 2C2, FIGS. 3A1 to 3C2, FIGS. 4A1 to 4B2, FIGS. 5A1 to 5B2, and FIGS. 6A1 to 6B2. FIGS. 2A1 to FIGS. 6B2 are cross-sectional views illustrating an example of the

method for manufacturing the semiconductor device illustrated in FIGS. 1A to 1C.

[0101]

First, as illustrated in FIGS. 2A1 and 2A2, the semiconductor layer 101 is prepared, the insulating layer 102 is formed over one flat surface of the semiconductor layer 101, and then the semiconductor layer 103 is formed over one flat surface of the semiconductor layer 101 with the insulating layer 102 provided therebetween. Note that an oxide insulating layer or a nitride insulating layer may be formed over the semiconductor layer 101 in advance.

[0102]

10 Here, an example of the formation method of the SOI substrate including the semiconductor layer 101, the insulating layer 102, and the semiconductor layer 103 is described below.

[0103]

15 For example, a first semiconductor substrate is prepared as the semiconductor layer 101, and a second semiconductor substrate whose top surface is provided with the insulating layer 102 is prepared. Note that an impurity element imparting n-type or p-type conductivity may be added to the first semiconductor substrate in advance.

[0104]

20 For example, the oxide insulating layer can be formed by formation of an oxide insulating film by thermal oxidation, CVD, sputtering, or the like. For example, the oxide insulating layer can be formed by formation of an oxide silicon film over the second semiconductor substrate with thermal oxidation treatment in thermal oxidation.

[0105]

25 In addition, an ion beam including ions which are accelerated by an electric field enters the second semiconductor substrate and a fragile region is formed in a region at a certain depth from a surface of the second semiconductor substrate. Note that the depth at which the fragile region is formed is adjusted by the kinetic energy, mass, electrical charge, or incidence angle of the ions, or the like.

[0106]

30 For example, ions can be introduced into the second semiconductor substrate with the use of an ion doping apparatus or an ion implantation apparatus.

[0107]

As ions used for irradiation, for example, hydrogen and/or helium can be used. For example, in the case where irradiation is performed with hydrogen ions using an ion doping apparatus, the efficiency of irradiation of ions can be improved by increasing the proportion of  $H_3^+$  in the ions used for irradiation. Specifically, it is preferable that the 5 proportion of  $H_3^+$  is higher than or equal to 50 % (further preferably, higher than or equal to 80 %) with respect to the total amount of  $H^+$ ,  $H_2^+$ , and  $H_3^+$ .

[0108]

Further, the first semiconductor substrate and the second semiconductor substrate are attached to each other with the insulating layer which is provided on the 10 second semiconductor substrate provided therebetween. Note that in the case where the first semiconductor substrate is also provided with an insulating layer, the first semiconductor substrate and the second semiconductor substrate are attached to each other with the insulating layer on the second semiconductor substrate and the insulating layer on the first semiconductor substrate provided therebetween. In that case, the 15 insulating layers provided between the first semiconductor substrate and the second semiconductor substrate correspond to the insulating layer 102.

[0109]

Furthermore, heat treatment is performed so that the second semiconductor substrate is separated with the fragile region used as a cleavage plane. Thus, the 20 semiconductor layer 103 can be formed over the insulating layer 102.

[0110]

Note that when a surface of the semiconductor layer 103 is irradiated with laser light, the flatness of the surface of the semiconductor layer 103 can be improved.

[0111]

25 However, this embodiment is not limited thereto, and for example, a Smart Cut (registered trademark) method or a SIMOX method can be used to form the SOI substrate.

[0112]

Next, as illustrated in FIGS. 2B1 and 2B2, part of the semiconductor layer 103 30 is etched.

[0113]

For example, a resist mask is formed over part of a layer or a film by a photolithography step, and the part of the layer or the film can be etched using the resist mask so that a layer can be formed. Note that in this case, the resist mask is removed after the layer is formed.

5 [0114]

Alternatively, the resist mask may be formed using a light-exposure mask having a plurality of regions with different transmittances (also referred to as a multi-tone mask). With the multi-tone mask, a resist mask having regions with different thicknesses can be formed, so that the number of resist masks used for the 10 manufacturing of the semiconductor device can be reduced.

[0115]

Next, as illustrated in FIGS. 2C1 and 2C2, the insulating layer 104 is formed over one flat surface of the semiconductor layer 103.

[0116]

15 For example, the insulating layer 104 can be formed by forming a film using a material that can be used for the insulating layer 104 by a sputtering method, a plasma CVD method, or the like. Alternatively, the insulating layer 104 can be a stack of films formed using materials that can be used for the insulating layer 104.

[0117]

20 Note that after the semiconductor layer 103 is formed, an impurity element imparting n-type or p-type conductivity type may be added to the semiconductor layer 103. For example, after the insulating layer 104 is formed, the impurity element may be added to part of the semiconductor layer 103. The addition of the impurity element to the semiconductor layer 103 makes it possible to easily control a threshold voltage of 25 a transistor including the semiconductor layer 103.

[0118]

Next, as illustrated in FIGS. 3A1 and 3A2, a first conductive film is formed 30 over the semiconductor layer 103 with the insulating layer 104 provided therebetween, and part of the first conductive film is etched, so that the conductive layer 105 is formed.

[0119]

For example, the first conductive film can be formed by forming a film using a

material that can be used for the conductive layer 105 by a sputtering method. The first conductive film can be formed by stacking layers each formed using a material that can be used for the first conductive film.

[0120]

5 Next, as illustrated in FIGS. 3B1 and 3B2, an impurity element imparting one of p-type conductivity type and n-type conductivity type is added using the conductive layer 105 and a resist mask as masks, so that the region 103\_b1 and the region 103\_b2 are formed, whereas an impurity element imparting the other of the p-type conductivity type and the n-type conductivity type is added using another conductive layer formed  
10 using the first conductive film or a resist mask as a mask, so that the region 103\_c is formed. At this time, in part of the semiconductor layer 103 which overlaps with the conductive layer 105 with the insulating layer 104 provided therebetween, a region between the region 103\_b1 and the region 103\_b2 is the region 103\_a.

[0121]

15 Next, as illustrated in FIGS. 3C1 and 3C2, a third insulating film is formed over the insulating layer 104 and the conductive layer 105 to form the insulating layer 106.

[0122]

20 For example, the insulating layer 106 can be formed in such a manner that a silicon oxynitride film is formed over the insulating layer 104 and the conductive layer 105, a silicon nitride oxide film is formed over the silicon oxynitride film, and a silicon oxide film is formed over the silicon nitride oxide film.

[0123]

25 Then, as illustrated in FIGS. 4A1 and 4A2, an oxide semiconductor film is formed over the insulating layer 106 and part of the oxide semiconductor film is etched to form the semiconductor layer 107.

[0124]

Here, as an example of the semiconductor layer 107, for example, an oxide semiconductor layer that is CAAC is formed by a method described below.

30 [0125]

In the example of the method for forming the semiconductor layer 107, one or

both of a step of performing heat treatment once or plural times and a step of removing part of a semiconductor film may be included. At this time, the timing of the step of removing the part of the semiconductor film is not particularly limited thereto as long as it is performed after the formation of the semiconductor film before the formation of the 5 conductive layer 110. Further, the timing of the step of performing heat treatment is not limited thereto as long as it is performed after the formation of the semiconductor film.

[0126]

For example, the semiconductor film is formed by forming a film using a 10 material that can be used for the semiconductor layer 107 by a sputtering method. At this time, the temperature of an element formation layer where the semiconductor film is formed is set higher than or equal to 100 °C and lower than or equal to 500 °C, preferably higher than or equal to 200 °C and lower than or equal to 350 °C. When the temperature of the element formation layer where the semiconductor film is formed is 15 high, the semiconductor film can have atoms arranged in a triangular, hexagonal, equilateral triangular, or regular hexagonal shape when seen from a direction perpendicular to an a-b plane, and have a phase in which metal atoms are arranged in a layered manner when seen from the direction perpendicular to the c-axis direction or a phase in which metal atoms and oxygen atoms are arranged in a layered manner when 20 seen from the direction perpendicular to the c-axis direction.

[0127]

As the step of performing heat treatment, heat treatment (also referred to as 25 heat treatment A) is performed at a temperature, for example, higher than or equal to 400 °C and lower than or equal to 750 °C or higher than or equal to 400 °C and lower than the strain point of the substrate. Note that the timing of the heat treatment A is not limited thereto as long as it is performed after the formation of the semiconductor film.

[0128]

The heat treatment A can increase crystallinity in the semiconductor layer 107.

30 [0129]

A heat treatment apparatus for the heat treatment A may be an electric furnace

or an apparatus for heating an object by heat conduction or heat radiation from a heating element such as a resistance heating element. For example, a rapid thermal anneal (RTA) apparatus such as a gas rapid thermal anneal (GRTA) apparatus or a lamp rapid thermal anneal (LRTA) apparatus can be used. An LRTA apparatus is an apparatus for heating a process object by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high-pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high-temperature gas. As the high-temperature gas, a rare gas or an inert gas (e.g., nitrogen) which does not react with the object by the heat treatment can be used.

[0130]

After the heat treatment A, a high-purity oxygen gas, a high-purity N<sub>2</sub>O gas, or ultra-dry air (with a dew point of lower than or equal to -40 °C, preferably lower than or equal to -60 °C) may be introduced into the furnace that has been used in the above heat treatment A. It is preferable that the oxygen gas or the N<sub>2</sub>O gas do not contain water, hydrogen, and the like. The purity of the oxygen gas or the N<sub>2</sub>O gas which is introduced into the heat treatment apparatus is preferably equal to or more than 6N, more preferably equal to or more than 7N (i.e., the impurity concentration of the oxygen gas or the N<sub>2</sub>O gas is preferably equal to or lower than 1 ppm, more preferably equal to or lower than 0.1 ppm). By the action of the oxygen gas or the N<sub>2</sub>O gas, oxygen is supplied to the semiconductor film or the semiconductor layer 107, so that defects caused by oxygen deficiency in the semiconductor film or the semiconductor layer 107 can be reduced.

[0131]

Next, as illustrated in FIGS. 4B1 and 4B2, for example, part of the insulating layer 104 and part of the insulating layer 106 are etched to form openings 111a to 111c which penetrate the insulating layer 104 and the insulating layer 106.

[0132]

Next, as illustrated in FIGS. 5A1 and 5A2, a second conductive film is formed over the insulating layer 106 and the semiconductor layer 107, and part of the second conductive film is etched, so that the conductive layers 108a to 108e are formed.

[0133]

For example, the second conductive film can be formed by forming a film using a material that can be used for the conductive layers 108a to 108e by a sputtering method. The second conductive film can be formed by stacking layers formed using materials that can be used for the second conductive film.

5

[0134]

Next, as illustrated in FIGS. 5B1 and 5B2, a fourth insulating film is formed over the insulating layer 106, the semiconductor layer 107, and the conductive layers 108a to 108e to be in contact with the semiconductor layer 107, so that the insulating 10 layer 109 is formed.

10

[0135]

For example, the fourth insulating film can be formed by forming a film using a material which can be used for the insulating layer 109 by a sputtering method, a plasma CVD method, or the like. The fourth insulating film can also be formed by 15 stacking films using materials that can be used for the fourth insulating film. Moreover, when a film using a material which can be used for the insulating layer 109 is formed by a high-density plasma CVD method (e.g., a high-density plasma CVD method using microwaves such as a microwave at a frequency of 2.45 GHz), the insulating layer 109 can be dense and the withstand voltage of the insulating layer 109 20 can be improved.

20

[0136]

Next, as illustrated in FIGS. 6A1 and 6A2, a third conductive film is formed over the insulating layer 109, and part of the third conductive film is etched to form the conductive layer 110.

25 [0137]

For example, the third conductive film can be formed by forming a film using a material that can be used for the conductive layer 110 by a sputtering method. The third conductive film can be formed by stacking layers formed of materials that can be used for the third conductive film.

30 [0138]

When a high-purity gas from which impurities such as hydrogen, water, a hydroxyl group, or a hydride are removed is used as a sputtering gas, the impurity

concentration of a film to be formed can be reduced.

[0139]

5 Note that before the film is formed by a sputtering method, heat treatment (also referred to as heat treatment B) may be performed in a preheating chamber of a sputtering apparatus. By the heat treatment B, impurities such as hydrogen or moisture can be eliminated.

[0140]

10 Moreover, before the film is formed by a sputtering method, it is possible to perform the following treatment (called reverse sputtering): instead of applying a voltage to the target side, an RF power source is used for applying a voltage to the substrate side in an argon, nitrogen, helium, or oxygen atmosphere so that plasma is generated to modify a surface where the film is to be formed. With reverse sputtering, powdery substances (also referred to as particles or dust) attached to the surface where the film is to be formed can be removed.

15 [0141]

20 In the case where the film is formed by a sputtering method, moisture remaining in a deposition chamber used for forming the film can be removed with an entrapment vacuum pump or the like. As the entrapment vacuum pump, a cryopump, an ion pump, or a titanium sublimation pump can be used, for example. Moreover, moisture remaining in the deposition chamber can be removed with a turbo pump provided with a cold trap.

[0142]

25 Further, after the insulating layer 109 is formed, heat treatment (also referred to as heat treatment C) may be performed in an inert gas atmosphere or an oxygen gas atmosphere. At this time, the heat treatment C can be performed at a temperature higher than or equal to 200 °C and lower than or equal to 400 °C, preferably higher than or equal to 250 °C and lower than or equal to 350 °C.

[0143]

30 Next, as illustrated in FIGS. 6B1 and 6B2, a dopant is added to the semiconductor layer 107 from a side on which the conductive layer 110 is formed through the insulating layer 109, whereby the region 107\_b1 and the region 107\_b2 are

formed in a self-aligned manner. Accordingly, as compared to the case where a dopant is directly added to the semiconductor layer, over etching of the semiconductor layer 107 can be prevented, excessive damage to the semiconductor layer 107 can be reduced, and an interface between the semiconductor layer 107 and the insulating layer 109 can 5 be kept clean. As a result, the characteristics and reliability of the transistor can be increased. At this time, a region between the region 107\_b1 and the region 107\_b2 is the region 107\_a.

[0144]

For example, the dopant can be added with the use of an ion doping apparatus 10 or an ion implantation apparatus.

[0145]

Note that after the dopant is added to the semiconductor layer 107, heat treatment may be performed.

[0146]

15 This is the example of the method for manufacturing the transistor illustrated in FIGS. 1A to 1C.

[0147]

20 In the example of the method for manufacturing the semiconductor device in this embodiment, when part of one conductive film is etched, a conductive layer functioning as the control terminal can be formed in the same step as conductive layers functioning as a source and a drain of a second field-effect transistor. As a result, an increase in the number of manufacturing steps can be suppressed.

[0148]

(Embodiment 2)

25 In this embodiment, a semiconductor device having a different structure from that of Embodiment 1 will be described. Note that the description of the semiconductor device circuit in Embodiment 1 can be referred to as appropriate for the same portions as those in the semiconductor device described in Embodiment 1.

[0149]

30 A structure example of the semiconductor device in this embodiment is described with reference to FIGS. 7A to 7C. FIG. 7A is a schematic top view, FIG. 7B

is a schematic cross-sectional view taken along line A2-B2 of FIG. 7A, and FIG. 7C is a schematic cross-sectional view taken along line C2-D2 of FIG. 7A.

[0150]

The semiconductor device illustrated in FIGS. 7A to 7C includes a 5 semiconductor layer 201, an insulating layer 202, semiconductor layers 203a and 203b, an insulating layer 204, conductive layers 205a and 205b, an insulating layer 206, a semiconductor layer 207, conductive layers 208a to 208h, an insulating layer 209, and a conductive layer 210. A transistor 200a, a transistor 200b, and a transistor 200c are formed using the above structure.

10 [0151]

The transistor 200a is formed using a signal crystal semiconductor layer of silicon or the like, for example. The transistor 200a is used as a transistor of a logic circuit in the semiconductor device, for example.

[0152]

15 The transistor 200b is formed using a signal crystal semiconductor layer of silicon or the like, for example, and has a different conductivity type from the transistor 200a. The transistor 200b is used as a transistor of a logic circuit in the semiconductor device, for example.

[0153]

20 However, this embodiment is not limited thereto, and the transistor 200a or the transistor 200b may be omitted.

[0154]

25 The transistor 200c is a transistor including an oxide semiconductor layer whose off-state current is lower than that of a conventional transistor including a semiconductor layer of silicon or the like. As the transistor 200c, a transistor which can be used for the transistor 100b can be used. Data is input to a portion where a source or a drain of the transistor 200c is electrically connected to another circuit or element, and then the transistor 200c is turned off, whereby the data can be retained for a long time. However, this embodiment is not limited thereto, and the transistor 200c 30 can also be used for a logic circuit or the like.

[0155]

The semiconductor layer 201 corresponds to a first semiconductor region of an

SOI substrate. The semiconductor layer 201 includes a region 201\_a to which an impurity element imparting one of n-type conductivity type and p-type conductivity type is added and a region 201\_b to which an impurity element imparting a conductivity type opposite to that of the region 201\_a is added. For example, before the 5 semiconductor layer 201 is attached to the semiconductor layer including the semiconductor layer 203a and the semiconductor layer 203b, an impurity element imparting n-type conductivity type or an impurity element imparting p-type conductivity type is selectively added to part of the semiconductor layer 201, whereby the region 201\_a and the region 201\_b can be formed.

10 [0156]

For the semiconductor layer 201, a material which can be used for the semiconductor layer 101 in FIGS. 1A to 1C can be used, for example.

[0157]

The insulating layer 202 is provided over the semiconductor layer 201

15 [0158]

The insulating layer 202 corresponds to an insulating region in the SOI substrate. The insulating layer 202 can be formed using a layer of a material which can be used for the insulating layer 102 in FIGS. 1A to 1C, for example, and can be formed by a manufacturing method similar to that of the insulating layer 102.

20 [0159]

The semiconductor layer 203a overlaps with the region 201\_a with the insulating layer 202 provided therebetween, and the semiconductor layer 203b overlaps with the region 201\_b with the insulating layer 202 provided therebetween.

[0160]

25 The semiconductor layer 203a includes a region 203a\_a, a region 203a\_b1, and a region 203a\_b2. Further, the semiconductor layer 203b includes a region 203b\_a, a region 203b\_b1, and a region 203b\_b2.

[0161]

30 The region 203a\_a is a region between the region 203a\_b1 and the region 203a\_b2, and the region 203b\_a is a region between the region 203b\_b1 and the region 203b\_b2. The region 203a\_a and the region 203b\_a are channel formation regions.

[0162]

The region 203a\_b1 and the region 203a\_b2 are apart from each other, and the region 203b\_b1 and the region 203b\_b2 are apart from each other. The region 203a\_b1 is a region serving as one of a source region and a drain region of the transistor 200a, and the region 203a\_b2 is a region serving as the other of the source region and the drain region of the transistor 200a. The region 203b\_b1 is a region serving as one of a source region and a drain region of the transistor 200b, and the region 203b\_b2 is a region serving as the other of the source region and the drain region of the transistor 200b. The region 203a\_b1 and the region 203a\_b2 include an impurity element imparting n-type or p-type conductivity type. The region 203b\_b1 and the region 203b\_b2 include an impurity element imparting a conductivity type opposite to that of the region 203a\_b1 and the region 203a\_b2.

[0163]

The semiconductor layer 203a and the semiconductor layer 203b each correspond to at least part of a second semiconductor region in the SOI substrate. Note that the transistor 200a can be formed using a semiconductor region surrounded by an insulating region instead of the semiconductor layer 203a, and the transistor 200b can be formed using another semiconductor region surrounded by an insulating region instead of the semiconductor layer 203b.

[0164]

The semiconductor layer 203a and the semiconductor layer 203b can be formed using a layer of a material which can be used for the semiconductor layer 103 in FIGS. 1A to 1C, for example, and can be formed using one semiconductor film by a manufacturing method similar to that of the semiconductor layer 103.

[0165]

The insulating layer 204 is provided over one flat surface of the semiconductor layer 203a and one flat surface of the semiconductor layer 203b.

[0166]

The insulating layer 204 can be formed using a layer of a material which can be used for the insulating layer 104 in FIGS. 1A to 1C, for example, and can be formed by a manufacturing method similar to that of the insulating layer 104.

[0167]

The insulating layer 204 functions as a gate insulating layer in the transistor 200a and a gate insulating layer in the transistor 200b.

[0168]

5 The conductive layer 205a overlaps with part of the semiconductor layer 203a (the region 203a\_a) with the insulating layer 204 provided therebetween, and the conductive layer 205b overlaps with part of the semiconductor layer 203b (the region 203b\_a) with the insulating layer 204 provided therebetween.

[0169]

10 The conductive layer 205a and the conductive layer 205b can be formed using a layer of a material which can be used for the conductive layer 105 in FIGS. 1A to 1C, for example, and can be formed using one conductive film by a manufacturing method similar to that of the conductive layer 105.

[0170]

15 The conductive layer 205a functions as a gate of the transistor 200a, and the conductive layer 205b functions as a gate of the transistor 200b.

[0171]

The insulating layer 206 is provided over the insulating layer 204, the conductive layer 205a, and the conductive layer 205b.

20 [0172]

The insulating layer 206 can be formed using a layer of a material which can be used for the insulating layer 106 in FIGS. 1A to 1C, for example, and can be formed by a manufacturing method similar to that of the insulating layer 106.

[0173]

25 The insulating layer 206 functions as a planarization insulating layer.

[0174]

The semiconductor layer 207 is provided over one flat surface of the insulating layer 206.

[0175]

30 The semiconductor layer 207 includes a region 207\_a. Further, a region 207\_b1 and a region 207\_b2 are provided in the semiconductor layer 207 as illustrated

in FIGS. 7A and 7B but are not necessarily provided.

[0176]

The region 207\_a is a region between the region 207\_b1 and the region 207\_b2. The region 207\_a is a channel formation region of the transistor 200c.

5 [0177]

The region 207\_b1 and the region 207\_b2 are apart from each other and include elements serving as dopants

[0178]

10 The semiconductor layer 207 can be formed using a layer of a material which can be used for the semiconductor layer 107 in FIGS. 1A to 1C, for example, and can be formed by a manufacturing method similar to that of semiconductor layer 107.

[0179]

The conductive layer 208a is electrically connected to the region 203a\_b1 via a first opening which penetrates the insulating layer 204 and the insulating layer 206.

15 [0180]

The conductive layer 208a functions as one of a source and a drain of the transistor 200a.

[0181]

20 The conductive layer 208b is electrically connected to the region 203a\_b2 via a second opening which penetrates the insulating layer 204 and the insulating layer 206.

[0182]

The conductive layer 208b functions as the other of the source and the drain of the transistor 200a.

[0183]

25 The conductive layer 208c is electrically connected to the region 201\_a via a third opening which penetrates the insulating layer 202, the insulating layer 204, and the insulating layer 206.

[0184]

30 The conductive layer 208c functions as a control terminal for controlling a voltage applied to the region 201\_a.

[0185]

The conductive layer 208d is electrically connected to the region 203b\_b1 via a fourth opening which penetrates the insulating layer 204 and the insulating layer 206.

[0186]

5 The conductive layer 208d functions as one of a source and a drain of the transistor 200b.

[0187]

The conductive layer 208e is electrically connected to the region 203b\_b2 via a fifth opening which penetrates the insulating layer 204 and the insulating layer 206.

[0188]

10 The conductive layer 208e functions as the other of the source and the drain of the transistor 200b.

[0189]

15 The conductive layer 208f is electrically connected to the region 201\_b via a sixth opening which penetrates the insulating layer 202, the insulating layer 204, and the insulating layer 206.

[0190]

The conductive layer 208f functions as a control terminal for controlling a voltage applied to the region 201\_b.

[0191]

20 The conductive layer 208g is electrically connected to the semiconductor layer 207.

[0192]

The conductive layer 208g functions as one of a source and a drain of the transistor 200c.

25 [0193]

The conductive layer 208h is electrically connected to the semiconductor layer 207.

[0194]

30 The conductive layer 208h functions as the other of the source and the drain of the transistor 200c.

[0195]

Note that although the conductive layer 208g and the conductive layer 208h are provided over the semiconductor layer 207 as illustrated in FIGS. 7A and 7B, this embodiment is not limited thereto, and the semiconductor layer 207 may be provided over the conductive layer 208g and the conductive layer 208h.

5 [0196]

The conductive layer 208c and the conductive layer 208f are formed in the same step as the conductive layer 208g and the conductive layer 208h. In addition, the conductive layer 208a and conductive layer 208b, and the conductive layer 208d and the conductive layer 208e may be formed in the same step as the conductive layer 208c, the 10 conductive layer 208f, the conductive layer 208g, and the conductive layer 208h. As the conductive layers 208a to 208h, a layer of a material which can be used for the conductive layers 108a to 108e in FIGS. 1A to 1C can be used. The conductive layers 208a to 208h can be used using one conductive film in the same manner as that of the conductive layers 108a to 108e.

15 [0197]

The insulating layer 209 is provided over the insulating layer 206, the semiconductor layer 207, and the conductive layers 208a to 208h.

[0198]

The insulating layer 209 can be formed using a layer of a material which can be 20 used for the insulating layer 109 in FIGS. 1A to 1C, for example, and can be formed by a manufacturing method similar to that of the insulating layer 109.

[0199]

The conductive layer 210 overlaps with the semiconductor layer 207 with the insulating layer 209 provided therebetween.

25 [0200]

The conductive layer 210 can be formed using a layer of a material which can be used for the conductive layer 110 in FIGS. 1A to 1C, for example, and can be formed by a manufacturing method similar to that of the conductive layer 110.

[0201]

30 In the semiconductor device illustrated in FIGS. 7A to 7C, when a first control voltage is applied via the conductive layer 208c, a voltage of the region 201\_a can be controlled to be a level in accordance with the first control voltage, and the voltage

applied to the semiconductor layer 203a can be controlled. In addition, when a second control voltage is applied via the conductive layer 208f, a voltage of the region 201\_b can be controlled to be a level in accordance with the second control voltage, and the voltage applied to the semiconductor layer 203b can be controlled. For example, in  
5 the case where the transistor 200a is a p-channel transistor, when the level of the first control voltage is set high, a threshold of the transistor 200a is negatively shifted. In the case where the transistor 200b is an n-channel transistor, when the level of the second control voltage is set low, a threshold voltage of the transistor 200b is positively shifted. Thus, even in the case where the threshold voltages of the transistor 200a and  
10 the transistor 200b vary owing to the semiconductor layer 201, when the voltages of the region 203a\_a and the region 203b\_a are controlled and the threshold voltages of the transistor 200a and the transistor 200b are controlled, whereby the amount of current flowing between the source and the drain of each of the transistor 200a and the transistor 200b which are in an off state can be reduced. For example, the threshold  
15 voltages of the transistor 200a and the transistor 200b are preferably levels at which the transistor 200a and the transistor 200b become enhancement type transistors.

[0202]

This is the example of the semiconductor device in this embodiment.

[0203]

20 In the example of the semiconductor device in this embodiment, a field-effect transistor provided on an SOI substrate and a field-effect transistor including an oxide semiconductor layer are used. The use of the transistors enables an improvement in operation speed and a reduction in unnecessary current, thereby reducing power consumption.

25 [0204]

Further, in the example of the semiconductor device in this embodiment, a control terminal for controlling a threshold voltage of the field-effect transistor provided on the SOI substrate is provided, and the threshold voltage of the field-effect transistor provided on the SOI substrate is controlled. As a result, it is possible to reduce the  
30 amount of current flowing between a source and a drain of the field-effect transistor which is provided on the SOI substrate and is in an off state, so that the power

consumption of the semiconductor device can be reduced. Further, the threshold voltages of n-channel transistors or p-channel transistors which are provided on the SOI substrate and have the above structure can be each controlled.

[0205]

5 Further, in the example of the semiconductor device in this embodiment, a conductive layer functioning as the control terminal can be formed in the same step as the source and the drain of the field-effect transistor including an oxide semiconductor layer. As a result, an increase in the number of manufacturing steps can be suppressed.

[0206]

10 (Embodiment 3)

In this embodiment, a semiconductor device having a different structure from those of Embodiment 1 and Embodiment 2 will be described. Note that the descriptions of the semiconductor devices in Embodiment 1 and Embodiment 2 can be referred to as appropriate for the same portions as those in the semiconductor devices 15 described in Embodiment 1 and Embodiment 2.

[0207]

A structure example of the semiconductor device in this embodiment is described with reference to FIGS. 8A to 8D. FIG. 8A is a schematic top view, FIG. 8B is a schematic cross-sectional view taken along line A3-B3 of FIG. 8A, FIG. 8C is a 20 schematic cross-sectional view taken along line C3-D3 of FIG. 8A, and FIG. 8D is a schematic cross-sectional view taken along line E3-F3 of FIG. 8A.

[0208]

The semiconductor device illustrated in FIGS. 8A to 8D includes a semiconductor layer 301, an insulating layer 302, a semiconductor layer 303, an 25 insulating layer 304, a conductive layer 305, an insulating layer 306, a semiconductor layer 307, conductive layers 308a to 308d, an insulating layer 309, a conductive layer 310a, and a conductive layer 310b. A transistor 300a and a transistor 300b are formed using the above structure.

[0209]

30 The transistor 300a is formed using a signal crystal semiconductor layer of silicon or the like, for example. For example, the transistor 300a is used as a transistor in any of various logic circuits. The transistor 300a can be used as an output transistor

in a memory circuit, for example.

[0210]

However, this embodiment is not limited thereto, and as illustrated in FIG. 7A to 7C, a transistor including a single crystal semiconductor layer may be provided in addition to the transistor 300a.

[0211]

The transistor 300b is a transistor including an oxide semiconductor layer whose off-state current is lower than that of a conventional transistor including a semiconductor layer of silicon or the like. As the transistor 300b, a transistor which can be used for the transistor 100b can be used. At this time, the transistor 300b and the transistor 300a have the same conductivity type. The transistor 300b can be used as a transistor of a memory circuit, for example. Data is input to a portion where a source or a drain of the transistor 300b is electrically connected to another circuit or element, and then the transistor 300b is turned off, whereby the data can be retained for a long time. However, this embodiment is not limited thereto, and the transistor 300b can also be used for a logic circuit or the like.

[0212]

The semiconductor layer 301 corresponds to a first semiconductor region in an SOI substrate. Note that in FIGS. 8A to 8D, the semiconductor layer 301 includes a region 301\_a to which an impurity element imparting n-type or p-type conductivity type is added. For example, the impurity element is added to part of the semiconductor layer 301 before the semiconductor layer 301 and a semiconductor layer including the semiconductor layer 303 are attached to each other, whereby the region 301\_a can be formed. Note that in the case where transistors including single crystal semiconductor layers having polarities different from each other, a plurality of impurity regions to which impurity elements having conductivity types different from each other are added may be provided. Note that it is possible to omit the region 301\_a.

[0213]

For the semiconductor layer 301, a material which can be used for the semiconductor layer 101 in FIGS. 1A to 1C can be used, for example.

[0214]

The insulating layer 302 is provided over the semiconductor layer 301  
[0215]

The insulating layer 302 corresponds to an insulating region in the SOI substrate. The insulating layer 302 can be formed using a layer of a material which 5 can be used for the insulating layer 102 in FIGS. 1A to 1C, for example, and can be formed by a manufacturing method similar to that of the insulating layer 102.

[0216]

The semiconductor layer 303 overlaps with the region 301\_a with the insulating layer 302 provided therebetween.

10 [0217]

The semiconductor layer 303 includes a region 303\_a, a region 303\_b1, a region 303\_b2, and a region 303\_c.

[0218]

The region 303\_a is a region between the region 303\_b1 and the region 303\_b2.  
15 The region 303\_a is a channel formation region.

[0219]

The region 303\_b1 and the region 303\_b2 are apart from each other. The region 303\_b1 is a region serving as one of a source region and a drain region of the transistor 300a, and the region 303\_b2 is a region serving as the other of the source 20 region and the drain region of the transistor 300a. The region 303\_b1 and the region 303\_b2 include an impurity element imparting n-type or p-type conductivity type.

[0220]

Further, the region 303\_c is in contact with the region 303\_a where the channel is formed and includes an impurity element imparting a conductivity type opposite to 25 that of the region 303\_b1 and the region 303\_b2. At this time, the region 303\_c has a conductivity type opposite to that of the region 303\_b1 and the region 303\_b2. A voltage is applied to the region 303\_a via the region 303\_c. Further, the concentration of the impurity element added to the region 303\_c is set higher than the concentration of 30 the impurity element added to the region 303\_a, whereby contact resistance with the region 303\_a can be reduced.

[0221]

The semiconductor layer 303 is at least part of a second semiconductor region in the SOI substrate. Note that the transistor 300a can also be formed in such a manner that a semiconductor region surrounded by an insulating region is used instead of the semiconductor layer 303.

5

[0222]

The semiconductor layer 303 can be formed using a layer of a material which can be used for the semiconductor layer 103 in FIGS. 1A to 1C, for example, and can be formed using one semiconductor film by a manufacturing method similar to that of the 10 semiconductor layer 103.

10

[0223]

The insulating layer 304 is provided over one flat surface of the semiconductor layer 303.

[0224]

15 The insulating layer 304 can be formed using a layer of a material which can be used for the insulating layer 104 in FIGS. 1A to 1C, for example, and can be formed by a manufacturing method similar to that of the insulating layer 104.

[0225]

20 The insulating layer 304 functions as a gate insulating layer in the transistor 300a.

[0226]

The conductive layer 305 overlaps with part of the semiconductor layer 303 (the region 303\_a) with the insulating layer 304 provided therebetween.

[0227]

25 The conductive layer 305 can be formed using a layer of a material which can be used for the conductive layer 105 in FIGS. 1A to 1C, for example, and can be formed using one conductive film by a manufacturing method similar to that of the conductive layer 105, for example.

[0228]

30 The conductive layer 305 functions as a gate in the transistor 300a.

[0229]

The insulating layer 306 is provided over the insulating layer 304 and the

conductive layer 305.

[0230]

The insulating layer 306 can be formed using a layer of a material which can be used for the insulating layer 106 in FIGS. 1A to 1C, for example, and can be formed by a manufacturing method similar to that of the insulating layer 106.

[0231]

The insulating layer 306 functions as a planarization insulating layer.

[0232]

The semiconductor layer 307 is provided over one flat surface of the insulating layer 306.

[0233]

The semiconductor layer 307 includes a region 307\_a. Further, a region 307\_b1 and a region 307\_b2 are provided in the semiconductor layer 307 as illustrated in FIGS. 8A and 8B but are not necessarily provided.

[0234]

The region 307\_a is a region between the region 307\_b1 and the region 307\_b2. The region 307\_a overlaps with the region 303\_c with the insulating layer 304 and the insulating layer 306 provided therebetween. The region 307\_a is a channel formation region of the transistor 300b.

[0235]

The region 307\_b1 and the region 307\_b2 are apart from each other and include elements serving as dopants.

[0236]

The semiconductor layer 307 can be formed using a layer of a material which can be used for the semiconductor layer 107 in FIGS. 1A to 1C, for example, and can be formed by a manufacturing method similar to that of the semiconductor layer 107.

[0237]

The conductive layer 308a is in contact with the conductive layer 305 and electrically connected to the semiconductor layer 307. The structure in which the conductive layer 308a is in contact with the conductive layer 305 can be formed in such a manner that, for example, after the insulating layer 306 is formed, a surface of the

conductive layer 305 is exposed by chemical polishing treatment or the like, and then the conductive layer 308a is formed.

[0238]

Note that although the conductive layer 308a is in contact with the conductive layer 305 in FIGS. 8A to 8D, this embodiment is not limited thereto. The structure in which the conductive layer 308a is in contact with the conductive layer 305 makes it possible to increase a contact area as compared to that in the case where the conductive layer 308a is electrically connected to the conductive layer 305 via an opening of an insulating layer. As a result, contact resistance can be reduced.

10 [0239]

The conductive layer 308a functions as one of the source and the drain of the transistor 300b.

[0240]

15 The conductive layer 308b is electrically connected to the semiconductor layer 307.

[0241]

The conductive layer 308b functions as the other of the source and the drain of the transistor 300b.

[0242]

20 Note that although the conductive layer 308a and the conductive layer 308b are provided over the semiconductor layer 307 in FIGS. 8A to 8D, this embodiment is not limited thereto, and the semiconductor layer 307 may be provided over the conductive layer 308a and the conductive layer 308b.

[0243]

25 The conductive layer 308c is electrically connected to the region 301\_a via a first opening which penetrates the insulating layer 302, the insulating layer 304, and the insulating layer 306.

[0244]

30 The conductive layer 308c functions as a control terminal for controlling a voltage applied to the region 301\_a.

[0245]

The conductive layer 308d is electrically connected to the region 303\_c via a second opening which penetrates the insulating layer 304 and the insulating layer 306.

[0246]

The conductive layer 308d functions as a second control terminal for 5 controlling a voltage applied to the region 303\_c.

[0247]

The conductive layer 308c and the conductive layer 308d are formed in the same step as the conductive layer 308a and the conductive layer 308b. As the conductive layers 308a to 308d, a layer of a material which can be used for the 10 conductive layers 108a to 108e in FIGS. 1A to 1C can be used. The conductive layers 308a to 308h can be used using one conductive film in the same manner as that of the conductive layers 108a to 108e.

[0248]

When the region 301\_a is not provided, it is possible to omit the conductive 15 layer 308c.

[0249]

The insulating layer 309 is provided over the insulating layer 306, the semiconductor layer 307, and the conductive layers 308a to 308d.

[0250]

20 The insulating layer 309 can be formed using a layer of a material which can be used for the insulating layer 109 in FIGS. 1A to 1C, for example, and can be formed by a manufacturing method similar to that of the insulating layer 109.

[0251]

25 The conductive layer 310a overlaps with the conductive layer 308a with the insulating layer 309 provided therebetween. The conductive layer 310a functions as a capacitor electrode of a capacitor.

[0252]

30 Note that the capacitor can be formed with the conductive layer 308a, the insulating layer 309, and the conductive layer 310a. However, the capacitor is not necessarily provided.

[0253]

The conductive layer 310b overlaps with the region 307\_a with the insulating layer 309 provided therebetween. The conductive layer 310b functions as a gate of the transistor 300b.

[0254]

5 The conductive layer 310a and the conductive layer 310b can be formed using a layer of a material which can be used for the conductive layer 110 in FIGS. 1A to 1C, for example, and can be formed by a manufacturing method similar to that of the conductive layer 110.

[0255]

10 In the semiconductor device illustrated in FIGS. 8A to 8D, when a first control voltage is applied via the conductive layer 308c that is a first control terminal, a voltage of the region 301\_a electrically connected to the conductive layer 308c can be controlled to be a level in accordance with the first control voltage. In addition, when a second control voltage is applied via the conductive layer 308d, a voltage of the region 15 303\_a can be controlled to be a level in accordance with the second control voltage. At this time, the first control voltage and the second control voltage preferably have the same levels. In addition, when the second control voltage is applied via the conductive layer 308d, a voltage of the semiconductor layer 307 can also be controlled, and both of the voltage applied to the region 303\_a and the voltage of the semiconductor layer 307 20 can be controlled. For example, in the case where the transistor 300a and the transistor 300b are n-channel transistors, when the levels of the first control voltage and the second control voltage are lowered, the threshold voltages of the transistor 300a and the transistor 300b are positively shifted. Accordingly, even in the case where the threshold voltages of the transistor 300a and the transistor 300b are varied, the voltages 25 applied to the region 303\_a and the region 307\_a are controlled and the threshold voltages of the transistor 300a and the transistor 300b are controlled, whereby the amount of current flowing between a source and a drain of each of the transistor 300a and the transistor 300b which are in an off state can be reduced. The threshold voltages of the transistor 300a and the transistor 300b are preferably levels at which the 30 transistor 300a and the transistor 300b become enhancement type transistors.

[0256]

Further, another transistor having a different conductivity type from the transistor 300a may be provided on the SOI substrate in a similar manner to FIGS. 7A to 7C. At this time, the transistor having the different conductivity type from the transistor 300a can have the same structure as the transistor 300a except that a conductivity type of an impurity region is different from that of the transistor 300a. Accordingly, the transistor having the different conductivity type can be formed while an increase in the number of manufacturing steps is suppressed.

5 [0257]

This is the example of the semiconductor device in this embodiment.

10 [0258]

In the example of the semiconductor device in this embodiment, a field-effect transistor provided on an SOI substrate and a field-effect transistor including an oxide semiconductor layer are used. The use of the transistors enables an improvement in operation speed and a reduction in unnecessary current, thereby reducing power consumption.

15 [0259]

Further, in the example of the semiconductor device in this embodiment, a control terminal for controlling a threshold voltage of the field-effect transistor provided on the SOI substrate is provided, and the threshold voltage of the field-effect transistor provided on the SOI substrate is controlled. As a result, it is possible to reduce the amount of current flowing between a source and a drain of the field-effect transistor which is provided on the SOI substrate and is in an off state, so that the power consumption of the semiconductor device can be reduced. Further, the threshold voltages of n-channel transistors or p-channel transistors which are provided on the SOI substrate and have the above structure can be each controlled.

20 [0260]

In addition, in the example of the semiconductor device in this embodiment, the impurity region formed in the SOI substrate functions as the gate of the field-effect transistor including the oxide semiconductor layer. Consequently, since the threshold voltages of the first field-effect transistor and the second field-effect transistor can be controlled by a common control voltage, the number of wirings can be reduced and the area of a circuit of the semiconductor device can be reduced.

[0261]

Further, in the example of the semiconductor device in this embodiment, a conductive layer functioning as the control terminal can be formed in the same step as the source and the drain of the second field-effect transistor including an oxide semiconductor layer. As a result, an increase in the number of manufacturing steps 5 can be suppressed.

[0262]

(Embodiment 4)

In this embodiment, an example of an arithmetic processing unit will be 10 described as one example of a semiconductor device.

[0263]

An example of the structure of the arithmetic processing unit in this embodiment is described with reference to FIG. 9. FIG. 9 illustrates the example of the structure of the arithmetic processing unit in this embodiment.

15 [0264]

The arithmetic processing unit illustrated in FIG. 9 includes a bus interface (also referred to as an IF) 501, a control unit (also referred to as a CTL) 502, a cache memory (also referred to as a CACH) 503,  $N$  ( $N$  is a natural number greater than or equal to 3) registers (also referred to as REGs) 504 (registers 504\_1 to 504\_N), an 20 instruction decoder (also referred to as an IDCD) 505, and an arithmetic logic unit (also referred to as an ALU) 506.

[0265]

The bus interface 501 has a function of exchanging signals with the external of 25 the arithmetic processing unit and a function of exchanging signals with circuits in the arithmetic processing unit, and the like.

[0266]

The control unit 502 has a function of controlling operations of the circuits in the arithmetic processing unit.

[0267]

30 The cache memory 503 is controlled by the control unit 502 and has a function of temporary retaining data during the operation of the arithmetic processing unit. Note that the arithmetic processing unit may include a plurality of cache memories 503.

[0268]

The  $N$  registers 504 are controlled by the control unit 502 and each have a function of storing data used for arithmetic processing. For example, one register 504 may be used as a register for the arithmetic logic unit 506 and another register 504 may be used as a register for the instruction decoder 505.

5

[0269]

For example, the  $N$  registers 504 can be formed by using a plurality of unit memory devices each of which is provided with the field-effect transistor provided on the SOI substrate and the field-effect transistor including the oxide semiconductor layer in the semiconductor device described in the above embodiment.

10

[0270]

The instruction decoder 505 has a function of translating an instruction signal which is read. The translated instruction signal is input to the control unit 502, and the control unit 502 outputs a control signal in accordance with the instruction signal to the arithmetic logic unit 506.

15

[0271]

The arithmetic logic unit 506 is controlled by the control unit 502 and has a function of performing arithmetic processing in accordance with the input instruction signal.

20

[0272]

Two unit memory devices are described with reference to FIGS. 10A and 10B and FIGS. 11A to 11C as examples of the unit memory device.

[0273]

25

First, the structure of one unit memory device is described with reference to FIG. 10A.

[0274]

30

The unit memory device illustrated in FIG. 10A includes an analog switch 611, a NOT gate (also referred to as an inverter) 612, a transistor 613, a capacitor 614, a NOT gate 615, a NAND gate 616, a clocked inverter 617, an analog switch 618, a NOT gate 619, a clocked NAND gate 620, and a NOT gate 621.

[0275]

A data signal D is input to a data input terminal of the analog switch 611, a

clock signal CLK is input to a first signal input terminal of the analog switch 611, and an inverted signal of the clock signal CLK is input to a second signal input terminal of the analog switch 611.

[0276]

5 The clock signal CLK is input to a data input terminal of the NOT gate 612.

[0277]

One of a source and a drain of the transistor 613 is electrically connected to a data output terminal of the analog switch 611, and the clock signal CLK is input to a gate of the transistor 613. The output signal from the analog switch 611 is input to the 10 one of the source and the drain of the transistor 613. As the transistor 613, for example, the transistor including an oxide semiconductor layer described in the above embodiment can be used. For example, the transistor 100b in FIGS. 1A to 1C, the transistor 200c in FIGS. 7A to 7C, or the transistor 300b in FIGS. 8A to 8D can be used.

[0278]

15 A first capacitor electrode of the capacitor 614 is electrically connected to the other of the source and the drain of the transistor 613. A low power supply voltage Vss is input to a second capacitor electrode of the capacitor 614.

[0279]

20 A data input terminal of the NOT gate 615 is electrically connected to the other of the source and the drain of the transistor 613.

[0280]

A first data input terminal of the NAND gate 616 is electrically connected to a data output terminal of the NOT gate 615. A reset signal RST is input to a second data input terminal of the NAND gate 616.

25 [0281]

A data input terminal of the clocked inverter 617 is electrically connected to a data output terminal of the NAND gate 616. The inverted signal of the clock signal CLK is input to a first signal input terminal of the clocked inverter 617. The clock signal CLK is input to a second signal input terminal of the clocked inverter 617. A 30 data output terminal of the clocked inverter 617 is electrically connected to the data output terminal of the NOT gate 615.

[0282]

A data input terminal of the analog switch 618 is electrically connected to the data output terminal of the NAND gate 616. The inverted signal of the clock signal CLK is input to a first signal input terminal of the analog switch 618. The clock signal CLK is input to a second signal input terminal of the analog switch 618.

5 [0283]

A data input terminal of the NOT gate 619 is electrically connected to a data output terminal of the analog switch 618.

[0284]

10 A first data input terminal of the clocked NAND gate 620 is electrically connected to a data output terminal of the NOT gate 619. The reset signal RST is input to a second data input terminal of the clocked NAND gate 620. The clock signal CLK is input to a first signal input terminal of the clocked NAND gate 620. The inverted signal of the clocked signal CLK is input to a second input terminal of the clocked NAND gate 620. A data output terminal of the clocked NAND gate 620 is 15 electrically connected to the data output terminal of the analog switch 618. The clocked NAND gate 620 is formed with a NAND gate and an analog switch, for example.

[0285]

20 A data input terminal of the NOT gate 621 is electrically connected to the data output terminal of the NOT gate 619 and the first data input terminal of the clocked NAND gate 620. A data signal Q is output from a data output terminal of the NOT gate 621.

[0286]

25 Further, one or more of the analog switch 611, the NOT gate 612, the NOT gate 615, a latch circuit 651, the analog switch 618, a latch circuit 652, and the NOT gate 621 include the field-effect transistor provided on an SOI substrate described in the above embodiment, and for example, the transistor 100a in FIGS. 1A to 1C, the transistor 200b in FIGS. 7A to 7C, or the transistor 300a in FIGS. 8A to 8D can be used.

[0287]

30 Next, an operation example of the unit memory device illustrated in FIG. 10A is described with reference to FIG. 10B. FIG. 10B is a timing chart showing the operation example of the sequential circuit in FIG. 10A.

[0288]

In a period 691, a power supply voltage Vp, the clock signal CLK, and the reset signal RST are supplied to the unit memory device illustrated in FIG. 10A. At this time, the reset signal is set at a high level.

5 [0289]

When the clock signal CLK is set at a high level, the analog switch 611 and the transistor 613 are turned on and the analog switch 618 is turned off. At this time, a voltage of the first capacitor electrode of the capacitor 614 becomes equal to a voltage of the data signal D. As a result, data of the data signal D is written in the unit 10 memory device.

[0290]

When the clock signal CLK is set at a low level, the analog switch 611 and the transistor 613 are turned off and the analog switch 618 is turned on. At this time, a voltage of a signal Q becomes a voltage of the data of the data signal D, and the written 15 data of the data signal D is output from the unit memory device.

[0291]

To stop the operation of the unit memory device, as shown in a period 692, the supply of the clock signal CLK and the supply of the reset signal RST are stopped, and then the supply of the power supply voltage Vp is stopped. At this time, the timing of 20 stopping the supply of the clock signal CLK may be different from the timing of stopping the supply of the reset signal RST.

[0292]

At this time, although operations of the analog switch 611, the NOT gate 612, the transistor 613, the latch circuit 651, the analog switch 618, the latch circuit 652, and 25 the NOT gate 621 are stopped, the voltage of the first capacitor electrode of the capacitor 614 is kept for a certain period, at the voltage of the data signal D in the period before the operation of the unit memory device is stopped because an off-state current of the transistor 613 is low.

[0293]

30 In addition, in the case where the operation of the unit memory device restarts, as shown in a period 693, the supply of the power supply voltage Vp restarts first; the supply of the reset signal RST restarts; and then, the supply of the clock signal CLK

restarts.

[0294]

At this time, the operations of the analog switch 611, the NOT gate 612, the transistor 613, the latch circuit 651, the analog switch 618, the latch circuit 652, and the NOT gate 621 restart. When the clock signal CLK is at a low level, the voltage of the signal Q becomes the voltage of the data of the data signal D written in the unit memory device, and the written data of the data signal D is output from the unit memory device. As a result, the state of the unit memory device can be returned to the state at the time before the operation of the unit memory device is stopped.

10 [0295]

This is the operation example of the unit memory device illustrated in FIG. 10A.

[0296]

Another example of the unit memory device is described with reference to FIGS. 11A to 11C.

[0297]

A unit memory device illustrated in FIG. 11A inputs a data signal IN71. The unit memory device illustrated in FIG. 11A outputs a data signal OUT72. The unit memory device illustrated in FIG. 11A includes a transistor 701, a transistor 702, a memory circuit 703, a capacitor 704, a NOT gate 705, a switching circuit (also referred to as a SW) 706, and a memory circuit (also referred to as a MEM) 707.

[0298]

A voltage V1 is input to one of a source and a drain of the transistor 701, and a signal S53 is input to a gate of the transistor 701.

25 [0299]

The transistor 702 has a different conductivity type from the transistor 701. One of a source and a drain of the transistor 702 is electrically connected to the other of the source and the drain of the transistor 701, and the signal S53 is input to a gate of the transistor 702.

30 [0300]

The memory circuit 703 includes a transistor 751, a transistor 752, and a capacitor 753.

[0301]

The data signal IN71 is input to one of a source and a drain of the transistor 751, and a signal S54 is input to a gate of the transistor 751.

[0302]

5 As the transistor 751, for example, the transistor including an oxide semiconductor layer described in the above embodiment can be used. For example, the transistor 100b in FIGS. 1A to 1C, the transistor 200c in FIGS. 7A to 7C, or the transistor 300b in FIGS. 8A to 8D can be used

[0303]

10 A gate of the transistor 752 is electrically connected to the other of the source and the drain of the transistor 751, one of a source and a drain of the transistor 752 is electrically connected to the other of the source and the drain of the transistor 702, and a voltage V2 is input to the other of the source and the drain of the transistor 752.

[0304]

15 As the transistor 752, for example, the field-effect transistor provided on the SOI substrate described in the above embodiment can be used. For example, the transistor 100a in FIGS. 1A to 1C, the transistor 200a or 200b in FIGS. 7A to 7C, or the transistor 300a in FIGS. 8A to 8D can be used.

[0305]

20 A first capacitor electrode of the capacitor 753 is electrically connected to the other of the source and the drain of the transistor 751, and the voltage V2 is input to a second capacitor electrode of the capacitor 753. As the capacitor 753, the capacitor illustrated in FIGS. 8A to 8D can be used. Note that the capacitor 753 is not necessarily provided.

25 [0306]

Note that a difference between the voltage V1 and the voltage V2 is the power supply voltage Vp in FIGS. 11A and 11B.

[0307]

30 A first capacitor electrode of the capacitor 704 is electrically connected to the other of the source and the drain of the transistor 701, and the voltage V2 is input to a second capacitor electrode of the capacitor 704.

[0308]

A data input terminal of the NOT gate 705 is electrically connected to the other of the source and the drain of the transistor 701.

[0309]

5 A signal S51, the data signal IN71, an output signal from the NOT gate 705 (also referred to as a data signal D71) are input to the switching circuit 706. The switching circuit 706 has a function of outputting, in accordance with the signal S51, a data signal D72 which has a value corresponding to the data signal IN71 or the data signal D71.

[0310]

10 The switching circuit 706 includes, for example, at least two analog switches. For example, when one of the two analog switches is turned on, the other of the two analog switches is turned off, whereby data of the data signal D72 can be switched to the value corresponding to the data signal IN71 or the data signal D71.

[0311]

15 A data signal D72 is input from the switching circuit 706 to the memory circuit 707. The memory circuit 707 outputs a signal S52 whose value is set in accordance with the signal input to the memory circuit 707. The signal S52 becomes the data signal OUT72.

[0312]

20 The memory circuit 707 includes a flip-flop formed using a transistor including a single crystal semiconductor layer, for example.

[0313]

25 The transistor 701, the transistor 702, the NOT gate 705, the switching circuit 706, and the memory circuit 707 are formed using, for example, the field-effect transistor provided on the SOI substrate described in the above embodiment. For example, the transistor 100a in FIGS. 1A to 1C, the transistor 200a or 200b in FIGS. 7A to 7C, or the transistor 300a in FIGS. 8A to 8D can be used

[0314]

30 Next, an operation example of the unit memory device illustrated in FIG. 11A is described with reference to FIGS. 11B and 11C. FIGS. 11B and 11C are each a timing chart for describing the operation example of the sequential circuit in FIG. 11A.

[0315]

In the unit memory device illustrated in FIG. 11A, during a period in which the power supply voltage  $V_p$  is supplied, the signal  $S51$  is set at a low level, the data signal  $D72$  becomes the value corresponding to the data signal  $IN71$  by the switching circuit 706, and the data of the data signal  $D72$  which has the value corresponding to the data signal  $IN71$  is stored in the memory circuit 707.

5 [0316]

whereto stop the operation of the unit memory device, as shown in FIG. 11B, the signal  $S51$  is set at a low level, and then a pulse of the signal  $S54$  is input to the gate of the transistor 751.

10 [0317]

At this time, the transistor 751 is turned on, and a voltage of the first capacitor electrode of the capacitor 753 becomes equal to a voltage of the data stored in the memory circuit 707. Then, after the input of the pulse of the signal  $S54$  is completed, the transistor 751 is turned off. At this time, the voltage of the first capacitor electrode of the capacitor 753 is kept for a certain period because an off-state current of the transistor 751 is low. After that, the supply of the power supply voltage  $V_p$  to the unit memory device is stopped.

15 [0318]

To restart the operation of the unit memory device, as shown in FIG. 11C, the supply of the power supply voltage  $V_p$  restarts, and then the signal  $S53$  is set at a low level. At this time, the signal  $S51$  and the signal  $S54$  are each set at a low level.

20 [0319]

At this time, the transistor 701 is turned on and the transistor 702 is turned off, so that the voltage of the first capacitor electrode of the capacitor 704 becomes equal to the voltage  $V1$ .

25 [0320]

After that, the signal  $S53$  is set at a high level. At this time, the transistor 701 is turned off and the transistor 702 is turned on, so that the voltage of the first capacitor electrode of the capacitor 704 is changed depending on a current flowing between the source and the drain of the transistor 752. The current flowing between the source and the drain of the transistor 752 is determined by a voltage of the gate of the transistor 752, that is, determined depending on the data input from the memory circuit 703 which is

stored in the first capacitor electrode of the capacitor. Therefore, when the transistor 702 is turned on, the voltage of the first capacitor electrode of the capacitor 704 can be the value corresponding to the data signal IN71.

[0321]

5 After that the signal S51 is set at a high level while keeping the signal S53 at the high level.

[0322]

10 At this time, the data signal D72 has the value corresponding to the signal D71 (the value corresponding to the data written in the memory circuit 703) by the switching circuit 706, and the signal D72 having the value corresponding to the data signal D71 is input to the memory circuit 707. As a result, the state of the memory circuit 707 can be returned to the state at the time before the operation of the unit memory device is stopped

[0323]

15 This is the operation example of the unit memory device illustrated in FIG. 11A.

[0324]

20 In the arithmetic processing unit of this embodiment in which the register includes the unit memory device, even when the supply of the power supply voltage is stopped, part of internal data in the state at the time just before the supply of the power supply voltage is stopped can be retained, and when the supply of the power supply voltage restarts, the state of the arithmetic processing unit can be returned to the state at the time just before the supply of the power supply voltage is stopped. Accordingly, even when power consumption is reduced by selectively stopping the supply of the 25 power supply voltage, a time after the supply of the power supply voltage restarts until the normal operation starts can be shortened.

[0325]

(Embodiment 5)

In this embodiment, CAAC will be described.

30 [0326]

The CAAC is not a single crystal, but this does not mean that the CAAC is composed of only an amorphous component. Although the CAAC includes a

crystallized portion (crystalline portion), a boundary between one crystalline portion and another crystalline portion is not clear in some cases.

[0327]

In the case where oxygen is included in the CAAC, nitrogen may be substituted for part of oxygen included in the CAAC. The c-axes of individual crystalline portions included in the CAAC may be aligned in one direction (e.g., a direction perpendicular to a surface of a substrate over which the CAAC is formed or a surface of the CAAC). Alternatively, the normals of the a-b planes of the individual crystalline portions included in the CAAC may be aligned in one direction (e.g., a direction perpendicular to a surface of a substrate over which the CAAC is formed or a surface of the CAAC).

[0328]

The CAAC becomes a conductor, a semiconductor, or an insulator depending on its composition or the like. The CAAC transmits or does not transmit visible light depending on its composition or the like.

15 [0329]

An example of such a CAAC is a crystal which is formed into a film shape and has a triangular or hexagonal atomic arrangement when observed from the direction perpendicular to a surface of the film or a surface of a supporting substrate, and in which metal atoms are arranged in a layered manner or metal atoms and oxygen atoms 20 (or nitrogen atoms) are arranged in a layered manner when a cross section of the film is observed.

[0330]

An example of a crystal structure of the CAAC will be described in detail with reference to FIGS. 13A to 13E, FIGS. 14A to 14C, and FIGS. 15A to 15C. In FIGS. 25 13A to 13E, FIGS. 14A to 14C, and FIGS. 15A to 15C, the vertical direction corresponds to the c-axis direction and a plane perpendicular to the c-axis direction corresponds to the a-b plane, unless otherwise specified. In the case where the expressions "an upper half" and "a lower half" are simply used, they refer to an upper half above the a-b plane and a lower half below the a-b plane (an upper half and a lower 30 half with respect to the a-b plane).

[0331]

FIG. 13A illustrates a structure including one hexacoordinate In atom and six

tetracoordinate oxygen (hereinafter referred to as tetracoordinate O) atoms proximate to the In atom. Here, a structure including one metal atom and oxygen atoms proximate to the metal atom is referred to as a small group. The structure in FIG. 13A is actually an octahedral structure, but is illustrated as a planar structure for simplicity. Note that 5 three tetracoordinate O atoms exist in each of an upper half and a lower half in FIG. 13A. In the small group illustrated in FIG. 13A, electric charge is 0.

[0332]

FIG. 13B illustrates a structure including one pentacoordinate Ga atom, three tricoordinate oxygen (hereinafter referred to as tricoordinate O) atoms proximate to the 10 Ga atom, and two tetracoordinate O atoms proximate to the Ga atom. All the tricoordinate O atoms exist on the a-b plane. One tetracoordinate O atom exists in each of an upper half and a lower half in FIG. 13B. An In atom can also have the structure illustrated in FIG. 13B because an In atom can have five ligands. In the small group illustrated in FIG. 13B, electric charge is 0.

15 [0333]

FIG. 13C illustrates a structure including one tetracoordinate Zn atom and four tetracoordinate O atoms proximate to the Zn atom. In FIG. 13C, one tetracoordinate O atom exists in an upper half and three tetracoordinate O atoms exist in a lower half. Alternatively, three tetracoordinate O atoms may exist in the upper half and one 20 tetracoordinate O atom may exist in the lower half in FIG. 13C. In the small group illustrated in FIG. 13C, electric charge is 0.

[0334]

FIG. 13D illustrates a structure including one hexacoordinate Sn atom and six tetracoordinate O atoms proximate to the Sn atom. In FIG. 13D, three tetracoordinate 25 O atoms exist in each of an upper half and a lower half. In the small group illustrated in FIG. 13D, electric charge is +1.

[0335]

FIG. 13E illustrates a small group including two Zn atoms. In FIG. 13E, one tetracoordinate O atom exists in each of an upper half and a lower half. In the small 30 group illustrated in FIG. 13E, electric charge is -1.

[0336]

Here, a plurality of small groups form a medium group, and a plurality of medium groups form a large group (also referred to as a unit cell).

[0337]

Now, a rule of bonding between the small groups will be described. The three O atoms in the upper half with respect to the hexacoordinate In atom in FIG. 13A each have three proximate In atoms in the downward direction, and the three O atoms in the lower half each have three proximate In atoms in the upward direction. The one O atom in the upper half with respect to the pentacoordinate Ga atom has one proximate Ga atom in the downward direction, and the one O atom in the lower half has one proximate Ga atom in the upward direction. The one O atom in the upper half with respect to the tetracoordinate Zn atom has one proximate Zn atom in the downward direction, and the three O atoms in the lower half each have three proximate Zn atoms in the upward direction. In this manner, the number of the tetracoordinate O atoms above the metal atom is equal to the number of the metal atoms proximate to and below each of the tetracoordinate O atoms. Similarly, the number of the tetracoordinate O atoms below the metal atom is equal to the number of the metal atoms proximate to and above each of the tetracoordinate O atoms. Since the coordination number of the tetracoordinate O atom is 4, the sum of the number of the metal atoms proximate to and below the O atom and the number of the metal atoms proximate to and above the O atom is 4. Accordingly, when the sum of the number of tetracoordinate O atoms above a metal atom and the number of tetracoordinate O atoms below another metal atom is 4, the two kinds of small groups including the metal atoms can be bonded. For example, in the case where the hexacoordinate metal (In or Sn) atom is bonded through three tetracoordinate O atoms in the lower half, it is bonded to the pentacoordinate metal (Ga or In) atom or the tetracoordinate metal (Zn) atom.

[0338]

A metal atom having the above coordination number is bonded to another metal atom having the above coordination number through a tetracoordinate O atom in the c-axis direction. In addition to the above, a medium group can be formed in a different manner by combining a plurality of small groups so that the total electric charge of the layered structure is 0.

[0339]

FIG. 14A illustrates a model of a medium group included in a layered structure of an In-Sn-Zn-O-based material. FIG. 14B illustrates a large group including three medium groups. FIG. 14C illustrates an arrangement order in the case where the layered structure in FIG. 14B is observed from the c-axis direction.

5 [0340]

In FIG. 14A, for simplicity, a tricoordinate O atom is omitted and tetracoordinate O atoms are shown by a circle; the number in the circle shows the number of tetracoordinate O atoms. For example, three tetracoordinate O atoms existing in each of an upper half and a lower half with respect to a Sn atom are denoted by circled 3. Similarly, in FIG. 14A, one tetracoordinate O atom existing in each of an upper half and a lower half with respect to an In atom is denoted by circled 1. FIG. 14A also illustrates a Zn atom proximate to one tetracoordinate O atom in a lower half and three tetracoordinate O atoms in an upper half, and a Zn atom proximate to one tetracoordinate O atom in an upper half and three tetracoordinate O atoms in a lower half.

15 [0341]

In the medium group included in the layered structure of the In-Sn-Zn-O-based material in FIG. 14A, in the order starting from the top, a Sn atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half is bonded to an In atom proximate to one tetracoordinate O atom in each of an upper half and a lower half, the In atom is bonded to a Zn atom proximate to three tetracoordinate O atoms in an upper half, the Zn atom is bonded to an In atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half through one tetracoordinate O atom in a lower half with respect to the Zn atom, the In atom is bonded to a small group that includes two Zn atoms and is proximate to one tetracoordinate O atom in an upper half, and the small group is bonded to a Sn atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half through one tetracoordinate O atom in a lower half with respect to the small group. A plurality of such medium groups are bonded, so that a large group is formed.

20 [0342]

Here, electric charge for one bond of a tricoordinate O atom and electric charge for one bond of a tetracoordinate O atom can be assumed to be -0.667 and -0.5,

respectively. For example, electric charge of a (hexacoordinate or pentacoordinate) In atom, electric charge of a (tetracoordinate) Zn atom, and electric charge of a (pentacoordinate or hexacoordinate) Sn atom are +3, +2, and +4, respectively. Accordingly, electric charge in a small group including a Sn atom is +1. Therefore, 5 electric charge of -1, which cancels +1, is needed to form a layered structure including a Sn atom. As a structure having electric charge of -1, the small group including two Zn atoms as illustrated in FIG. 13E can be given. For example, with one small group including two Zn atoms, electric charge of one small group including a Sn atom can be cancelled, so that the total electric charge of the layered structure can be 0.

## 10 [0343]

When the large group illustrated in FIG. 14B is repeated, an In-Sn-Zn-O-based crystal ( $\text{In}_2\text{SnZn}_3\text{O}_8$ ) can be obtained. Note that a layered structure of the obtained In-Sn-Zn-O-based crystal can be expressed as a composition formula,  $\text{In}_2\text{SnZn}_2\text{O}_7(\text{ZnO})_m$  ( $m$  is 0 or a natural number). As larger  $m$  is, the crystallinity of the 15 In-Sn-Zn-O-based crystal is improved, which is preferable.

## [0344]

The above-described rule also applies to the followings: a four-component metal oxide such as an In-Sn-Ga-Zn-O-based metal oxide; a three-component metal oxide such as an In-Ga-Zn-O-based metal oxide (also referred to as IGZO), an 20 In-Al-Zn-O-based metal oxide, a Sn-Ga-Zn-O-based metal oxide, an Al-Ga-Zn-O-based metal oxide, a Sn-Al-Zn-O-based metal oxide, an In-Hf-Zn-O-based metal oxide, an In-La-Zn-O-based metal oxide, an In-Ce-Zn-O-based metal oxide, an In-Pr-Zn-O-based metal oxide, an In-Nd-Zn-O-based metal oxide, an In-Sm-Zn-O-based metal oxide, an In-Eu-Zn-O-based metal oxide, an In-Gd-Zn-O-based metal oxide, an 25 In-Tb-Zn-O-based metal oxide, an In-Dy-Zn-O-based metal oxide, an In-Ho-Zn-O-based metal oxide, an In-Er-Zn-O-based metal oxide, an In-Tm-Zn-O-based metal oxide, an In-Yb-Zn-O-based metal oxide, or an In-Lu-Zn-O-based metal oxide; a two-component metal oxide such as an In-Zn-O-based metal oxide, a Sn-Zn-O-based metal oxide, an Al-Zn-O-based metal oxide, a 30 Zn-Mg-O-based metal oxide, a Sn-Mg-O-based metal oxide, an In-Mg-O-based metal oxide, or an In-Ga-O-based metal oxide; a single-component metal oxide such as an

In-O-based metal oxide, a Sn-O-based metal oxide, or a Zn-O-based metal oxide; and the like.

[0345]

As an example, FIG. 15A illustrates a model of a medium group included in a 5 layered structure of an In-Ga-Zn-O-based material.

[0346]

In the medium group included in the layered structure of the In-Ga-Zn-O-based material in FIG. 15A, in the order starting from the top, an In atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half is bonded to a Zn 10 atom proximate to one tetracoordinate O atom in an upper half, the Zn atom is bonded to a Ga atom proximate to one tetracoordinate O atom in each of an upper half and a lower half through three tetracoordinate O atoms in a lower half with respect to the Zn atom, and the Ga atom is bonded to an In atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half through one tetracoordinate O atom in a 15 lower half with respect to the Ga atom. A plurality of such medium groups are bonded, so that a large group is formed.

[0347]

FIG. 15B illustrates a large group including three medium groups. FIG. 15C 20 illustrates an atomic arrangement in the case where the layered structure in FIG. 15B is observed from the c-axis direction.

[0348]

Here, since electric charge of a (hexacoordinate or pentacoordinate) In atom, electric charge of a (tetracoordinate) Zn atom, and electric charge of a (pentacoordinate) Ga atom are +3, +2, and +3, respectively, electric charge of a small group including any 25 of an In atom, a Zn atom, and a Ga atom is 0. As a result, the total electric charge of a medium group having a combination of such small groups is always 0.

[0349]

In order to form the layered structure of the In-Ga-Zn-O-based material, a large group can be formed using not only the medium group illustrated in FIG. 15A but also a 30 medium group in which the arrangement of the In atom, the Ga atom, and the Zn atom is different from that in FIG. 15A.

[0350]

(Embodiment 6)

In this embodiment, the field-effect mobility of a transistor will be described.

[0351]

The actually measured field-effect mobility of an insulated gate transistor can  
5 be lower than its original mobility because of a variety of reasons; this phenomenon  
occurs not only in the case of using an oxide semiconductor. One of the factors that  
reduce the mobility is a defect inside a semiconductor or a defect at an interface  
between the semiconductor and an insulating film. When a Levinson model is used,  
the field-effect mobility on the assumption that no defect exists inside the  
10 semiconductor can be calculated theoretically.

[0352]

Assuming that the original mobility and the measured field-effect mobility of a  
semiconductor are  $\mu_0$  and  $\mu$ , respectively, and a potential barrier (such as a grain  
boundary) exists in the semiconductor, the measured field-effect mobility can be  
15 expressed as the following formula.

[0353]

[Formula 2]

$$\mu = \mu_0 \exp\left(-\frac{E}{kT}\right)$$

[0354]

20 Here,  $E$  represents the height of the potential barrier,  $k$  represents the  
Boltzmann constant, and  $T$  represents the absolute temperature. When the potential  
barrier is assumed to be attributed to a defect, the height of the potential barrier can be  
expressed as the following formula according to the Levinson model.

[0355]

25 [Formula 3]

$$E = \frac{e^2 N^2}{8 \varepsilon n} = \frac{e^3 N^2 t}{8 \varepsilon C_{ox} V_g}$$

[0356]

Here,  $e$  represents the elementary charge,  $N$  represents the average defect  
density per unit area in a channel,  $\varepsilon$  represents the dielectric constant of the  
30 semiconductor,  $n$  represents the number of carriers per unit area in the channel,  $C_{ox}$

represents the capacitance per unit area,  $V_g$  represents the gate voltage, and  $t$  represents the thickness of the channel. In the case where the thickness of the semiconductor layer is 30 nm or less, the thickness of the channel may be regarded as being the same as the thickness of the semiconductor layer. The drain current  $I_d$  in a linear region can 5 be expressed as the following formula.

[0357]

[Formula 4]

$$I_d = \frac{W\mu V_g V_d C_{ox}}{L} \exp\left(-\frac{E}{kT}\right)$$

[0358]

10 Here,  $L$  represents the channel length and  $W$  represents the channel width, and  $L$  and  $W$  are each 10  $\mu\text{m}$ . In addition,  $V_d$  represents the drain voltage. When dividing both sides of the above equation by  $V_g$  and then taking logarithms of both sides, the following formula can be obtained.

[0359]

15 [Formula 5]

$$\ln\left(\frac{I_d}{V_g}\right) = \ln\left(\frac{W\mu V_d C_{ox}}{L}\right) - \frac{E}{kT} = \ln\left(\frac{W\mu V_d C_{ox}}{L}\right) - \frac{e^3 N^2 t}{8kT \epsilon C_{ox} V_g}$$

[0360]

20 The right side of Formula 5 is a function of  $V_g$ . From the formula, it is found that the defect density  $N$  can be obtained from the slope of a line in which  $\ln(I_d/V_g)$  is the ordinate and  $1/V_g$  is the abscissa. That is, the defect density can be evaluated from the  $I_d$ - $V_g$  characteristics of the transistor. The defect density  $N$  of an oxide semiconductor in which the ratio of indium (In), tin (Sn), and zinc (Zn) is 1:1:1 is approximately  $1 \times 10^{12} / \text{cm}^2$ .

[0361]

25 On the basis of the defect density obtained in this manner, or the like,  $\mu_0$  can be calculated to be  $120 \text{ cm}^2/\text{Vs}$  from Formula 2 and Formula 3. The measured mobility of an In-Sn-Zn oxide including a defect is approximately  $35 \text{ cm}^2/\text{Vs}$ . However, assuming that no defect exists inside the semiconductor and at the interface between the semiconductor and an insulating film, the mobility  $\mu_0$  of the oxide semiconductor is 30 expected to be  $120 \text{ cm}^2/\text{Vs}$ .

[0362]

Note that even when no defect exists inside a semiconductor, scattering at an interface between a channel and a gate insulating layer affects the transport property of the transistor. In other words, the mobility  $\mu_1$  at a position that is distance  $x$  away from the interface between the channel and the gate insulating layer can be expressed as the following formula.

[0363]

[Formula 6]

$$\frac{1}{\mu_1} = \frac{1}{\mu_0} + \frac{D}{B} \exp\left(-\frac{x}{G}\right)$$

10 [0364]

Here,  $D$  represents the electric field in the gate direction, and  $B$  and  $G$  are constants.  $B$  and  $G$  can be obtained from actual measurement results; according to the above measurement results,  $B$  is  $4.75 \times 10^7$  cm/s and  $G$  is 10 nm (the depth to which the influence of interface scattering reaches). When  $D$  is increased (i.e., when the gate voltage is increased), the second term of Formula 6 is increased and accordingly the mobility  $\mu_1$  is decreased.

15 [0365]

Calculation results of the mobility  $\mu_2$  of a transistor whose channel includes an ideal oxide semiconductor without a defect inside the semiconductor are shown in FIG. 20 16. For the calculation, device simulation software Sentaurus Device manufactured by Synopsys, Inc. was used, and the band gap, the electron affinity, the relative permittivity, and the thickness of the oxide semiconductor were assumed to be 2.8 eV, 4.7 eV, 15, and 15 nm, respectively. These values were obtained by measurement of a thin film that was formed by sputtering.

25 [0366]

Further, the work functions of a gate, a source, and a drain were assumed to be 5.5 eV, 4.6 eV, and 4.6 eV, respectively. The thickness of a gate insulating layer was assumed to be 100 nm, and the relative permittivity thereof was assumed to be 4.1. The channel length and the channel width were each assumed to be 10  $\mu\text{m}$ , and the 30 drain voltage  $V_d$  was assumed to be 0.1 V.

[0367]

As shown in FIG. 16, the mobility has a peak of  $100 \text{ cm}^2/\text{Vs}$  or more at a gate voltage that is a little over 1 V and is decreased as the gate voltage becomes higher because the influence of interface scattering is increased. Note that in order to reduce 5 interface scattering, it is desirable that a surface of the semiconductor layer be flat at the atomic level (atomic layer flatness).

[0368]

Calculation results of characteristics of minute transistors which are manufactured using an oxide semiconductor having such a mobility are shown in FIGS. 10 17A to 17C, FIGS. 18A to 18C, and FIGS. 19A to 19C. FIGS. 20A and 20B illustrate cross-sectional structures of the transistors used for the calculation. The transistors illustrated in FIGS. 20A and 20B each include a semiconductor region 2103a and a semiconductor region 2103c which have  $n^+$ -type conductivity in an oxide semiconductor layer. The resistivities of the semiconductor region 2103a and the 15 semiconductor region 2103c are  $2 \times 10^{-3} \Omega\text{cm}$ .

[0369]

The transistor illustrated in FIG. 20A is formed over a base insulating layer 2101 and an embedded insulator 2102 which is embedded in the base insulating layer 2101 and formed of aluminum oxide. The transistor includes the semiconductor 20 region 2103a, the semiconductor region 2103c, an intrinsic semiconductor region 2103b serving as a channel formation region therebetween, and a gate 2105. The width of the gate 2105 is 33 nm.

[0370]

A gate insulating layer 2104 is formed between the gate 2105 and the 25 semiconductor region 2103b. In addition, a sidewall insulator 2106a and a sidewall insulator 2106b are formed on both side surfaces of the gate 2105, and an insulator 2107 is formed over the gate 2105 so as to prevent a short circuit between the gate 2105 and another wiring. The sidewall insulator has a width of 5 nm. A source 2108a and a drain 2108b are provided in contact with the semiconductor region 2103a and the 30 semiconductor region 2103c, respectively. Note that the channel width of this transistor is 40 nm.

[0371]

The transistor of FIG. 20B is the same as the transistor of FIG. 20A in that it is formed over the base insulating layer 2101 and the embedded insulator 2102 formed of aluminum oxide and that it includes the semiconductor region 2103a, the semiconductor region 2103c, the intrinsic semiconductor region 2103b provided therebetween, the gate 5 2105 having a width of 33 nm, the gate insulating layer 2104, the sidewall insulator 2106a, the sidewall insulator 2106b, the insulator 2107, the source 2108a, and the drain 2108b.

[0372]

10 The transistor illustrated in FIG. 20B is different from the transistor illustrated in FIG. 20A in the conductivity type of semiconductor regions under the sidewall insulator 2106a and the sidewall insulator 2106b. In the transistor illustrated in FIG. 20A, the semiconductor regions under the sidewall insulator 2106a and the sidewall insulator 2106b are part of the semiconductor region 2103a having n<sup>+</sup>-type conductivity 15 and part of the semiconductor region 2103c having n<sup>+</sup>-type conductivity, whereas in the transistor illustrated in FIG. 20B, the semiconductor regions under the sidewall insulator 2106a and the sidewall insulator 2106b are part of the intrinsic semiconductor region 2103b. In other words, a region having a width of  $L_{off}$  which overlaps with neither the semiconductor region 2103a (the semiconductor region 2103c) nor the gate 2105 is 20 provided. This region is called an offset region, and the width  $L_{off}$  is called an offset length. As is seen from the drawing, the offset length is equal to the width of the sidewall insulator 2106a (the sidewall insulator 2106b).

[0373]

25 The other parameters used in calculation are as described above. For the calculation, device simulation software Sentaurus Device manufactured by Synopsys, Inc. was used. FIGS. 17A to 17C show the gate voltage ( $V_g$ : a potential difference between the gate and the source) dependence of the drain current ( $I_d$ , a solid line) and the mobility ( $\mu$ , a dotted line) of the transistor having the structure illustrated in FIG. 20A. The drain current  $I_d$  is obtained by calculation under the assumption that the 30 drain voltage (a potential difference between the drain and the source) is +1 V and the mobility  $\mu$  is obtained by calculation under the assumption that the drain voltage is +0.1

V.

[0374]

FIG. 17A shows the gate voltage dependence of the transistor in the case where the thickness of the gate insulating layer is 15 nm, FIG. 17B shows that of the transistor in the case where the thickness of the gate insulating layer is 10 nm, and FIG. 17C shows that of the transistor in the case where the thickness of the gate insulating layer is 5 nm. As the gate insulating layer is thinner, the drain current  $I_d$  (off-state current) particularly in an off state is significantly decreased. In contrast, there is no noticeable change in the peak value of the mobility  $\mu$  and the drain current  $I_d$  in an on state (on-state current). The graphs show that the drain current exceeds 10  $\mu$ A at a gate voltage of around 1 V.

[0375]

FIGS. 18A to 18C show the gate voltage  $V_g$  dependence of the drain current  $I_d$  (a solid line) and the mobility  $\mu$  (a dotted line) of the transistor having the structure illustrated in FIG. 20B where the offset length  $L_{off}$  is 5 nm. The drain current  $I_d$  is obtained by calculation under the assumption that the drain voltage is +1 V and the mobility  $\mu$  is obtained by calculation under the assumption that the drain voltage is +0.1 V. FIG. 18A shows the gate voltage dependence of the transistor in the case where the thickness of the gate insulating layer is 15 nm, FIG. 18B shows that of the transistor in the case where the thickness of the gate insulating layer is 10 nm, and FIG. 18C shows that of the transistor in the case where the thickness of the gate insulating layer is 5 nm.

[0376]

Further, FIGS. 19A to 19C show the gate voltage dependence of the drain current  $I_d$  (a solid line) and the mobility  $\mu$  (a dotted line) of the transistor having the structure illustrated in FIG. 20B where the offset length  $L_{off}$  is 15 nm. The drain current  $I_d$  is obtained by calculation under the assumption that the drain voltage is +1 V and the mobility  $\mu$  is obtained by calculation under the assumption that the drain voltage is +0.1 V. FIG. 19A shows the gate voltage dependence of the transistor in the case where the thickness of the gate insulating layer is 15 nm, FIG. 19B shows that of the transistor in the case where the thickness of the gate insulating layer is 10 nm, and FIG. 19C shows that of the transistor in the case where the thickness of the gate insulating

layer is 5 nm.

[0377]

In either of the structures, as the gate insulating layer is thinner, the off-state current is significantly decreased, whereas no noticeable change arises in the peak value 5 of the mobility  $\mu$  and the on-state current.

[0378]

Note that the peak of the mobility  $\mu$  is approximately  $80 \text{ cm}^2/\text{Vs}$  in FIGS. 17A to 17C, approximately  $60 \text{ cm}^2/\text{Vs}$  in FIGS. 18A to 18C, and approximately  $40 \text{ cm}^2/\text{Vs}$  in FIGS. 19A to 19C; thus, the peak of the mobility  $\mu$  is decreased as the offset length 10  $L_{\text{off}}$  is increased. Further, the same applies to the off-state current. The on-state current is also decreased as the offset length  $L_{\text{off}}$  is increased; however, the decrease in the on-state current is much more gradual than the decrease in the off-state current. Further, the graphs show that in either of the structures, the drain current exceeds  $10 \mu\text{A}$  at a gate voltage of around 1 V.

[0379]

(Embodiment 7)

In this embodiment, a transistor in which an oxide semiconductor including In, Sn, and Zn as main components is used as an oxide semiconductor will be described.

[0380]

20 A transistor in which an oxide semiconductor including In, Sn, and Zn as main components is used as a channel formation region can have favorable characteristics by depositing the oxide semiconductor while heating a substrate or by performing heat treatment after an oxide semiconductor film is formed. Note that a main component refers to an element included in composition at 5 atomic% or more.

[0381]

By intentionally heating the substrate after formation of the oxide semiconductor film including In, Sn, and Zn as main components, the field-effect mobility of the transistor can be improved. Further, the threshold voltage of the transistor can be positively shifted to make the transistor normally off.

[0382]

As an example, FIGS. 21A to 21C each show characteristics of a transistor that

includes an oxide semiconductor film including In, Sn, and Zn as main components and having a channel length  $L$  of 3  $\mu\text{m}$  and a channel width  $W$  of 10  $\mu\text{m}$ , and a gate insulating layer with a thickness of 100 nm. Note that  $V_d$  was set to 10 V.

[0383]

5 FIG. 21A shows characteristics of a transistor whose oxide semiconductor film including In, Sn, and Zn as main components was formed by a sputtering method without heating a substrate intentionally. The field-effect mobility of the transistor is 18.8  $\text{cm}^2/\text{Vsec}$ . On the other hand, when the oxide semiconductor film including In, Sn, and Zn as main components is formed while heating the substrate intentionally, the 10 field-effect mobility can be improved. FIG. 21B shows characteristics of a transistor whose oxide semiconductor film including In, Sn, and Zn as main components was formed while heating a substrate at 200  $^{\circ}\text{C}$ . The field-effect mobility of the transistor is 32.2  $\text{cm}^2/\text{Vsec}$ .

[0384]

15 The field-effect mobility can be further improved by performing heat treatment after formation of the oxide semiconductor film including In, Sn, and Zn as main components. FIG. 21C shows characteristics of a transistor whose oxide semiconductor film including In, Sn, and Zn as main components was formed by a sputtering method at 200  $^{\circ}\text{C}$  and then subjected to heat treatment at 650  $^{\circ}\text{C}$ . The 20 field-effect mobility of the transistor is 34.5  $\text{cm}^2/\text{Vsec}$ .

[0385]

25 The intentional heating of the substrate is expected to have an effect of reducing moisture taken into the oxide semiconductor film during the deposition by sputtering. Further, the heat treatment after deposition enables hydrogen, a hydroxyl group, or moisture to be released and removed from the oxide semiconductor film. In this manner, the field-effect mobility can be improved. Such an improvement in field-effect mobility is presumed to be achieved not only by removal of impurities by dehydration or dehydrogenation but also by a reduction in interatomic distance due to an increase in density. The oxide semiconductor can be crystallized by being highly 30 purified by removal of impurities from the oxide semiconductor. In the case of using such a purified non-single-crystal oxide semiconductor, ideally, a field-effect mobility

exceeding 100 cm<sup>2</sup>/Vsec is expected to be achieved.

[0386]

The oxide semiconductor including In, Sn, and Zn as main components may be crystallized in the following manner: oxygen ions are implanted into the oxide semiconductor, hydrogen, a hydroxyl group, or moisture included in the oxide semiconductor is released by heat treatment, and the oxide semiconductor is crystallized through the heat treatment or by heat treatment performed later. By such crystallization treatment or recrystallization treatment, a non-single crystal oxide semiconductor having favorable crystallinity can be obtained.

[0387]

The intentional heating of the substrate during deposition and/or the heat treatment after the deposition contributes not only to improving field-effect mobility but also to making the transistor normally off. In a transistor in which an oxide semiconductor film that includes In, Sn, and Zn as main components and is formed without heating a substrate intentionally is used as a channel formation region, the threshold voltage tends to be shifted negatively. However, when the oxide semiconductor film formed while heating the substrate intentionally is used, the problem of the negative shift of the threshold voltage can be solved. That is, the threshold voltage is shifted so that the transistor becomes normally off; this tendency can be confirmed by comparison between FIGS. 21A and 21B.

[0388]

Note that the threshold voltage can also be controlled by changing the ratio of In, Sn, and Zn; when the composition ratio of In, Sn, and Zn is 2:1:3, a normally-off transistor is expected to be formed. In addition, an oxide semiconductor film having high crystallinity can be obtained by setting the composition ratio of a target as follows: In:Sn:Zn = 2:1:3.

[0389]

The temperature of the intentional heating of the substrate or the temperature of the heat treatment is 150 °C or higher, preferably 200 °C or higher, further preferably 400 °C or higher. When deposition or heat treatment is performed at a high temperature, the transistor can be normally off.

[0390]

By intentionally heating the substrate during deposition and/or by performing heat treatment after the deposition, the stability against a gate-bias stress can be increased. For example, when a gate bias is applied with an intensity of 2 MV/cm at 5 150 °C for one hour, drift of the threshold voltage can be less than  $\pm 1.5$  V, preferably less than  $\pm 1.0$  V.

[0391]

A BT test was performed on the following two transistors: Sample 1 on which heat treatment was not performed after formation of an oxide semiconductor film, and 10 Sample 2 on which heat treatment at 650 °C was performed after formation of an oxide semiconductor film.

[0392]

First,  $V_g$ - $I_d$  characteristics of the transistors were measured at a substrate temperature of 25 °C and  $V_d$  of 10 V. Then, the substrate temperature was set to 15 150 °C and  $V_d$  was set to 0.1 V. After that, 20 V of  $V_g$  was applied so that the intensity of an electric field applied to gate insulating layers was 2 MV/cm, and the condition was kept for one hour. Next,  $V_g$  was set to 0 V. Then,  $V_g$ - $I_d$  characteristics of the transistors were measured at a substrate temperature of 25 °C and  $V_d$  of 10 V. This process is called a positive BT test.

20 [0393]

In a similar manner, first,  $V_g$ - $I_d$  characteristics of the transistors were measured at a substrate temperature of 25 °C and  $V_d$  of 10 V. Then, the substrate temperature was set to 150 °C and  $V_d$  was set to 0.1 V. After that, -20 V of  $V_g$  was applied so that the intensity of an electric field applied to the gate insulating layers was -2 MV/cm, and 25 the condition was kept for one hour. Next,  $V_g$  was set to 0 V. Then,  $V_g$ - $I_d$  characteristics of the transistors were measured at a substrate temperature of 25 °C and  $V_d$  of 10 V. This process is called a negative BT test.

[0394]

FIGS. 22A and 22B show results of the positive BT test and the negative BT 30 test, respectively, of Sample 1. FIGS. 23A and 23B show results of the positive BT test and the negative BT test, respectively, of Sample 2.

[0395]

The amount of shift in the threshold voltage of Sample 1 due to the positive BT test and that due to the negative BT test were 1.80 V and -0.42 V, respectively. The amount of shift in the threshold voltage of Sample 2 due to the positive BT test and that due to the negative BT test were 0.79 V and 0.76 V, respectively. It is found that, in each of Sample 1 and Sample 2, the amount of shift in the threshold voltage between before and after the BT tests is small and the reliability thereof is high.

[0396]

The heat treatment can be performed in an oxygen atmosphere; alternatively, the heat treatment may be performed first in an atmosphere of nitrogen or an inert gas or under reduced pressure, and then in an atmosphere including oxygen. Oxygen is supplied to the oxide semiconductor after dehydration or dehydrogenation, whereby an effect of the heat treatment can be further increased. As a method for supplying oxygen after dehydration or dehydrogenation, a method in which oxygen ions are accelerated by an electric field and implanted into the oxide semiconductor film may be employed.

[0397]

A defect due to oxygen deficiency is easily caused in the oxide semiconductor or at an interface between the oxide semiconductor and a stacked film; however, when excess oxygen is included in the oxide semiconductor by the heat treatment, oxygen deficiency caused constantly can be compensated for with excess oxygen. The excess oxygen is mainly oxygen existing between lattices. When the concentration of oxygen is set in the range of  $1 \times 10^{16} /cm^3$  to  $2 \times 10^{20} /cm^3$ , excess oxygen can be included in the oxide semiconductor without causing crystal distortion or the like.

[0398]

When heat treatment is performed so that at least part of the oxide semiconductor includes crystal, a more stable oxide semiconductor film can be obtained. For example, when an oxide semiconductor film which is formed by sputtering using a target having a composition ratio of In:Sn:Zn = 1:1:1 without heating a substrate intentionally is analyzed by X-ray diffraction (XRD), a halo pattern is observed. The formed oxide semiconductor film can be crystallized by being subjected to heat

treatment. The temperature of the heat treatment can be set as appropriate; when the heat treatment is performed at 650 °C, for example, a clear diffraction peak can be observed in an X-ray diffraction analysis.

[0399]

5 An XRD analysis of an In-Sn-Zn-O film was conducted. The XRD analysis was conducted using an X-ray diffractometer D8 ADVANCE manufactured by Bruker AXS, and measurement was performed by an out-of-plane method.

[0400]

10 Sample A and Sample B were prepared and the XRD analysis was performed thereon. A method for manufacturing Sample A and Sample B will be described below.

[0401]

An In-Sn-Zn-O film with a thickness of 100 nm was formed over a quartz substrate that had been subjected to dehydrogenation treatment.

15 [0402]

The In-Sn-Zn-O film was formed with a sputtering apparatus with a power of 100 W (DC) in an oxygen atmosphere. An In-Sn-Zn-O target of In:Sn:Zn = 1:1:1 [atomic ratio] was used as a target. Note that the substrate heating temperature in film formation was set at 200 °C. A sample manufactured in this manner was used as 20 Sample A.

[0403]

25 Next, a sample manufactured by a method similar to that of Sample A was subjected to heat treatment at 650 °C. As the heat treatment, heat treatment in a nitrogen atmosphere was first performed for one hour and heat treatment in an oxygen atmosphere was further performed for one hour without lowering the temperature. A sample manufactured in this manner was used as Sample B.

[0404]

FIG. 26 shows XRD spectra of Sample A and Sample B. No peak derived from crystal was observed in Sample A, whereas peaks derived from crystal were 30 observed when 2θ was around 35 deg. and at 37 deg. to 38 deg. in Sample B.

[0405]

As described above, by intentionally heating a substrate during deposition of an oxide semiconductor including In, Sn, and Zn as main components and/or by performing heat treatment after the deposition, characteristics of a transistor can be improved.

5 [0406]

These substrate heating and heat treatment have an effect of preventing hydrogen and a hydroxyl group, which are unfavorable impurities for an oxide semiconductor, from being included in the film or an effect of removing hydrogen and a hydroxyl group from the film. That is, an oxide semiconductor can be highly purified 10 by removing hydrogen serving as a donor impurity from the oxide semiconductor, whereby a normally-off transistor can be obtained. The high purification of an oxide semiconductor enables the off-state current of the transistor to be 1 aA/μm or lower. Here, the unit of the off-state current represents current per micrometer of a channel width.

15 [0407]

FIG. 27 shows a relation between the off-state current of a transistor and the inverse of substrate temperature (absolute temperature) at measurement. Here, for simplicity, the horizontal axis represents a value (1000/T) obtained by multiplying an inverse of substrate temperature at measurement by 1000.

20 [0408]

Specifically, as shown in FIG. 27, the off-state current can be 1 aA/μm (1 × 10<sup>-18</sup> A/μm) or lower, 100 zA/μm (1 × 10<sup>-19</sup> A/μm) or lower, and 1 zA/μm (1 × 10<sup>-21</sup> A/μm) or lower when the substrate temperature is 125 °C, 85 °C, and room temperature (27 °C), respectively. Preferably, the off-state current can be 0.1 aA/μm (1×10<sup>-19</sup> A/μm) or lower, 10 zA/μm (1×10<sup>-20</sup> A/μm) or lower, and 0.1 zA/μm (1×10<sup>-22</sup> A/μm) or lower at 125 °C, 85 °C, and room temperature, respectively.

[0409]

Note that in order to prevent hydrogen and moisture from being included in the oxide semiconductor film during formation thereof, it is preferable to increase the purity 30 of a sputtering gas by sufficiently suppressing leakage from the outside of a deposition chamber and degasification through an inner wall of the deposition chamber. For

example, a gas with a dew point of  $-70^{\circ}\text{C}$  or lower is preferably used as the sputtering gas in order to prevent moisture from being included in the film. In addition, it is preferable to use a target which is highly purified so as not to include impurities such as hydrogen and moisture. Although it is possible to remove moisture from a film of an oxide semiconductor including In, Sn, and Zn as main components by heat treatment, a film which does not include moisture originally is preferably formed because moisture is released from the oxide semiconductor including In, Sn, and Zn as main components at a higher temperature than from an oxide semiconductor including In, Ga, and Zn as main components.

10 [0410]

The relation between the substrate temperature and electric characteristics of a transistor of Sample B, on which heat treatment at  $650^{\circ}\text{C}$  was performed after formation of the oxide semiconductor film, was evaluated.

[0411]

15 The transistor used for the measurement has a channel length  $L$  of  $3\text{ }\mu\text{m}$ , a channel width  $W$  of  $10\text{ }\mu\text{m}$ ,  $L_{\text{ov}}$  of  $0\text{ }\mu\text{m}$ , and  $dW$  of  $0\text{ }\mu\text{m}$ . Note that  $V_{\text{d}}$  was set to  $10\text{ V}$ . Note that the substrate temperature was  $-40^{\circ}\text{C}$ ,  $-25^{\circ}\text{C}$ ,  $25^{\circ}\text{C}$ ,  $75^{\circ}\text{C}$ ,  $125^{\circ}\text{C}$ , and  $150^{\circ}\text{C}$ . Here, in a transistor, the width of a portion where a gate electrode overlaps with one of a pair of electrodes is referred to as  $L_{\text{ov}}$ , and the width of a portion of the 20 pair of electrodes, which does not overlap with an oxide semiconductor film, is referred to as  $dW$ .

[0412]

25 FIG. 24 shows the  $V_{\text{g}}$  dependence of  $I_{\text{d}}$  (a solid line) and field-effect mobility (a dotted line). FIG. 25A shows a relation between the substrate temperature and the threshold voltage, and FIG. 25B shows a relation between the substrate temperature and the field-effect mobility.

[0413]

30 From FIG. 25A, it is found that the threshold voltage gets lower as the substrate temperature increases. Note that the threshold voltage is decreased from  $1.09\text{ V}$  to  $-0.23\text{ V}$  in the range from  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ .

[0414]

From FIG. 25B, it is found that the field-effect mobility gets lower as the substrate temperature increases. Note that the field-effect mobility is decreased from  $36 \text{ cm}^2/\text{Vs}$  to  $32 \text{ cm}^2/\text{Vs}$  in the range from  $-40^\circ\text{C}$  to  $150^\circ\text{C}$ . Thus, it is found that variation in electric characteristics is small in the above temperature range.

5 [0415]

In a transistor in which such an oxide semiconductor including In, Sn, and Zn as main components is used as a channel formation region, a field-effect mobility of  $30 \text{ cm}^2/\text{Vsec}$  or higher, preferably  $40 \text{ cm}^2/\text{Vsec}$  or higher, further preferably  $60 \text{ cm}^2/\text{Vsec}$  or higher can be obtained with the off-state current maintained at  $1 \text{ aA}/\mu\text{m}$  or lower, 10 which can achieve on-state current needed for an LSI. For example, in an FET where  $L/W$  is  $33 \text{ nm}/40 \text{ nm}$ , an on-state current of  $12 \mu\text{A}$  or higher can flow when the gate voltage is  $2.7 \text{ V}$  and the drain voltage is  $1.0 \text{ V}$ . In addition, sufficient electric characteristics can be ensured in a temperature range needed for operation of a transistor. 15 With such characteristics, an integrated circuit having a novel function can be realized without decreasing the operation speed even when a transistor including an oxide semiconductor is also provided in an integrated circuit formed using a Si semiconductor.

[0416]

An example of a transistor in which an In-Sn-Zn-O film is used as an oxide 20 semiconductor film will be described below.

[0417]

FIGS. 28A and 28B are a top view and a cross-sectional view of a coplanar transistor having a top-gate top-contact structure. FIG. 28A is the top view of the transistor. FIG. 28B illustrates cross section A-B along dashed-dotted line A-B in FIG. 25 28A.

[0418]

The transistor illustrated in FIG. 28B includes a substrate 1200; a base insulating layer 1202 provided over the substrate 1200; a protective insulating film 1204 provided in the periphery of the base insulating layer 1202; an oxide semiconductor film 30 1206 that is provided over the base insulating layer 1202 and the protective insulating film 1204 and includes a high-resistance region 1206a and low-resistance regions

1206b; a gate insulating layer 1208 provided over the oxide semiconductor film 1206; a gate electrode 1210 provided to overlap with the oxide semiconductor film 1206 with the gate insulating layer 1208 provided therebetween; a sidewall insulating film 1212 provided in contact with a side surface of the gate electrode 1210; a pair of electrodes 5 1214 provided in contact with at least the low-resistance regions 1206b; an interlayer insulating film 1216 provided to cover at least the oxide semiconductor film 1206, the gate electrode 1210, and the pair of electrodes 1214; and a wiring 1218 provided to be connected to at least one of the pair of electrodes 1214 through an opening formed in the interlayer insulating film 1216.

10 [0419]

Although not illustrated, a protective film may be provided to cover the interlayer insulating film 1216 and the wiring 1218. With the protective film, a minute amount of leakage current generated by surface conduction of the interlayer insulating film 1216 can be reduced and thus the off-state current of the transistor can be reduced.

15 [0420]

Another example of a transistor in which an In-Sn-Zn-O film is used as an oxide semiconductor film will be described below.

[0421]

FIGS. 29A and 29B are a top view and a cross-sectional view illustrating a 20 structure of a transistor. FIG. 29A is the top view of the transistor. FIG. 29B is a cross-sectional view along dashed-dotted line A-B in FIG. 29A.

[0422]

The transistor illustrated in FIG. 29B includes a substrate 1600; a base insulating layer 1602 provided over the substrate 1600; an oxide semiconductor film 25 1606 provided over the base insulating layer 1602; a pair of electrodes 1614 in contact with the oxide semiconductor film 1606; a gate insulating layer 1608 provided over the oxide semiconductor film 1606 and the pair of electrodes 1614; a gate electrode 1610 provided to overlap with the oxide semiconductor film 1606 with the gate insulating layer 1608 provided therebetween; an interlayer insulating film 1616 provided to cover 30 the gate insulating layer 1608 and the gate electrode 1610; wirings 1618 connected to the pair of electrodes 1614 through openings formed in the interlayer insulating film 1616; and a protective film 1620 provided to cover the interlayer insulating film 1616

and the wirings 1618.

[0423]

As the substrate 1600, a glass substrate can be used. As the base insulating layer 1602, a silicon oxide film can be used. As the oxide semiconductor film 1606, 5 an In-Sn-Zn-O film can be used. As the pair of electrodes 1614, a tungsten film can be used. As the gate insulating layer 1608, a silicon oxide film can be used. The gate electrode 1610 can have a stacked structure of a tantalum nitride film and a tungsten film. The interlayer insulating film 1616 can have a stacked structure of a silicon oxynitride film and a polyimide film. The wirings 1618 can each have a stacked 10 structure in which a titanium film, an aluminum film, and a titanium film are formed in this order. As the protective film 1620, a polyimide film can be used.

[0424]

Note that in the transistor having the structure illustrated in FIG. 29A, the width of a portion where the gate electrode 1610 overlaps with one of the pair of 15 electrodes 1614 is referred to as  $L_{ov}$ . Similarly, the width of a portion of the pair of electrodes 1614, which does not overlap with the oxide semiconductor film 1606, is referred to as  $dW$ .

[0425]

(Embodiment 8)

20 In this embodiment, examples of electronic devices each including the semiconductor device in the above embodiment are described.

[0426]

Examples of structures of electronic devices in this embodiment are described with reference to FIGS. 12A to 12D.

25 [0427]

The electronic device illustrated in FIG. 12A is an example of a personal digital assistant. The personal digital assistant illustrated in FIG. 12A includes a housing 1001a and a display portion 1002a provided in the housing 1001a.

[0428]

30 Note that a side surface 1003a of the housing 1001a may be provided with a connection terminal for connecting the personal digital assistant to an external device and/or a button for operating the personal digital assistant illustrated in FIG. 12A.

[0429]

The personal digital assistant illustrated in FIG. 12A includes a CPU, a memory circuit, an interface for transmitting and receiving a signal between the external device and each of the CPU and the memory circuit, and an antenna for transmitting and 5 receiving a signal to and from the external device, in the housing 1001a.

[0430]

The personal digital assistant illustrated in FIG. 12A serves as one or more of a telephone set, an e-book reader, a personal computer, and a game machine, for example.

[0431]

10 The electronic device illustrated in FIG. 12B is an example of a folding personal digital assistant. The personal digital assistant illustrated in FIG. 12B includes a housing 1001b, a display portion 1002b provided in the housing 1001b, a housing 1004, a display portion 1005 provided in the housing 1004, and a hinge 1006 for connecting the housing 1001b and the housing 1004.

15 [0432]

In the personal digital assistant illustrated in FIG. 12B, the housing 1001b can be stacked on the housing 1004 by moving the housing 1001b or the housing 1004 with the hinge 1006.

[0433]

20 Note that a side surface 1003b of the housing 1001b or a side surface 1007 of the housing 1004 may be provided with a connection terminal for connecting the personal digital assistant to an external device and/or a button for operating the personal digital assistant illustrated in FIG. 12B.

[0434]

25 The display portion 1002b and the display portion 1005 may display different images or one image. Note that the display portion 1005 is not necessarily provided, and a keyboard which is an input device may be provided instead of the display portion 1005.

[0435]

30 The personal digital assistant illustrated in FIG. 12B includes a CPU, a memory circuit, and an interface for transmitting and receiving a signal between the external device and each of the CPU and the memory circuit in the housing 1001b or the

housing 1004. Note that the personal digital assistant illustrated in FIG. 12B may include an antenna for transmitting and receiving a signal to and from the external device.

[0436]

5 The personal digital assistant illustrated in FIG. 12B serves as one or more of a telephone set, an e-book reader, a personal computer, and a game machine, for example.

[0437]

10 The electronic device illustrated in FIG. 12C is an example of a stationary information terminal. The stationary information terminal illustrated in FIG. 12C includes a housing 1001c and a display portion 1002c provided in the housing 1001c.

[0438]

Note that the display portion 1002c can be provided on a deck portion 1008 in the housing 1001c.

[0439]

15 The stationary information terminal illustrated in FIG. 12C includes a CPU, a memory circuit, and an interface for transmitting and receiving a signal between the external device and each of the CPU and the memory circuit in the housing 1001c. Note that the stationary information terminal illustrated in FIG. 12C may include an antenna for transmitting and receiving a signal to and from the external device.

20 [0440]

Further, a side surface 1003c of the housing 1001c in the stationary information terminal illustrated in FIG. 12C may be provided with one or more of a ticket output portion that outputs a ticket or the like, a coin slot, and a bill slot.

[0441]

25 The stationary information terminal illustrated in FIG. 12C serves as an automated teller machine, an information communication terminal (also referred to as a multimedia station) for ordering a ticket or the like, or a game machine, for example.

[0442]

30 The electronic device illustrated in FIG. 12D is an example of a stationary information terminal. The stationary information terminal illustrated in FIG. 12D includes a housing 1001d and a display portion 1002d provided in the housing 1001d. Note that a support for supporting the housing 1001d may also be provided.

[0443]

Note that a side surface 1003d of the housing 1001d may be provided with a connection terminal for connecting the stationary information terminal to an external device and/or a button for operating the stationary information terminal illustrated in

5 FIG. 12D.

[0444]

The stationary information terminal illustrated in FIG. 12D may include a CPU, a memory circuit, and an interface for transmitting and receiving a signal between the external device and each of the CPU and the memory circuit in the housing 1001d.

10 Note that the stationary information terminal illustrated in FIG. 12D may include an antenna for transmitting and receiving a signal to and from the external device.

[0445]

The stationary information terminal illustrated in FIG. 12D serves as a digital photo frame, a monitor, or a television set, for example.

15 [0446]

The semiconductor device in the above embodiment is used as a CPU in an electronic device, for example. For example, the semiconductor device in the above embodiment is used as one of the CPUs in the electronic devices illustrated in FIGS. 12A to 12D.

20 [0447]

As described with reference to FIGS. 12A to 12D, the examples of the electronic devices in this embodiment each include a CPU which includes the semiconductor device in the above embodiment.

[0448]

25 With such a structure, even when power is not supplied, data in an electronic device can be retained for a certain period. Thus, a time after the supply of the power supply voltage starts until a normal operation starts can be shortened and power consumption can be reduced.

30 EXPLANATION OF REFERENCE

[0449]

100a: transistor, 100b: transistor, 101: semiconductor layer, 102: insulating

layer, 103\_a: region, 103\_b1: region, 103\_b2: region, 103\_c: region, 104: insulating layer, 105: conductive layer, 106: insulating layer, 107: semiconductor layer, 107\_a: region, 107\_b1: region, 107\_b2: region, 108a: conductive layer, 108b: conductive layer, 108c: conductive layer, 108d: conductive layer, 108e: conductive layer, 109: insulating layer, 110: conductive layer, 111a: opening, 111b: opening, 111c: opening, 200a: transistor, 200b: transistor, 200c: transistor, 201: semiconductor layer, 201\_a: region, 201\_b: region, 202: insulating layer, 203a\_a: region, 203a\_b1: region, 203a\_b2: region, 203b: semiconductor layer, 203b\_a: region, 203b\_b1: region, 203b\_b2: region, 204: insulating layer, 205a: conductive layer, 205b: conductive layer, 206: insulating layer, 207: semiconductor layer, 207\_a: region, 207\_b1: region, 207\_b2: region, 208a: conductive layer, 208b: conductive layer, 208c: conductive layer, 208d: conductive layer, 208e: conductive layer, 208f: conductive layer, 208g: conductive layer, 208h: conductive layer, 209: insulating layer, 210: conductive layer, 300a: transistor, 300b, transistor, 301: semiconductor layer, 301a: region, 302: insulating layer, 303: semiconductor layer, 303\_a: region, 303\_b1: region, 303\_b2: region, 303\_c: region, 304: insulating layer, 305: conductive layer, 306: insulating layer, 307: semiconductor layer, 307\_a: region, 307\_b1: region, 307\_b2: region, 308a: conductive layer; 308b: conductive layer; 308c: conductive layer; 308d: conductive layer; 309: insulating layer; 310a: conductive layer; 310b: conductive layer; 501: bus interface; 502: control unit; 503: cache memory; 504: register; 505: instruction decoder; 506: arithmetic logic unit; 611: analog switch; 612: NOT gate; 613: transistor; 614: capacitor; 615: NOT gate; 616: NAND gate; 617: clocked inverter; 618: analog switch; 619: NOT gate; 620: clocked NAND gate; 621: NOT gate; 651: larch circuit; 652: larch circuit; 691: period; 692: period; 693: period; 701: transistor; 702: transistor; 703: memory circuit; 704: capacitor; 705: NOT gate; 706: switching circuit; 707: memory circuit; 751: transistor; 752: transistor; 753: capacitor; 1001a: housing; 1001b: housing; 1001c: housing; 1001d: housing; 1002a: display portion; 1002b: display portion; 1002c: display portion; 1002d: display portion; 1003a: side surface; 1003b: side surface; 1003c: side surface; 1003d: side surface; 1004: housing; 1005: display portion; 1006: hinge; 1007: side surface; 1008: deck portion; 1200: substrate; 1202: base insulating layer; 1204: protective insulating film; 1206: oxide semiconductor film; 1206a: high-resistance region; 1206b: low-resistance region; 1208: gate insulating layer; 1210: gate electrode; 1212: sidewall

insulating film; 1214: electrode; 1216: interlayer insulating film; 1218: wiring; 1600: substrate; 1602: base insulating layer; 1606: oxide semiconductor film; 1608: gate insulating layer; 1610: gate electrode; 1614: wiring; 1616: interlayer insulating film; 1618: wiring; 1620: protective film; 2101: base insulating layer; 2102: insulator; 2103a: 5 semiconductor region; 2103b: semiconductor region; 2103c: semiconductor region; 2104: gate insulating layer; 2105: gate; 2106a: sidewall insulator; 2106b: sidewall insulator; 2107: insulator; 2108a: source; 2108b: drain;

This application is based on Japanese Patent Application serial No. 10 2011-015871 filed with Japan Patent Office on January 28, 2011 and Japanese Patent Application serial No. 2011-108880 filed with Japan Patent Office on May 14, 2011, the entire contents of which are hereby incorporated by reference.

## CLAIMS

1. A semiconductor device comprising:

5 a bus interface;

a control unit;

a cache memory which is controlled by the control unit and temporarily retains data during arithmetic processing;

*N* registers, wherein *N* is a natural number greater than or equal to 3;

10 an instruction decoder which translates an instruction signal read from at least one of the *N* registers and outputs the translated instruction signal to the control unit; and

an arithmetic logic unit which is controlled by the control unit and performs arithmetic processing,

15 wherein the *N* registers comprises a plurality of unit memory devices,

wherein the plurality of unit memory devices each comprise a first transistor and a second transistor,

wherein the first transistor comprises:

a first semiconductor layer comprising:

20 a first region having a first conductivity type;

a second region having the first conductivity type;

a third region in contact with the first region and the second region; and

a fourth region having a second conductivity type opposite to

25 the first conductivity type and being in contact with the third region;

a first electrode over the third region of the first semiconductor layer with an first insulating layer provided therebetween;

a second electrode over the first insulating layer, wherein the second electrode is electrically connected to the first region of the first semiconductor layer;

30 a third electrode over the first insulating layer, wherein the third electrode is electrically connected to the second region of the first semiconductor layer; and

a fourth electrode over the first insulating layer and electrically connected to the fourth region, and

wherein the second transistor comprises a second semiconductor layer comprising oxide semiconductor.

5

2. The semiconductor device according to Claims 1, wherein the oxide semiconductor comprises indium, gallium, and zinc.

10 3. The semiconductor device according to Claim 1, wherein the fourth region of the first semiconductor layer overlaps with the second semiconductor layer.

4. The semiconductor device according to Claim 1, further comprising a second insulating layer over the first insulating layer, wherein the second semiconductor layer is provided over the second insulating layer.

15

5. The semiconductor device according to Claim 1, wherein the first semiconductor layer is provided over a silicon substrate.

20 6. The semiconductor device according to Claim 1, wherein the first semiconductor layer comprises single crystal silicon.

25 7. An electronic device comprising a CPU comprising the semiconductor device according to Claim 1, wherein the electronic device is one selected from the group consisting of a telephone set, an e-book reader, a personal computer, and a game machine.

8. A semiconductor device comprising:

a first memory circuit comprising:

a first transistor comprising:

30 a first gate;

a first source; and

a first drain;

a second transistor comprising:

    a second gate electrically connected to one of the first source

and the first drain;

    a second source;

    a second drain; and

    a first terminal;

a first capacitor comprising:

    a second terminal electrically connected to the one of the first

source and the first drain and the second gate; and

10                   a third terminal electrically connected to one of the second  
source and the second drain;

    a third transistor comprising:

        a third gate;

        a third source; and

15                   a third drain, wherein one of the third source and the third drain is  
electrically connected to the other of the second source and the second drain;

    a fourth transistor comprising:

        a fourth gate electrically connected to the third gate;

        a fourth source; and

20                   a fourth drain, wherein one of the fourth source and the fourth drain is  
electrically connected to the other of the third source and the third drain;

    a second capacitor comprising:

        a fourth terminal electrically connected to the other of the third source  
and the third drain and the one of the fourth source and the fourth drain; and

25                   a fifth terminal electrically connected to the one of the second source  
and the second drain and the third terminal of the first capacitor;

    a NOT gate comprising:

        a first input terminal electrically connected to the other of the third  
source and the third drain, the one of the fourth source and the fourth drain, and the  
30                   fourth terminal of the second capacitor; and

        a first output terminal;

    a switching circuit comprising:

a second input terminal electrically connected to the other of the first source and the first drain;

a third input terminal electrically connected to the first output terminal of the NOT gate; and

5 a second output terminal;

a second memory circuit comprising:

a fourth input terminal electrically connected to the second output terminal of the switching circuit; and

10 a third output terminal electrically connected to the second input terminal of the switching circuit and the other of the first source and the first drain,

wherein:

the second transistor comprises:

a first semiconductor layer comprising:

a first region having a first conductivity type;

15 a second region having the first conductivity type;

a third region in contact with the first region and the second region; and

a fourth region having a second conductivity type opposite to the first conductivity type and being in contact with the third region;

20 the second gate over the third region of the first semiconductor layer with an first insulating layer provided therebetween;

the second source over the first insulating layer, wherein the second source is electrically connected to the first region of the first semiconductor layer; and

25 the second drain over the first insulating layer, wherein the second drain is electrically connected to the second region of the first semiconductor layer;

the first transistor comprises:

a second semiconductor layer comprising oxide semiconductor, wherein the second semiconductor layer is provided over the first insulating layer;

the first source electrically connected to the second semiconductor

30 layer;

the first drain electrically connected to the second semiconductor layer; and

the first gate over the second semiconductor layer with a second insulating layer provided therebetween, and

the first terminal is provided over the first insulating layer and electrically connected to the fourth region.

5

9. The semiconductor device according to Claim 8, wherein the oxide semiconductor comprises indium, gallium, and zinc.

10. The semiconductor device according to Claim 8, wherein the fourth region of the first semiconductor layer overlaps with the first gate.

11. The semiconductor device according to Claim 8, further comprising a third insulating layer over the first insulating layer, wherein the second semiconductor layer, the first source, the first drain, the first gate are provided over the third insulating layer.

15

12. The semiconductor device according to Claim 8, wherein the first semiconductor layer comprises single crystal silicon.

13. The semiconductor device according to Claim 8, wherein the first source and the first drain are provided on the second semiconductor layer.

20  
25 14. An electronic device comprising a CPU comprising the semiconductor device according to Claim 8, wherein the electronic device is one selected from the group consisting of a telephone set, an e-book reader, a personal computer, and a game machine.

15. A semiconductor device comprising:

a first transistor comprising:

a first semiconductor layer comprising:

30

a first region having a first conductivity type;

a second region having the first conductivity type;

a third region in contact with the first region and the second

region; and

a fourth region having a second conductivity type opposite to the first conductivity type and being in contact with the third region;

5 a first electrode over the third region of the first semiconductor layer with an first insulating layer provided therebetween;

a second electrode over the first insulating layer, wherein the second electrode is electrically connected to the first region of the first semiconductor layer;

a third electrode over the first insulating layer, wherein the third electrode is electrically connected to the second region of the first semiconductor layer;

10 and

a fourth electrode over the first insulating layer and electrically connected to the fourth region;

15 a second transistor comprising a second semiconductor layer comprising oxide semiconductor, wherein the second semiconductor layer is provided over the first insulating layer.

16. The semiconductor device according to Claim 15, wherein the oxide semiconductor comprises indium, gallium, and zinc.

20 17. The semiconductor device according to Claim 15, wherein the fourth region of the first semiconductor layer overlaps with the second semiconductor layer.

18. The semiconductor device according to Claim 15, wherein the first semiconductor layer is provided over a silicon substrate.

25

19. The semiconductor device according to Claim 15, wherein the first semiconductor layer comprises single crystal silicon.

30 20. An electronic device comprising a CPU comprising the semiconductor device according to Claim 15, wherein the electronic device is one selected from the group consisting of a telephone set, an e-book reader, a personal computer, and a game machine.

21. A semiconductor device comprising:

a first transistor comprising:

a first semiconductor layer over a second semiconductor layer with a

5 first insulating layer provided therebetween, wherein the first semiconductor layer comprises:

a first region having a first conductivity type;

a second region having the first conductivity type; and

a third region in contact with the first region and the second

10 region; and

a first electrode over the third region of the first semiconductor layer with an second insulating layer provided therebetween;

a second electrode over the second insulating layer, wherein the second electrode is electrically connected to the first region of the first semiconductor

15 layer;

a third electrode over the second insulating layer, wherein the third electrode is electrically connected to the second region of the first semiconductor layer; and

20 a fourth electrode over the second insulating layer and electrically connected to the second semiconductor layer;

a second transistor comprising a third semiconductor layer comprising oxide semiconductor, wherein the third semiconductor layer is provided over the second insulating layer,

25 wherein the second semiconductor layer has a second conductivity type opposite to the first conductivity type.

22. The semiconductor device according to Claim 21, wherein the oxide semiconductor comprises indium, gallium, and zinc.

30 23. The semiconductor device according to Claim 21, wherein the second semiconductor layer overlaps with the third semiconductor layer.

24. The semiconductor device according to Claim 21, wherein the second semiconductor layer is a silicon substrate.

25. The semiconductor device according to Claim 21, wherein the first  
5 semiconductor layer comprises single crystal silicon.

26. An electronic device comprising a CPU comprising the semiconductor  
device according to Claim 21, wherein the electronic device is one selected from the  
group consisting of a telephone set, an e-book reader, a personal computer, and a game  
10 machine.

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FIG. 1A

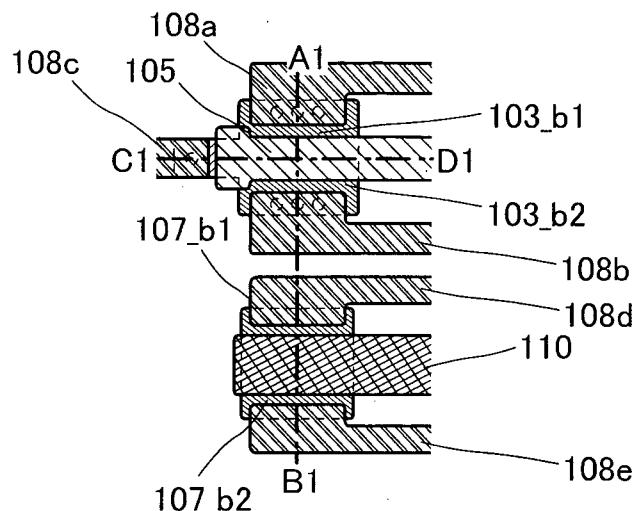


FIG. 1B

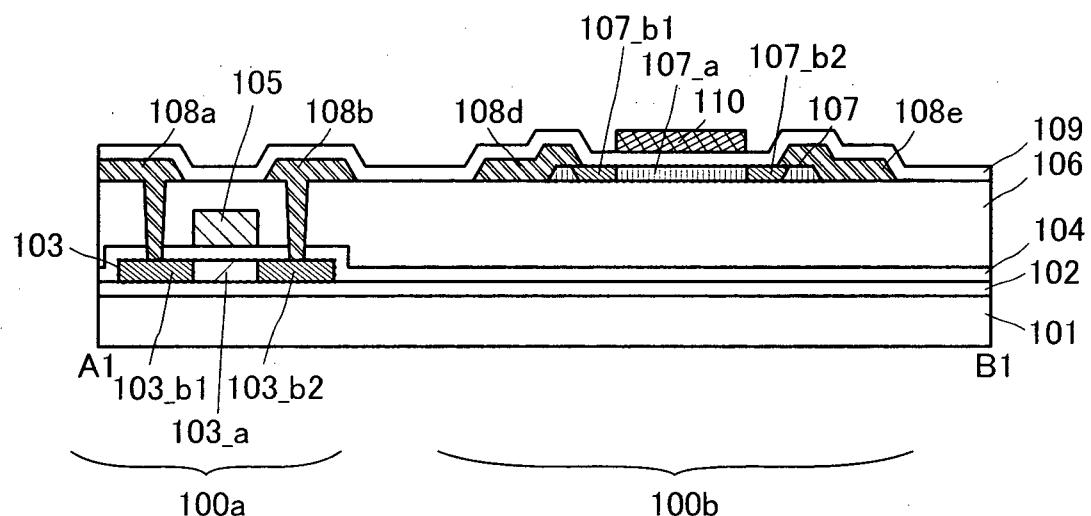


FIG. 1C

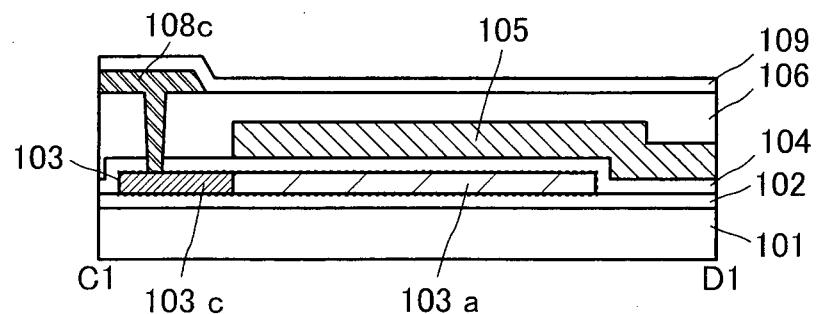


FIG. 2A1

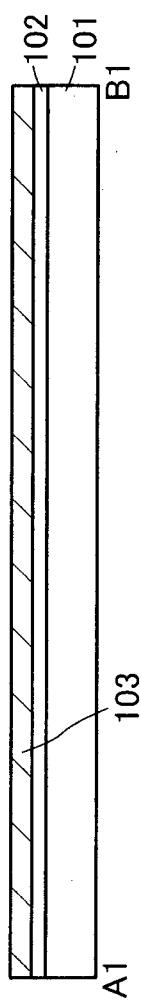


FIG. 2A2

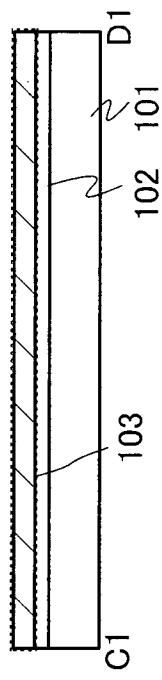


FIG. 2B1

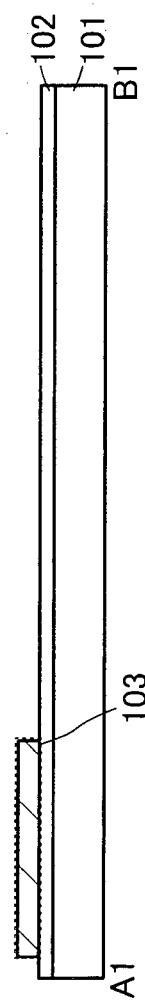


FIG. 2B2

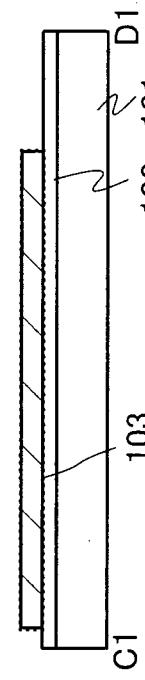


FIG. 2C1

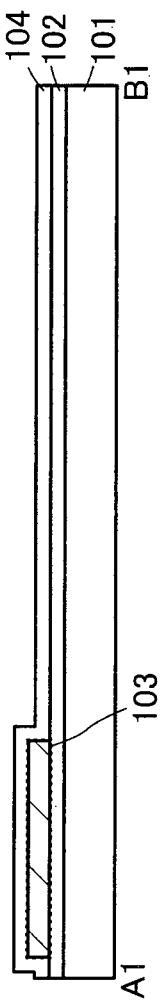


FIG. 2C2

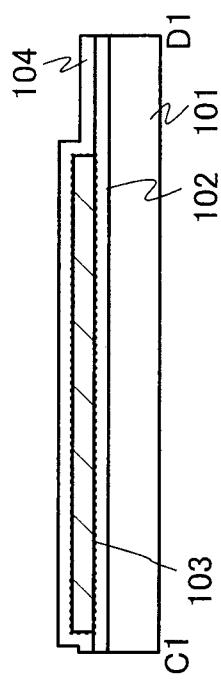


FIG. 3A1

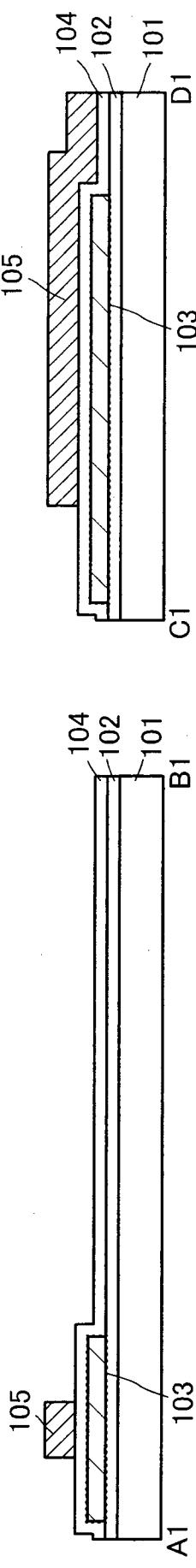


FIG. 3A2

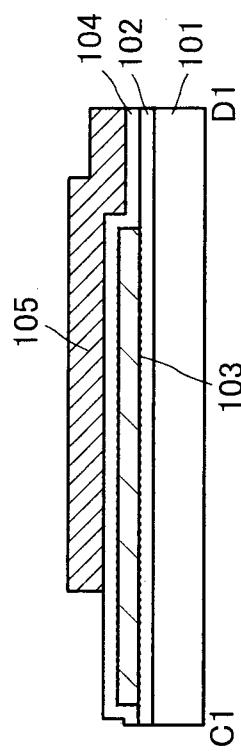


FIG. 3B1

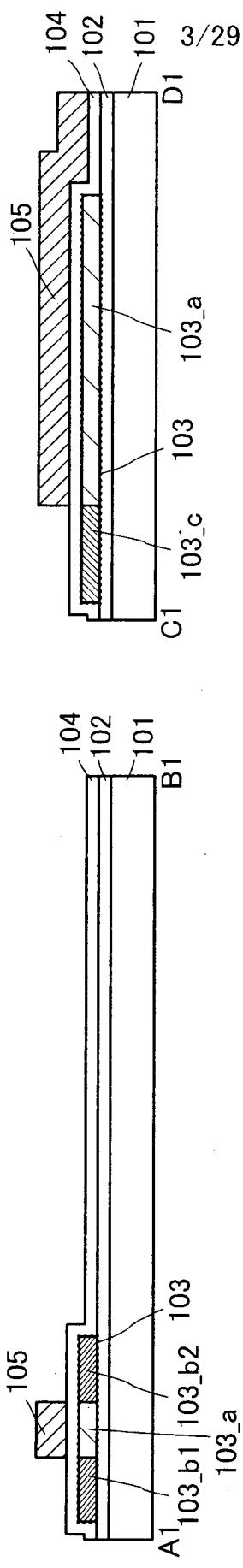


FIG. 3B2

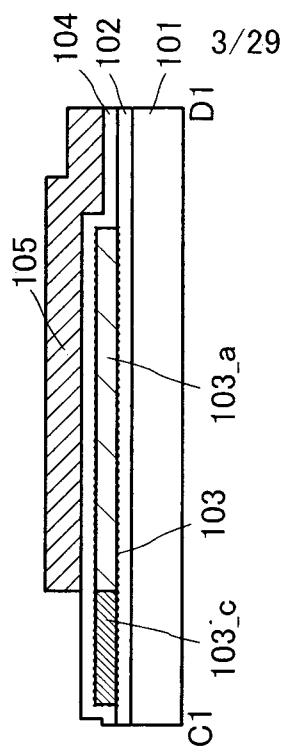


FIG. 3C1

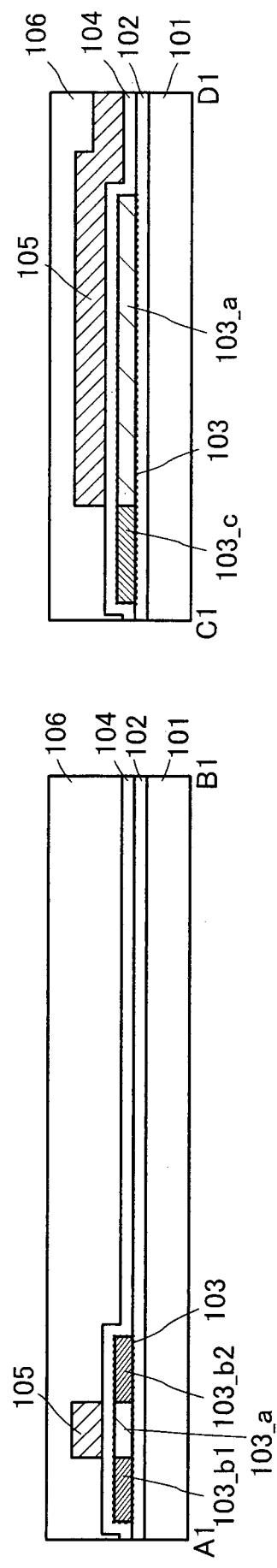
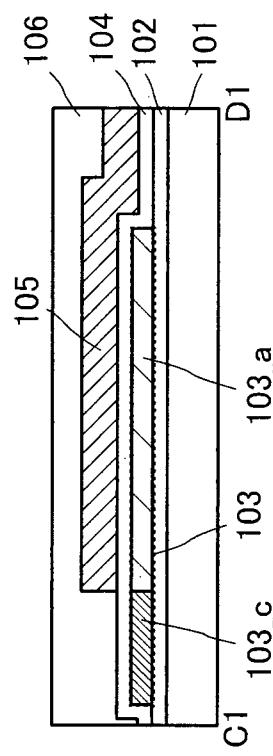


FIG. 3C2



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FIG. 4A1

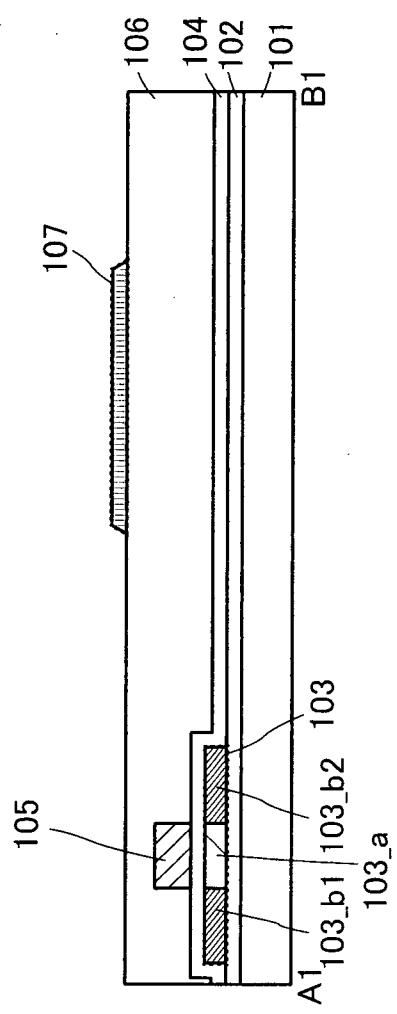
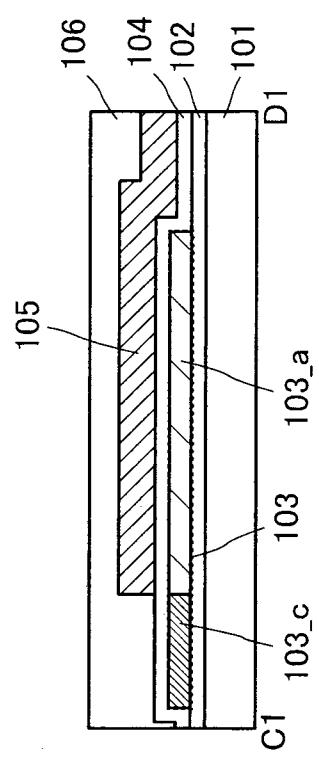


FIG. 4A2



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FIG. 4B1

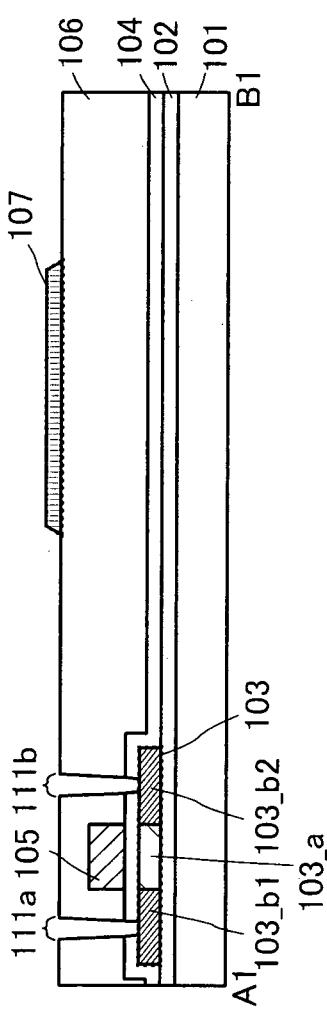


FIG. 4B2

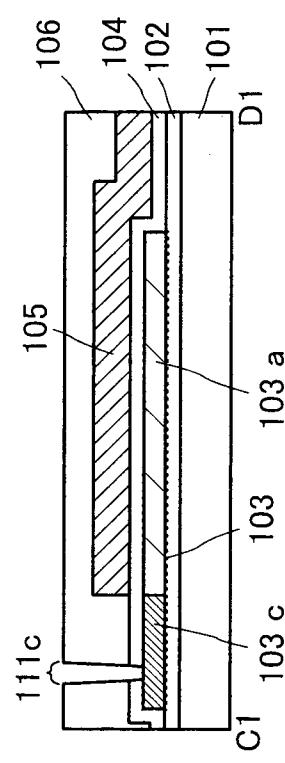


FIG. 5A1

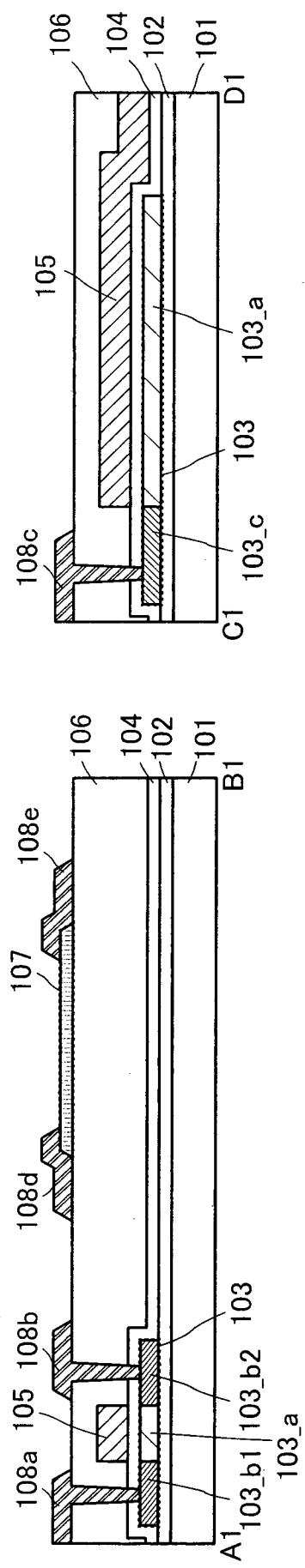
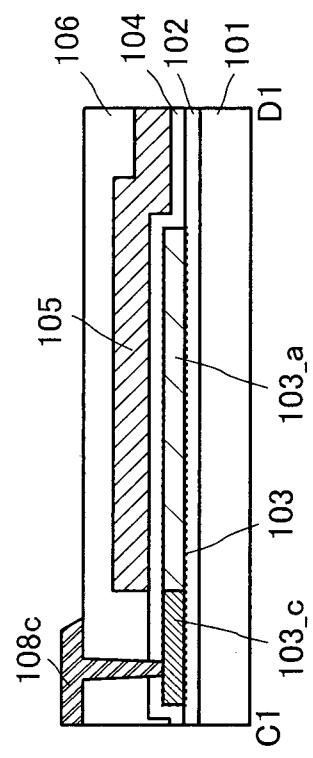


FIG. 5A2



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FIG. 5B2

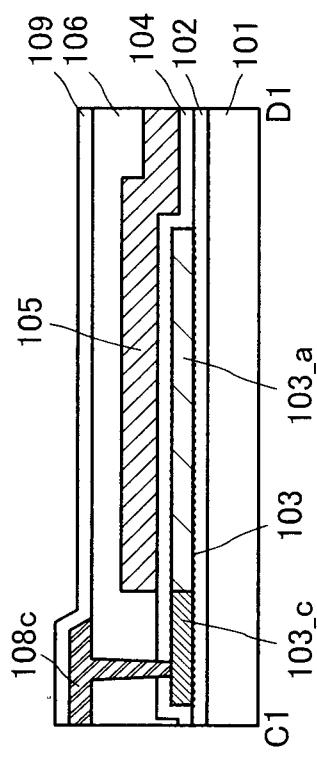


FIG. 5B1

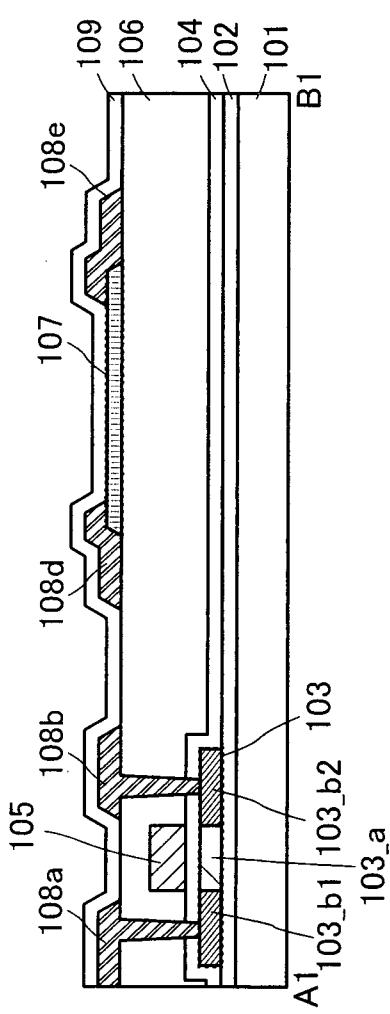


FIG. 6A1

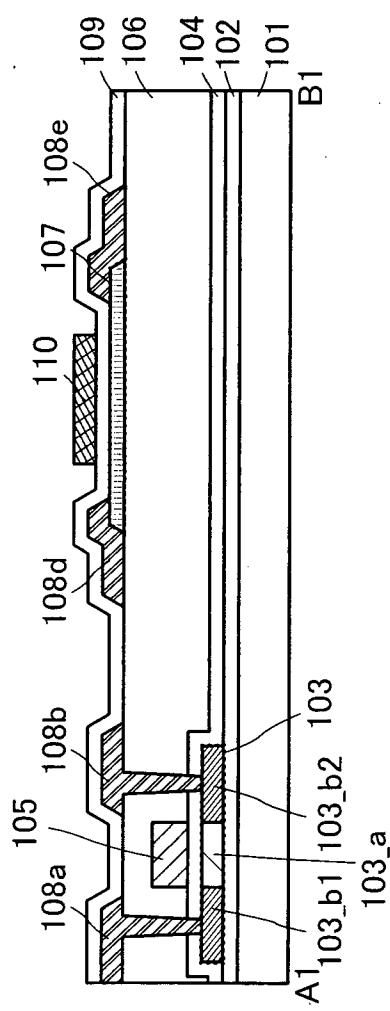
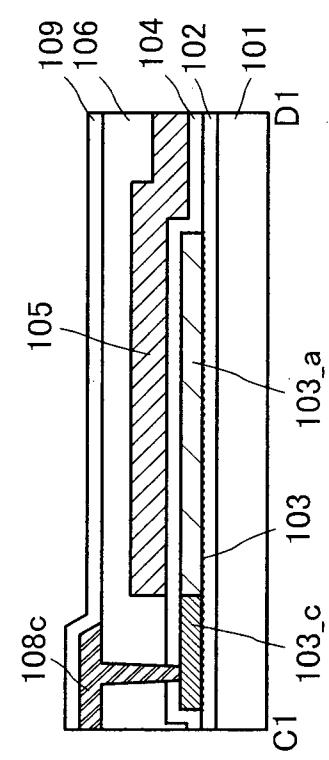


FIG. 6A2



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FIG. 6B1

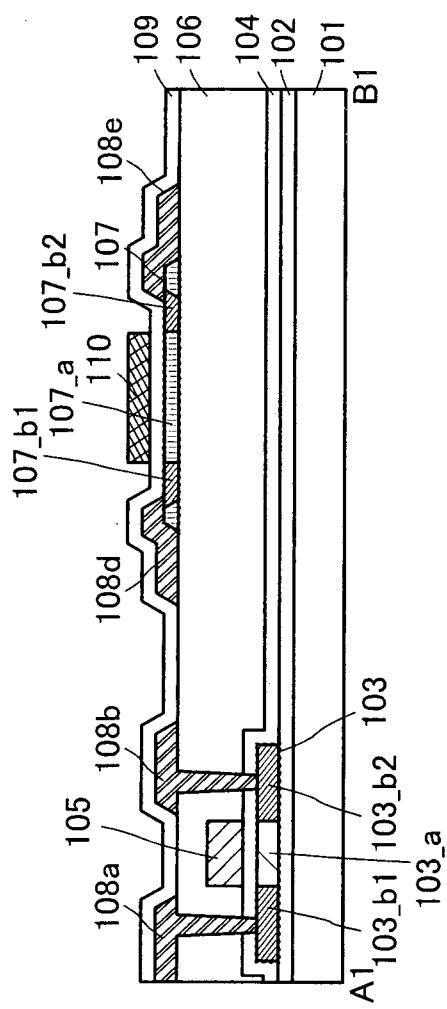


FIG. 6B2

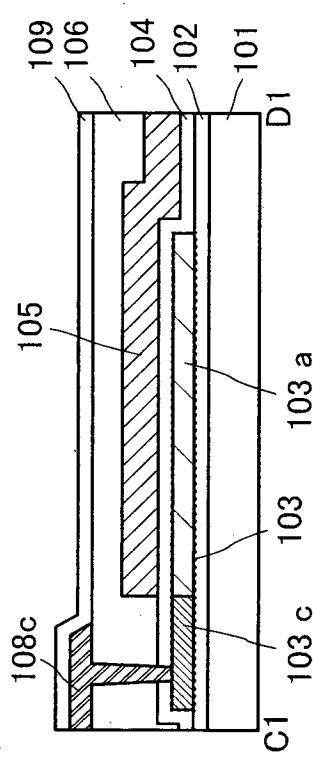


FIG. 7A

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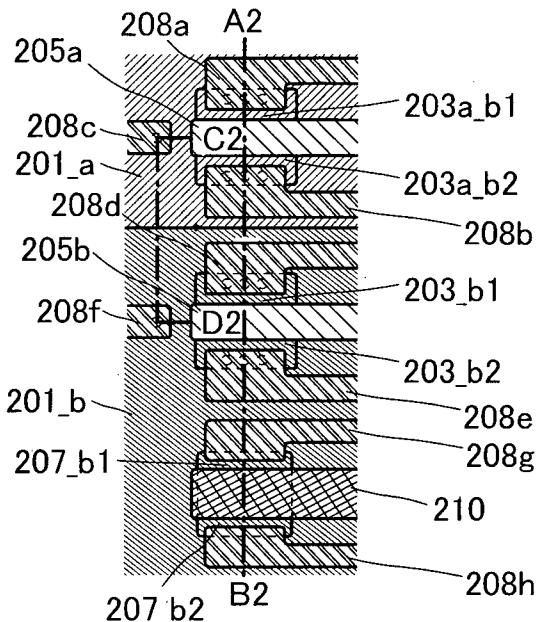


FIG. 7B

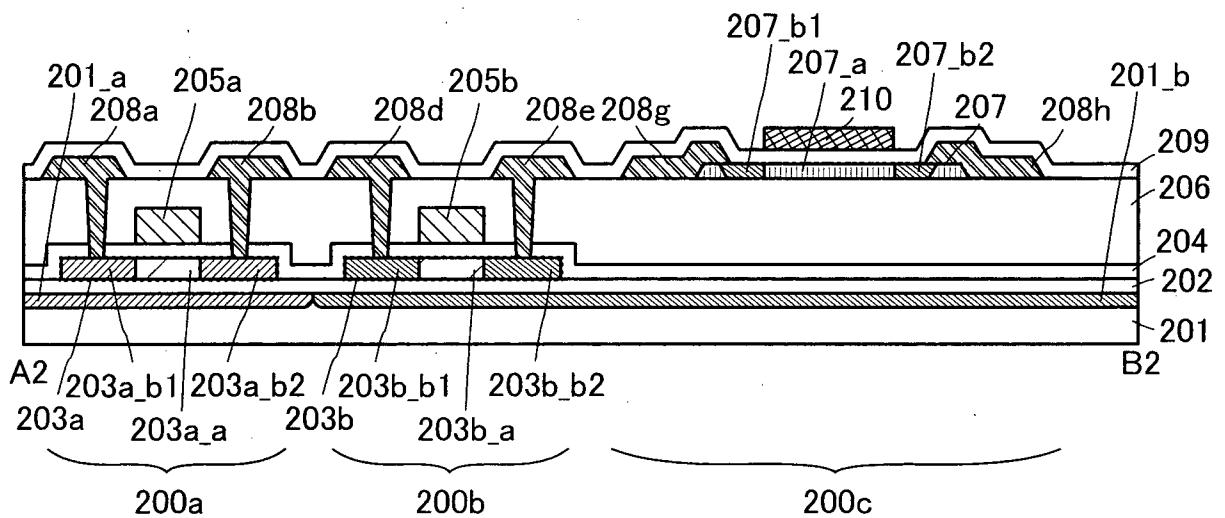
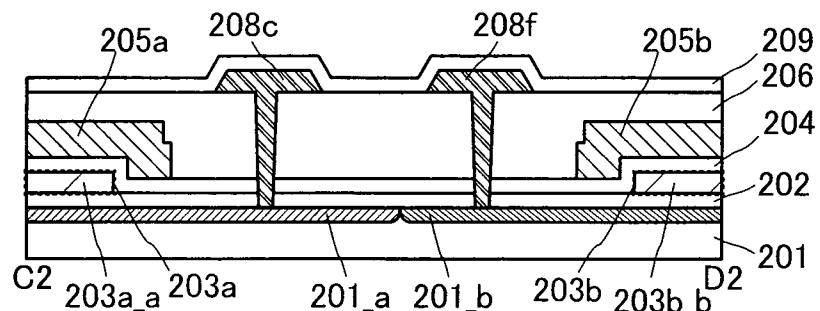


FIG. 7C



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FIG. 8A

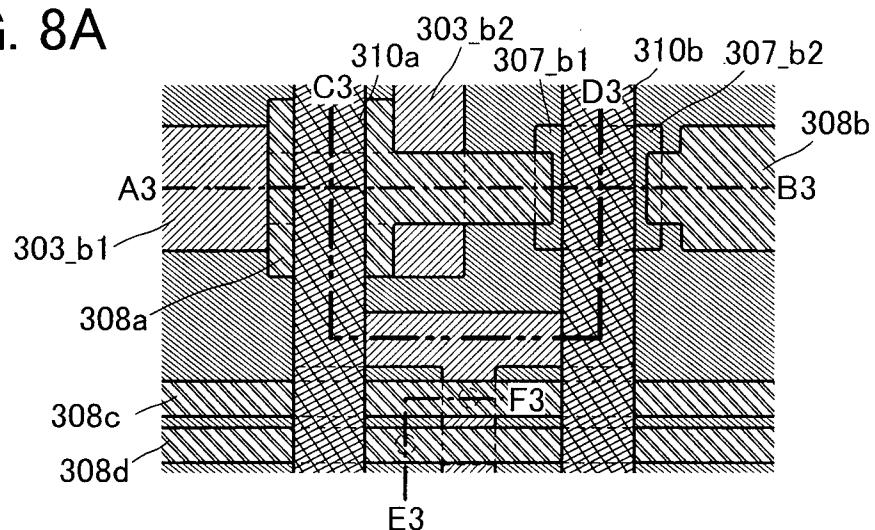


FIG. 8B

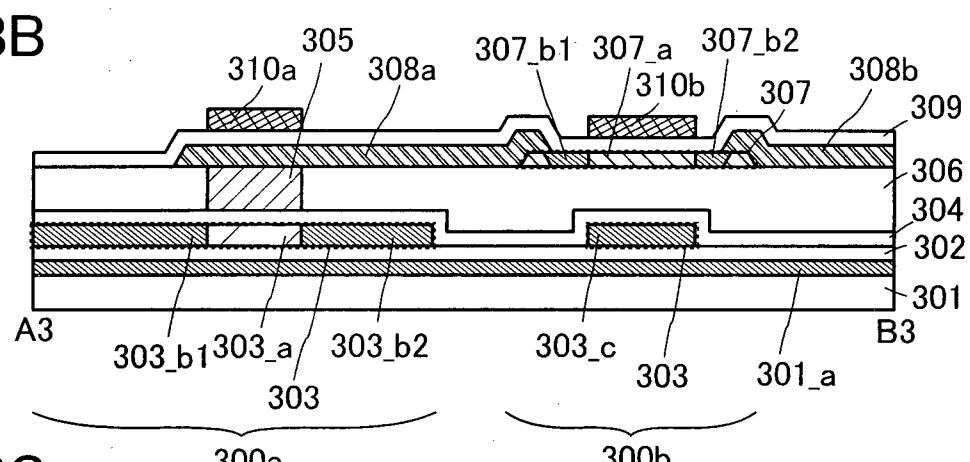


FIG. 8C

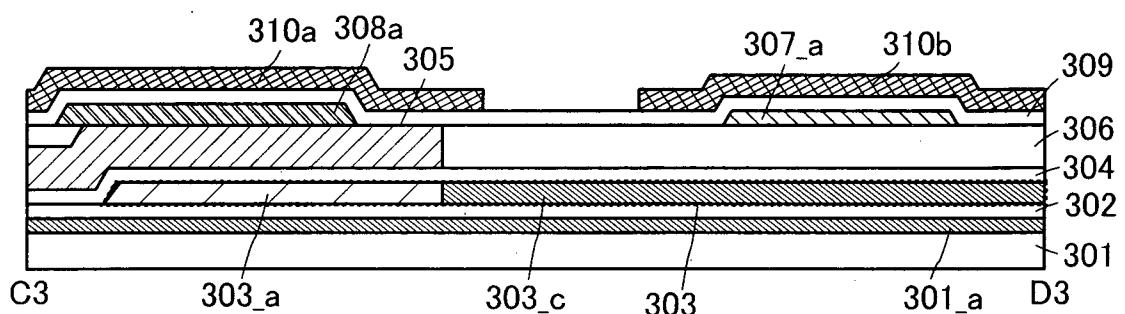


FIG. 8D

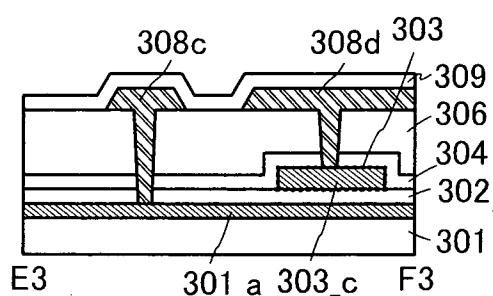
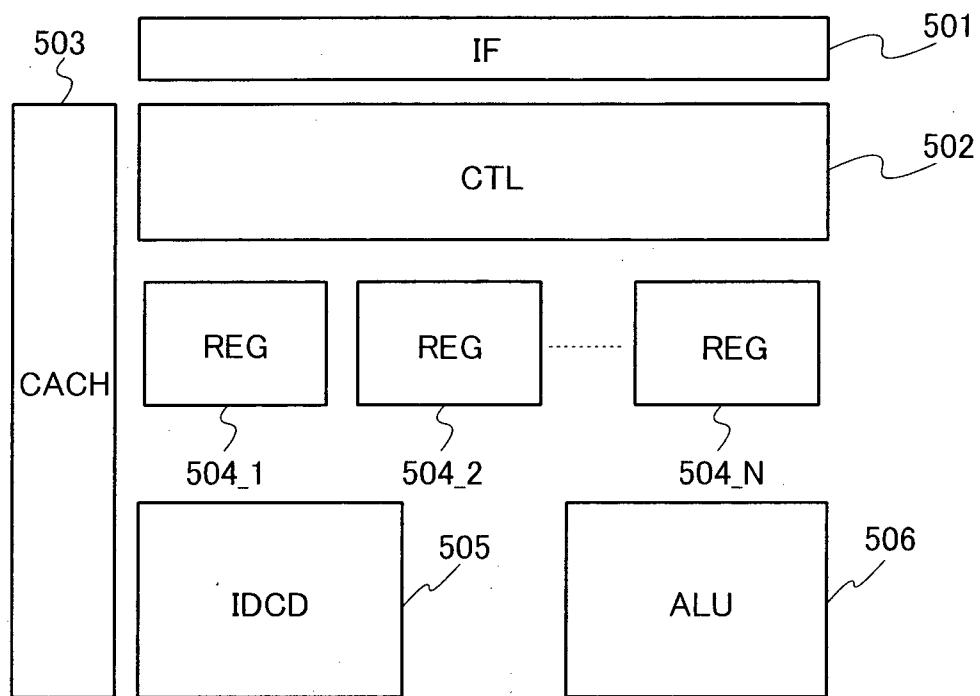


FIG. 9

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FIG. 10A

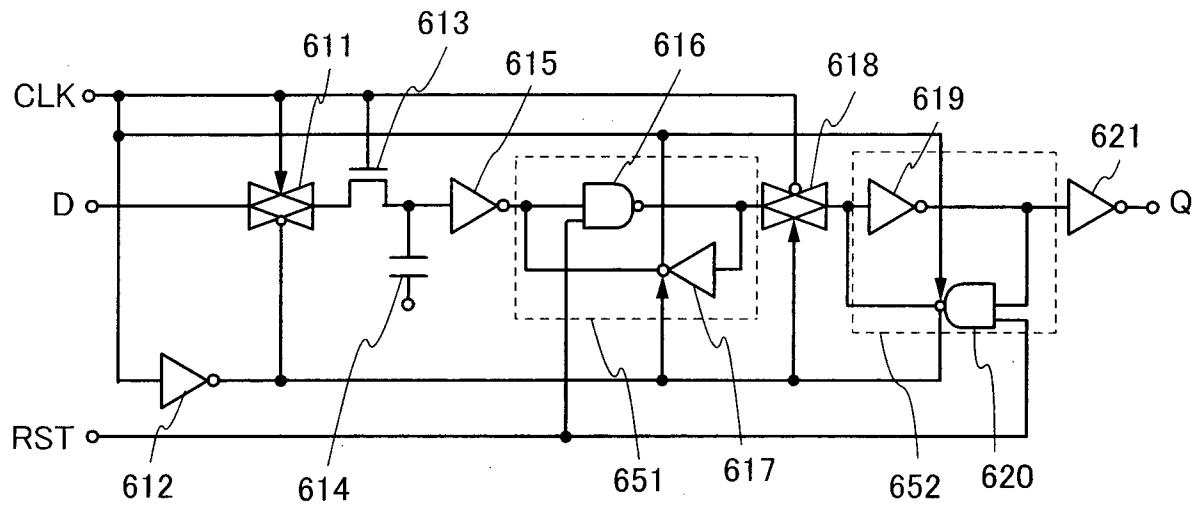
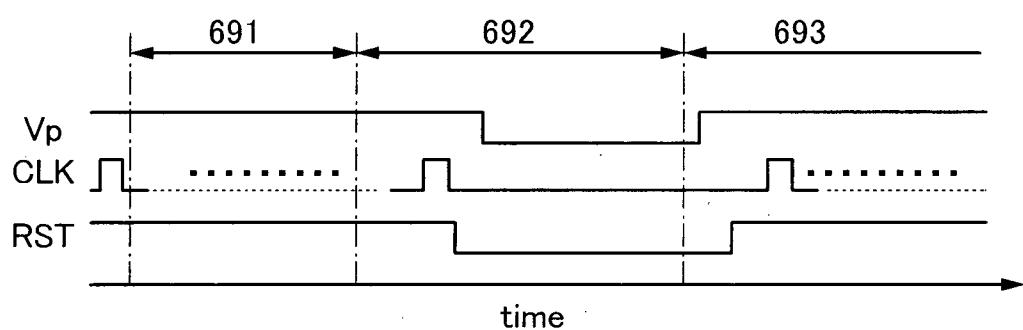


FIG. 10B



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FIG. 11A

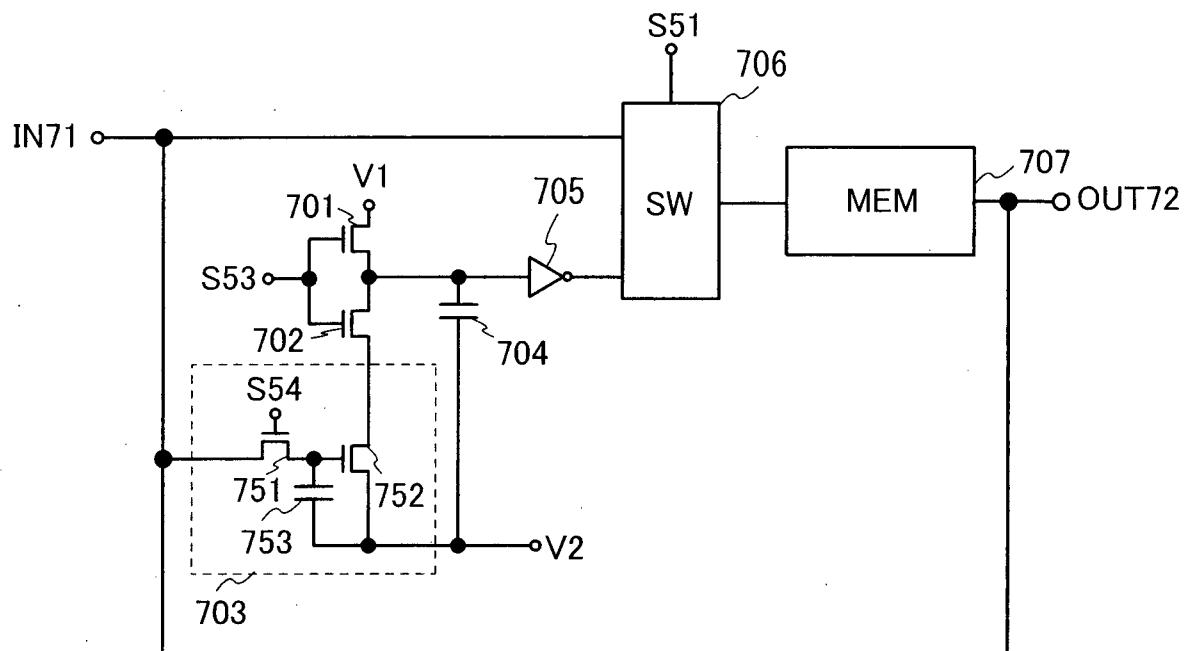
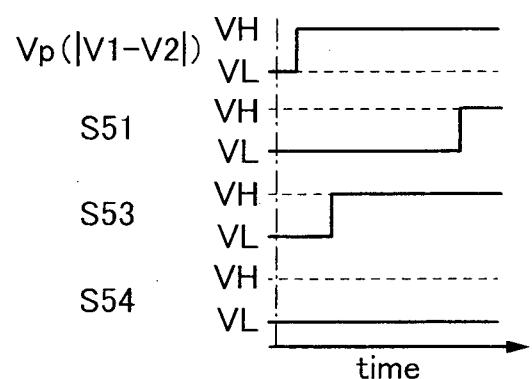
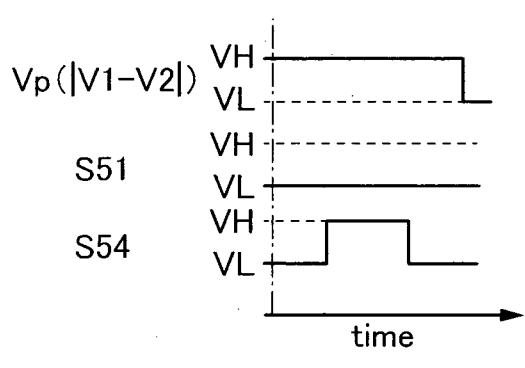


FIG. 11B

FIG. 11C

STOP

## RESTART



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FIG. 12A

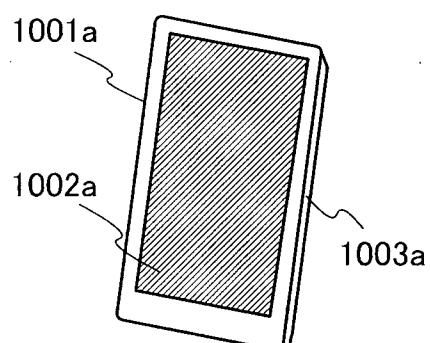


FIG. 12C

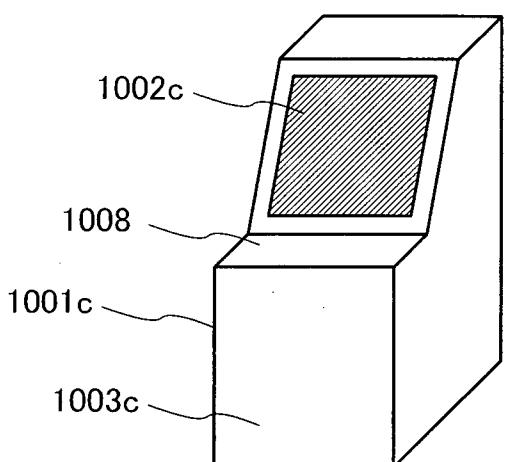


FIG. 12B

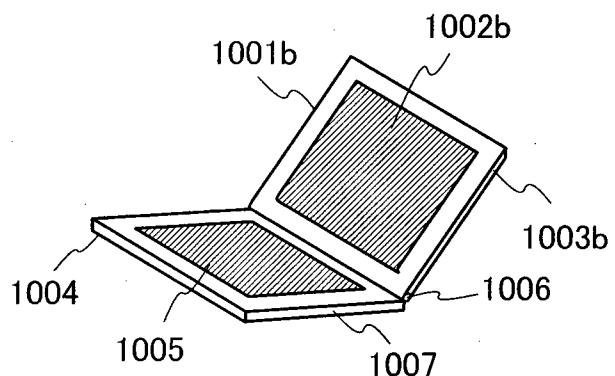
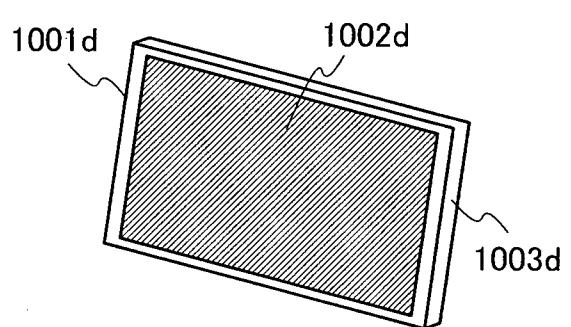


FIG. 12D



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FIG. 13A

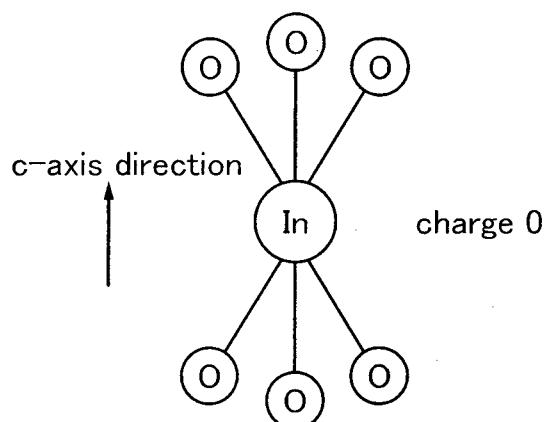


FIG. 13D

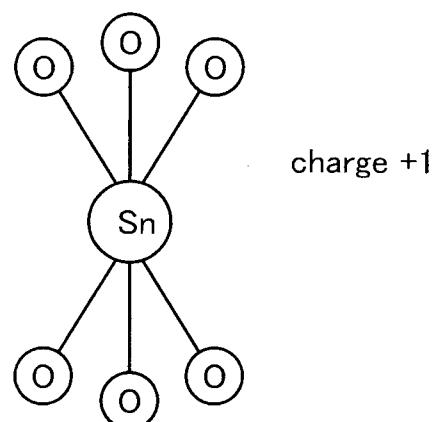


FIG. 13B

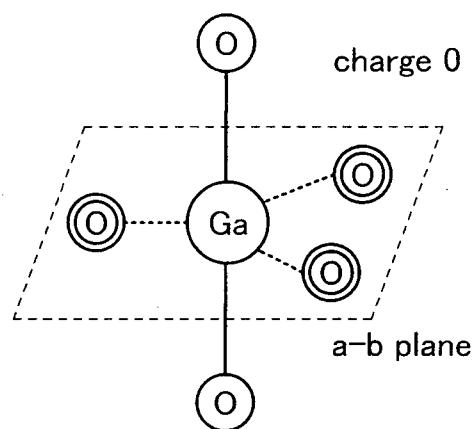


FIG. 13E

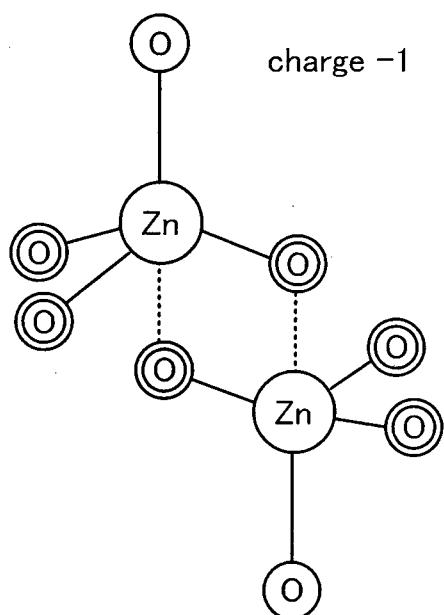
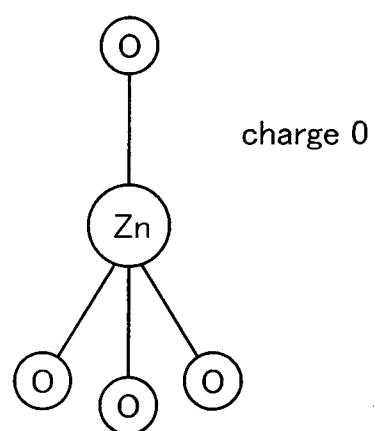


FIG. 13C



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FIG. 14A

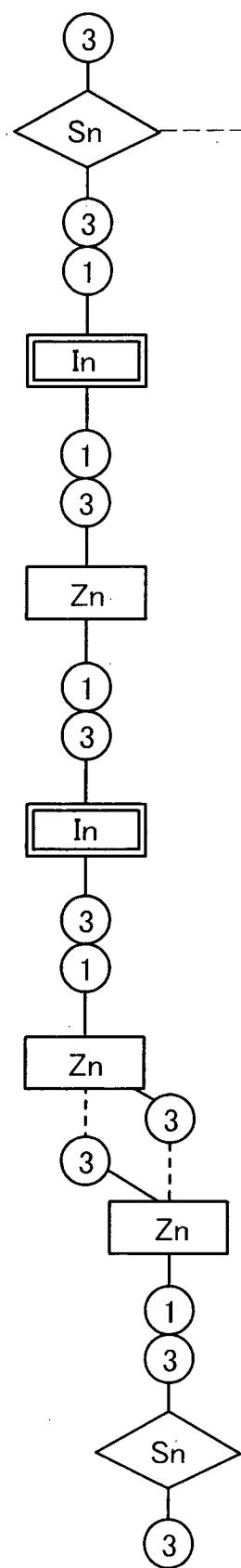
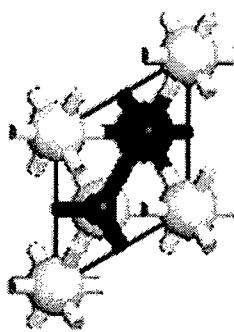


FIG. 14B



FIG. 14C



- In
- Sn
- Zn
- O

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FIG. 15A

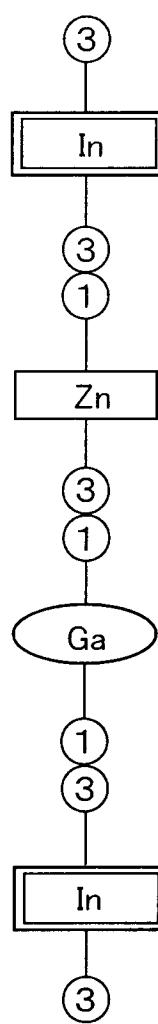


FIG. 15B

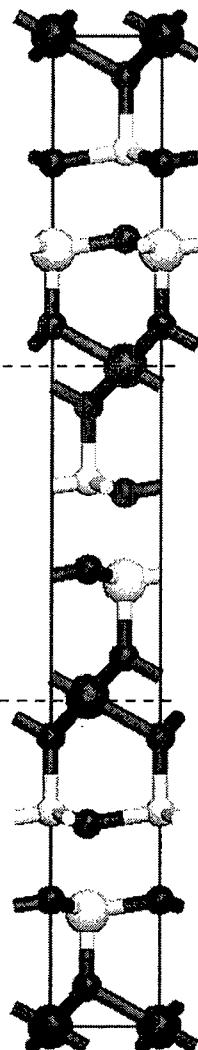
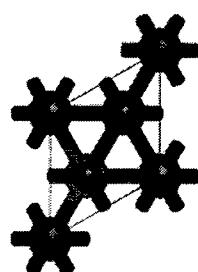


FIG. 15C



● In  
● Ga  
● Zn  
● O

FIG. 16

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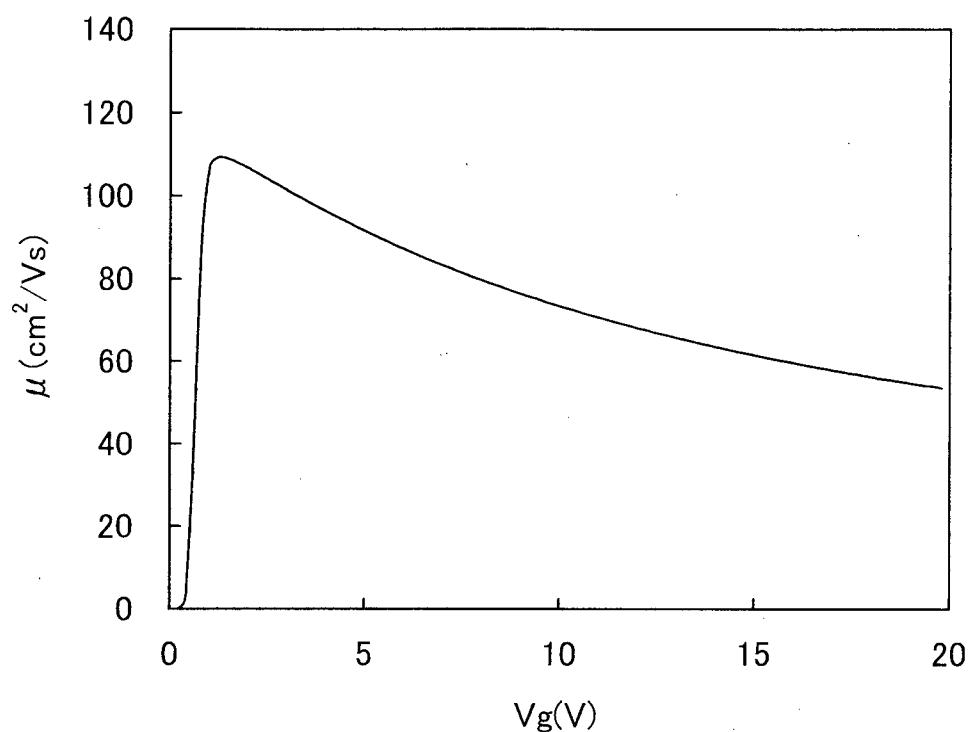


FIG. 17A

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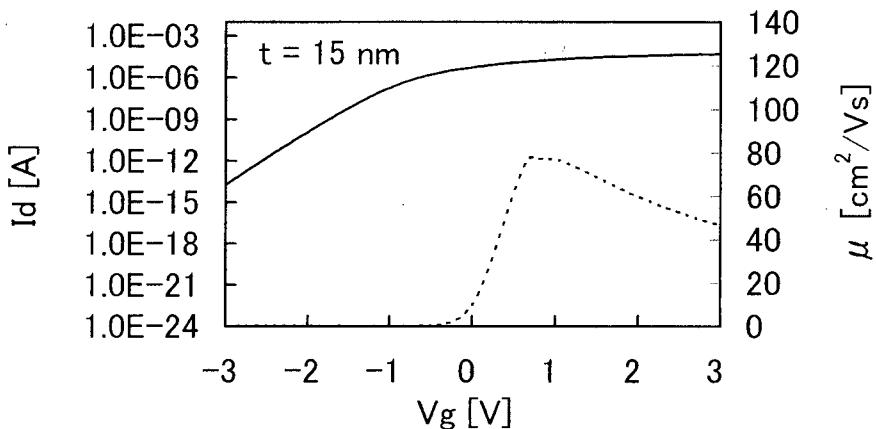


FIG. 17B

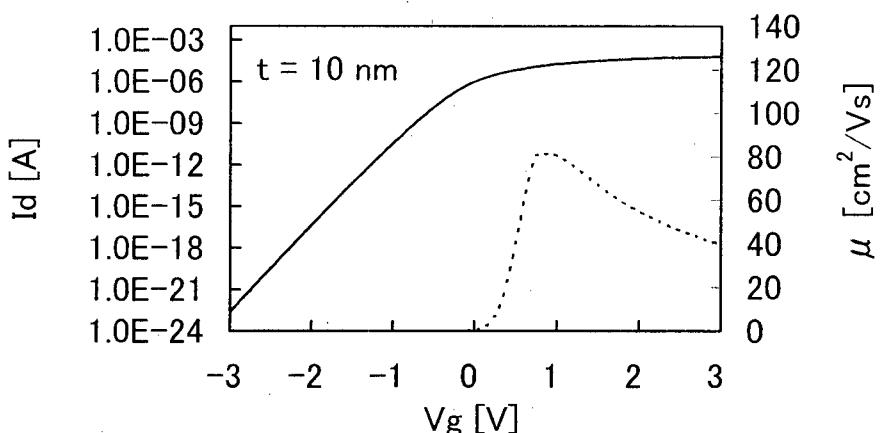
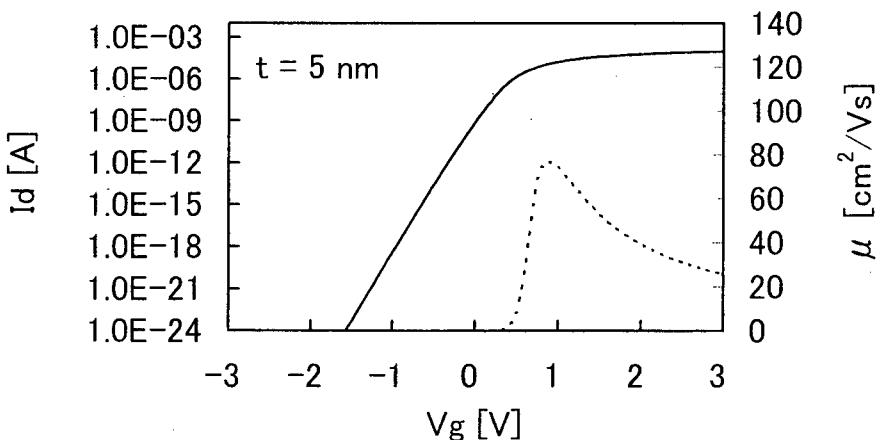


FIG. 17C



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FIG. 18A

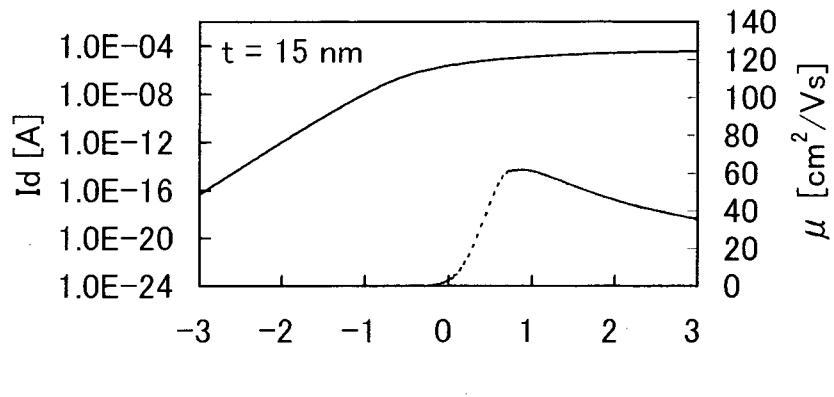


FIG. 18B

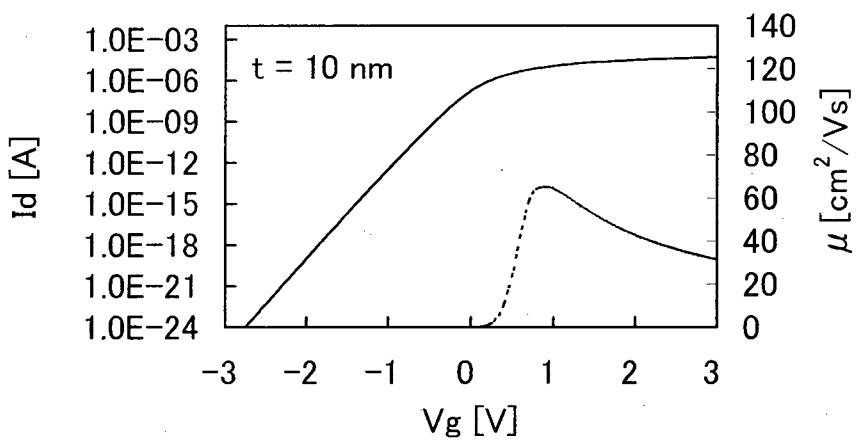


FIG. 18C

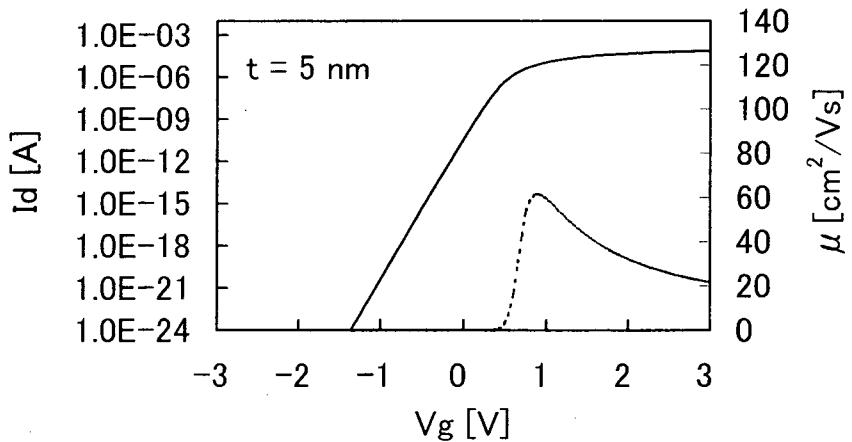


FIG. 19A

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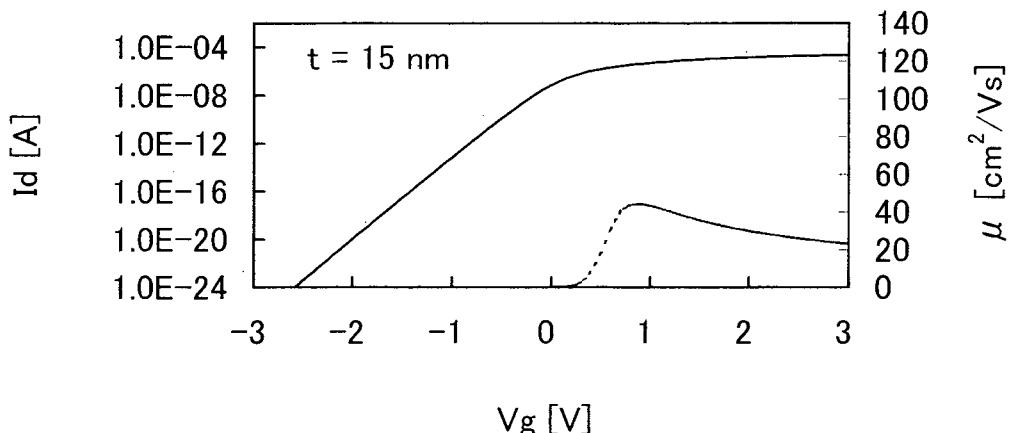


FIG. 19B

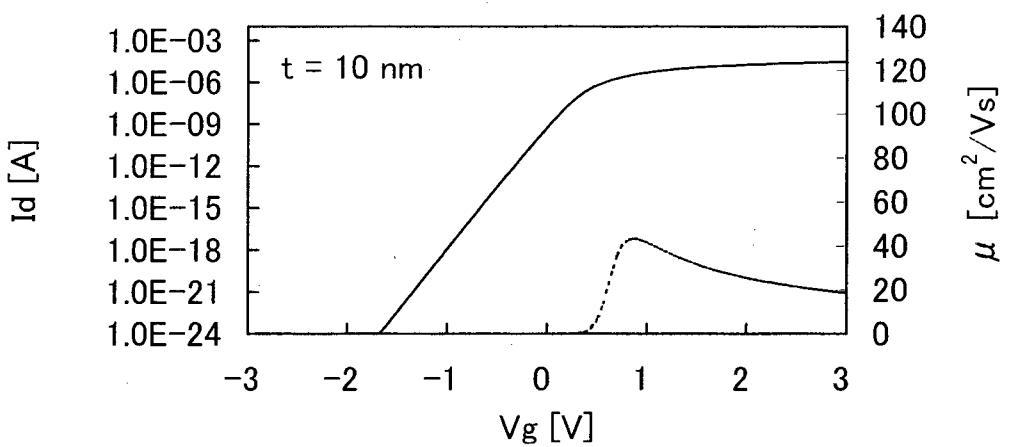
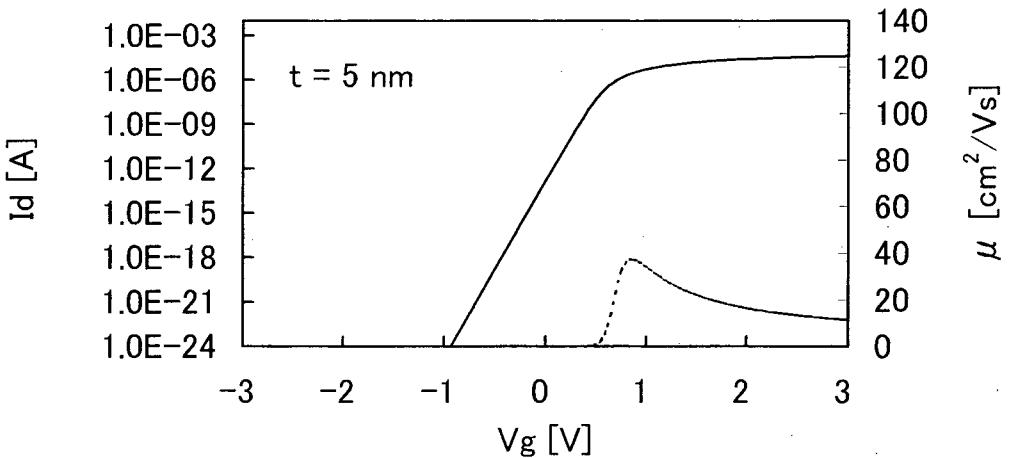


FIG. 19C



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FIG. 20A

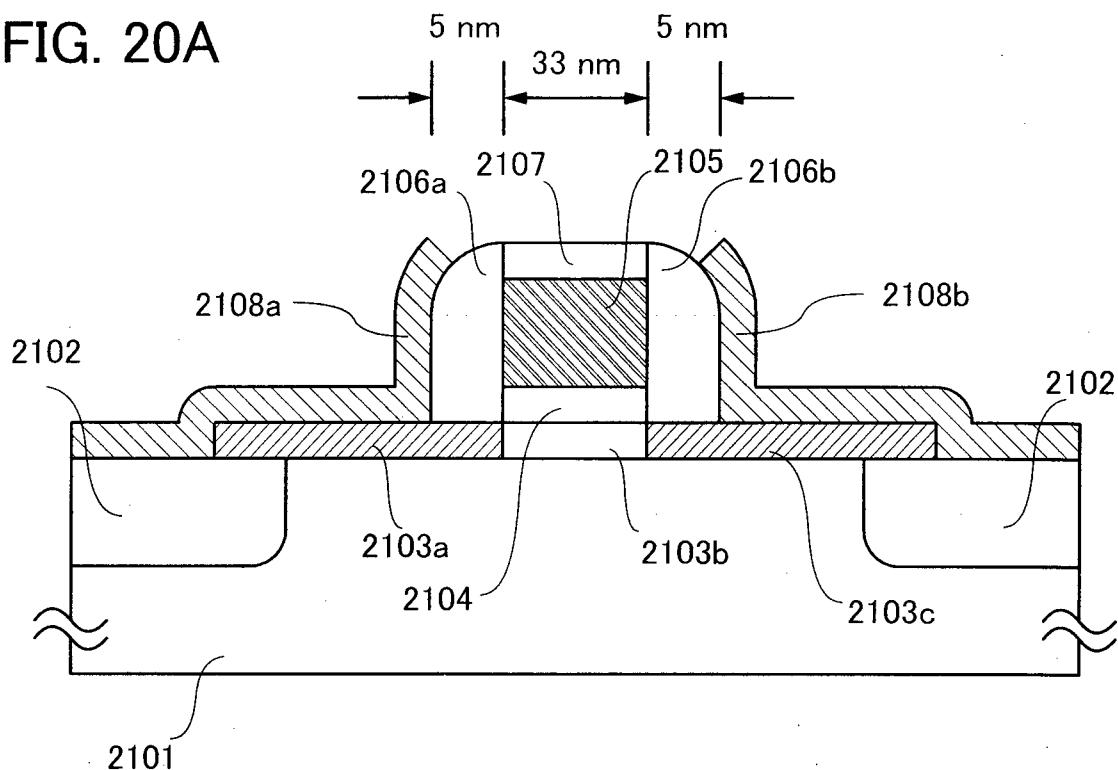
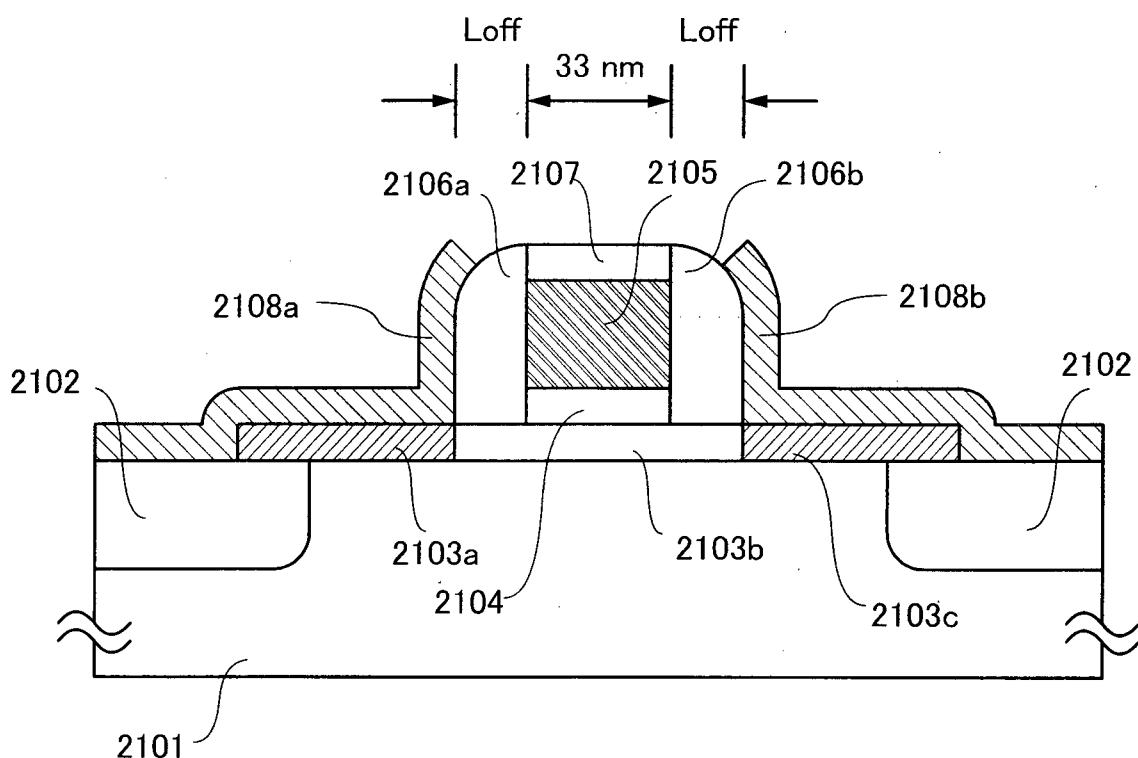


FIG. 20B



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FIG. 21A

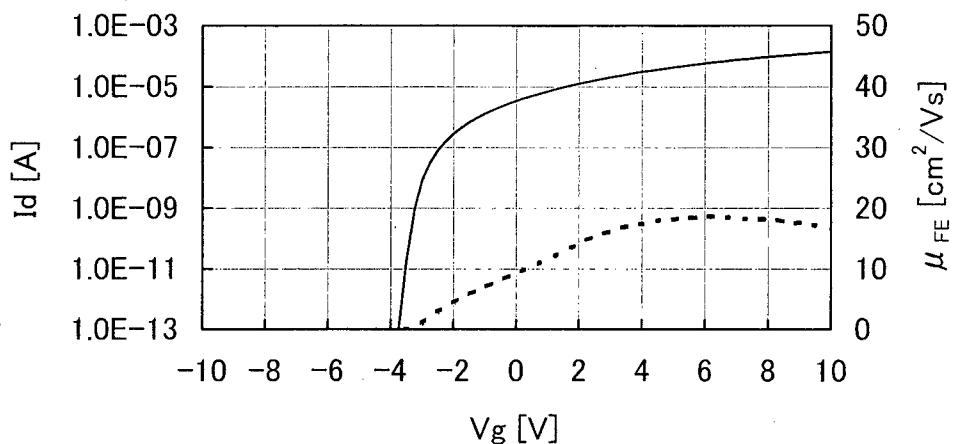


FIG. 21B

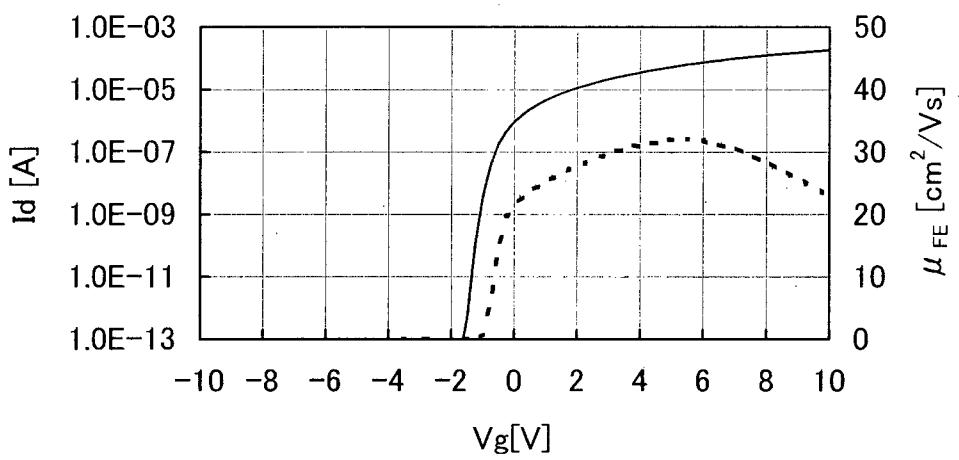
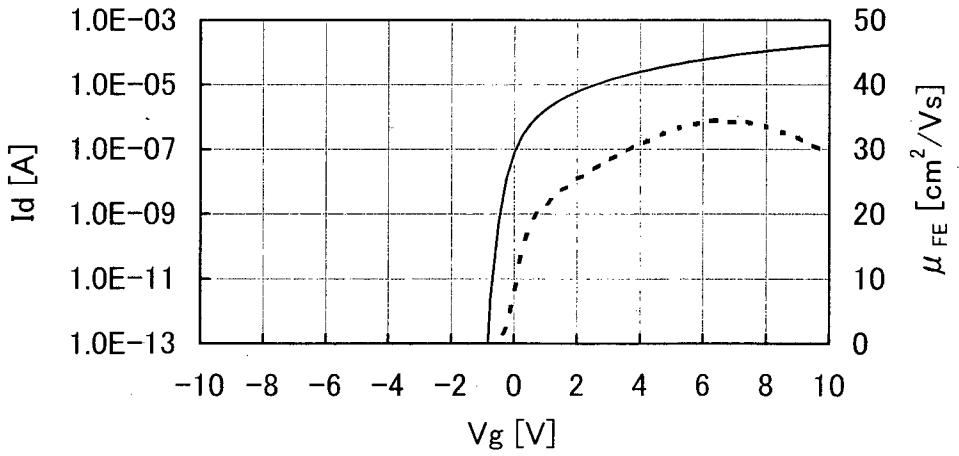


FIG. 21C



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FIG. 22A

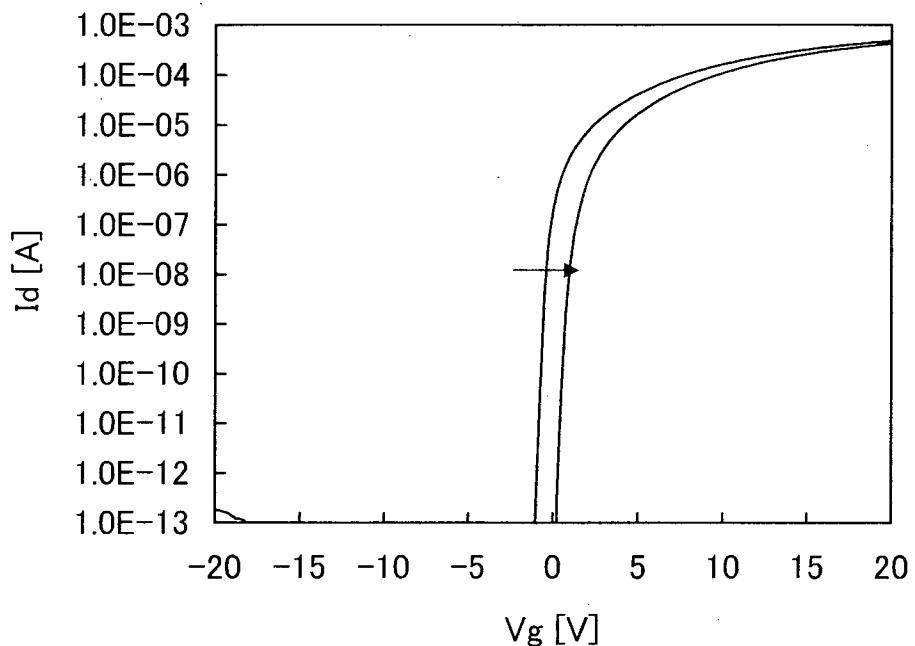
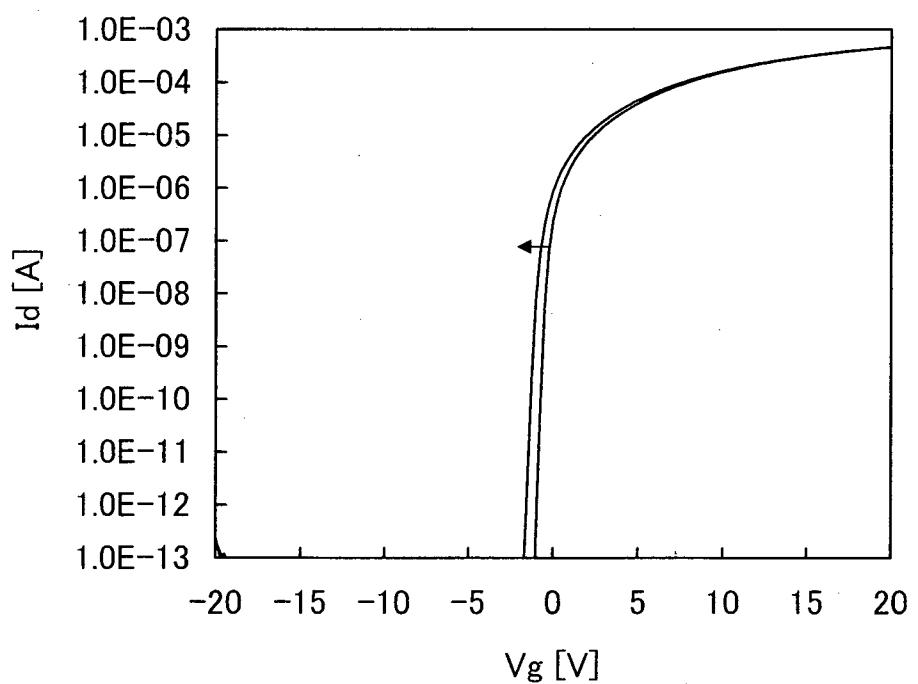


FIG. 22B



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FIG. 23A

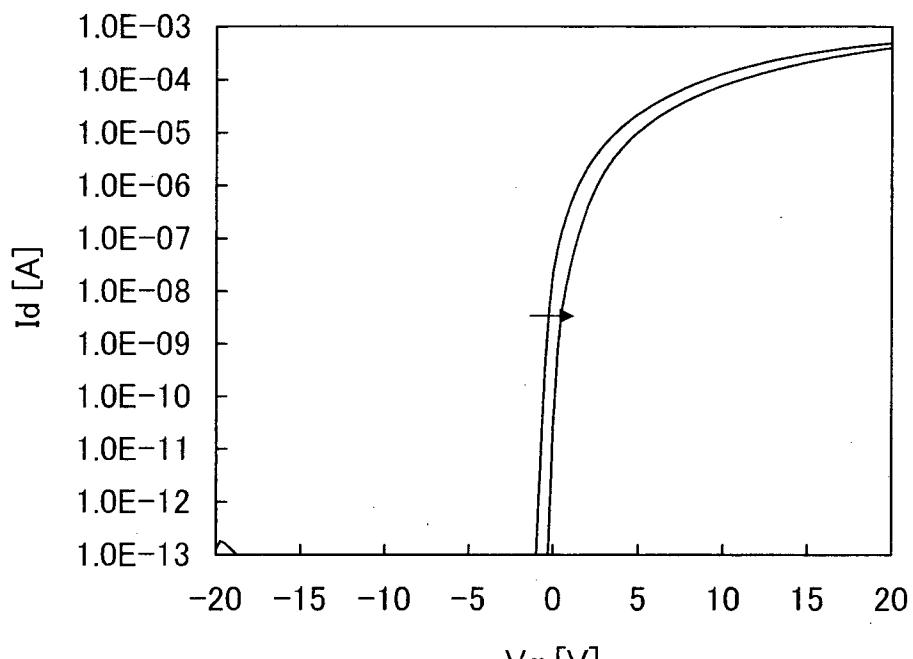


FIG. 23B

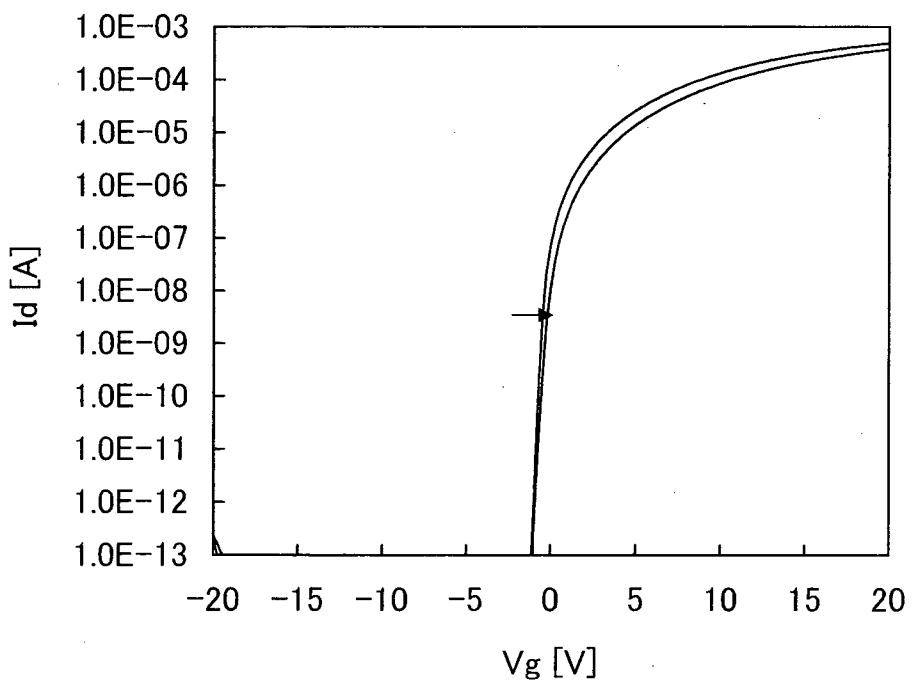
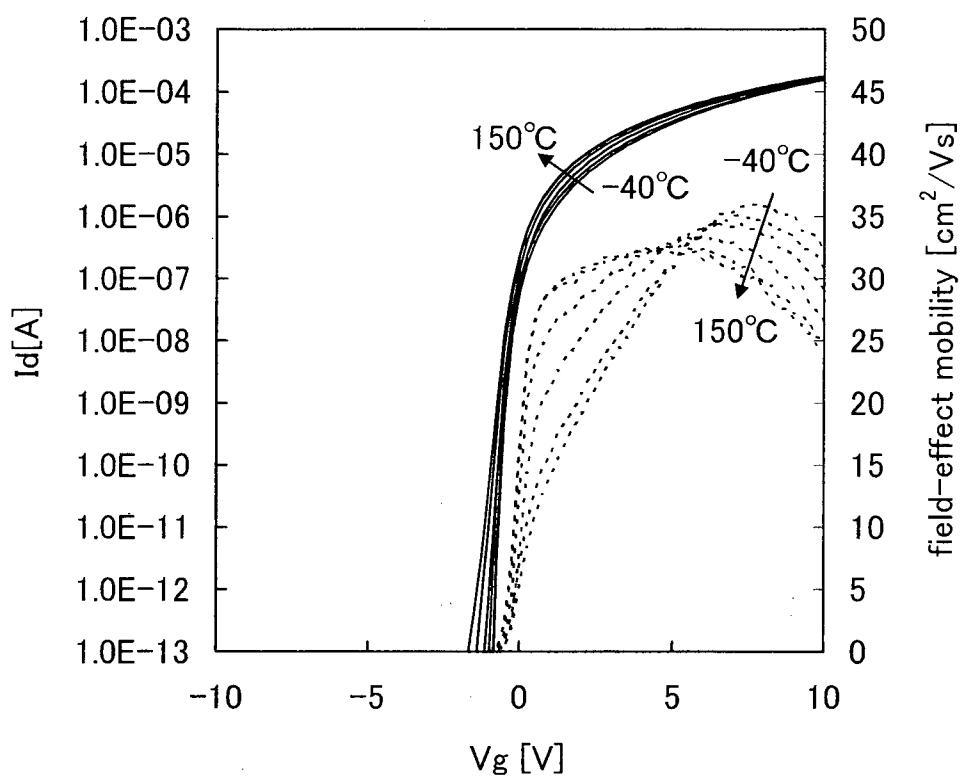


FIG. 24

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FIG. 25A

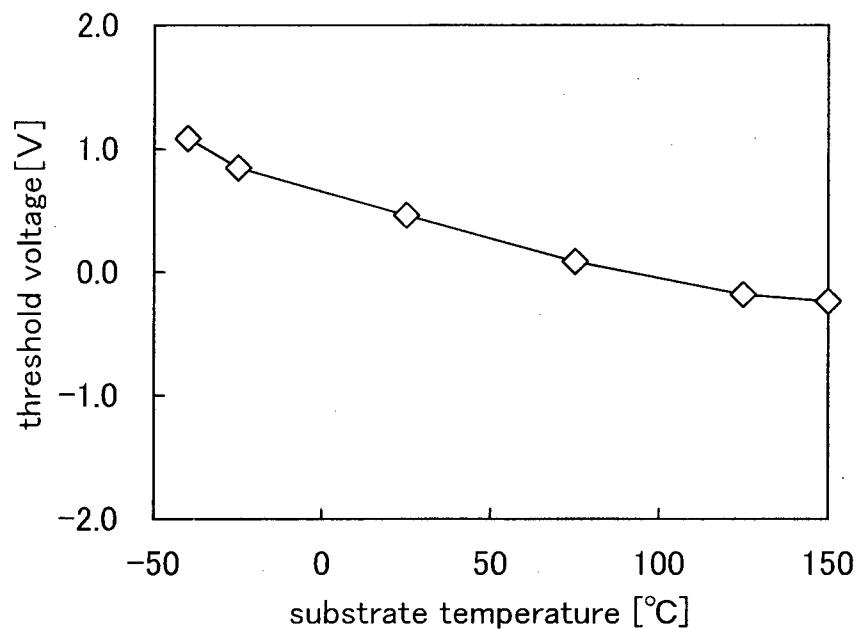


FIG. 25B

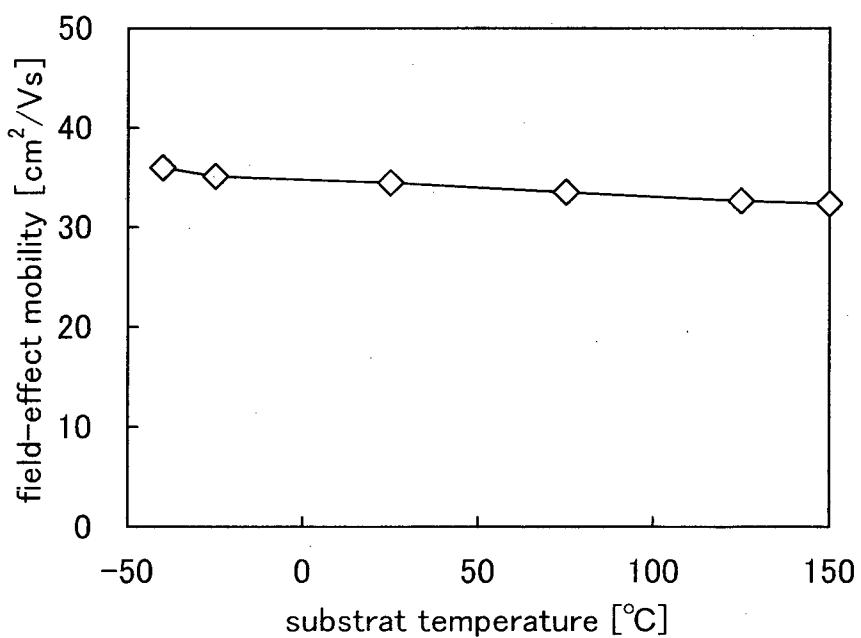


FIG. 26

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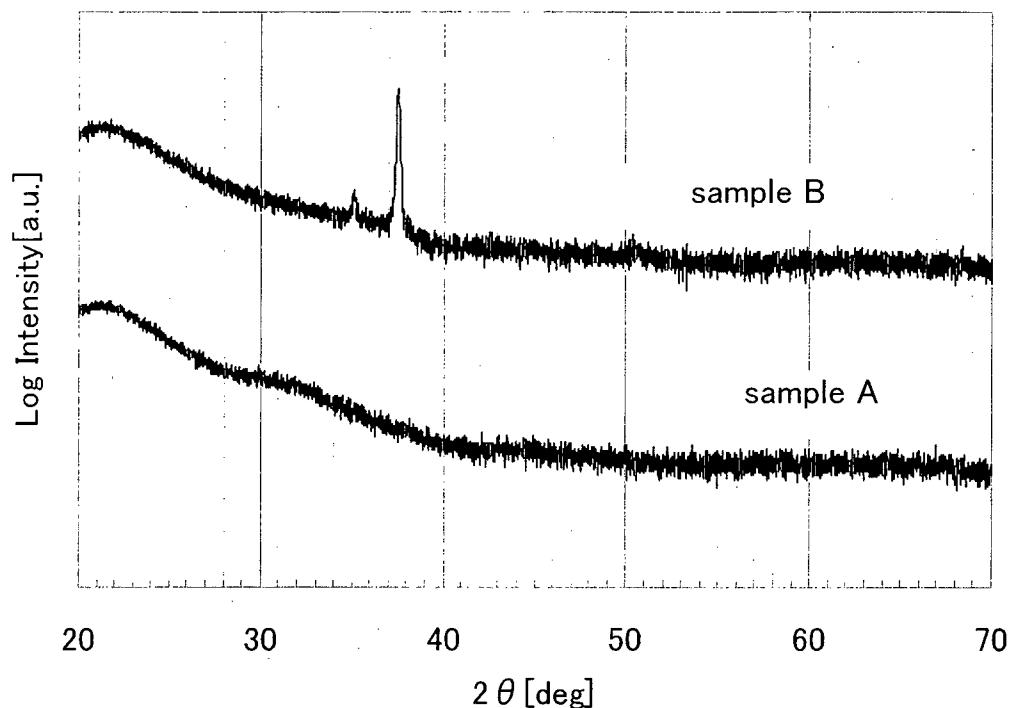
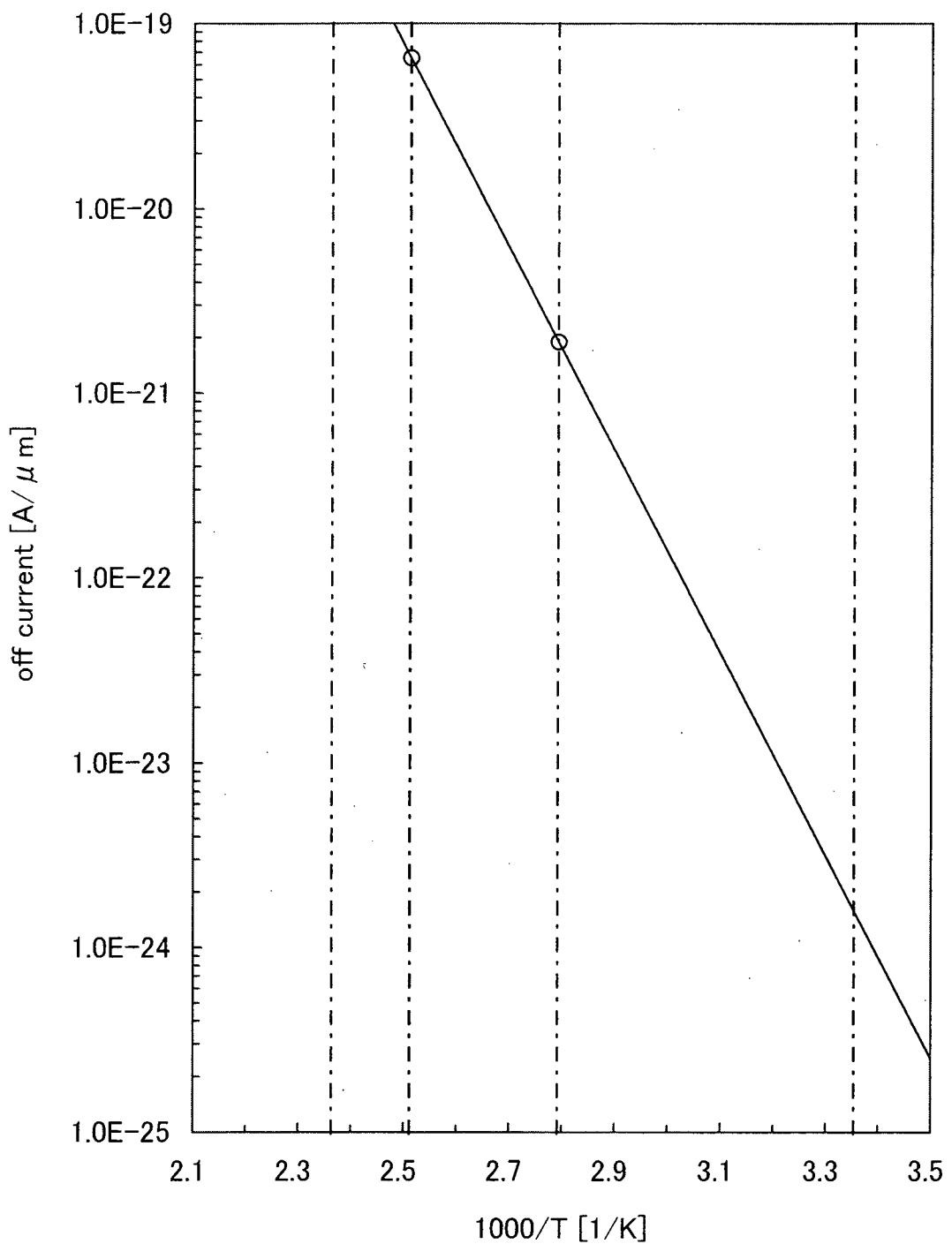


FIG. 27

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FIG. 28A

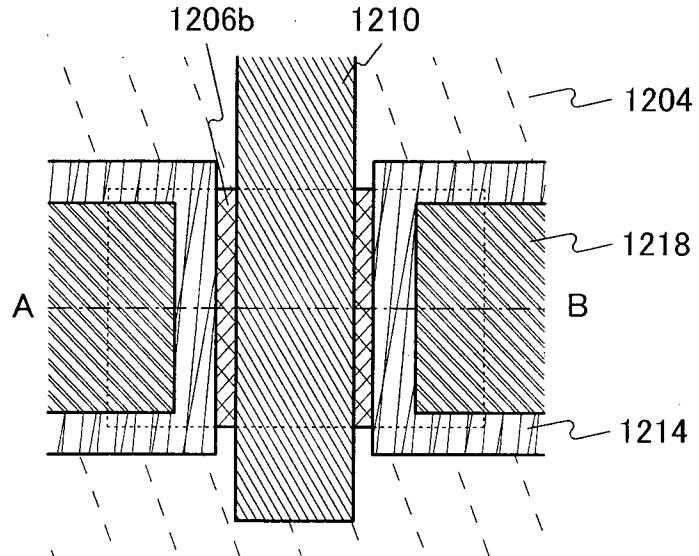
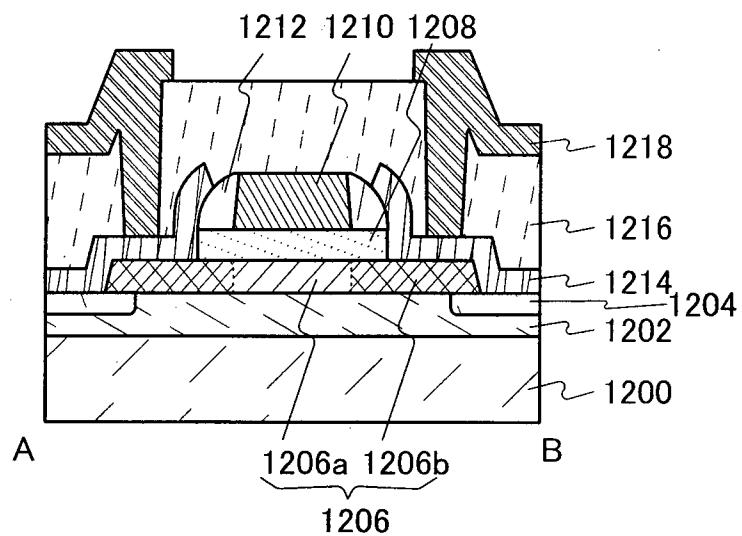


FIG. 28B



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FIG. 29A

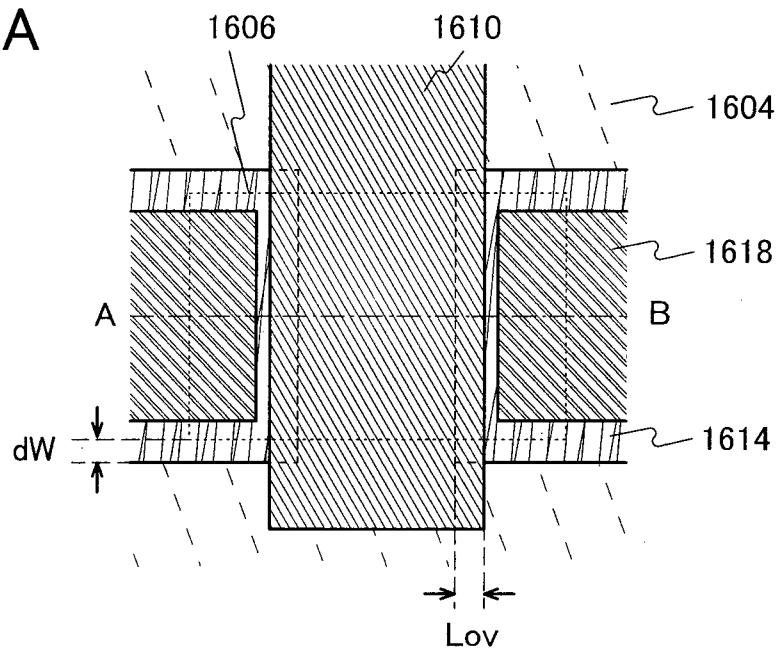
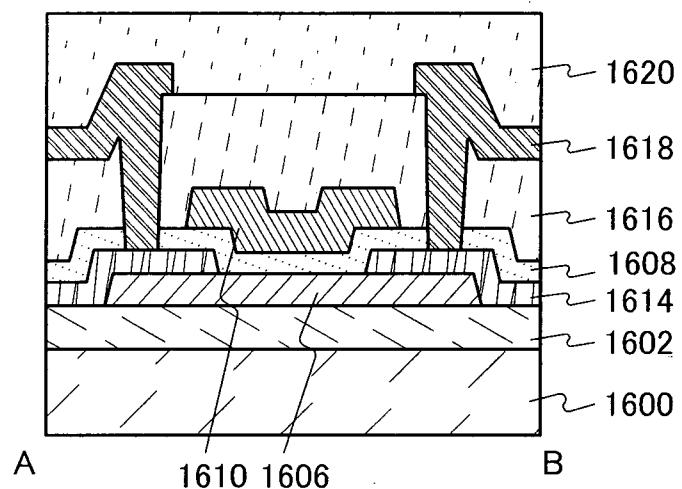


FIG. 29B



# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/JP2012/051484

## A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L29/786(2006.01)i, H01L21/8234(2006.01)i, H01L21/8238(2006.01)i, H01L27/08(2006.01)i, H01L27/088(2006.01)i, H01L27/092(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, H01L21/8234, H01L21/8238, H01L27/08, H01L27/088, H01L27/092

## Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996

Published unexamined utility model applications of Japan 1971-2012

Registered utility model specifications of Japan 1996-2012

Published registered utility model applications of Japan 1994-2012

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2010-3910 A (TOSHIBA MOBILE DISPLAY CO., LTD.) 2010.01.07, Par. Nos. [0012] to [0035], Fig. 1 (Family: none)	1, 2, 4-7, 15, 16, 18-22, 24-26
A		3, 8-14, 17, 23
Y	JP 9-107107 A (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.) 1997.04.22, Par. Nos. [0015] to [0018], [0026] Figs 1 and 2 (Family: none)	1, 2, 4-7, 15, 16, 18-22, 24-26
A		3, 8-14, 17, 23
A	JP 2010-161382 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2010.07.22, Full text; all drawings & US 2009/0002590 A1 & CN 101335273 A	1-26

Further documents are listed in the continuation of Box C.

See patent family annex.

\* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search

13.04.2012

Date of mailing of the international search report

24.04.2012

Name and mailing address of the ISA/JP

**Japan Patent Office**

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**INTERNATIONAL SEARCH REPORT**

International application No. PCT/JP2012/051484
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## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2008-269751 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2008.11.06, Full text; all drawings (Family; none)	1-26