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(54) Title: PIPELINE ADC WITH SHARED GAIN STAGES

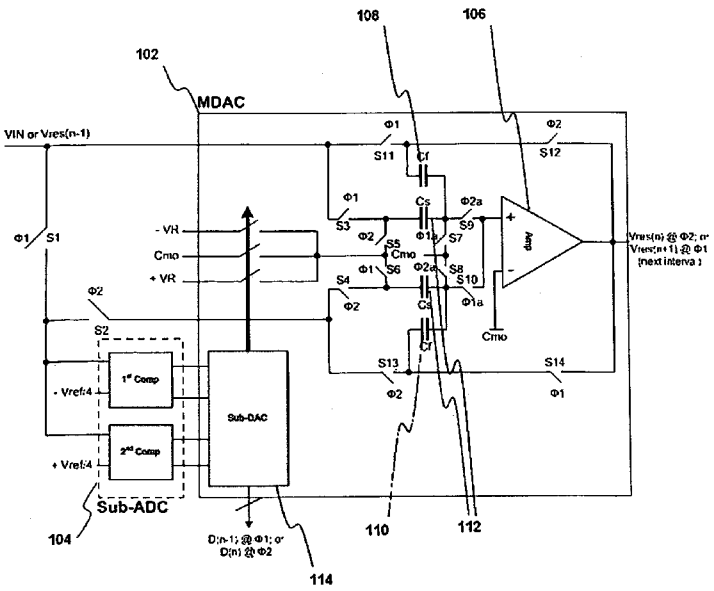

FIG. 5

(57) Abstract: A shared gain-stage circuit of a pipelined analog-to-digital converter (ADC) that allows for sharing at least one multiplying digital-to-analog converter (MDAC) (102) and at least one sub-ADC (104) between two successive stages. The at least one MDAC (102) comprises an amplifier (106), a first feedback capacitor (108), a second feedback capacitor (110), at least two sampling capacitors (112), a plurality of reference voltages and a sub- DAC (114).

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PIPELINE ADC WITH SHARED GAIN STAGES

FIELD OF INVENTION

The present invention relates to a pipeline analog-to-digital converter with shared gain stages.

BACKGROUND ART

Analog-to-digital converter (ADC) are used in digital communication systems, data acquisition system and high quality video systems. Evolution of these application systems has driven the design of ADC towards achieving a higher sampling rates, higher dynamic ranges, higher resolutions, lower power dissipation, lower supply voltage and smaller chip size. Many ADC architectures have been invented to satisfy different requirements for different applications. Some of the examples are flash ADC, folding and interpolating ADC, two-step ADC, pipeline ADC, successive approximation register (SAR) ADC, sigma-delta ADC, integrating ADC and many others.

Pipeline ADC is an accepted choice because of its high accuracy and high throughput rate. In addition, the pipeline architecture generally provides better performance for a given power and semiconductor die area than other ADC architecture. The typical m-bit pipeline ADC includes a sample and hold (S/H) circuit, an array of n-gain stages and a digital error correction (DEC). In each gain stage, there is a multiplying digital-to-analog converter (MDAC) and sub-ADC (comparators). The MDAC consists of gain amplifier, sub-DAC, sampling and feedback capacitors, while the sub-ADC consists of comparators.

In conventional architecture, the amplifiers are used for only half of the clock cycle, which is during amplification phase. In the sampling phase, the amplifier is in an idle state.

In prior art of US Patent No. 7,265,705 shared amplifiers and capacitors are used only for S/H circuitry and the first gain stage, and sub-DAC's are present in each gain stage. US Patent No. 6,462,695 utilizes dynamic biasing technique using switched amplifiers, wherein amplifiers are switched-off in sampling modes and this requires an additional control switching signal.

SUMMARY OF INVENTION

In one embodiment of the present invention is a shared gain-stage circuit of a pipelined analog-to-digital converter (ADC) that allows for sharing at least one multiplying digital-to-analog converter (MDAC) and at least one sub-ADC between two successive stages. The at least one MDAC comprises an amplifier, a first feedback capacitor, a second feedback capacitor, at least two sampling capacitors, a plurality of reference voltages and a sub-DAC. The amplifier further comprises a positive terminal connected to an analog input and a negative terminal connected to a voltage source. The first feedback capacitor further comprises a first plate switchably on a phase 1 clock signal connected to the analog input and a second plate switchably on a phase 2 clock signal connected to the positive terminal of the amplifier. The second feedback capacitor further comprises a first plate switchably on the phase 2 clock signal connected to an analog output voltage and a second plate switchably on the phase 1 clock signal connected to the positive terminal of the amplifier. The at least two sampling capacitors further comprises a first plate switchably on the phase 1 clock signal connected to the analog input voltage and a second plate switchably on the phase 2 clock signal to positive terminal of the amplifier and a first plate switchably on the phase 2 clock signal connected to the analog output voltage and a second plate switchably on the phase 1 clock signal connected to the positive terminal of the amplifier. The plurality of reference voltages is switchably on either the phase 1 or the phase 2 clock signals connected to the first plate of the at least two sampling capacitors. The sub-DAC further comprises a plurality of input terminals connected to an output of a plurality of comparators of the at least one sub-ADC.

The present invention consists of features and a combination of parts hereinafter fully described and illustrated in the accompanying drawings, it being understood that various changes in the details may be made without departing from the scope of the invention or sacrificing any of the advantages of the present invention.

BRIEF DESCRIPTION OF THE ACCOMPANYING DRAWINGS

To further clarify various aspects of some embodiments of the present invention, a more particular description of the invention will be rendered by references to specific embodiments thereof, which are illustrated, in the appended drawings. It is appreciated that these drawings depict only typical embodiments of the invention and are therefore not to be considered limiting of its scope. The invention will be described and explained with additional specificity and detail through the accompanying drawings in which:

FIG. 1 illustrates a conventional architecture for a pipeline ADC (Prior Art).

FIG. 2 illustrates a conventional architecture for a typical 1.5-bit gain stage for pipeline ADC (Prior Art).

FIG. 3 illustrates the sampling and amplification phase of two consecutive gain stages

FIG. 4 illustrates an architecture for a pipeline ADC with shared gain stages.

FIG. 5 illustrates an architecture for a pipeline ADC that allows gain stage sharing.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention relates to a pipeline analog-to-digital converter with shared gain stages. Hereinafter, this specification will describe the present invention according to the preferred embodiments of the present invention. However, it is to be understood that limiting the description to the preferred embodiments of the invention is merely to facilitate discussion of the present invention and it is envisioned that those skilled in the art may devise various modifications and equivalents without departing from the scope of the appended claims.

The present invention relates to low power and small die area pipeline analog-to-digital converter (ADC). The innovation utilizes shared gain stages between multiplying digital-to-analog converter (MDAC) and sub-ADC (comparators) that allow for lower power consumption and reduction of sub-components used in pipeline ADC.

Most of the power consumption in pipeline ADC is contributed by amplifiers where sample and hold (S/H) amplifier is the largest contributor followed by gain-stage amplifiers. A large number of sub-ADC also contribute to the overall power consumption in pipeline ADC. Through the sharing scheme of the present invention, the usage of ADC sub-components that is the MDAC and sub-ADC is optimized. This provides for low power consumption as well as reduction of sub-components used in pipeline ADC.

Reference is being made to FIG. 3. FIG. 3 illustrates the sampling and amplification phase of two consecutive gain stages. The sharing scheme of the present invention is motivated by the fact that in the MDAC architecture, the amplifier is used for only one half of a clock cycle, which is during the amplification phase. As shown in FIG. 3, gain stage *n* is in the sampling mode and the amplifier is idle state. However, in gain stage *n+1*, the amplifier is active in a

closed feedback loop during the same clock phase. Therefore, this amplifier can be shared between these two consecutive gain stages, gain stage *n* and gain stage *n+1*.

Reference is being made to FIG. 4. FIG. 4 illustrates the architecture for the pipeline ADC with shared gain stages according to the embodiments of the present invention. From FIG. 4, it is clear that the architecture for the pipeline ADC with shared gain stages of the present invention utilizes only half (N/2) number of gain stages to develop *m*-bit pipelined ADC compare to the conventional architecture. This is due to the shared gain stage between two successive stages. Additionally, the S/H circuit of the conventional architecture is discarded.

Reference is being made to FIG. 5. FIG. 5 illustrates the architecture for a pipeline ADC that allows gain stage sharing. The description and illustration herein is provided for the implementation of single-ended 1.5bit/stage pipeline ADC for ease of explanation. However, pipeline ADC with shared gain stages can be implemented for any bit/stage architecture with differential configuration.

According to the embodiments of the present invention, the shared gain-stage circuit of a pipelined analog-to-digital converter (ADC) allows for sharing at least one multiplying digital-to-analog converter (MDAC) (102) and at least one sub-ADC (104) between two successive stages. The at least one MDAC (102) circuit comprises an amplifier (106), a first feedback capacitor (108), a second feedback capacitor (110), at least two sampling capacitors (112), a plurality of reference voltages and a sub-DAC (114).

The amplifier (106) further comprises a positive terminal connected to an analog input and a negative terminal connected to a voltage source. The first feedback capacitor (108) further comprises a first plate switchably on a phase 1 clock signal connected to the analog input and a second plate switchably on a phase 2 clock signal connected to the positive terminal of the amplifier (106). The second feedback capacitor (110) further comprises a first plate

switchably on the phase 2 clock signal connected to an analog output voltage and a second plate switchably on the phase 1 clock signal connected to the positive terminal of the amplifier (106).

The at least two sampling capacitors (112) further comprises a first plate switchably on the phase 1 clock signal connected to the analog input voltage and a second plate switchably on the phase 2 clock signal to positive terminal of the amplifier (106) and a first plate switchably on the phase 2 clock signal connected to the analog output voltage and a second plate switchably on the phase 1 clock signal connected to the positive terminal of the amplifier (106).

The plurality of reference voltages is switchably on either the phase 1 or the phase 2 clock signals connected to the first plate of the at least two sampling capacitors. The sub-DAC (114) further comprises a plurality of input terminals connected to an output of a plurality of comparators of the at least one sub-ADC (104).

During phase 1 of the clock signal, C_s1 and C_f1 sample the analog input or $Vres_{(n-1)}$. During the phase 2 of the clock signal, the analog residue $Vres_{(n)}$ is developed through the MDAC (102) by combination of C_s1, C_f1 and the amplifier (106), operating under the control of digital input D_{n-1} produced by the sub-ADC (104) and the sub-DAC (114). This residue is then sampled by C_s2 and C_f2 and is simultaneously processed by the sub-ADC (104) and the sub-DAC (114) to generate the digital signal D_n. During phase 1 clock signal of the next interval, C_s2, C_f2 and the amplifier (106) combine to generate the analog residue $Vres_{(n+1)}$ under the control of digital input D_n.

According to the various embodiments of the present invention, the MDAC (102) can be implemented in a differential configuration and the MDAC (102) can be adjusted for any bit/stage architecture. The shared gain-stage circuit of the present invention may further

comprise of a plurality of shared gain-stage circuits. In another embodiment of the present invention, the shared gain-stage circuit further comprises of at least one digital error correction (DEC) circuit.

CLAIMS

1. A shared gain-stage circuit of a pipelined analog-to-digital converter (ADC) that allows for sharing at least one multiplying digital-to-analog converter (MDAC) (102) and at least one sub-ADC (104) between two successive stages, the at least one MDAC (102) comprises

an amplifier (106);

a first feedback capacitor (108);

a second feedback capacitor (110);

at least two sampling capacitors (112);

a plurality of reference voltages; and

a sub-DAC (114);

characterized in that

the amplifier (106) further comprises a positive terminal connected to an analog input and a negative terminal connected to a voltage source;

the first feedback capacitor (108) further comprises a first plate switchably on a phase 1 clock signal connected to the analog input and a second plate switchably on a phase 2 clock signal connected to the positive terminal of the amplifier (106);

the second feedback capacitor (110) further comprises a first plate switchably on the phase 2 clock signal connected to an analog output voltage and a second plate switchably on the phase 1 clock signal connected to the positive terminal of the amplifier (106);

the at least two sampling capacitors (112) further comprises

a first plate switchably on the phase 1 clock signal connected to the analog input voltage and a second plate switchably on the phase 2 clock signal to positive terminal of the amplifier (106); and

a first plate switchably on the phase 2 clock signal connected to the analog output voltage and a second plate switchably on the phase 1 clock signal connected to the positive terminal of the amplifier (106);

the plurality of reference voltages is switchably on either the phase 1 or the phase 2 clock signals connected to the first plate of the at least two sampling capacitors; and

the sub-DAC (114) further comprises a plurality of input terminals connected to an output of a plurality of comparators of the at least one sub-ADC (104).

2. The shared gain-stage circuit according to claim 1, wherein the MDAC (102) is implemented in a differential configuration.

3. The shared gain-stage circuit according to claim 1, wherein the MDAC (102) is adjusted for any bit/stage architecture.

4. The shared gain-stage circuit according to claim 1 further comprising of a plurality of shared gain-stage circuits.

5. The shared gain-stage circuit according to claim 1 further comprising of at least one digital error correction (DEC) circuit.

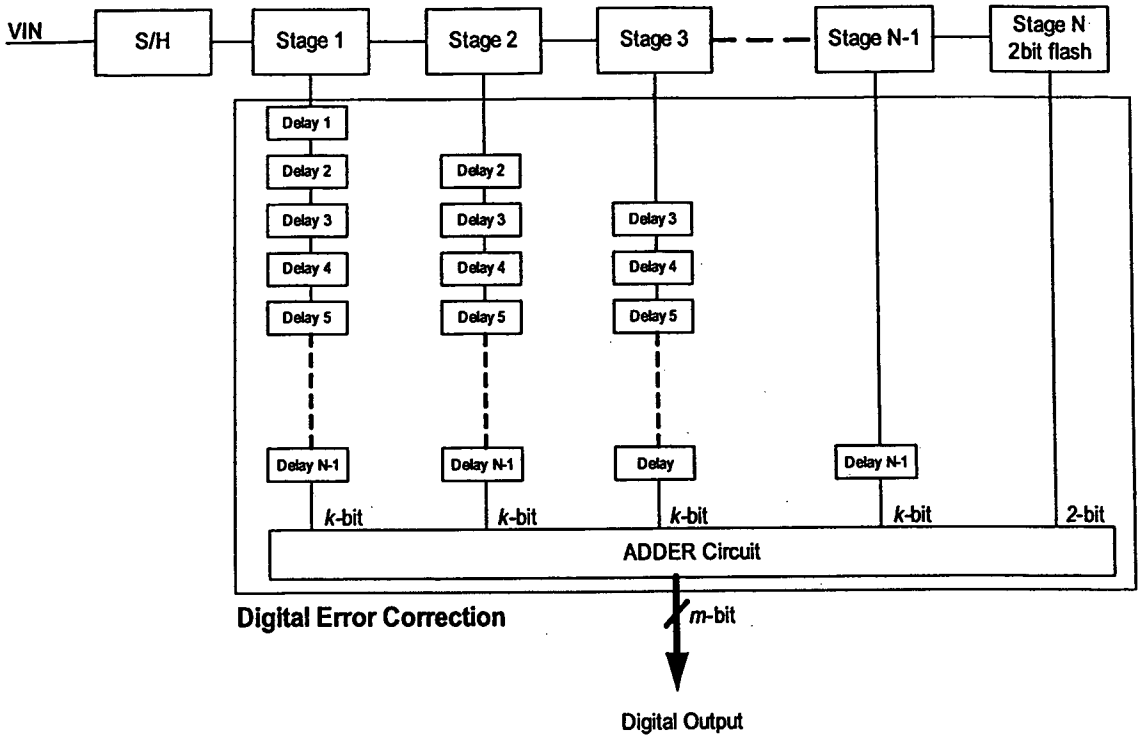

FIG. 1 (Prior Art)

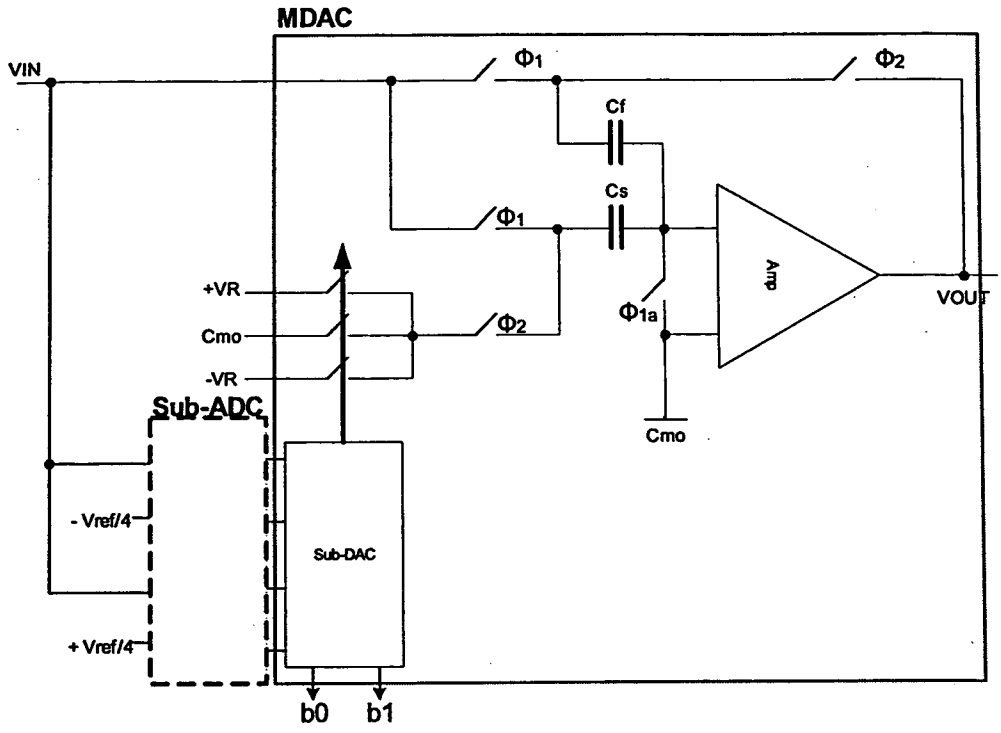

FIG. 2 (Prior Art)

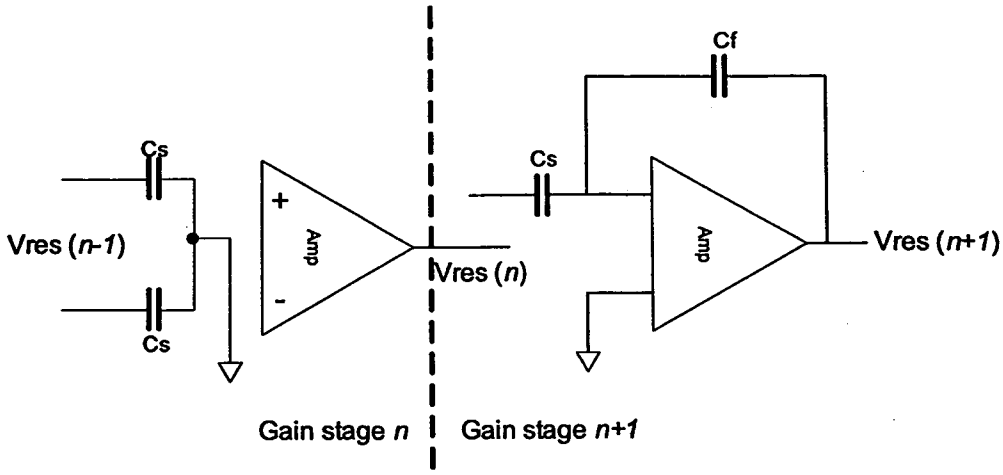
Cf
Cs
Cs
Amp
Vres (n-1)
Amp
Vres (n)
Vres (n+1)
Cs
Gain stage n
Gain stage n+1

FIG. 3

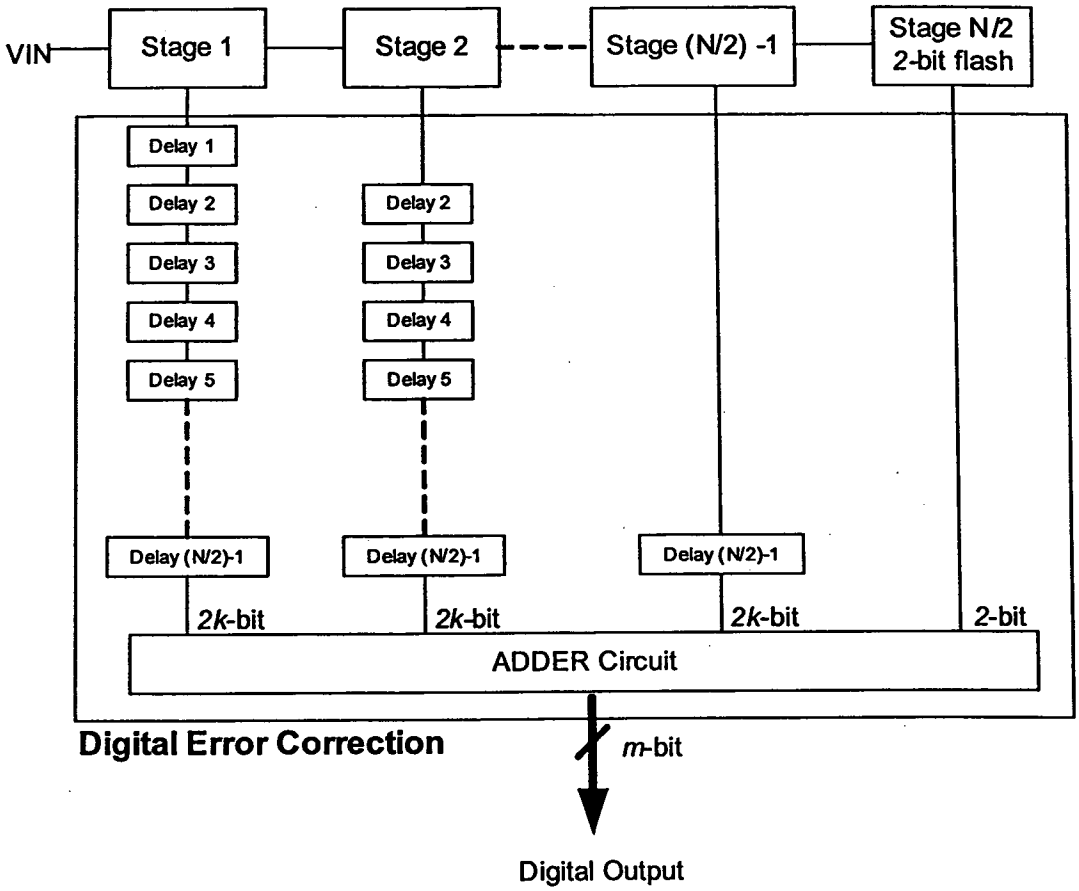
VIN
Stage 1
Stage 2
Stage (N/2) -1
Stage N/2
2-bit flash
Delay 1
Delay 2
Delay 3
Delay 4
Delay 5
Delay 2
Delay 3
Delay 4
Delay 5
Delay (N/2)-1
Delay (N/2)-1
Delay (N/2)-1
2k-bit
2k-bit
2k-bit
2-bit
ADDER Circuit
Digital Error Correction
m-bit
Digital Output

FIG. 4

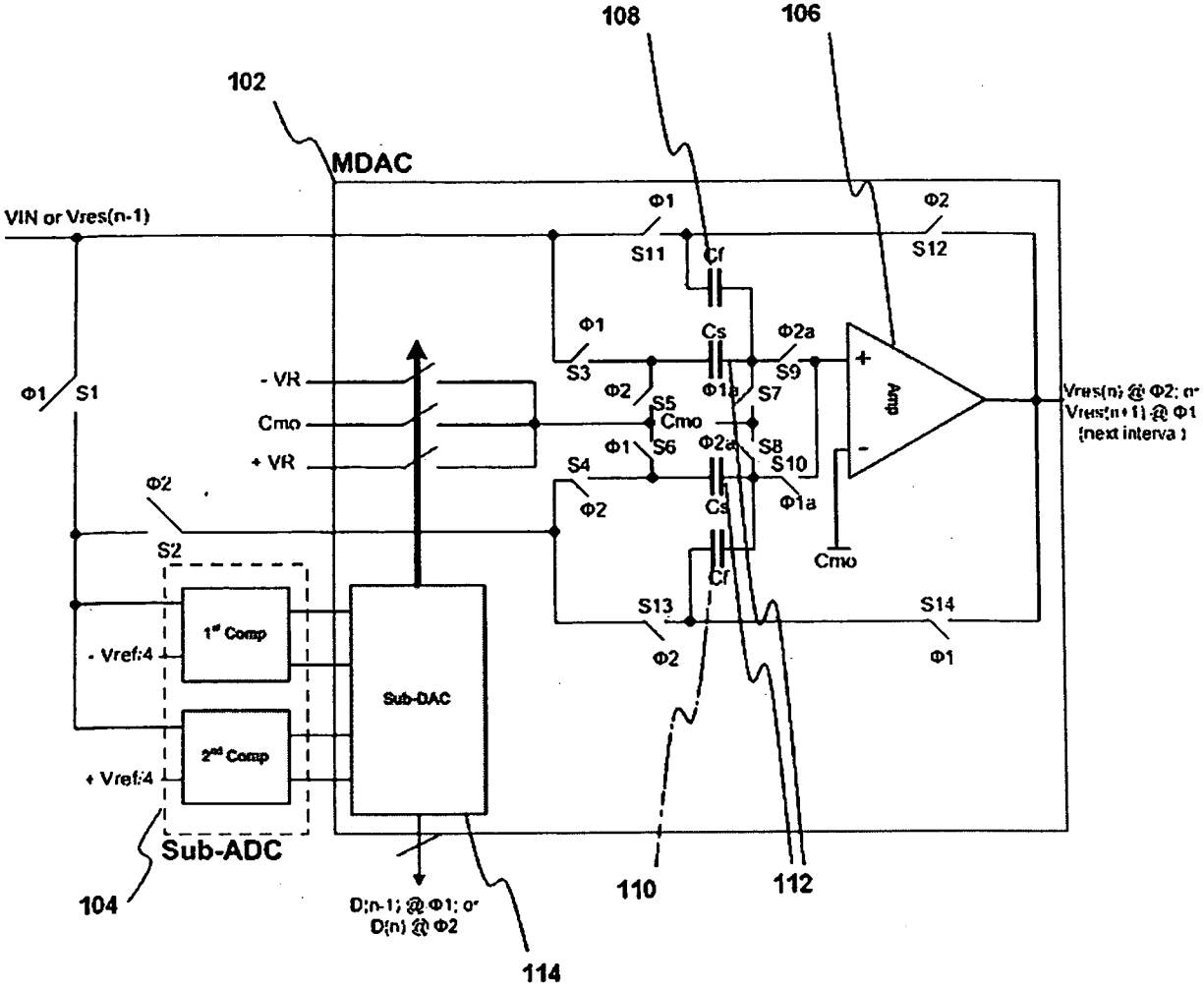
108
106
102
MDAC
VIN or Vres(n-1)
Φ1
Φ2
S11
Cf
S12
Φ1
Cs
Φ2a
S3
S9
Φ1
S1
- VR
Φ2
S5
Φ1a
S7
Cmo
Cmo
Φ1
S6
Φ2a
S8
+ VR
S4
S10
Φ2
Φ2
Cs
Φ1a
S2
Cmo
Cf
S13
S14
Φ2
Φ1
- Vref:4
1st Comp
Sub-DAC
2nd Comp
+ Vref:4
Sub-ADC
104
D[n-1; @Φ1; or
D[n] @ Φ2
110
112
114

FIG. 5