



(51) International Patent Classification:

H01L 29/68 (2006.01) *H01L 21/36* (2006.01)
H01L 51/05 (2006.01)

(21) International Application Number:

PCT/AU2017/050399

(22) International Filing Date:

01 May 2017 (01.05.2017)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

2016901607 02 May 2016 (02.05.2016) AU

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— of inventorship (Rule 4.17(iv))

(54) Title: DIRAC SEMIMETAL STRUCTURE

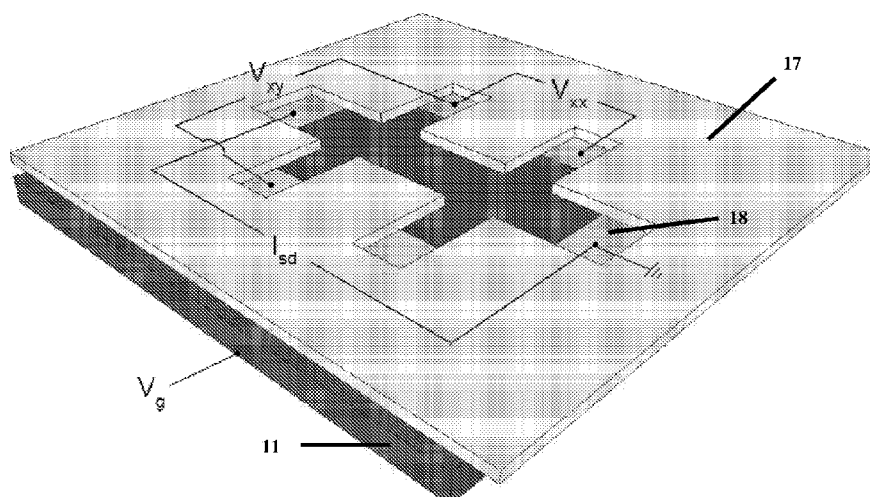


Figure 4B

(57) Abstract: The invention relates to Dirac semimetals, methods for modulating charge carrying density and/or band gap in a Dirac semimetal, devices including a Dirac semimetal layer, and methods for forming a Dirac semimetal layer on a substrate.



Published:

— *with international search report (Art. 21(3))*

Dirac semimetal structure

Field of the invention

The invention relates to Dirac semimetals, methods for modulating charge carrying density and/or band gap in a Dirac semimetal, devices including a Dirac
5 semimetal layer, and methods for forming a Dirac semimetal layer on a substrate.

Background of the invention

Topological Dirac semimetals (TDS) are a recently proposed state of quantum matter that has attracted significant interest. TDS may be considered as three-dimensional analogues of graphene, with linear electronic dispersions in three
10 dimensions.

Detailed theoretical calculations on the TDS Na_3Bi have predicted a conventional-to-topological quantum phase transition (QPT) occurs with increasing film thickness, and that the QPT can also be tuned by electric field (by e.g. gate electrodes) to enable a topological transistor. However, these calculations and predictions are either
15 purely theoretical or relate to thin films of Na_3Bi which have been formed on conducting substrates such as graphene and $\text{Si}[111]$, which makes the characterisation, analysis, and exploitation of these electronic transport properties difficult.

Control of carrier density and electronic conduction via electric fields is an important step toward electronic devices based on TDS. However, to date useful
20 structures including Dirac semimetal layers have not been reported. The present invention addresses this issue.

Reference to any prior art in the specification is not an acknowledgment or suggestion that this prior art forms part of the common general knowledge in any jurisdiction or that this prior art could reasonably be expected to be understood,
25 regarded as relevant, and/or combined with other pieces of prior art by a skilled person in the art.

Summary of the invention

In one aspect of the invention, there is provided a structure including: means for generating an electric field, and a topological Dirac semimetal layer, wherein the topological Dirac semimetal layer is non-conductively separated from the means for generating the electric field, and the means for generating the electric field is configured to apply the electric field to at least a portion of the topological Dirac semimetal layer. By non-conductively separated, it is meant that the topological Dirac semimetal layer is not in conductive contact with the means for generating the electric field, and may be, for example, separated from the means for generating the electric field by an insulator.

In another aspect of the invention, there is provided a structure for altering the charge carrier density in a topological Dirac semimetal, the structure comprising: a conductor, an insulating layer; a topological Dirac semimetal layer separated from the conductor by at least the insulating layer, and at least one electrode contacting the topological Dirac semimetal layer, wherein the conductor and the at least one electrode are configured to apply an electric field to at least a portion of the topological Dirac semimetal layer to alter the charge carrier density of the topological Dirac semimetal layer.

The inventors have found that charge carrier density of a topological Dirac semimetal layer can be changed by subjecting the topological Dirac semimetal layer to an electric field. This effect can advantageously be used to control the current passing through the topological Dirac semimetal layer to enable the topological Dirac semimetal to act as a structure in an electronic component, such as a diode or transistor.

It will be understood that a range of different Dirac semimetals may be used. For example, the Dirac semimetal may be selected from: Cd_3As_2 , Bi_2Se_3 , or of the form A_3Bi where A is an alkali metal as discussed in Wang, Z. *et al.* Dirac semimetal and topological phase transitions in A_3Bi (A=Na, K, Rb). Physical Review B, 85(19):195320 (2012). doi: 10.1103/PhysRevB.85. 195320. The disclosure of which is hereby incorporated by reference. Preferably, A is selected from the group consisting of Na, K and Rb. Most preferably, A is Na.

In an embodiment, the topological Dirac semimetal layer is an A_3Bi layer. Preferably the thickness of the A_3Bi layer is at least 7 nm. More preferably, the

thickness of the topological Dirac semimetal layer is at least 10 nm. Even more preferably, the thickness of the topological Dirac semimetal layer is at least 15 nm. Most preferably, the thickness of the topological Dirac semimetal layer is at least 18 nm.

In one or more embodiments a surface of the topological Dirac semimetal layer exhibits point defects. Preferably, the point defects are vacancy defects. In embodiments where the topological Dirac semimetal layer is an A_3Bi layer, it is preferred that the vacancy defects are due to missing A atoms.

In still another aspect of the invention, there is provided a structure for altering the band gap of a topological Dirac semimetal, the structure comprising: a conductor, an insulating layer; a topological Dirac semimetal layer separated from the conductor by at least the insulating layer, and wherein the conductor is configured to apply an electric field to at least a portion of the topological Dirac semimetal layer to alter the band gap of the topological Dirac semimetal layer.

As above, in an embodiment, the topological Dirac semimetal layer is an A_3Bi layer. Preferably, A is selected from the group consisting of Na, K and Rb. Most preferably, A is Na.

In an embodiment of the aspect relating to a structure for altering the band gap of a topological Dirac semimetal, the topological Dirac semimetal layer has a thickness of less than 20nm. Preferably, the topological Dirac semimetal layer is an ultrathin film and has a thickness of 3 unit cells or less. More preferably, the Dirac semimetal film layer has a thickness of 2 unit cells or less. Most preferably, the Dirac semimetal film layer has a thickness of 1.5 unit cells or less.

In an embodiment of one or more of the above aspects, the structure further comprises a layer for donating or accepting charge carriers from the topological Dirac semimetal layer. This layer is preferably deposited on a surface of the topological Dirac semimetal layer. The layer may be an organic layer, such as an organic electron accepting layer or an organic electron donating layer. Preferably the layer is an electron accepting layer, such as an organic electron accepting layer. More preferably, the layer is a tetrafluorotetracyanoquinodimethane (F4-TCNQ) layer. F4-TCNQ doping can achieve charge neutrality and even a net *p*-type doping. That is, under certain

conditions, F4-TCNQ allows the topological Dirac semimetal layer to undergo an n- type to p- type transition.

In an embodiment of one or more of the above aspects, the structure further comprises a capping layer for preventing oxidation of the topological Dirac semimetal layer. In one form, the capping layer is deposited on the surface of the topological Dirac semimetal layer. However, in other forms where additional layers are present, such as where the structure comprises a layer for donating or accepting charge carriers, the capping layer is applied to the exposed surface of an outermost layer – which in this example is the layer for donating or accepting charge carriers. In preferred forms the capping layer is a layer of a material selected from a metal oxide and/or a metalloid oxide. More preferably, the material is an aluminium or silicon oxide. It is preferred that the capping layer has a thickness in the range of from about 1 nm to about 1000 nm in thickness.

In embodiments where the structure includes an organic electron accepting or electron donating layer, it is preferred that the layer has a thickness of 0.25 Å or greater. More preferably, the layer has a thickness of 0.85 nm or greater. Most preferably, the layer has a thickness that is about 1 nm or greater. It is also preferred that the layer has a thickness of less than 2 nm due to saturation of the charge transfer process.

In particular embodiments, such as where the structure includes an F4-TCNQ of thickness of greater than 0.25 Å, modulation of the electrical field can affect an n- to p- type transition in the topological Dirac semimetal layer. Ideally, the structure is configured such that the n- to p- type transition occurs at an applied voltage between the conductor and the electrode of between -100 and 100 V. More preferably, the n- to p- type transition occurs at an applied voltage of between -75 and 75 V. Most preferably, n- to p- type transition occurs at an applied voltage of between -60 and 60 V.

In the forms of the invention where the structure includes an insulating layer, it is preferred that the insulating layer is formed directly on a surface of the conductor. It is further preferred that the topological Dirac semimetal is formed directly on the surface of the insulating layer. It will be appreciated that a wide range of different conductors and insulating layers may be used. However, it is preferred that the insulating layer is a passivation layer that is formed on the surface of the conductor. That is, where the

conductor is a metal, the insulator may be an oxide of that metal formed, for example due to natural oxidation. However, it will be appreciated that other forms of passivation may be used. In one illustrative embodiment, where the conductor is aluminium, then the insulating layer may be aluminium oxide, such as $\alpha\text{-Al}_2\text{O}_3$. Alternatively, the conductor may be a metalloid, such as Si in which case the insulating layer may also be an oxide of that metalloid, for example SiO_2 . As discussed above, other forms of passivation may also be employed which result in non-oxide passivation layers, an example of this is silicon nitride on a silicon conductor. The advantage of having a passivated insulating layer is that the insulating layer can be formed as a very thin film, which is particularly useful in certain applications. It is preferred that the insulating layer has a thickness in the range of from about 1 nm to about 1000 nm in thickness. Minimising the thickness of the insulator is desirable as larger distances between the conductor and the topological Dirac semimetal reduces the strength of the applied electric field at a given applied voltage between conductor and electrode.

The structure may be a layered structure with various embodiments exhibiting a different layered arrangement. In a first form, the device has the following layered arrangement: conductor, insulator, topological Dirac semimetal. In a second form, the device has the following layered arrangement: conductor, insulator, topological Dirac semimetal, electron donating or electron accepting layer. In a third form, the device has the following layered arrangement: conductor, insulator, electron donating or electron accepting layer, topological Dirac semimetal. Each of these layered structures may additionally comprise a capping layer on the outermost layer, e.g. directly on the surface of the topological Dirac semimetal in the first or third of the aforementioned forms, or directly on the electron donating or electron accepting layer in the second of the above mentioned forms.

In embodiments of one or more of the above aspects, the structure further comprises at least two conductive electrodes in contact with the topological Dirac semimetal layer, the at least two electrodes being spaced apart from each other and between which current may flow from a current or voltage source through the topological Dirac semimetal layer; and at least one electrode of the at least two electrodes is configured to be connected to the current or voltage source. This arrangement is particularly useful where the structure is a transistor.

In a further aspect of the invention, there is provided a method of altering the charge carrier density in a topological Dirac semimetal, the method comprising: providing a structure including: a conductor, an insulating layer, a topological Dirac semimetal layer separated from the conductor by at least the insulating layer, at least
5 one electrode contacting the topological Dirac semimetal layer; and applying a voltage to the conductor relative to the at least one electrode to subject at least a portion of the topological Dirac semimetal layer to an electric field to alter the charge carrier density of the topological Dirac semimetal layer. This method may be practiced in respect of the structures generally discussed above.

10 In still a further aspect of the invention, there is provided a method of altering the band gap of a topological Dirac semimetal, the method comprising: providing a structure including: a conductor, an insulating layer, a topological Dirac semimetal layer separated from the conductor by at least the insulating layer, at least one electrode contacting the topological Dirac semimetal layer; and applying a voltage to the
15 conductor relative to the at least one electrode to subject at least a portion of the topological Dirac semimetal layer to an electric field to alter the band gap of the topological Dirac semimetal layer.

In preferred form of the above aspect, the method further includes varying a strength of the electric field to vary the band gap. In addition or alternatively, it is
20 preferred that the topological Dirac semimetal layer has a thickness of less than 20nm. Preferably, the topological Dirac semimetal layer is an ultrathin film and has a thickness of 3 unit cells or less. More preferably, the Dirac semimetal film layer has a thickness of 2 unit cells or less. Most preferably, the Dirac semimetal film layer has a thickness of 1.5 unit cells or less.

25 In embodiments of the above aspects, the method further includes switching the voltage between a first voltage and a second voltage to increase or decrease the charge carrier density in the topological Dirac semimetal layer.

In embodiments of the above aspects, the method further includes switching the voltage between a first voltage and a second voltage to change a charge carrying
30 mechanism from n- type to p- type, or from p- type to n- type.

In embodiments of the above aspects, the method further includes providing at least two electrodes in contact with the topological Dirac semimetal, the at least two electrodes spaced apart from each other and between which current may flow from a current or voltage source through the topological Dirac semimetal layer; wherein when
5 current is passing between the at least two electrodes, the step of subjecting the topological Dirac semimetal to an electric field alters the magnitude of the voltage between the at least two electrodes.

In embodiments of the above aspects, the method further includes providing at least two electrodes in contact with the topological Dirac semimetal, the at least two
10 electrodes spaced apart from each other and between which current may flow from a voltage source through the topological Dirac semimetal layer; wherein when current is passing between the at least two electrodes, the step of subjecting the topological Dirac semimetal to an electric field alters the magnitude and/or direction of the current passing between the at least two electrodes.

15 In an embodiment, the method further includes providing a capping layer for preventing oxidation of the topological Dirac semimetal layer.

In still another aspect of the invention, there is provided a method of forming a topological Dirac semimetal layer on a substrate; the method including: (a) providing constituent elements of a Dirac semimetal to a surface of a substrate at a first
20 temperature to nucleate the Dirac semimetal on the surface of the substrate forming a nucleation layer of the topological Dirac semimetal layer having a first thickness; and (b) increasing the first temperature to a second temperature and further providing constituent elements of the Dirac semimetal at the second temperature to grow the thickness of the Dirac semimetal layer to a final thickness.

25 In an embodiment, the first temperature is from about 100°C to about 140°C. Preferably, the first temperature is from about 110°C to about 130°C.

In an embodiment, the second temperature is from about 240°C to about 400°C. In an embodiment, the second temperature is from about 250°C to about 390°C.

In an embodiment the Dirac semimetal layer is an A₃Bi layer, and the constituent
30 elements are A and Bi, wherein A is an alkali metal, and the method further comprises:

providing A and Bi atoms with a Bi:A flux ratio of at least 1:8 to about 1:12 or possibly higher, and preferably the flux ratio is about 1:10. In an embodiment, Bi is provided at a flux rate of at least 0.03Å/sec and A is provided at a flux rate of at least 0.7Å/sec. It is preferred that A is selected from the group consisting of Na, K and Rb. Most preferably,

5 A is Na.

In an embodiment, the constituent elements are continuously provided to the surface of the substrate until the thickness of the Dirac semimetal layer has reached the final thickness.

In an embodiment, the step of increasing the first temperature to the second
10 temperature commences when the first thickness reaches 2 nm.

In an embodiment, as the first temperature increases to the second temperature, the process further includes an intermediate growth stage wherein the constituent elements are provided to the surface of the substrate, and the topological Dirac semimetal layer increases in thickness from the first thickness to an intermediate
15 thickness.

In an embodiment, during the intermediate growth stage, the thickness of the topological Dirac semimetal layer increases by up to 30% or less of the final thickness. Preferably up to 25% or less of the final thickness. Thus, for a topological Dirac semimetal layer with a final thickness of 20 nm, during this intermediate growth stage
20 where the temperature is ramped from the first temperature to the second temperature, the film grows preferably up to 6 nm or less, and more preferably up to 5nm or less. In still other embodiments, the increase in thickness of the topological Dirac semimetal layer during the intermediate stage is not dependent on the final thickness. In such cases, during this intermediate stage, the thickness of the topological Dirac semimetal
25 layer increases by up to 6 nm or less. Preferably up to 5 nm or less.

In an embodiment, the pressure during steps (a) and (b) is about 3×10^{-9} Torr or less.

In an embodiment, the method further includes, after step (b), a step (c) of annealing the topological Dirac semimetal layer at an annealing temperature for an
30 annealing time. Preferably, the annealing temperature is from about 240°C to about

400°C. More preferably, the annealing temperature is from about 250°C to about 390°C. Even more preferably, the annealing temperature is the second temperature. Additionally, or alternatively it is preferred that the annealing time is less than 1 hour. Preferably, less than 30 minutes. More preferably, the annealing time is less than 20
5 minutes. Most preferably, the annealing time is about 10 minutes or less.

It is further preferred that step (c) is conducted under a flux of A. Such as that a flux of Bi is not provided during step (c).

It is further preferred that the topological Dirac semimetal layer does not increase in thickness during step (c).

10 In another embodiment, the substrate is an electrically insulating material, and/or the substrate includes a layer of an electrically insulating material disposed thereon, and wherein the topological Dirac semimetal layer is formed on a surface of the electrically insulating material.

In still another embodiment, the method can include providing an electron
15 donating or accepting layer for donating or accepting charge carriers from the topological Dirac semimetal layer. This may include applying the electron accepting layer over the topological Dirac semimetal layer as discussed previously. In some embodiments the method can include tuning charge carrier donating or accepting properties of the topological Dirac semimetal layer by altering a property of the electron
20 donating or accepting layer. For example, in certain embodiments the thickness of the electron accepting or electron donating layer can affect the charge carrying properties of the Dirac semimetal layer. Thus, particularly where it is desired that the Dirac semimetal layer undergo an n-type to p-type transition in the presence of a stimuli (such as an electric field), it is preferred that the electron accepting or electron donating layer has a
25 thickness that 0.25 Å or greater. More preferably, the electron accepting or electron donating layer has a thickness greater than 0.85 nm. Most preferably, the electron accepting or electron donating layer has a thickness greater that is about 1 nm. It is also preferred that the electron accepting or electron donating layer has a thickness of less than 2 nm.

As used herein, except where the context requires otherwise, the term "comprise" and variations of the term, such as "comprising", "comprises" and "comprised", are not intended to exclude further additives, components, integers or steps.

5

Brief description of the drawings

Further aspects of the present invention and further embodiments of the aspects described in the preceding paragraphs will become apparent from the following description, given by way of example and with reference to the accompanying drawings.

Figure 1 illustrates the structure of Na₃Bi thin films. All data corresponds to 20 nm-thick Na₃Bi grown at 345 °C on α -Al₂O₃ [0001]. Figure 1(a) is a schematic representation of device geometry showing location of Ti/Au pads used to make electrical contact with the Na₃Bi film grown on sapphire. The inset shows the crystal structure of Na₃Bi with the in-plane and c-axis lattice constants labelled, where Na and Bi atoms are coloured grey and black, respectively. Figure 1(b) is a large-scale STM image showing the morphology of Na₃Bi with step height 4.7 Å ($V_{\text{bias}} = 1$ V, $I = 100$ pA, $T = 5$ K). The inset is an atomic-resolution STM image of surface with lattice constant 5.45 Å ($V_{\text{bias}} = 500$ mV, $I = 200$ pA, $T = 5$ K). Figure 1(c) is a LEED image taken at 17.5 eV showing the 1x1 symmetry of the Na₃Bi surface. Figure (d) is a scanning tunnelling spectrum dI/dV vs V averaged over 20 nm x 20nm area. (Bias modulation amplitude $V_{\text{mod}} = 5$ mV_{rms}). The bias voltage position of minimum dI/dV is labelled ED = -35 mV and identified as the Dirac point energy.

Figure 2 illustrates Hall mobility and Hall carrier density of Na₃Bi thin films measured at a temperature of 5 K for samples grown with different thermal profiles. Figure 2(a) illustrates mobility and Figure 2(b) illustrates Hall carrier density (n-type) plotted against the final growth temperature for the various samples. As can be seen, the 120-345 °C growth profile achieves the highest measured mobility (6,310 cm²/vs) and lowest carrier density (4.6×10^{17} cm⁻³). The grey shaded region represents the range of final growth temperatures for which the sample quality significantly degrades. Figure 2(c) is a log-log plot of experimental mobility vs. carrier density (black squares). The hashed region was calculated for best estimates of the effective fine structure

constant $\alpha = 0.06-0.17$. The dashed line is a fit to the experimental data yielding an effective fine structure constant $\alpha = 0.44$.

Figure 3 illustrates the transverse magnetoresistance (about 0.5T) of Na_3Bi thin films at a temperature of 5 K. Figure 2(a) shows the normalized magnetoresistance $\rho_{xx}(B)/\rho_{xx}(B = 0)$ as a function of B for samples prepared at final growth temperatures indicated in the legend. "345* no flux" indicates growth without the post-growth anneal in Na flux. Lines are fits to Eqn. 1. Figure 2(b) shows the quadratic coefficient of MR A from fits to Eqn. 1 in Figure 2(a) as a function of carrier density for the various films measured. Figure (c) is a plot of residual magnetoconductance $\Delta\sigma = \sigma(B) - \sigma(B = 0)$ vs B after subtraction of fit to Eqn. 1 from data in Figure 2(a). Fits are to the strong spin-orbit limit of the HLN theory (Eqn. 2). The single fitting parameter, the coherence length L_ϕ , is plotted against carrier density in Figure 2(d). The points in Figure 2(b) and Figure 2(d) correspond to the sample growth temperatures indicated.

Figure 4a and 4b show, diagrammatically, devices used in film deposition. Figure 4b is a device diagram, showing Hall bar film geometry defined by a surface stencil mask affixed on the $\text{Si}:\text{SiO}_2$ substrate that serves as a back gate.

Figure 5 plots Hall effect carrier density against gate voltage for various top surface coverages of molecular dopant F4-TCNQ. For coverages of +.85nm and +1.08nm F4-TCNQ, the ambipolar, n- to p- type transition is clearly visible at +50 Vg and -35 Vg, respectively.

Figure 6 is an STM topographic image (400 nm x 400 nm) of few atomic layer $\text{Na}_3\text{Bi}(001)$ film grown on $\text{Si}(111)$.

Figure 7(a) shows differential conductance, dI/dV spectra taken on a pristine region of Na_3Bi at different tip-sample separations.

Figure 7(b) shows extracted bandgap as a function of relative height (or tip-sample separation height) from the dI/dV spectra in Figure 7(a).

Figure 8 is a Scanning tunneling microscopy (STM) image showing the morphology of a sample 50 x 50 nm, with 2 nm vertical scale, $V_{\text{bias}} = -300$ mV, $I = 200$ pA. The observable step edges have height of 4.2 Å.

Figure 9(a) shows zero field conductivity (S / cm) and **Figure 9(b)** shows low-field Hall carrier density ($10^{18} cm^{-3}$) vs. back gate voltage (V_g), for the Na_3Bi film as-grown (circles), and after the deposition of $6.2 \text{ \AA}$ F4-TCNQ on the surface (squares)

Figure 10(a) shows the gate dependence of the zero-field resistivity ρ_{xx} ($\Omega\text{-cm}$)
5 after top-gating with F4-TCNQ.

Figure 10(b) shows transverse magnetoresistance ρ_{xy} (Ω/sq) plotted versus perpendicular applied magnetic field (T), for back gate voltages (V_g) indicated in the legend (V).

Figure 10(c) shows theoretical fits to the data in Figure 10(b) using charge
10 puddling theory.

Figure 11 shows carrier density plotted as a fit parameter to the curves in Figure 10(b) against V_g (line).

Figure 12(a) is a large area ($400 \text{ nm} \times 380 \text{ nm}$) topographic STM image of 20 nm Na_3Bi on Si(111) (bias voltage $V = -3 \text{ V}$ and tunnel current $I = 50 \text{ pA}$). Inset: Atomic
15 resolution STM image with lattice constant $5.45 \text{ \AA}$ (taken on separate 20 nm Na_3Bi film) showing an individual Na vacancy at the surface.

Figure 12(b) is an STM topography image ($V = 300 \text{ mV}$ and $I = 250 \text{ pA}$) on a $45 \text{ nm} \times 45 \text{ nm}$ region of Na_3Bi .

Figure 12(c) is an STM topography image ($V = -550 \text{ mV}$ and $I = 200 \text{ pA}$) on a 30
20 $\text{nm} \times 30 \text{ nm}$ region of Na_3Bi .

Figure 12(d) is an STM topography image ($V = -50 \text{ mV}$ and $I = 100 \text{ pA}$) on a $30 \text{ nm} \times 30 \text{ nm}$ region of Na_3Bi on sapphire ($\alpha\text{-Al}_2\text{O}_3(0001)$).

Figure 12(e) is an area-averaged STS spectra (vertically offset for clarity) corresponding to four different regions of the sample.

Figure 13(a) is a Dirac point energy map of $45 \text{ nm} \times 45 \text{ nm}$ ($90 \text{ pixels} \times 90 \text{ pixels}$)
25 region of Na_3Bi ($V = -250 \text{ mV}$ and $I = 250 \text{ pA}$), corresponding to Region A represented in Figure 12(b). Scale bar is 15 nm .

Figure 13(b) is a Dirac-point energy map of 30 nm x 30 nm (60 pixels x 60 pixels) region of Na₃Bi corresponding to Region B of Figure 12(c) ($V = -150$ mV and $I = 200$ pA). Scale bar is 10 nm.

Figure 13(c) is a Dirac-point energy map of 30 nm x 30 nm (60 pixels x 60 pixels) region of Na₃Bi grown on α -Al₂O₃(0001) (labelled Region C) ($V = -150$ mV and $I = 200$ pA). Scale bar is 10 nm.

Figure 13(d) are upper, middle and lower panels representing histograms of the Dirac point energy maps in Figures 13(a)–(c) respectively.

Detailed description of the embodiments

Topological Dirac semimetals (TDS) are three-dimensional analogues of graphene, with linear electronic dispersions in three dimensions. The inventors have found a method for forming a topological Dirac semimetal layer on a range of substrates, including electrically insulating materials, which allows the characterisation and analysis of the properties of these Dirac semimetals, and exploitation of their unique electronic properties, such as in an electronic component.

Example 1

This example demonstrates the formation of high quality, c-axis oriented thin film Na₃Bi on insulating Al₂O₃ [0001] substrates. It will be appreciated that a wide variety of different substrates can be selected for formation of the Na₃Bi Dirac semimetal layer. However, in this instance and as discussed above, the use of insulating Al₂O₃ is advantageous as it allows the properties of the Na₃Bi to be analysed in a controlled manner in the absence of a conductive layer.

Films are grown using the two-step method of an embodiment of the present invention. Briefly, a thin (2 nm) nucleation layer is deposited under simultaneous Bi and Na flux at low (120 °C) temperature, followed by additional growth at a higher final temperature of between 250 and 390 °C. The resultant films were subsequently characterized using low temperature magneto-transport and scanning tunnelling microscopy and spectroscopy (STM and STS) in situ in ultrahigh vacuum (UHV).

To form the films, $\text{Al}_2\text{O}_3[0001]$ substrates were annealed in air at 1350 °C for three hours, and subsequently annealed at 1050 °C in pure O_2 atmosphere, to provide an atomically flat surface for film growth. Ti/Au contacts (5/50 nm) were deposited through a stencil mask onto the corners of the substrate, and wirebonded to a contact
5 busbar on the sample plate. Substrates were introduced into ultra-high vacuum (UHV) immediately after wire bonding to minimise exposure to ambient conditions, and then annealed at 400 °C for 1 hour to remove adsorbed atmospheric species.

Effusion cells were used to simultaneously evaporate elemental Bi (99.999%, Alfa Aesar) in an overflux of Na (99.95%, Sigma Aldrich) with a Bi:Na flux ratio not less
10 than 1:10, calibrated by quartz microbalance. The Bi rate used was about 0.03 Å/sec, and Na was about 0.7 Å/sec. The pressure during growth was less than 3×10^{-9} Torr.

For each sample, the first 2 nm of Na_3Bi was deposited with the substrate temperature at 120 °C. The substrate temperature was then increased to a value ranging between 250-390 °C over the next 5 nm of film growth as determined by the
15 bismuth deposition rate. Once the desired temperature was reached, the remaining 13 nm of film was grown to form a 20nm thick film. The samples were then annealed at the growth temperature for an additional 10 minutes in Na flux only, before cooling to room temperature for subsequent transfer to the analysis chamber. An additional sample grown only at 330 °C (without the low temperature nucleation layer) was of similarly
20 inferior quality to the samples grown at hot temperatures above 380 °C (or much thinner than expected), indicating the importance of the low temperature nucleation layer.

Sample characterization was carried out in a Createc LT-STM operating in ultra-high vacuum (UHV) (10^{-11} Torr) with base temperature 4.8K. A PtIr STM tip was prepared and calibrated using an Au(111) single crystal and the Shockley surface state
25 before all measurements. STM differential conductance (dI/dV) was measured using a 5 mVrms AC excitation voltage (673 Hz) that was added to the tunnelling bias. Differential conductance measurements were made under open feedback conditions with the tip in a fixed position above the surface. The data in **Figure 1** was analysed and prepared using WSxM software. LEED measurements were done with the commercial 8" system
30 (OCI) on the soft X-ray endstation of the Australian synchrotron. Transport

measurements were carried out in the Createc LT-STM using van der Pauw geometry and standard DC electrical measurements in a magnetic field up to 0.5T at 5K.

Figure 1 shows the crystalline quality of Na₃Bi thin films formed according to the present invention. As shown in **Figure 1**, the structure comprises single crystal Al₂O₃ [0001] pre-patterned with electrical contacts in van der Pauw geometry, and the Na₃Bi is deposited on top, making electrical contact. **Figure 1(a)** inset shows the crystal structure of Na₃Bi. **Figure 1(b)** shows STM topography at a temperature of 5 K, showing a large area (about 80x80 nm) atomically flat terrace, with a step height of 4.7 Å, consistent with the half-unit cell distance of 4.83 Å between NaBi planes. Atomic resolution of the surface (inset) shows a (1x1) termination with the expected in-plane lattice constant of 5.45 Å. The 1x1 triangular lattice rather than hexagonal lattice is strongly suggestive that the surface is Na-terminated. Figure 1c) shows low energy electron diffraction (LEED) image taken at 17.5 eV. The low background and sharp hexagonal diffraction pattern confirm that the (1x1) structure is coherent across the LEED spot size of about 200 µm. Faintly visible is the same pattern rotated 30°, indicating the presence of a small fraction of the sample with that alignment. Similar quality LEED patterns were observed on samples grown across the range of final temperatures tested. **Figure 1(d)** shows STS (differential conductance vs bias voltage) averaged over an area of 400 nm². STS reflect the energy dependent local density of states of the sample. The sharp dip near zero energy reflects the dip in LDOS at the Dirac point, with Dirac point energy $E_D = -35$ meV, consistent with the n-type doping measured via transport. This value in conjunction with carrier density measured via transport (see below, about 3.8×10^{18} cm⁻³) can be used to estimate the average Fermi velocity in the samples, $v_F = 1.4 \times 10^5$ m/s, in reasonable agreement with the value 2.4×10^5 m/s obtained from ARPES.

The *ex situ* prepared corner contacts illustrated in **Figure 1(a)** allows van der Pauw measurements of the longitudinal and transverse resistivity ρ_{xx} and ρ_{xy} in magnetic field up to 0.5 T at a temperature of 5 K, from which the Hall carrier density $n = (e d \rho_{xy} / dB)^{-1}$ and the Hall mobility $\mu = (n e \rho_{xx})^{-1}$ can be determined, where $d = 20$ nm is the thickness, and e is the elementary charge. **Figure 2** shows μ (**Figure 2(a)**) and n (**Figure 2(b)**) plotted against the final growth temperature for each sample. Samples with a final temperature above 380 °C had a substantial reduction in measured mobility,

and intermittent electrical contact problems, probably indicating dewetting of the film on the substrate at these growth temperatures. Therefore these samples were discounted from further analysis. A trend of decreasing n and increasing μ was exhibited with increasing growth temperature, up to 360 °C. The highest measured mobility (6,310
 5 cm^2/Vs) and lowest carrier density ($4.6 \times 10^{17} \text{ cm}^{-3}$) were measured on a sample grown at 345 °C. This lowest carrier density is still about an order of magnitude larger than the lowest reported bulk crystal value in literature. However, the observed range of doping (4.6×10^{17} to $1.7 \times 10^{19} \text{ cm}^{-3}$) falls within the range observed in bulk crystal values reported in literature. For the desired ambipolar effect to be observable in the operable
 10 range of the SiO_2 voltage gate, the n-type minimum carrier density should not exceed $4.4 \times 10^{15} \text{ cm}^{-3}$. Given the Fermi wavevector $k_F = (6\pi_2 n/g)^{1/3}$, the mean free path L can be calculated, which ranged between 75-135 nm for the prepared samples.

Increasing mobility with decreasing carrier density is consistent with expectations assuming that the impurities that give rise to doping are also responsible for the
 15 disorder limiting the mobility. To better understand the relationship between the mobility and carrier density, these parameters were plotted against one another (**Figure 2(c)**). The hashed region is the theoretical prediction for a TDS using the random phase approximation (RPA) assuming that all the impurities are dopants of a single sign, i.e. the impurity density n_{imp} equals the carrier density n . The only materials parameters are
 20 the fine structure constant $\alpha = e^2/k\hbar v_F$ and the spin/valley degeneracy product $g = 4$. Based on the results, the effective fine structure constant for Na_3Bi was estimated to be between $\alpha = 0.06$ to 0.17 , based on a κ of about $120 \pm_{30}^{10}$, and a Fermi velocity between $v_F = 1.4 \times 10^5 \text{ m/s}$ from STS (**Figure 1(d)**), and $v_F = 2.43 \times 10^5 \text{ m/s}$ from single crystal ARPES experiments.

25 This data lies close to, but about an order of magnitude below the theoretical prediction of the mobility. There are several possible reasons for this. First, an incorrect value for α may have been used. If α is taken as a fit parameter in the theory, the best fit to the data (line in **Figure 2(c)**) yields $\alpha = 0.44$, 2.5-7 times higher than expected. Second, theory disregards other contributions to disorder in the prepared
 30 samples, notably point defects, structural incoherence due to grain boundaries or strain effects, all of which should be expected to some degree for a large area, van der Waals epitaxial film. Third, the theory assumes $n_{\text{imp}} = n$ however the presence of both positive

and negative charge carriers will cause $n_{\text{imp}} > n$. For the latter two reasons, the theoretical prediction is an upper bound.

Figure 3(a) shows the transverse MR $\rho_{xx}(B)=\rho_{xx}(B = 0)$ plotted as a function of perpendicular applied field, labelled according to the final growth temperature. An overall positive magnetoresistance (MR) is observed, with a cusp below about 0.1T. For field values above 0.1T the data are well described by a quadratic dependence:

$$\rho_{xx}(B) = \rho_{xx}(B = 0)[1 + A(\mu B)^2] \quad (1)$$

Figure 3(b) shows the prefactor A determined from fits to Eqn. 1 plotted as a function carrier density n.

In the simplest instance, a single band, two-dimensional system evinces zero transverse MR. There are several possible origins for the observed quadratic MR. Without wishing to be bound by theory, the inventors postulate the following. Multiple conduction bands of differing mobility and/or carrier density can produce quadratic low-field MR, however this possibility is excluded due to the close proximity of the Dirac point as measured by both Hall effect and STS. Another possible explanation is spatial inhomogeneity, for example in carrier density, known to give a quadratic MR at low field. However, to our knowledge all theories of spatial inhomogeneity give $A < \frac{1}{2}$. This strict limit contrasts with the values we have obtained in the present work, ranging from about 0.1 to 4.5 (**Figure 3(b)**). Notably, measurements on single crystal samples show similar unusually large quadratic MR coefficients $A > \frac{1}{2}$ in the low field regime ($\mu B \ll 1$). Recent theoretical efforts have been made to understand charge inhomogeneity in a Dirac semimetal system and propose that in the spatially inhomogeneous regime the Hall carrier density overestimates the average carrier density, and hence the mobility is underestimated and A overestimated. While the inhomogeneous theory can be made to be consistent with both the observed mobility and the large apparent A, this explanation seems very unlikely for the prepared samples.

The inhomogeneous regime is very small in Na_3Bi (with α about 0:1); the characteristic carrier density inhomogeneity is only a few percent of the impurity density, requiring donor and acceptor concentrations to also be balanced within a few percent. We find this scenario unlikely to occur generically in all our samples across a range of

growth conditions, where the observed Hall carrier density varies by almost two orders of magnitude.

Figure 3(c) shows the MR after subtracting the quadratic MR from fits to Eqn. 1). The low field data is replotted as the change in 2D conductivity ($\Delta\sigma = \sigma(B) - \sigma(B = 0)$), in units of e^2/h . The low-field MR data are well described by the strong spin-orbit coupling limit of the Hikami-Larkin-Nagaoka (HLN) formula:

$$\sigma(B) - \sigma(0) = \frac{1}{2} \frac{e^2}{2\pi^2\hbar} \left(\ln\left(\frac{B_\phi}{B}\right) - \Psi\left(\frac{1}{2} + \frac{B_\phi}{B}\right) \right)$$

where the only fit parameter is the phase coherence field B_ϕ . **Figure 3(d)** shows the phase coherence length as a function of carrier density for the various films:

$$L_\phi = \sqrt{\frac{\hbar}{4\pi B_\phi}}$$

In each instance the coherence length is substantially larger than the thickness of the samples (20 nm), consistent with the assumption of two-dimensionality. Efforts to fit this data using a three-dimensional theory for weak localization yielded poor fits regardless of the limiting cases in temperature and magnetic field used, again illustrating a deviation between practice and theory. 3D weak anti-localization in bulk crystals of TDS have previously been predicted. However, this was for a bulk crystal and not a thin film. The observations of 2D weak anti-localization in these films is a new and unexpected property. Accordingly, in certain embodiments, the topological Dirac semimetal layer in the structure exhibits 2D weak anti-localisation.

The coherence length L_ϕ at densities above $6 \times 10^{18} \text{ cm}^{-3}$ exceeds $1\mu\text{m}$, but is suppressed in lower carrier density samples, a phenomena that has been previously observed in other Dirac materials such as graphene and the Dirac surface state of bismuth selenide. The fact that the obtained weak field MR is well described by the HLN formula indicates that Na_3Bi films of the present invention are well described by non-interacting Dirac cones, i.e. intervalley scattering is weak.

In summary, the growth of electrically isolated, highly oriented, large area thin film Na_3Bi on $\alpha\text{-Al}_2\text{O}_3$ [0001] substrates has been demonstrated. The high sample

quality is reflected in a record high mobility and near-ideal weak anti-localization behaviour. High quality TDS thin films on insulators open a route toward novel topological phenomena and devices, including electric field control via gate electrodes, as illustrated in Example 2.

5 Example 2

Figure 4(a) and **Figure 4(b)** illustrate a stencil mask 17 and prepared substrate structure 10 used in an embodiment of the present invention. The substrate structure 10 includes a sample plate 11. An insulating substrate was applied over it to electrically insulate the created structure. Next a back gate electrode 14 is provided on top of which
10 an Si:SiO₂ substrate is placed.

Ti/Au contacts (5/50 nm) 18 were deposited through a stencil mask 17 onto the solvent-cleaned pieces of 1µm oxide thickness Si:SiO₂ substrate pieces 16. A stencil mask 17 in the Hall bar pattern was affixed to the substrate surface, and the electrodes were subsequently wire bonded to a contact busbar on the sample plate. Substrates
15 were introduced into UHV immediately after wire bonding to minimise exposure to ambient conditions, and then annealed at 450 °C for 90 minutes to remove adsorbed atmospheric species.

Effusion cells were used to simultaneously evaporate elemental Bi (99.999%, Alfa Aesar) in an over flux of Na (99.95%, Sigma Aldrich) with a Bi:Na flux ratio not less
20 than 1:10, calibrated by quartz microbalance. The Bi deposition rate was about 0.03 Å/sec, and the Na deposition rate was about 0.7 Å/sec. The pressure during growth was less than 3×10^{-9} Torr.

For each sample, the first 2 nm of Na₃Bi was deposited with the substrate temperature at 120 °C. The substrate temperature was then increased to 345 °C over
25 the next 5 nm of film growth as determined by the bismuth deposition rate. Once a temperature of 345 °C was reached, the remaining 13 nm of film was grown, thus forming the structure illustrated in Figure 4b. The samples were annealed at the growth temperature for an additional 10 minutes in Na flux only, before cooling to room temperature for subsequent transfer to the analysis chamber. Sample characterization
30 was carried out in a Createc LT-STM operating in ultra-high vacuum (UHV) (10^{-11} Torr)

with base temperature 4.8K using a Hall bar geometry and standard DC electrical measurements in a magnetic field up to 1T at 5K.

In **Figure 5**, the Hall carrier density $1/n = edR_{xy}/dB$, rescaled by sample thickness $t = 18\text{nm}$, is plotted against the gate voltage applied across the SiO_2 dielectric. For sufficient top surface coverage of molecular electron acceptor F4-TCNQ, $+0.85\text{nm}$ and $+1.08\text{nm}$, the ambipolar, n- to p-type transition is clearly observed at $+50\text{ Vg}$ and -35 Vg , respectively.

Example 3

The example reports results relating to controlling the bandgap of ultra-thin topological Dirac semimetal Na_3Bi .

Ultrathin Na_3Bi films were grown in a ultra-high vacuum (UHV) (10^{-10} Torr) molecular beam epitaxy (MBE) chamber and then transferred immediately after the growth to the interconnected Createc LT-STM operating in UHV (10^{-11} Torr) for STM/STS measurements at 5 K. For Na_3Bi film growth effusion cells were used to simultaneously evaporate elemental Bi (99.999%, Alfa Aesar) in an overflux of Na (99.95%, Sigma Aldrich) with a Bi:Na flux ratio not less than 1:10, calibrated by quartz microbalance. The Bi rate used was $\sim 0.03\text{ \AA/s}$, and Na was $\sim 0.7\text{ \AA/s}$. The pressure during growth was less than 3×10^{-9} Torr.

Growth on Si(111) - To prepare an atomically flat substrate, a Si(111) wafer was flash annealed in order to achieve 7×7 surface reconstruction, confirmed using STM and low energy electron diffraction (LEED). During the growth, the substrate temperature was 345°C for successful crystallization. At the end of the growth the sample was left at 345°C for 10 min in a Na overflux to improve the film quality. The sample was cooled to 315°C in Na overflux to minimise Na vacancies due to desorption at elevated temperature before cooling to room temperature.

A PtIr STM tip was prepared and calibrated using an Au(111) single crystal and the Shockley surface state at $\sim 0.5\text{V}$ and flat LDOS near the Fermi level before all measurements. STM differential conductance (dI/dV) was measured using a 5 mV AC excitation voltage (673 Hz) that was added to the tunnelling bias. Differential

conductance measurements were made under open feedback conditions with the tip in a fixed position above the surface.

Figure 6 shows the successful growth of a continuous few atomic layer thick Na_3Bi film grown via molecular beam epitaxy on a $\text{Si}(111)$ substrate. The unit cell of Na_3Bi is shown with the c-axis height of 0.96 nm (reflecting the thickness of a (001) film). The zero of the height scale represents the $\text{Si}(111)$ substrate. The majority of the film has a thickness of 0.96 nm and 1.44 nm, demonstrating continuous film with atomically flat terraces larger than 40nm.

Scanning tunnelling spectroscopy, which measures the differential conductance with respect to the bias voltage (reflecting the energy dependent local density of states of the material) was measured on the film at different uniform and atomically flat regions of the sample away from any step edges. **Figure 7(a)** shows the differential conductance, dI/dV , at one such region at different tip-height separations. The black curve represents the dI/dV spectra taken at tunnelling parameters ($V = -300\text{mV}$, $I = 500\text{pA}$, $V_{\text{rms}} = 5\text{mV}$, $f = 673\text{ Hz}$). The spectra lines represents an increase in the tip-sample separation of 0.3 nm, 0.9 nm, 1.5 nm and 2.7 nm respectively with respect to the initial tip-sample separation. Changing the tip-sample separation changes the electric field induced from the potential difference between tip and sample. Initially the system has a dI/dV that possesses a sharp dip near the zero in energy but does not go all the way to zero (which is taken as 0.03 in the dI/dV scale and represents the noise floor of the instrument). This behaviour reflects a semi-metal (with zero bandgap) expected for bulk topological Dirac semimetal Na_3Bi . As the tip is moved further from the sample (i.e. decreasing the electric field) a distinct zero in the differential conductance emerges that reflects the opening of a bandgap. As the electric field is decreased, this zero increases in width with monotonic behaviour. The rapid increase in intensity below the zero in energy (which reflects the Fermi energy) represents the valence band edge and the rapid increase above zero represents the conduction band edge. The difference between these two values reflects the overall size of the bandgap. **Figure 7(b)** plots the bandgap as a function of relative tip-sample separation for the dI/dV spectra in **Figure 7(a)**. In this Figure, the bandgap is extracted from the onset of the conduction and valence bands in each spectra. A clear trend emerges as the tip-samples separation increases (i.e. electric field decreases) the bandgap transitions from

a semi-metal state (0 mV bandgap) to an insulator which saturates at a bandgap value of 300mV.

This example demonstrates for the first time, electric field control of the bandgap in a topological Dirac semimetal, with a transition from insulator with a bandgap well
5 above room temperature to semimetal (or even non-trivial insulator phase).

Example 4

This example reports data from high quality thin films of Na₃Bi grown on amorphous Si:SiO₂ substrates. The films were grown using the two-step thermal process.

10 Ti/Au contacts (5/50 nm) were deposited through a stencil mask onto solvent-cleaned pieces of 1µm oxide thickness Si:SiO₂ substrate pieces. A stencil mask in the Hall bar pattern was affixed to the substrate surface, and electrodes were subsequently wire-bonded to a contact busbar on the sample plate. **Figure 4(b)** is a sample diagram, showing the stencil mask used to define the Hall bar geometry for thin film growth on
15 the Si:SiO₂ substrate. Substrates were introduced into UHV immediately after wire bonding to minimise exposure to ambient conditions, and then annealed at 450°C for 90 minutes to remove adsorbed atmospheric species.

Effusion cells were used to simultaneously evaporate elemental Bi (99.999%, Alfa Aesar) in an overflux of Na (99.95%, Sigma Aldrich) with a Bi:Na flux ratio not less
20 than 1:10, calibrated by quartz microbalance. The Bi rate used was about 0.03_A/sec, and Na was about 0.7_A/sec. The pressure during growth was less than 3×10^{-9} Torr.

For each sample, the first 2 nm of Na₃Bi was deposited with the substrate temperature at 120°C. The substrate temperature was then increased to 345°C over the next 5 nm of film growth as determined by the bismuth deposition rate. After the
25 remaining 13 nm of film was grown, the samples were annealed at the growth temperature for an additional 10 minutes in Na flux only, before cooling to room temperature for subsequent transfer to the analysis chamber. Sample characterization was carried out in a Createc LT-STM operating in ultra-high vacuum (UHV) (10^{-11} Torr) with base temperature 4.8K using a Hall bar geometry and standard DC electrical
30 measurements in a magnetic field up to 1T at 5K. The sample was transferred back to

the growth chamber for sequential deposition of molecular dopant F4-TCNQ (Sigma-Aldrich) onto the surface, and subsequent transport characterization. The organic molecule F4-TCNQ acts as a p-type dopant due to its high electron affinity (as previously discussed in Example 2) and was deposited onto the surface of the as-grown Na₃Bi to induce a depletion layer at the surface of the film, before further modulation of the carrier density using the SiO₂ back gate.

Figure 8 is a Scanning tunneling microscopy (STM) image showing the morphology of a sample 50 x 50 nm, with 2 nm vertical scale, $V_{\text{bias}} = -300$ mV, $I = 200$ pA. The observable step edges have height of 4.2 Å. **Figure 9** demonstrates the effects of depositing F4-TCNQ on the sample surface. The 'as-grown' Na₃Bi film (circles) has an intrinsic ($V_g = 0$) n-type carrier density of $5.7 \times 10^{12} \text{ cm}^{-2}$, calculated from the low-field ($B < .05$ T), linear Hall response: $n = 1/(e d\rho_{xy}/dB)$. This corresponds to a Hall mobility of 0.7 T^{-1} ($\mu = \sigma_{xx}/ne$). The roughly linear dependence of the gate dependent carrier density in b) confirms that the sample is above the Dirac point, away from the charge puddling regime. Two features are apparent when 6.2 Å of F4-TCNQ is deposited on the film surface (squares). The conductivity of the sample is reduced by more than an order of magnitude, and the gate dependence reveals a minimum conductivity value as expected for a Dirac system. This is correlated with an asymptotic divergence in carrier density, caused by a change in sign of the slope of the low-field $\rho_{xy}(B)$ dependence.

Before and after depositing F4-TCNQ, the full-field (1T) MR shows anomalously large quadratic response. For the sample as-grown, the $\rho_{xy}(B)$ component is completely linear, indicating unipolar n-type response. This is in contrast to what is observed upon deposition of F4-TCNQ. **Figure 10(a)** shows the gate dependence of the zero-field resistivity after deposition of F4-TCNQ. In the plot, $\circ$ the line shows the measured values and the points represent the theoretical fit values. The plot shows a maximum at $V_g = -20$ V, as expected for a Dirac-like system ($\circ$). There are several notable features in the gate dependent Hall response, shown in **Figure 10(b)**. In the measurement convention adopted in Figure 10(b), a positive (negative) ρ_{xy} slope corresponds to electron (hole) type conduction. As can be seen, at low-field ($B < 0.25$ T) there is a clear transition from electron- to hole-like response as the gate is modulated from positive to negative bias. Furthermore, when the low-field response becomes hole-like (negative slope), the overall signal becomes non-linear, which indicates contributions from

multiple carrier types. Reasonable fits to the $\rho_{xy}(B)$ data using the two-carrier model captured several essential features, namely the curvature, indicating that the mobility of the hole-like channel is much higher than the electron-like channel: however the gate dependence of the total carrier number (e.g. the sum of the two contributions, $n + p$) is
 5 qualitatively incorrect, indicating that the number of electrons in the sample is increasing with negative applied gate voltage.

The anomalously large coefficient of the quadratic magnetoresistance, the change in slope sign, and non-linearity of the Hall response, all indicate that these samples are in the charge inhomogeneous regime near the Dirac point. For the data
 10 taken following the F4-TCNQ deposition, the MR response at each applied gate voltage is fitted using three global fit parameters: the proportionalities between electron/hole conductivity and $n^{4/3}$, denoted A_e , A_h , and n_{rms} , the measure of the disorder induced carrier density fluctuations. The carrier density n is taken as the only V_g dependent fit parameter. Normally with a Si:SiO₂ capacitive gate, the change in carrier density can be
 15 treated as proportional to the change in gate voltage, Δn is proportional to ΔV_g . However in this instance a non-linear gate response on the negative side was observed, which is attributed to charge traps likely introduced as a result of the exposure to Na flux intrinsic to the sample growth process.

Figure 10(c) and **Figure 11** show the results of using this theory to model the
 20 measured gate response of these samples. The measured zero (magnetic) field conductivity shows a non-zero minimum value of $5.6 \text{ e}^2/h$. We get the closest agreement between the experiment and theory (**Figure 10(b)** and **Figure 10(c)**) when there is asymmetry between the electron and hole mobilities, and that the appropriate proportionality constant is between σ_{xx} and $n^{4/3}/n_{imp}$. For electrons and holes, these
 25 proportionalities were found to be $A_e = 0.009$ and $A_h = 0.11 \text{ e}^2/h / 10^{15} \text{ cm}^{-3}$, respectively. The final global fit parameter is the Gaussian width that determines the 'size' of the charge inhomogeneous regime $n_{rms} = 218 \times 10^{15} \text{ cm}^{-3}$.

This can be related to the density of impurities:

$$n_{imp} = \frac{3\sqrt{2\pi}}{\sqrt{g}\alpha^{3/2}} \frac{n_{rms}}{\sqrt{15}} = 1.14 \times 10^{19} \text{ cm}^{-3}$$

where $g = 4$ and $\alpha = 0.07$.

The hole conductivity coefficient is an order of magnitude larger than that for electrons: this interpretation is in qualitative agreement with the non-linear Hall response on the p-type side of the charge neutrality point: the high mobility, low field slope is p-type, but the (low mobility carrier) curvature at higher field is n-type. This observation could be taken as evidence that the Dirac point in this material is generated by the band inversion of the S and P states of different total angular momentum.

The values of the carrier density from the theory are all n-type, but are within the Gaussian profile of the inhomogeneous regime, characterized by n_{rms} . This is shown in **Figure 11**, where the (only) V_g dependent fit parameter n is plotted (see the plotted line), indicating that the sample remains on the n-type side of the Dirac point, but is in the inhomogeneous regime. To make this more apparent, the Gaussian profile defined by the fit parameter $n_{\text{rms}} = 218 \times 10^{15} \text{ cm}^{-3}$ is plotted on the carrier density axis. The (dashed) Gaussian envelope (arbitrary height) is the size of the charge inhomogeneous region determined by the global fit parameter n_{rms} . The dots are the as-grown carrier density for comparison. The overlap of the profile and the carrier density is a rough indication of how far into the inhomogeneous regime the sample approaches. The conductivity minimum at $V_g = -20 \text{ V}$ (**Figure 9(a)**) does not correspond to a change in carrier sign; this counterintuitive observation is not unexpected in the case of this huge asymmetry between electron and hole conductivities.

In summary, this example demonstrates the growth of high quality, large area thin film of Na_3Bi directly on amorphous SiO_2 . The gate dependent MR shows two distinct features, a non-zero minimum of the zero-field conductivity, and a non-linear Hall response indicating the presence of electrons and holes with different mobilities. These fits indicate that our samples are on the n-type side of the Dirac point, in the inhomogeneous regime, and unexpectedly, that the hole conductivity in this material is two orders of magnitude higher than the electron conductivity.

Example 5

This example reports potential fluctuations in Fermi energy in three-dimensional topological Dirac semimetals TDS Na_3Bi using a scanning tunneling microscope (STM).

TDS such as Na_3Bi and Cd_3As_2 express the pseudorelativistic physics of two-dimensional Dirac material graphene, but extended to three dimensions. TDS can yield ultra-high mobilities as well as new physics such as the chiral anomaly. The close approach of the Fermi energy E_F of a Dirac semimetal to the Dirac point E_D uncovers new physics such as velocity renormalization, and the Dirac plasma at $|E_F - E_D| < k_B T$, where $k_B T$ is the thermal energy. However, this close approach can be limited by fluctuations in the Fermi energy due to charge puddling. Potential fluctuations arise in Dirac semimetals when the Fermi energy E_F measured relative to the Dirac point energy E_D approaches zero, meaning the carrier density tends to zero and metallic screening disappears. Poorly screened disorder induces spatial fluctuations in the local E_D and hence fluctuations ΔE_F , corresponding to local electron and hole “puddles”. The carriers in puddles in turn screen the disorder, with ΔE_F determined self-consistently by the disorder and the screening properties of the Dirac materials. Puddles have been visualized in graphene using scanning single electron transistor microscopy and scanning tunnelling spectroscopy, where the fluctuations are largely governed by the underlying substrate, and have also been measured in the Dirac surface state of a topological insulator.

This example reports the use of 20 nm Na_3Bi thin films grown via molecular beam epitaxy (MBE) on both semiconducting $[\text{Si}(111)]$ and insulating $[\alpha\text{-Al}_2\text{O}_3(0001)]$ substrates in ultra-high vacuum (UHV) to probe ΔE_F fluctuations using scanning tunneling microscopy and spectroscopy (STM/STS).

Figure 12(a) shows a large area (400 nm x 380 nm) topographic STM image of a thin 20nm film of Na_3Bi on $\text{Si}(111)$, with several atomically flat terraces >100 nm in size. The inset to **Figure 12(a)** reveals the (1 x 1) Na-terminated atomic lattice ($a = 5.45 \text{ \AA}$) with an individual Na vacancy. **Figure 12(b)** (45 nm x 45 nm taken immediately after growth) and **Figure 12(c)** (30nm x 30nm taken seven days after growth) show the topography of two atomically flat regions away from step edges or the screw dislocations seen in **Figure 12(a)**. **Figure 12(d)** shows an atomically flat region (30 nm x 30 nm) of Na_3Bi grown on sapphire ($\alpha\text{-Al}_2\text{O}_3(0001)$). Whilst atomically flat regions of Na_3Bi up to 100 nm x 100 nm can be obtained on $\text{Si}(111)$, sparse defect cluster sites (few per 100 nm x 100 nm) give rise to tip-induced ionization ring features that will be

discussed further below. This necessitated focusing on smaller areas free of ionization rings in order to unambiguously determine the variation in Dirac point.

Figure 12(e) shows area-averaged scanning tunneling spectra (STS) of the Na₃Bi film. STS measures the differential conductance dI/dV as a function of sample bias V , proportional to the local density of states (DOS) at energy eV relative to E_F . STS was performed at points on a grid encompassing the entire regions shown in **Figure 12(b)** and **Figure 12(c)**, along with two other regions not shown. **Figure 12(e)** shows the averaged spectra of these four areas. In **Figure 12(e)** the “as-grown” spectra (i) corresponding to the region in **Figure 12(b)** and spectra (ii) - topography not shown - were taken immediately after growth, whilst spectra (iii) corresponding to the region in **Figure 12(c)** and spectra (iv) - topography not shown - were taken one week after growth. Feature E_D reflects the Dirac point, which corresponds to the minimum in the LDOS, and D represents the resonance feature. Two key features are prominent in all spectra: a distinct minimum in the DOS corresponding to the Dirac-point energy (E_D), and a resonant feature ~ 35 meV below E_D , labelled D. As-grown, the Dirac point is located ~ 20 meV above the Fermi level indicating p -type doping. Similar doping (~ 25 meV) has been reported on similar thickness Na₃Bi films on Si(111) measured with angle-resolved photoelectron spectroscopy (ARPES), validating our assumption that the minimum in the DOS reflects the Dirac point. Seven days after growth, the Dirac point has shifted to approximately 15 meV below the Fermi level, reflecting a gradual global n -type doping of the Na₃Bi due to the adsorption of atomic species present in UHV. This adsorption results in the formation of intermittent impurity clusters on the surface, as such all topography and spectroscopic measurements were deliberately performed away from such sites. The resonance feature D is unambiguously tied to E_D , and not to the E_F , as the relative energy shift of D with respect to E_D remains unchanged within experimental accuracy during the transition from p -type to n -type doping.

The spatial variation of the Dirac point energy, E_D , can be found by tracking the position of the minimum differential conductance in STS (alternatively, the shift in the defect resonance D in each spectrum gives similar results). **Figure 13(a)** and **Figure 13(b)** show the spatial variation of E_D for regions ‘A’ and ‘B’ corresponding to **Figure 12(b)** and **Figure 12(c)** respectively. In both Dirac-point energy maps, it can be seen that a clear, continuously connected local potential modulation emerges, correlated on a

scale much larger than the crystal lattice or point-spectroscopy grid. This modulation in E_D represents the puddling of charge density at the surface. The variation in E_D is found to be correlated with the individual Na vacancy sites which possess a more positive Dirac point energy, identifying the Na vacancies as acceptors and a significant source of charge disorder. In addition, **Figure 13(c)** shows the local E_D of 20 nm Na_3Bi on $\alpha\text{-Al}_2\text{O}_3(0001)$ (labelled Region C) which possesses a larger n -type doping. The upper, middle and lower panels of **Figure 13(d)** show histograms of E_D relative to E_F for the scans in **Figures 13(a)-(c)** respectively. From spatial autocorrelation analysis of the puddle maps, we determine spatial coherence lengths ξ of 13.4 ± 5.2 nm, 9.3 ± 2.4 nm and 5.1 ± 1.9 nm for Regions A, B and C respectively. The observed histograms of E_D have mean values 19.7 ± 1.7 meV (Region A), -15.4 ± 1.3 meV (Region B) and -47.2 ± 0.6 meV (Region C), and standard deviations ΔE_F of 5.6 meV, 4.2 meV and 3.5 meV respectively. These values are comparable to the 5.4 meV observed for graphene on h-BN. However, undersampling results in an underestimate in the magnitude of ΔE_F by a factor $(L/\xi)^2/[(L/\xi)^2 - 1]$ where L is the scan size in each region, hence the corrected ΔE_F values are 6.1 meV and 4.6 meV for Regions A and B respectively, whilst Region C remains essentially unchanged due to the small coherence length.

This example has demonstrated, using scanning tunneling microscopy and spectroscopy, the existence of charge puddles in the topological Dirac semimetal, Na_3Bi . The ultra-low Dirac-point energy fluctuations, which occur over length scales of approximately 5-15 nm, are of the order of 4-6 meV = 40-70 K well below room temperature and comparable to the highest quality graphene on h-BN. The ultra-low potential fluctuations in this 3D Dirac system will enable the exploration of novel physics associated with the Dirac point.

It will be understood that the invention disclosed and defined in this specification extends to all alternative combinations of two or more of the individual features mentioned or evident from the text or drawings. All of these different combinations constitute various alternative aspects of the invention.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A method of altering the charge carrier density in a topological Dirac semimetal, the method comprising:

providing a structure including:

5 a conductor,

an insulating layer,

a topological Dirac semimetal layer separated from the conductor by at least the insulating layer,

at least one electrode contacting the topological Dirac semimetal layer;

10 and

applying a voltage to the conductor relative to the at least one electrode to subject at least a portion of the topological Dirac semimetal layer to an electric field to alter the charge carrier density of the topological Dirac semimetal layer.

2. The method of claim 1, wherein the method includes switching the voltage
15 between a first voltage and a second voltage to increase or decrease the charge carrier density in the topological Dirac semimetal layer.

3. The method of any one of the preceding claims, wherein the topological Dirac semimetal layer is formed from a material of the form $A_3\text{Bi}$, where A is an alkali metal.

4. The method of claim 3, wherein the thickness of the $A_3\text{Bi}$ layer is at least 15 nm.

20 5. A method of altering the band gap of a topological Dirac semimetal, the method comprising:

providing a structure including:

a conductor,

an insulating layer,

a topological Dirac semimetal layer separated from the conductor by at least the insulating layer,

at least one electrode contacting the topological Dirac semimetal layer;
and

5 applying a voltage to the conductor relative to the at least one electrode to subject at least a portion of the topological Dirac semimetal layer to an electric field to alter the band gap of the topological Dirac semimetal layer.

6. The method of claim 5, wherein the method further includes varying a strength of the electric field to vary the band gap.

10 7. The method of claims 5 or 6, wherein the topological Dirac semimetal layer is formed from a material of the form A_3Bi , where A is an alkali metal.

8. The method of claim 3, 4, or 7, wherein the alkali metal is Na.

9. The method of any one of claims 5 to 7, wherein the topological Dirac semimetal layer is an ultrathin film and has a thickness of 2 unit cells or less.

15 10. The method of any one of the preceding claims, wherein the method further includes:

providing at least two electrodes in contact with the topological Dirac semimetal, the at least two electrodes spaced apart from each other and between which current may flow from a current or voltage source through the topological Dirac semimetal layer;

20 wherein when current is passing between the at least two electrodes, the step of subjecting the topological Dirac semimetal to an electric field alters the magnitude and/or direction of the current passing between the at least two electrodes.

11. The method of any one of the preceding claims, wherein the method further includes providing a layer for donating or accepting charge carriers from the topological

25 Dirac semimetal layer.

12. The method of any one of the preceding claims, wherein the method further include providing a capping layer for preventing oxidation of the topological Dirac semimetal layer.

13. A structure including:

5 means for generating an electric field,

a topological Dirac semimetal layer,

wherein the topological Dirac semimetal layer is non-conductively separated from the means for generating the electric field, and the means for generating the electric field is configured to apply the electric field to at least a portion of the topological Dirac

10 semimetal layer.

14. A structure for altering the charge carrier density in a topological Dirac semimetal, the structure comprising:

a conductor,

an insulating layer;

15 a topological Dirac semimetal layer separated from the conductor by at least the insulating layer, and

at least one electrode contacting the topological Dirac semimetal layer,

wherein the conductor and the at least one electrode are configured to apply an electric field to at least a portion of the topological Dirac semimetal layer to alter the

20 charge carrier density of the topological Dirac semimetal layer.

15. The structure of claims 13 or 14, wherein the topological Dirac semimetal layer is formed from a material of the form A_3Bi , where A is an alkali metal.

16. The structure of claim 15, wherein the thickness of the A_3Bi layer is at least 15 nm.

25 17. A structure for altering the band gap of a topological Dirac semimetal, the structure comprising:

a conductor,

an insulating layer;

a topological Dirac semimetal layer separated from the conductor by at least the insulating layer, and

5 wherein the conductor is configured to apply an electric field to at least a portion of the topological Dirac semimetal layer to alter the band gap of the topological Dirac semimetal layer.

18. The structure of claim 17, wherein the topological Dirac semimetal layer is formed from a material of the form A_3Bi , where A is an alkali metal.

10 19. The structure of claim 15, 16, or 18, wherein the alkali metal is Na.

20. The structure of claims 17 or 18, wherein the topological Dirac semimetal layer is an ultrathin film and has a thickness of 2 unit cells or less.

21. The structure of any one of claims 13 to 20, the structure further comprising:

15 at least two conductive electrodes in contact with the topological Dirac semimetal layer, the at least two electrodes spaced apart from each other and between which current may flow from a current or voltage source through the topological Dirac semimetal layer; and

at least one electrode of the at least two electrodes is configured to be connected to the current or voltage source.

20 22. The structure of any one of claims 13 to 21, the structure further comprising:

a layer for donating or accepting charge carriers from the topological Dirac semimetal layer.

23. The structure of claim 22, wherein the layer for donating or accepting charge carriers from the topological Dirac semimetal layer is an electron accepting layer.

24. The structure of any one of claims 13 to 23, wherein the structure further comprises a capping layer for preventing oxidation of the topological Dirac semimetal layer.

25. A method of forming a topological Dirac semimetal layer on a substrate; the
5 method including:

(a) providing constituent elements of a Dirac semimetal to a surface of a substrate at a first temperature to nucleate the Dirac semimetal on the surface of the substrate forming a nucleation layer of the topological Dirac semimetal layer having a first thickness; and

10 (b) increasing the first temperature to a second temperature and further providing constituent elements of the Dirac semimetal at the second temperature to grow the thickness of the Dirac semimetal layer to a final thickness.

26. The method of claim 25, wherein the first temperature is from about 100°C to about 140°C, and the second temperature is from about 240°C to about 400°C.

15 27. The method of any one of claims 25 or 26, wherein the Dirac semimetal layer is a A_3Bi layer, and the constituent elements are A and Bi, wherein A is an alkali metal, and the method further comprises:

providing A and Bi atoms with a Bi:A flux ratio of at least 1:10, and with a Bi flux rate of at least 0.03 Å/sec and an A flux rate of at least 0.7 Å/sec.

20 28. The method of any one of claims 25 to 27 wherein the step of increasing the first temperature to the second temperature commences when the first thickness reaches 2 nm.

29. The method of any one of claim 25 to 28, wherein the method further includes, after step (b):

25 step (c) of annealing the topological Dirac semimetal layer at an annealing temperature for an annealing time.

30. A structure formed according to the method of any one of claims 25 to 29.

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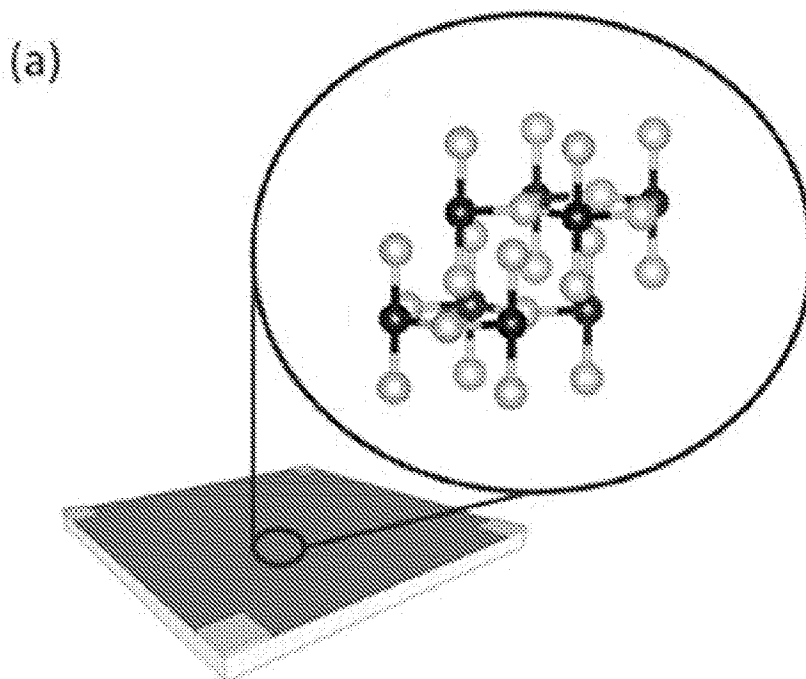


Figure 1(a)

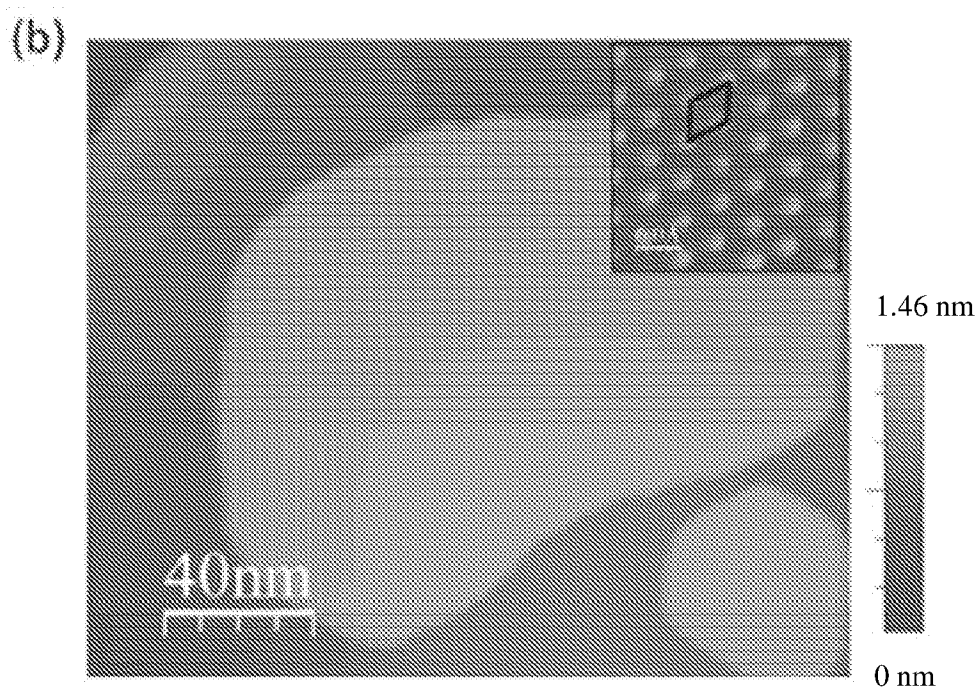


Figure 1(b)

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(c)

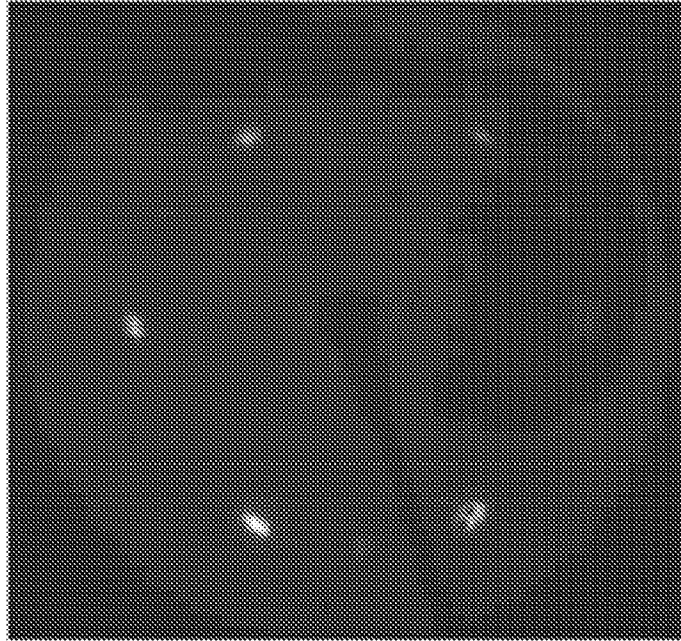


Figure 1(c)

(d)

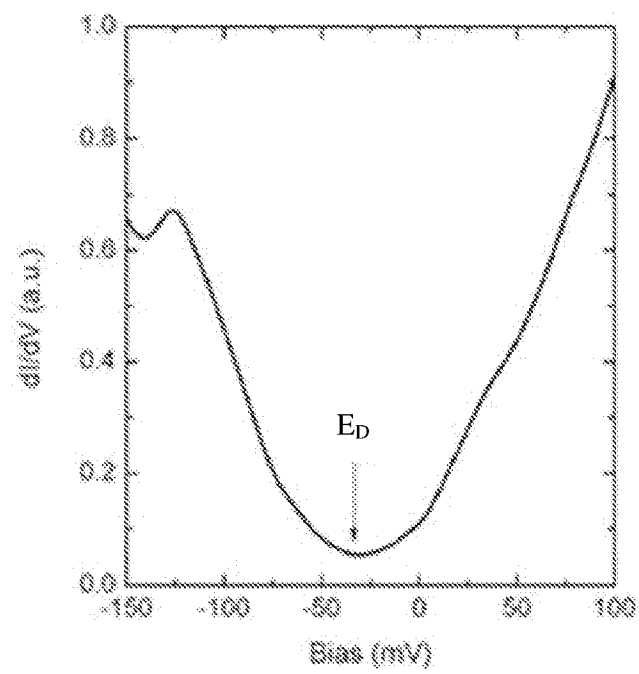


Figure 1(d)

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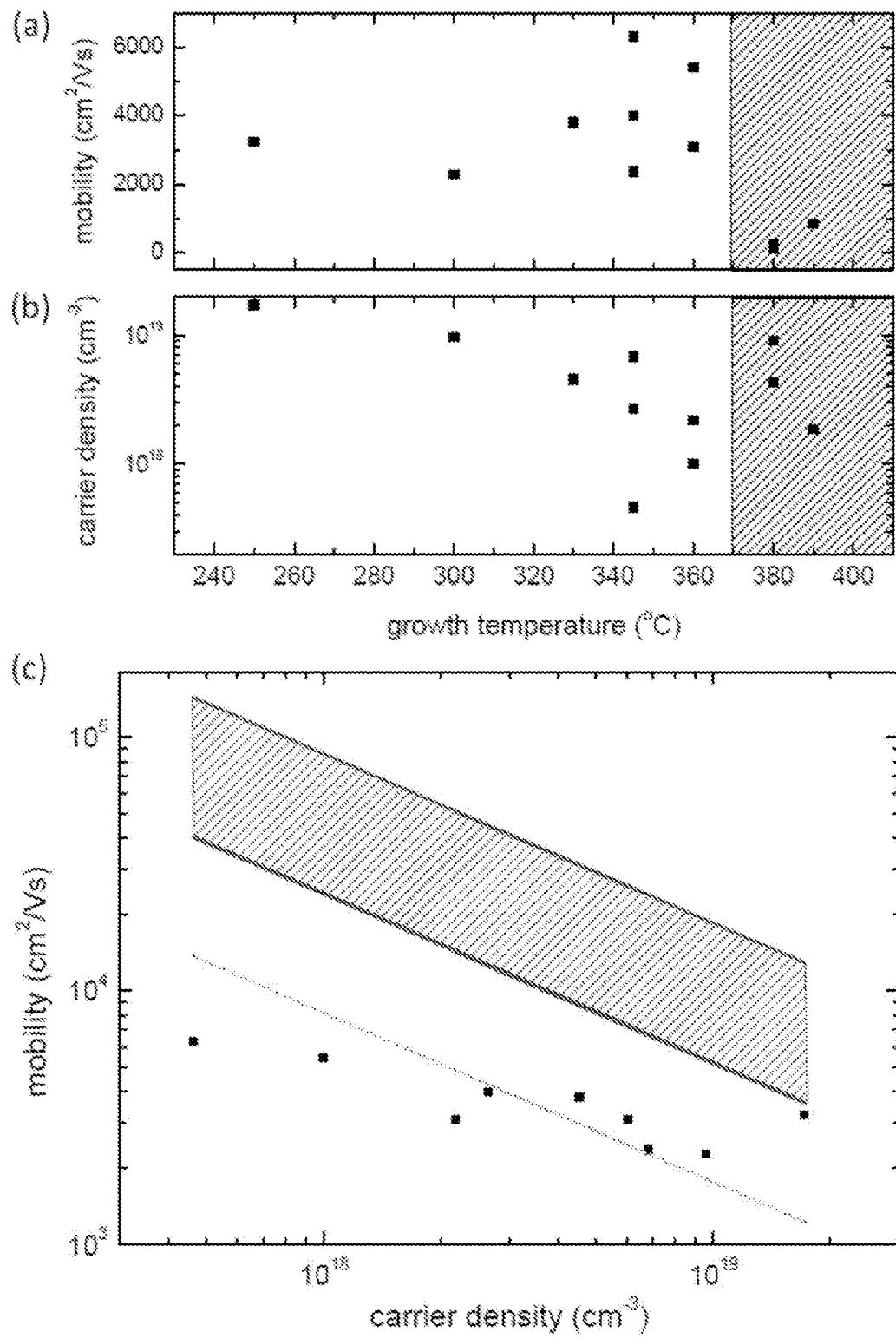


Figure 2

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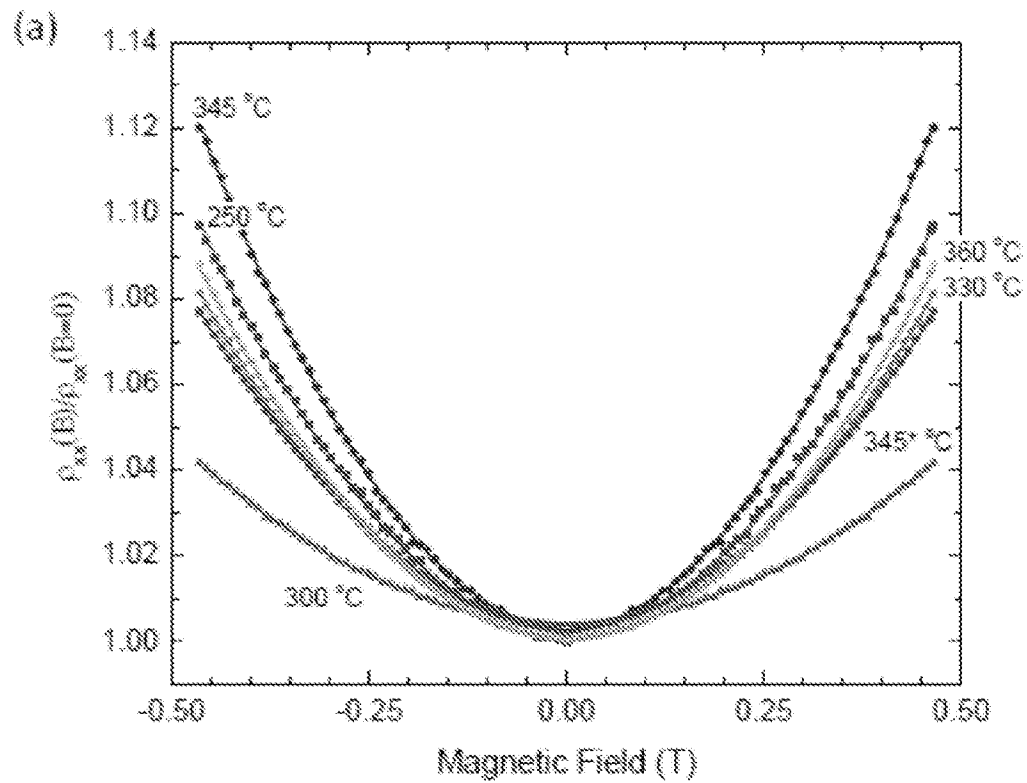


Figure 3A

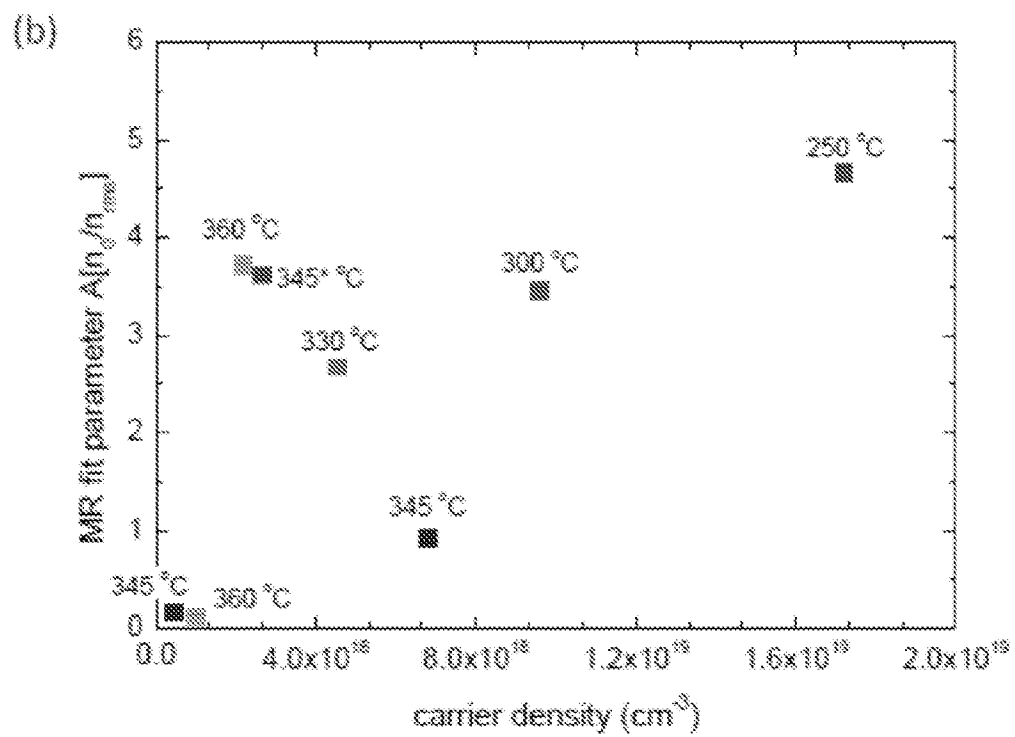
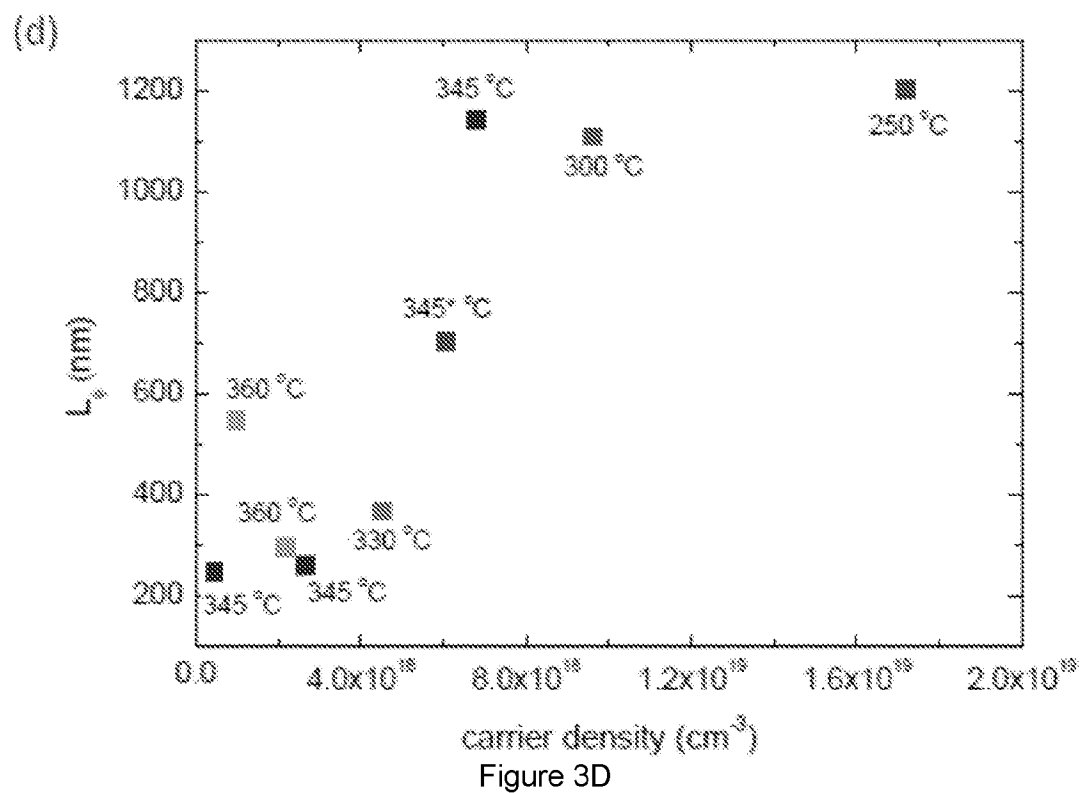
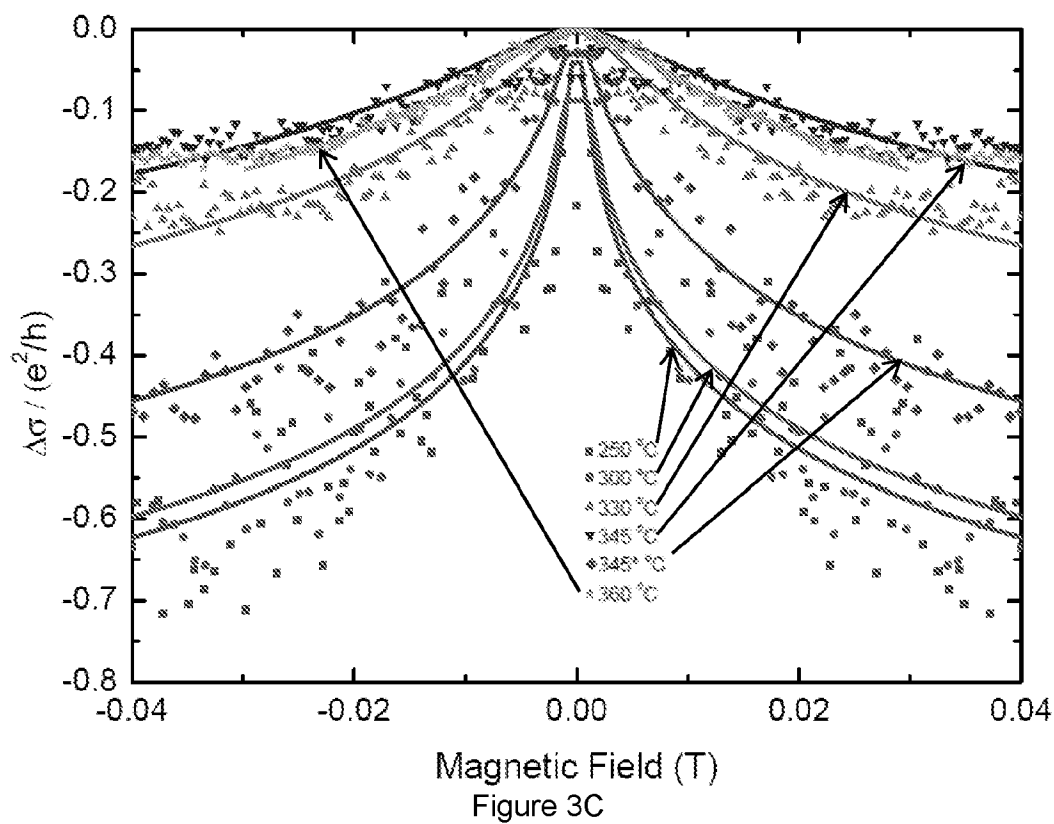


Figure 3B

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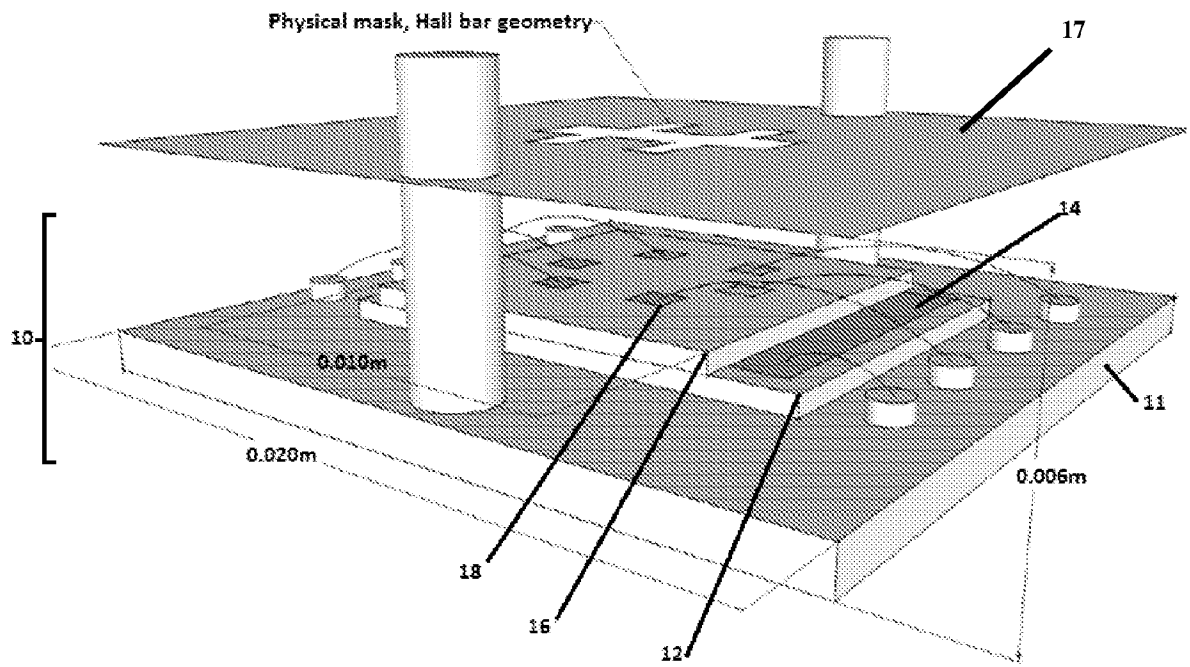


Figure 4A

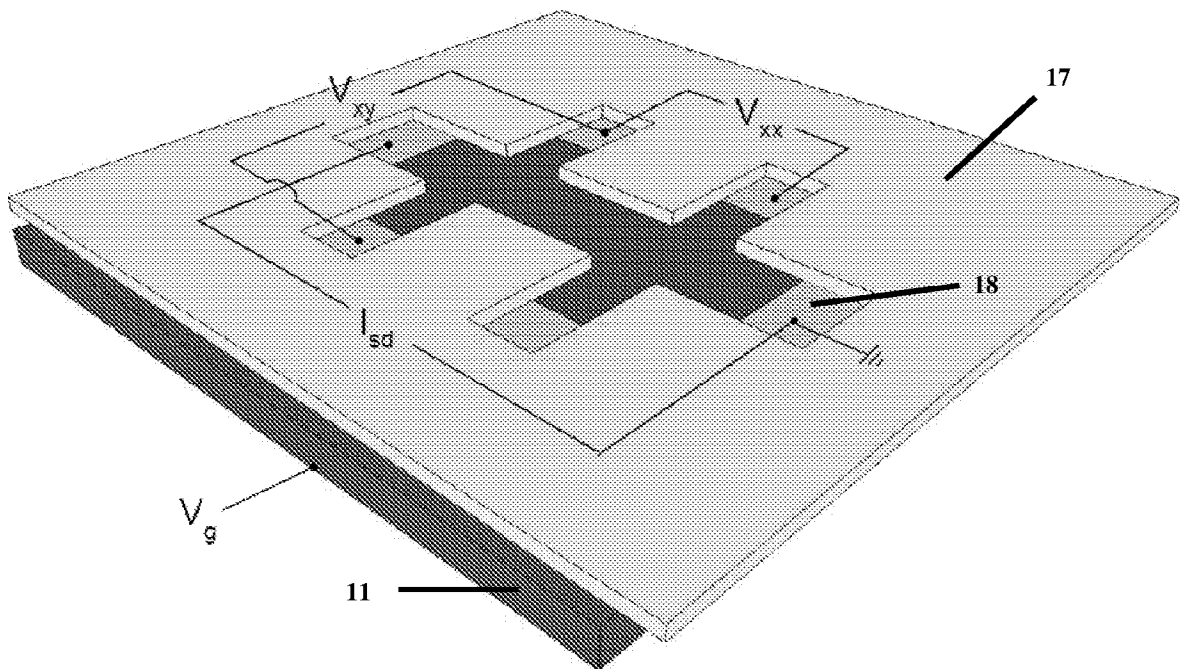


Figure 4B

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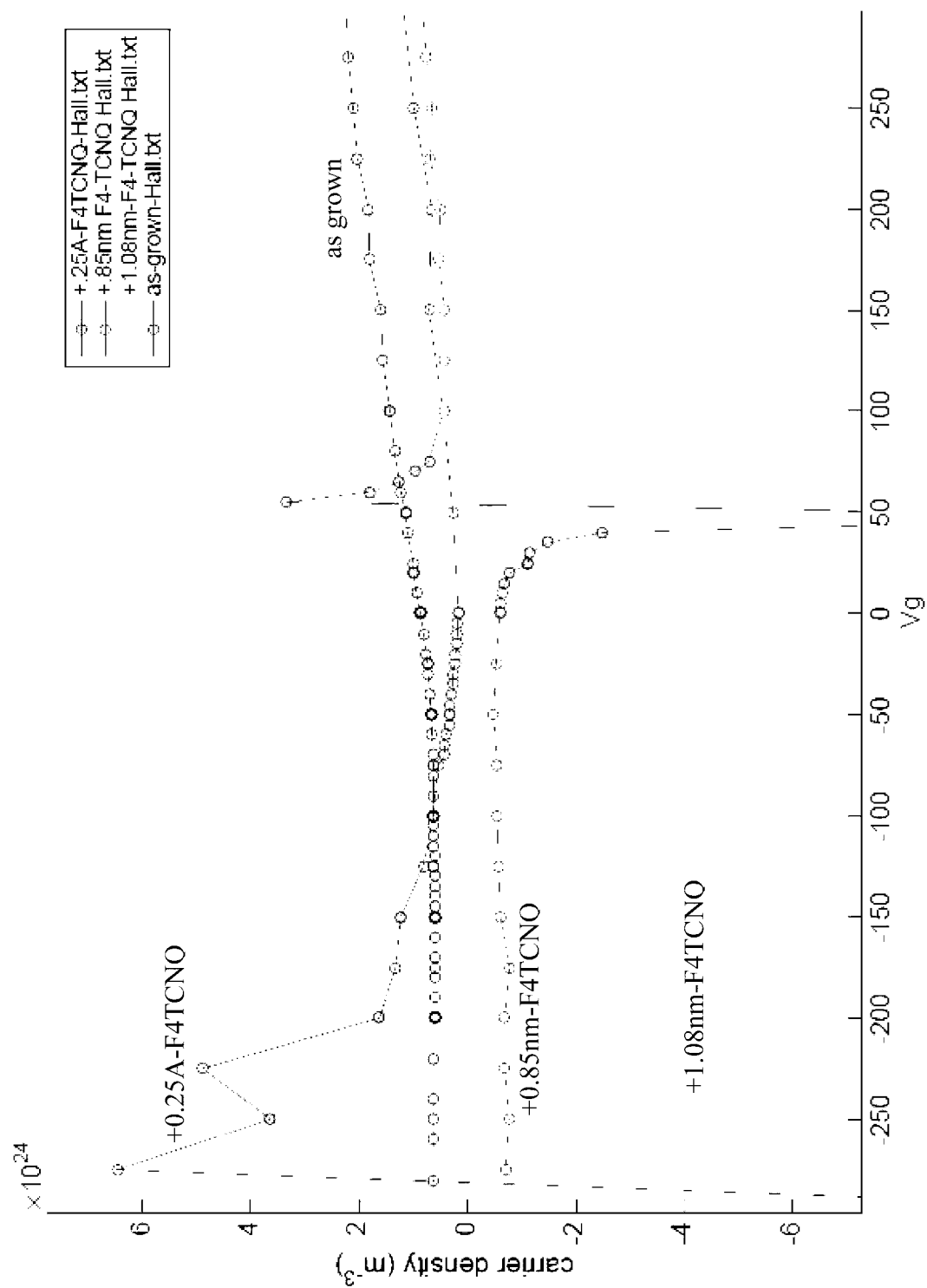


Figure 5

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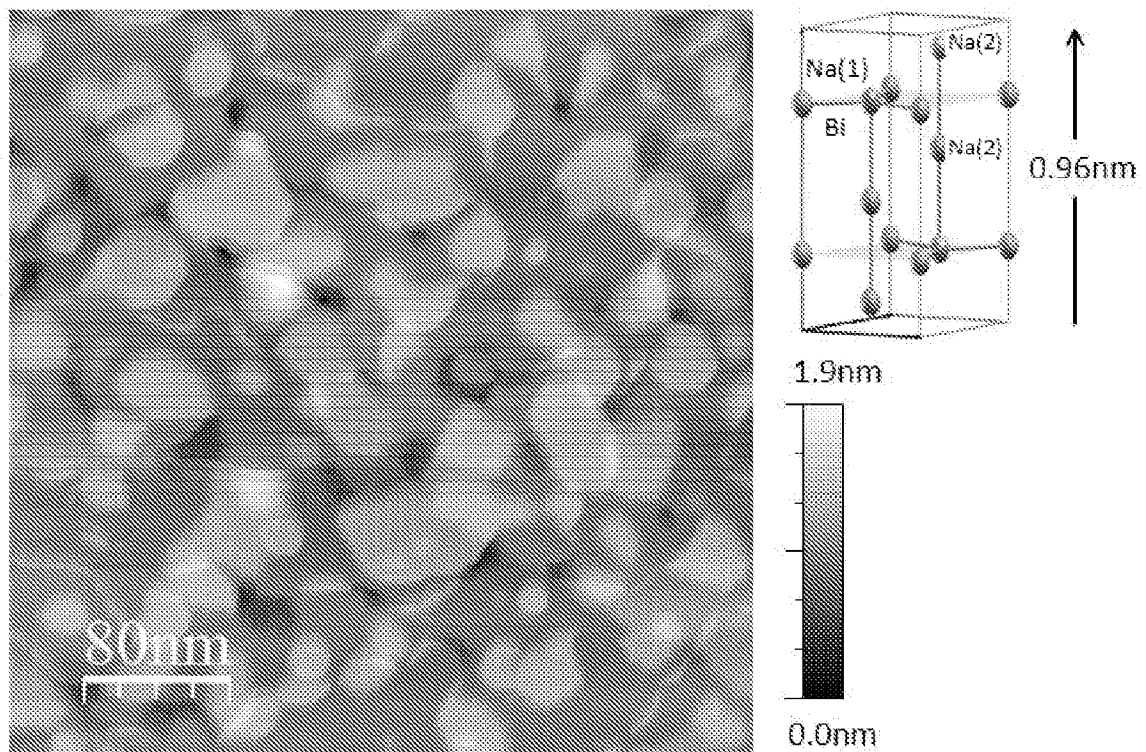


Figure 6

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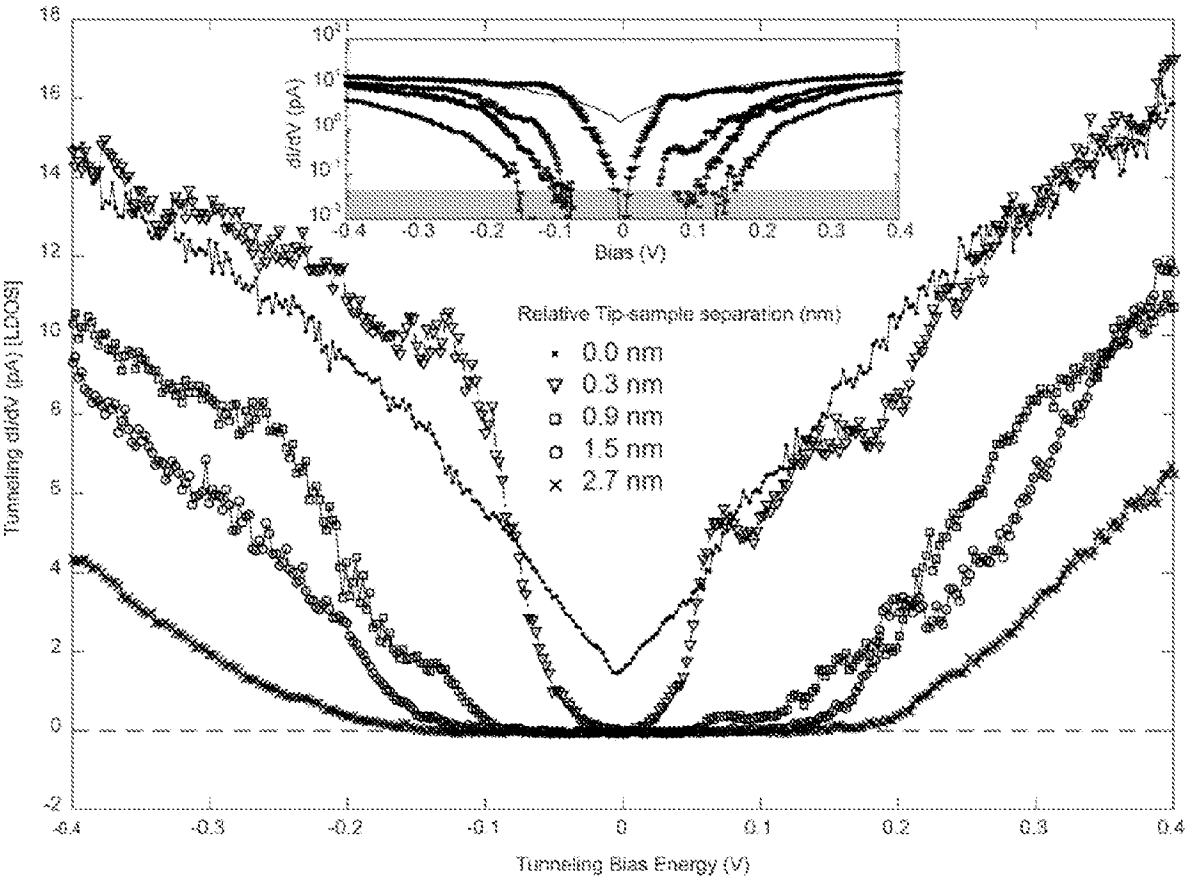


Figure 7(a)

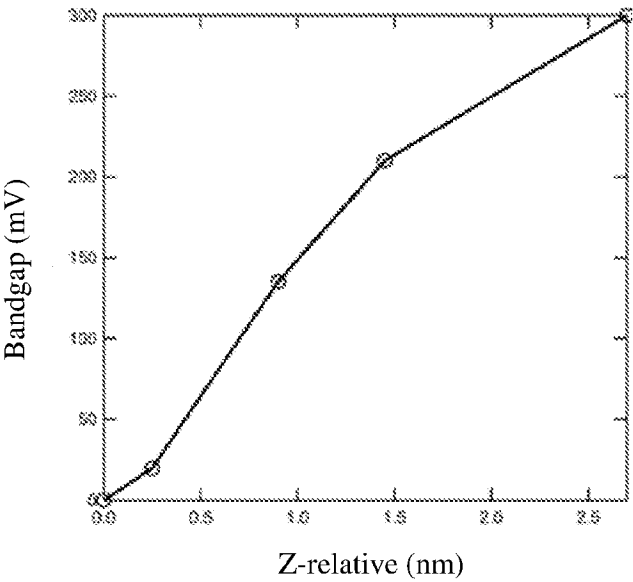


Figure 7(b)

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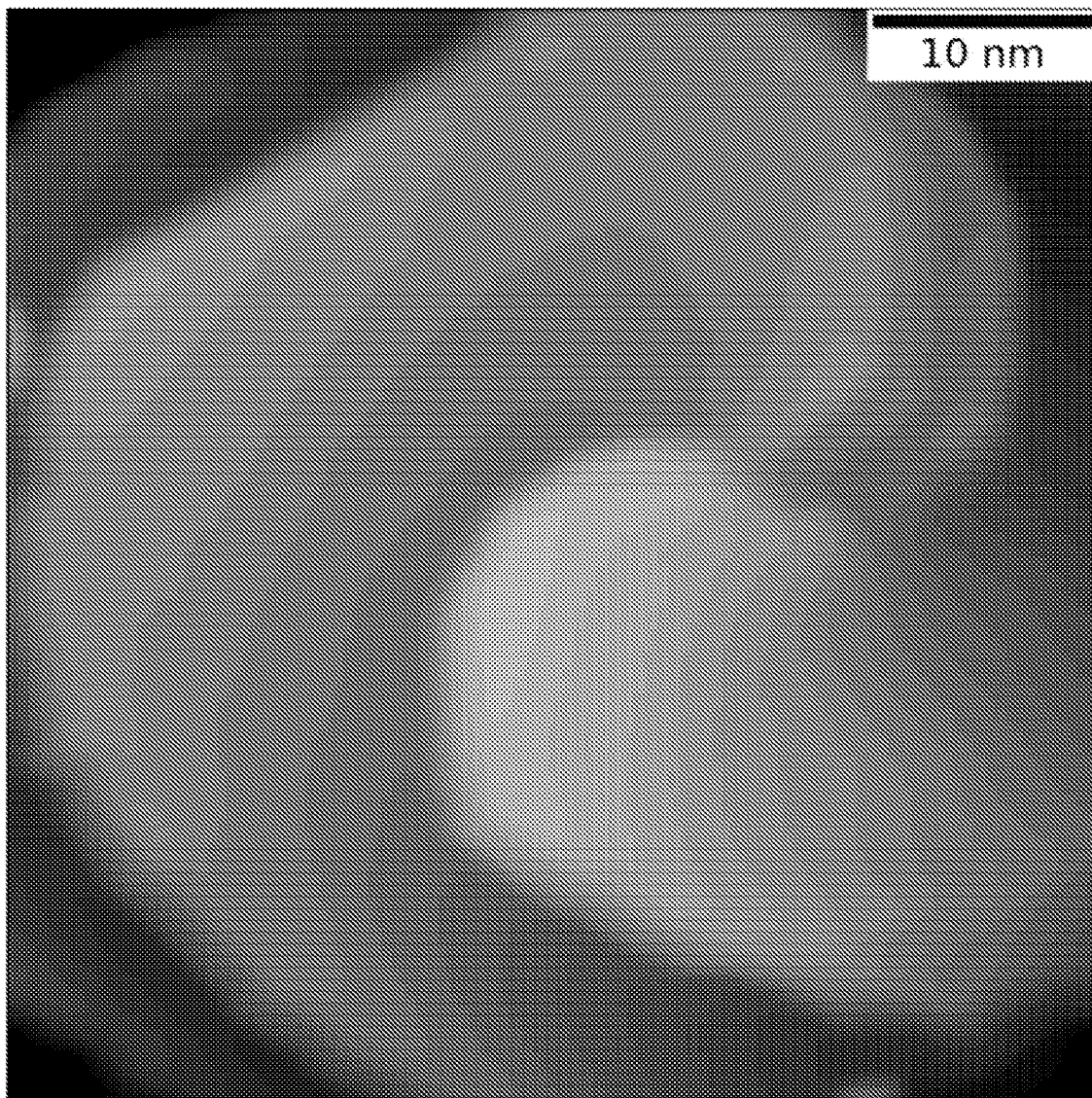


Figure 8

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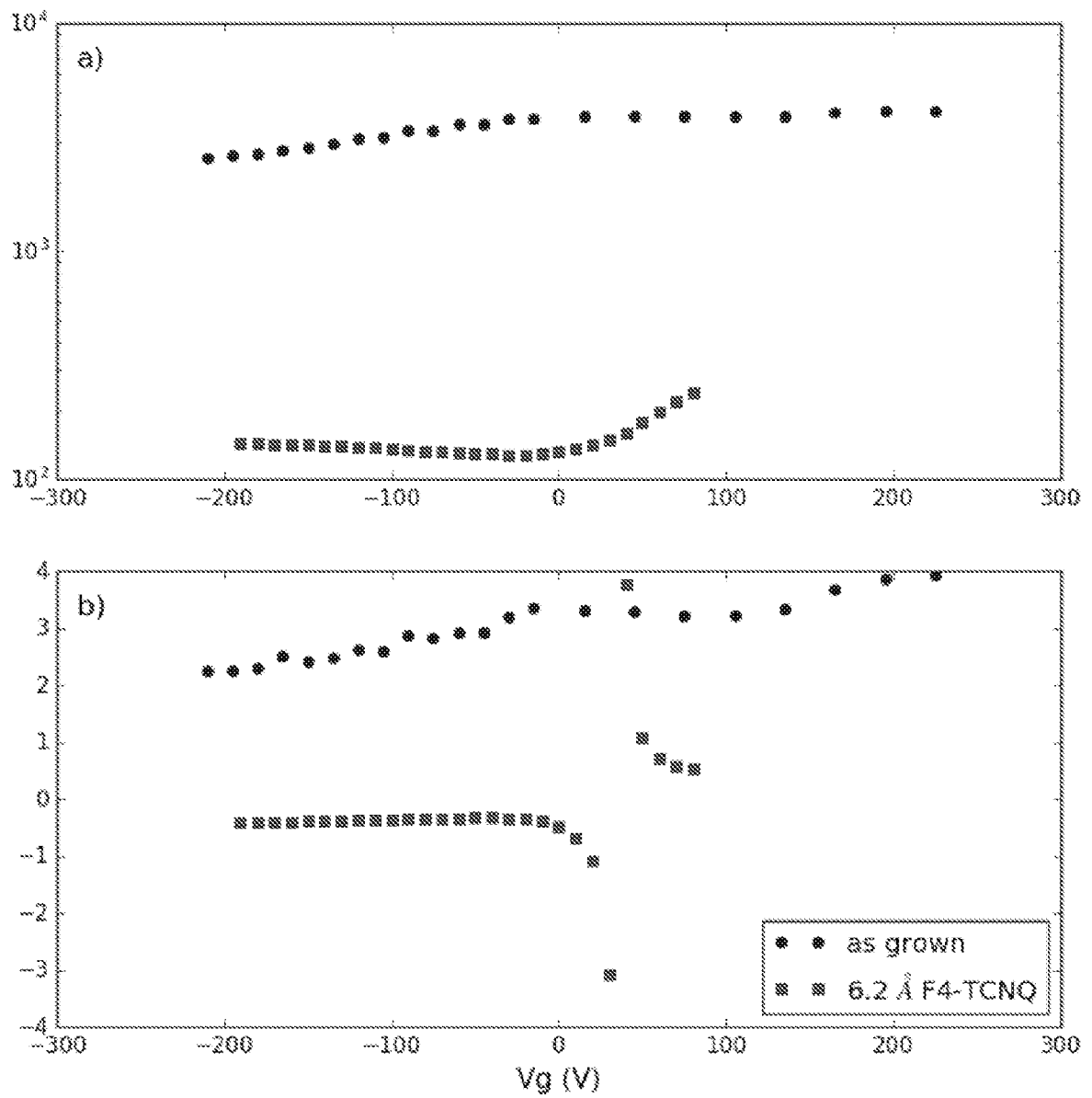


Figure 9

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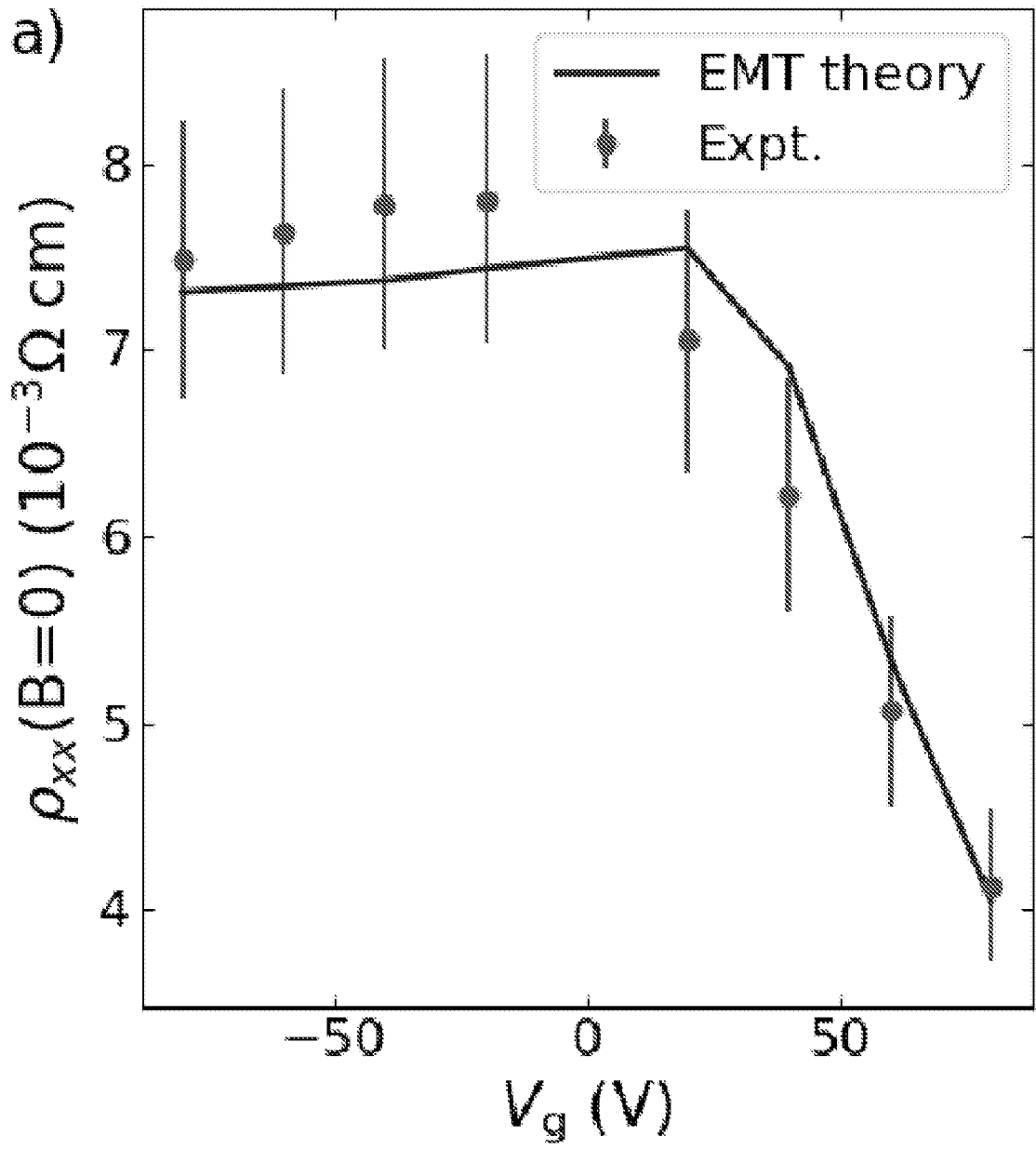


Figure 10(a)

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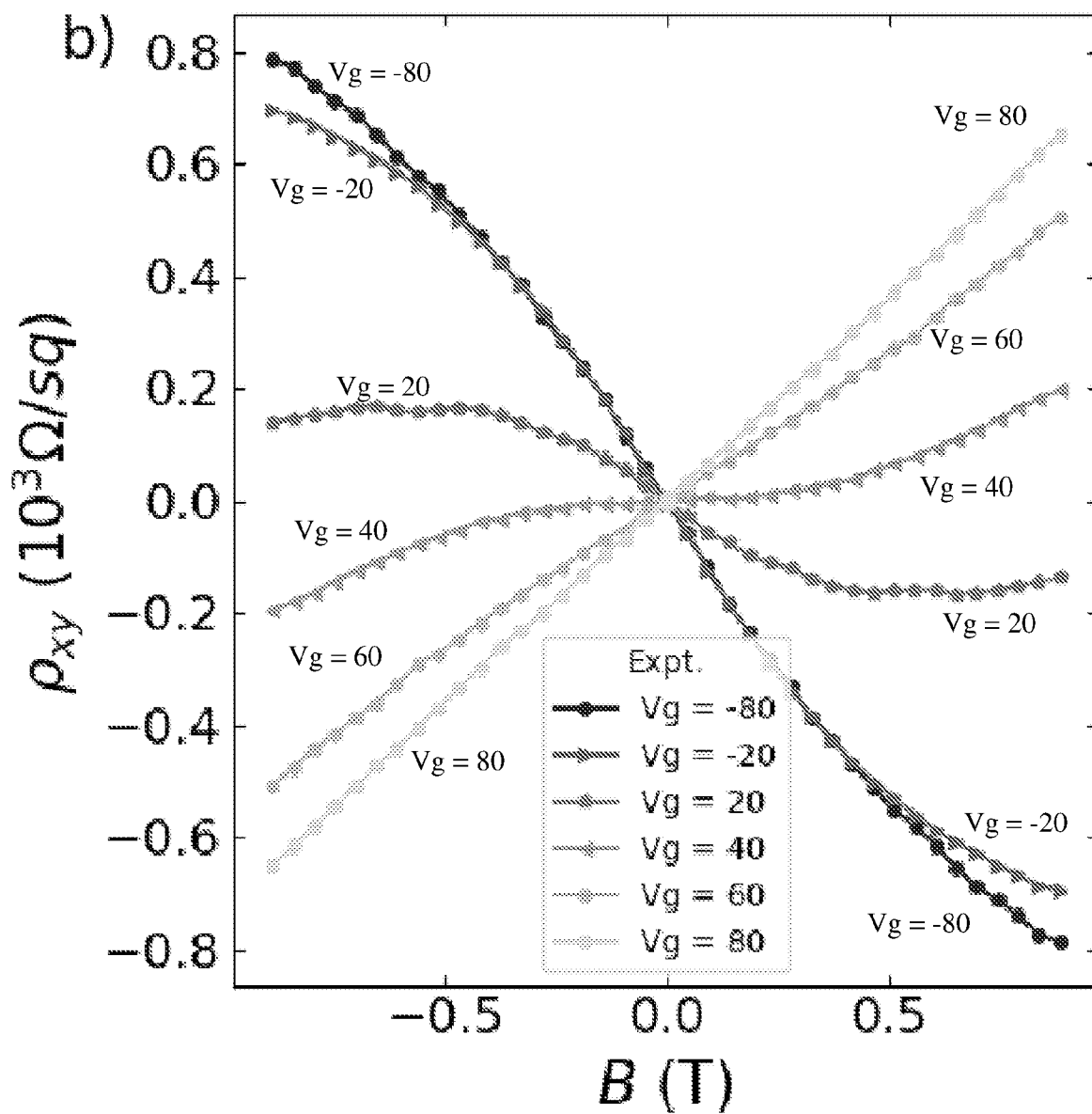


Figure 10(b)

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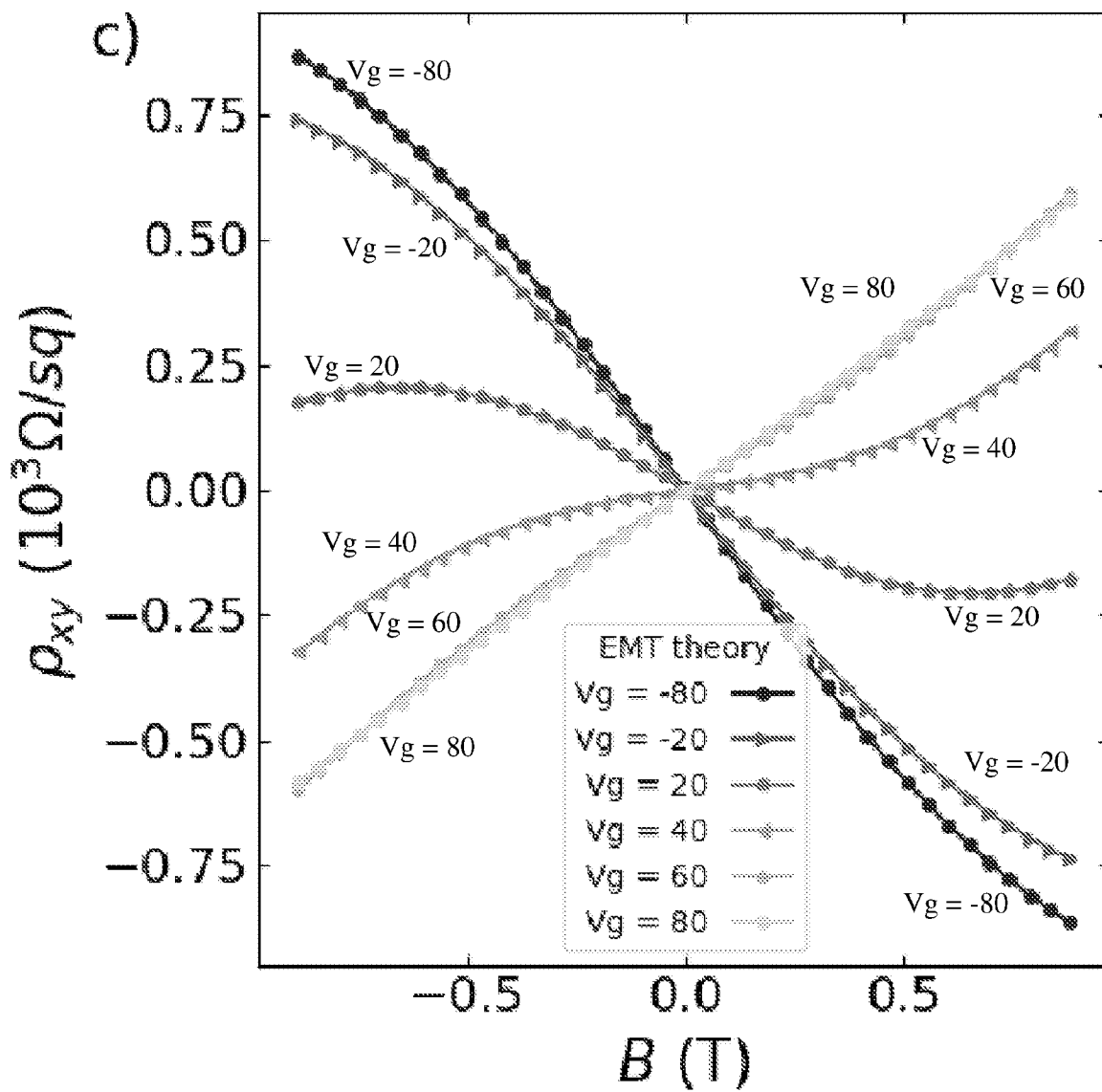


Figure 10(c)

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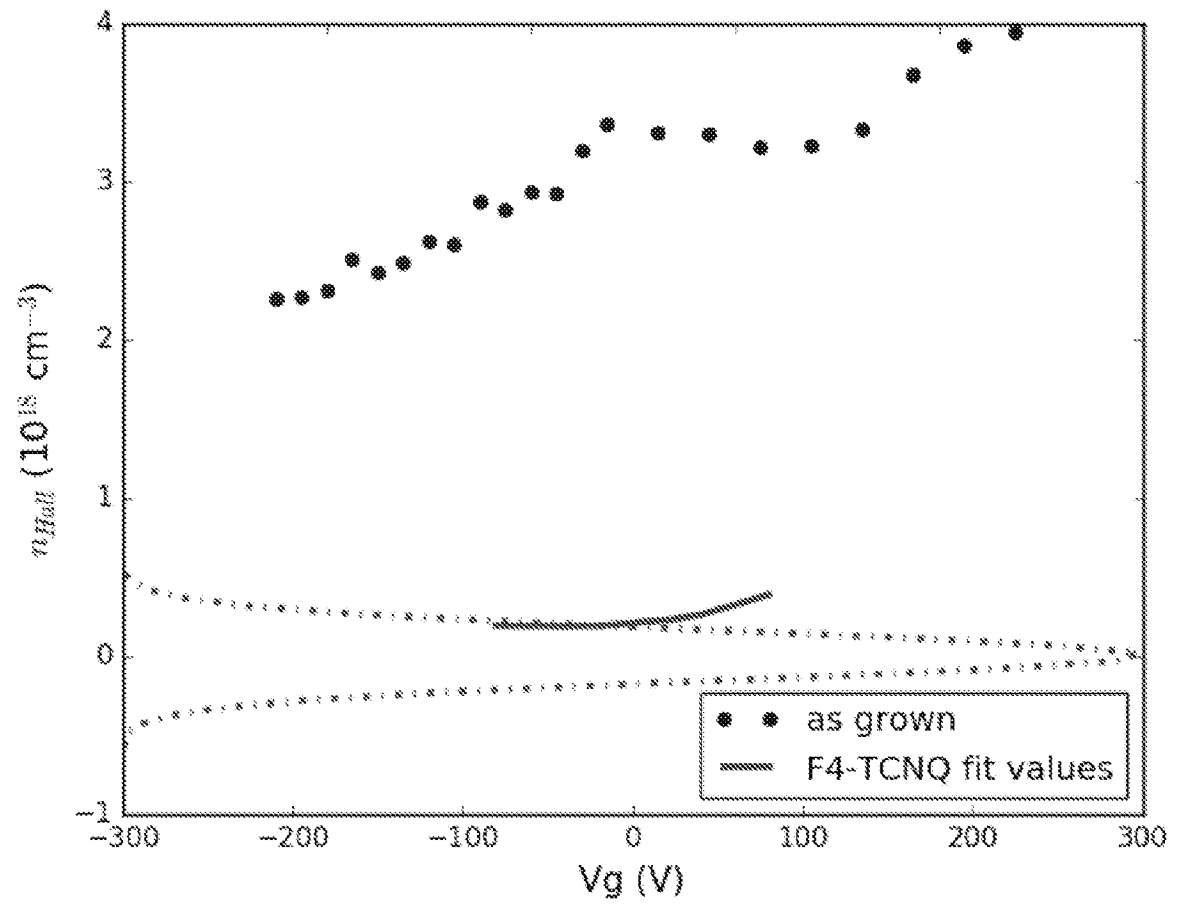


Figure 11

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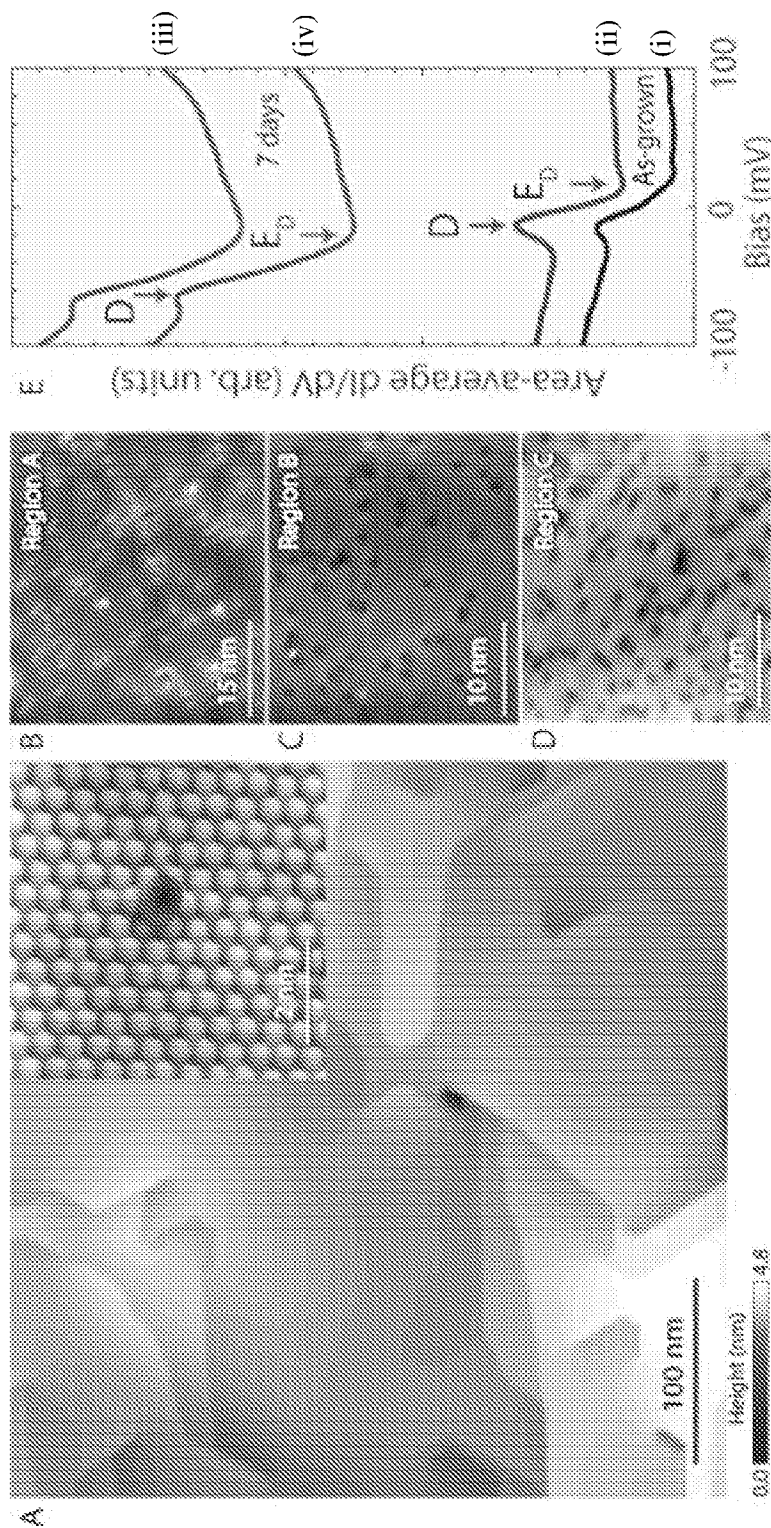


Figure 12

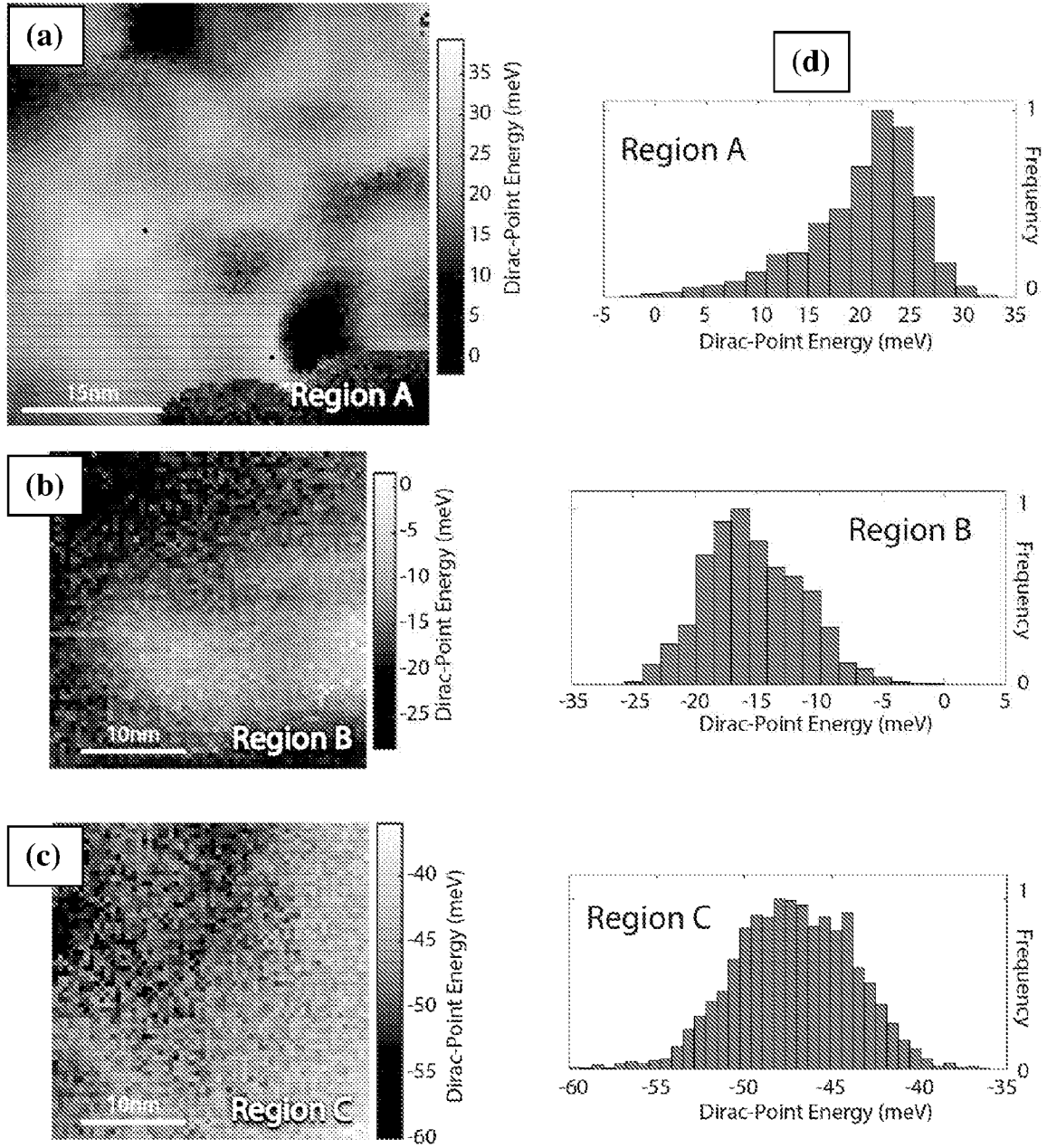


Figure 13

INTERNATIONAL SEARCH REPORT

 International application No.
PCT/AU2017/050399

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/68 (2006.01) H01L 51/05 (2006.01) H01L 21/36 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases: PATENW with the following keywords: DIRAC, SEMI+, TOPOLOGICAL, NA3BI, CD3AS2 and like terms.

Espacenet, PAMS Non-OPI Enquiry, Google, Google Patents and Google Scholar: Applicant and inventor names, along with H01L 29/68, H01L 21/36, Na3Bi, trisodium bismuth, bismuth sodium, Cd3As2, cadmium arsenide, cadmium diarsenide, alumina, Al2O3, mica, silica, SiO2, oxide, heterostructure, thin film, layer, 2D, junction, interface, MBE, epitaxy, deposition, vapour phase, insulator, conductor, electrode, gate, voltage, current, electric field, density of states, mobility, spin, carrier, F4-TCNQ, donor, acceptor, topological, Dirac semimetal, Dirac semiconductor, nucleation, temperature, two-step, two-stage, growth and related terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	



Further documents are listed in the continuation of Box C



See patent family annex

* "A"	Special categories of cited documents: document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E"	earlier application or patent but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 17 August 2017	Date of mailing of the international search report 17 August 2017
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA Email address: pct@ipaaustralia.gov.au	Authorised officer Tim Burgess AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No. +61262832421

INTERNATIONAL SEARCH REPORT		International application No.
C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		PCT/AU2017/050399
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 105006485 A (UNIV BEIJING) 28 October 2015 items 202-205, Fig. 2, [0041], [0042]	1-5, 7-24
X	Liu, Y. et al., "Gate-tunable quantum oscillations in ambipolar Cd ₃ As ₂ thin films." NPG Asia Materials. 2015, vol. 7, pp. 1-8. abstract, Fig. 2, paras 2-3, pg. 2, para. 1, pg. 4.	1-24
A	Wang, Z. et al. "Dirac semimetal and topological phase transitions in A ₃ Bi (A= Na, K, Rb)." Physical Review B. 2012, vol. 85, pp. 195320-1 - 195320-5. abstract, introduction	3, 7, 8, 15, 18, 19
X A	Hellerstedt, J. et al., "Electronic properties of high-quality epitaxial topological Dirac semimetal thin films." Nano letters. 22nd April 2016, vol. 16, pp. 3210-3214. pg. 3210, para. 3, pg. S2 abstract, introduction, pg. 3210, para. 3	25-30 4, 9, 16, 20
A	Xiao, X. et al., "Anisotropic quantum confinement effect and electric control of surface states in Dirac semimetal nanostructures." Scientific reports. 2015 vol. 5, pp. 7898-1 - 7898-5. whole document	6
A	Kim, Dohun, et al. "Surface conduction of topological Dirac electrons in bulk insulating Bi ₂ Se ₃ ." <i>arXiv preprint</i> . 2011 <i>arXiv:1105.1410</i> introduction	11, 22, 23
A	Kushwaha, S. K. et al., "Bulk crystal growth and electronic characterization of the 3D Dirac semimetal Na ₃ Bi." APL materials. 2015, vol. 3, pp. 041504-1 - 041504-9. para. 4, pg. 43	12, 24
A	He, Hong-Tao, et al. "Impurity effect on weak anti-localization in the topological insulator Bi ₂ Te ₃ ." <i>arXiv preprint</i> . 2010 <i>arXiv:1008.0141</i> . pg. 2 para. 2	12, 24
P,X	Edmonds, M. T. et al. "Molecular Doping the Topological Dirac Semimetal Na ₃ Bi across the Charge Neutrality Point with F ₄ -TCNQ." ACS applied materials & interfaces. 16th Jun 2016, vol. 8, pp. 16412-16418. abstract, pg. 16416 para. 3	21-30
P,X P,A	Edmonds, M. T. et al. "Spatial Charge Inhomogeneity and Defect States in Topological Dirac Semimetal Thin Films." <i>arXiv preprint</i> . 11th Dec 2016, <i>arXiv:1612.03385</i> pg. 4, Experimental methods pp. 23, 24	25-30 9, 20
X Y	Bansal, Namrata, et al. "Epitaxial growth of topological insulator Bi ₂ Se ₃ film on Si (111) with atomically sharp interface." <i>arXiv preprint</i> . 2011, <i>arXiv:1104.3438</i> pg. 7, para. 1 pg. 7, para. 1	25, 29, 30 26, 27
X Y	Hellerstedt, Jack, et al. "Thickness and growth-condition dependence of in-situ mobility and carrier density of epitaxial thin-film Bi ₂ Se ₃ ." <i>arXiv preprint</i> . 2014, <i>arXiv:1405.5692</i> . pg. 1, para. 3 and 4 pg. 1, para. 3 and 4	25, 28, 30 27
	Wen, Jing, et al. "Synthesis of semimetal A ₃ Bi (A= Na, K) thin films by molecular beam epitaxy." <i>Applied Surface Science</i> . 2015, vol. 327, pages 213-217.	

INTERNATIONAL SEARCH REPORT		International application No.
C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		PCT/AU2017/050399
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	pg. 213, para. 2	27
A	pg. 213, para. 2	25
Y	Wen, Jing, et al. "Semimetal Na ₃ Bi Thin Film Grown on Double-Layer Graphene by Molecular Beam Epitaxy." <i>Chinese Physics Letters</i> . 2014, vol. 31, pages 116802-1 - 116802-3. pg. 116802-2, para. 2	26, 27

Form PCT/ISA/210 (fifth sheet) (July 2009)

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
the subject matter listed in Rule 39 on which, under Article 17(2)(a)(i), an international search is not required to be carried out, including
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See Supplemental Box for Details

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☒ No protest accompanied the payment of additional search fees.

Supplemental Box**Continuation of: Box III**

This International Application does not comply with the requirements of unity of invention because it does not relate to one invention or to a group of inventions so linked as to form a single general inventive concept.

This Authority has found that there are different inventions based on the following features that separate the claims into distinct groups:

- Claims 1-24 are directed to a method/structure for altering the charge carrier density/band gap in a topological Dirac semimetal. The feature of the topological Dirac semimetal layer being separated from the conductor/electric field generator by an insulator/non-conducting layer is specific to this group of claims.
- Claims 25-30 are directed to a method of forming a topological Dirac semimetal layer on a substrate. The feature of (a) providing constituent elements of a Dirac semimetal to a surface of a substrate at a first temperature to nucleate the Dirac semimetal on the surface of the substrate forming a nucleation layer of the topological Dirac semimetal layer having a first thickness; and (b) increasing the first temperature to a second temperature and further providing constituent elements of the Dirac semimetal at the second temperature to grow the thickness of the Dirac semimetal layer to a final thickness, is specific to this group of claims.

PCT Rule 13.2, first sentence, states that unity of invention is only fulfilled when there is a technical relationship among the claimed inventions involving one or more of the same or corresponding special technical features. PCT Rule 13.2, second sentence, defines a special technical feature as a feature which makes a contribution over the prior art.

When there is no special technical feature common to all the claimed inventions there is no unity of invention.

In the above groups of claims, the identified features may have the potential to make a contribution over the prior art but are not common to all the claimed inventions and therefore cannot provide the required technical relationship. The only feature common to all of the claimed inventions and which provides a technical relationship among them is topological Dirac semimetal layer

However it is considered that this feature is generic in this particular art. Therefore in this light this common feature cannot be a special technical feature. Hence there is no special technical feature common to all the claimed inventions and the requirements for unity of invention are consequently not satisfied *a priori*.

INTERNATIONAL SEARCH REPORT Information on patent family members		International application No. PCT/AU2017/050399	
This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.			
Patent Document/s Cited in Search Report		Patent Family Member/s	
Publication Number	Publication Date	Publication Number	Publication Date
CN 105006485 A	28 October 2015	CN 105006485 A	28 Oct 2015
End of Annex			
Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001. Form PCT/ISA/210 (Family Annex)(July 2009)			