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(54) **Title:** METHOD FOR ENHANCING THE SEMICONDUCTOR MANUFACTURING YIELD

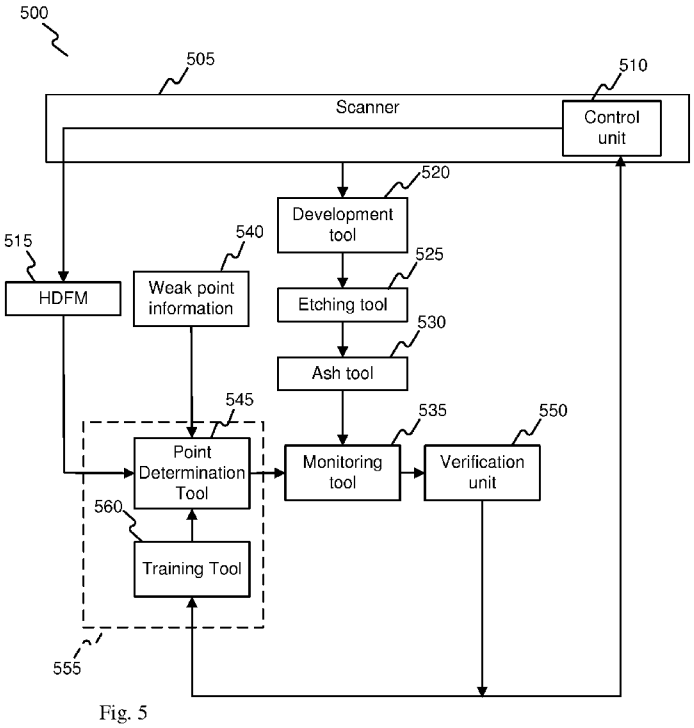

Fig. 5

(57) **Abstract:** Embodiments of the present disclosure provide systems and methods for enhancing the semiconductor manufacturing yield. Embodiments of the present disclosure provide a yield improvement system. The system comprises a training tool configured to generate training data based on receipt of one or more verified results of an inspection of a first substrate. The system also comprises a point determination tool configured to determine one or more regions on a second substrate to inspect based on the training data, weak point information for the second substrate, and an exposure recipe for a scanner of the second substrate.

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METHOD FOR ENHANCING THE SEMICONDUCTOR MANUFACTURING YIELD

CROSS-REFERENCE TO RELATED APPLICATIONS

[001] This application claims priority of US application 62/375,257 which was filed on August 15, 2016 and US application 62/543,242 which was filed on August 09, 2017 which are incorporated herein in its entirety by reference.

TECHNICAL FIELD

[002] The present disclosure generally relates to the field of semiconductor manufacturing, and more particularly, to systems and methods for enhancing the semiconductor manufacturing yield.

BACKGROUND

[003] In manufacturing processes of integrated circuits (ICs), unfinished or finished circuit components are inspected to ensure that they are manufactured according to design and are free of defects. An inspection system utilizing an optical microscope can provide high throughput but typically has resolution down to a few hundred nanometers; and the resolution is limited by the wavelength of light. As the physical sizes of IC components continue to reduce down to a sub-100 or even sub-10 nanometers, inspection systems capable of higher resolution than those utilizing optical microscopes are needed.

[004] A charged particle (e.g., electron) beam microscope, such as a scanning electron microscope (SEM) or a transmission electron microscope (TEM), capable of resolution down to less than a nanometer, serves as a practicable tool for inspecting IC components having a feature size that is sub-100 nanometers. With an SEM, electrons of a single primary electron beam, or electrons of a plurality of primary electron beams, can be focused at probe spots of a wafer under inspection. The interactions of the primary electrons with the wafer can result in one or more secondary electron beams. The secondary electron beams may comprise backscattered electrons, secondary electrons, or Auger electrons, resulting from the interactions of the primary electrons with the wafer. The intensity of the one or more secondary electron beams can vary based on the properties of the internal and/or external structures of the wafer. However, the throughput of a charge particle beam microscope at high resolution can be significantly lower compared with a lower resolution optical microscope.

[005] Different semiconductor manufacturing processes, for example, photo-resist coating, exposure, development, etch, and photo-resist removal (ashing) can be batch processes. Batch processing can cause non-uniformity in patterning of multiple substrates (also referred to herein as wafers) within a batch. Further, if defect inspection of patterned substrates is conducted after the entire patterning process is completed, the defective wafers may be scrapped or may have to be converted to a down-graded product. This can cause a significant reduction in semiconductor

manufacturing yield.

SUMMARY

[006] Embodiments of the present disclosure provide systems and methods for enhancing the semiconductor manufacturing yield. In some embodiments, a yield improvement system is provided. The system comprises a training tool configured to generate training data based on receipt of one or more verified results of an inspection of a first substrate. The system also comprises a point determination tool configured to determine one or more regions on a second substrate to inspect based on the training data, weak point information for the second substrate, and an exposure recipe for a scanner of the second substrate.

[007] In some embodiments, a method for yield improvement is provided. The method comprises receiving one or more verified results of an inspection of a first substrate; and generating training data based on the received verified results. The method further comprises determining one or more regions on a second substrate to inspect based on the training data, weak point information for the second substrate, and an exposure recipe for a scanner of the second substrate.

[008] In some embodiments, a non-transitory computer readable storage medium is provided. The medium stores instructions that are executable by a computing device, which includes one or more processors, causing the computing device to perform a method for yield improvement. The method comprises receiving one or more verified results of an inspection of a first substrate; and generating training data based on the received verified results. The method further comprises determining one or more regions on a second substrate to inspect based on the training data, weak point information for the second substrate, and an exposure recipe for a scanner of the second substrate.

[009] Additional objects and advantages of the disclosed embodiments will be set forth in part in the following description, and in part will be apparent from the description, or may be learned by practice of the embodiments. The objects and advantages of the disclosed embodiments may be realized and attained by the elements and combinations set forth in the claims.

[010] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the disclosed embodiments, as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[011] **FIG. 1** is a schematic diagram illustrating an exemplary electron beam inspection system, consistent with embodiments of the present disclosure.

[012] **FIG. 2** is a schematic diagram illustrating an exemplary electron beam tool that can

be a part of the exemplary electron beam inspection system of **FIG. 1**, consistent with embodiments of the present disclosure.

[013] **FIG. 3** is a schematic diagram illustrating a semiconductor processing system.

[014] **FIG. 4** is a flowchart illustrating a method for semiconductor processing.

[015] **FIG. 5** is a schematic diagram illustrating an exemplary yield improvement system, consistent with embodiments of the present disclosure.

[016] **FIGs. 6A, 6B** are schematic diagrams illustrating inspection regions on substrates, consistent with embodiments of the present disclosure.

[017] **FIG. 7** is a flowchart illustrating an exemplary method for yield improvement, consistent with embodiments of the present disclosure.

DESCRIPTION OF THE EMBODIMENTS

[018] Reference will now be made in detail to exemplary embodiments, examples of which are illustrated in the accompanying drawings. The following description refers to the accompanying drawings in which the same numbers in different drawings represent the same or similar elements unless otherwise represented. The implementations set forth in the following description of exemplary embodiments do not represent all implementations consistent with the invention. Instead, they are merely examples of apparatuses and methods consistent with aspects related to the invention as recited in the appended claims.

[019] The present disclosure relates to systems and methods for enhancing the semiconductor manufacturing yield. A test wafer or a first wafer can be processed from exposure to development and an exposure recipe of a scanner, for example, a high density focus map (HDFM) can be recorded. Embodiments of the present disclosure provide a point determination tool that can be configured to determine one or more regions of the test wafer or the first wafer to inspect, based on the exposure recipe and hot spot information for the wafer. The exposure recipe for subsequent processed wafers can be optimized based on the inspection results of the test wafer or the first wafer. Embodiments of the present disclosure also provide a training tool that can be configured to generate training data based on the inspection results. The training data can be provided to the point determination tool to determine one or more regions of the subsequent processed wafers to inspect, based on the training data, exposure recipe, and hot spot information for the wafer. The disclosed systems and methods enable dynamic updates of the exposure recipe and the regions to be monitored. The updates to the exposure recipe can reduce defects in subsequent processed wafers and therefore improve the semiconductor manufacturing yield. The updates to monitoring may include monitoring fewer hot spots thereby improving the throughput. The updates to monitoring can also include a change in the monitoring to improve detection of defects. The improved defect detection can help in further improving the semiconductor manufacturing yield.

[020] Reference is now made to **FIG. 1**, which illustrates an exemplary electron beam inspection (EBI) system 100 consistent with embodiments of the present disclosure. As shown in **FIG. 1**, EBI system 100 includes a main chamber 101, a load/lock chamber 102, an electron beam tool 104, and an equipment front end module (EFEM) 106. Electron beam tool 104 is located within main chamber 101.

[021] EFEM 106 includes a first loading port 106a and a second loading port 106b. EFEM 106 may include additional loading port(s). First loading port 106a and second loading port 106b can receive wafer front opening unified pods (FOUPs) that contain wafers (e.g., semiconductor wafers or wafers made of other material(s)) or samples to be inspected (wafers and samples are collectively referred to as "wafers" hereafter). One or more robot arms (not shown) in EFEM 106 can transport the wafers to load/lock chamber 102.

[022] Load/lock chamber 102 is connected to a load/lock vacuum pump system (not shown), which removes gas molecules in load/lock chamber 102 to reach a first pressure below the atmospheric pressure. After reaching the first pressure, one or more robot arms (not shown) can transport the wafer from load/lock chamber 102 to main chamber 101. Main chamber 101 is connected to a main chamber vacuum pump system (not shown), which removes gas molecules in main chamber 101 to reach a second pressure below the first pressure. After reaching the second pressure, the wafer is subject to inspection by electron beam tool 104.

[023] Reference is now made to **FIG. 2**, which illustrates exemplary components of electron beam tool 104 consistent with embodiments of the present disclosure. As shown in **FIG. 2**, electron beam tool 104 includes a motorized stage 200, and a wafer holder 202 supported by motorized stage 200 to hold a wafer 203 to be inspected. Electron beam tool 104 further includes an objective lens assembly 204, electron detector 206, an objective aperture 208, a condenser lens 210, a beam limit aperture 212, a gun aperture 214, an anode 216, and a cathode 218. Objective lens assembly 204, in some embodiments, can include a modified swing objective retarding immersion lens (SORIL), which includes a pole piece 204a, a control electrode 204b, a deflector 204c, and an exciting coil 204d. Electron beam tool 104 may additionally include an energy dispersive X-ray spectrometer (EDS) detector (not shown) to characterize the materials on the wafer.

[024] A primary electron beam 220 is emitted from cathode 218 by applying a voltage between anode 216 and cathode 218. Primary electron beam 220 passes through gun aperture 214 and beam limit aperture 212, both of which can determine the size of electron beam entering condenser lens 210, which resides below beam limit aperture 212. Condenser lens 210 focuses primary electron beam 220 before the beam enters objective aperture 208 to set the size of the electron beam before entering objective lens assembly 204. Deflector 204c deflects primary electron beam 220 to facilitate beam scanning on the wafer. For example, in a scanning process, deflector 204c can be controlled to deflect primary electron beam 220 sequentially onto different locations of top surface of wafer 203 at

different time points, to provide data for image reconstruction for different parts of wafer 203. Further, in some embodiments, anode 216 and cathode 218 can be configured to generate multiple primary electron beams 220, and electron beam tool 104 can include a plurality of deflectors 204c to project the multiple primary electron beams 220 to different portions of the wafer at the same time, to provide data for image reconstruction for different portions of wafer 203.

[025] Exciting coil 204d and pole piece 204a generate a magnetic field that begins at one end of pole piece 204a and terminates at the other end of pole piece 204a. A part of wafer 203 being scanned by primary electron beam 220 can be immersed in the magnetic field and can be electrically charged, which, in turn, creates an electric field. The electric field reduces the energy of impinging primary electron beam 220 near the surface of the wafer before it collides with the wafer. Control electrode 204b, being electrically isolated from pole piece 204a, controls an electric field on the wafer to prevent micro-arching of the wafer and to ensure proper beam focus.

[026] A secondary electron beam 222 can be emitted from the part of wafer 203 upon receiving primary electron beam 220. Secondary electron beam 222 can form a beam spot on sensor surfaces of electron detector 206. Electron detector 206 can generate a signal (e.g., a voltage, a current, etc.) that represents an intensity of the beam spot, and provide the signal to a processing system (not shown in **FIG. 2**). The intensity of secondary electron beam 222, and the resultant beam spot, can vary according to the external and/or internal structure of wafer 203. Moreover, as discussed above, primary electron beam 220 can be projected onto different locations of the surface of the wafer, to generate secondary electron beams 222 (and the resultant beam spot) of different intensities. Therefore, by mapping the intensities of the beam spots with the locations of wafer 203, the processing system can reconstruct an image that reflects the internal and/or external structures of wafer 203.

[027] Reference is now made to **FIG. 3**, which is a schematic diagram illustrating a semiconductor processing system. **FIG. 3** illustrates a conventional semiconductor processing system 300 comprising a scanner 305, a development tool 320, an etching tool 325, an ash tool 330, a monitoring tool 335, a point determination tool 345, and a verification unit 350. Scanner 305 can comprise a control unit 310.

[028] Scanner 305 can expose a wafer coated with photoresist to a circuit pattern to be transferred to the wafer. Control unit 310 can control an exposure recipe used to expose the wafer. Control unit 310 can adjust various exposure recipe parameters, for example, exposure time, source intensity, and exposure dose. An HDFM 315 can be recorded corresponding to the exposure.

[029] Development tool 320 can develop the pattern on the exposed wafer by removing the photoresist from unwanted regions. For a positive photoresist, the portion of the photoresist that is exposed to light in scanner 305 becomes soluble to the photoresist developer and the unexposed portion of the photoresist remains insoluble to the photoresist developer. For a negative photoresist,

the portion of the photoresist that is exposed to light in scanner 305 becomes insoluble to the photoresist developer and the unexposed portion of the photoresist remains soluble to the photoresist developer.

[030] Etching tool 325 can transfer the pattern to one or more films under the photoresist by etching the films from portions of the wafer where the photoresist has been removed. Etching tool 325 can be a dry etch or wet etch tool. Ash tool 330 can remove the remaining photoresist from the etched wafer and the pattern transfer process to the film on the wafer can be completed.

[031] Monitoring tool 335 can inspect the processed wafer at one or more locations on the wafer to generate monitor results. The monitor results can be based on spatial pattern determination, size measurement of different pattern features or a positional shift in different pattern features. The inspection locations can be determined by point determination tool 345.

[032] Point determination tool 345 can comprise one or more pre-determined models to determine the inspection locations based on HDFM 315 and weak point information 340.

[033] Weak point information 340 can include information regarding locations with a high probability of problems related to the patterning process. Weak point information 340 can be based on the transferred pattern, various process parameters and properties of the wafer, scanner 305, and etching tool 325.

[034] Verification unit 350 can compare the monitor results from monitoring tool 335 with corresponding design parameters to generate verified results. Verification unit 350 can provide the verified results to control unit 310 of scanner 305. Control unit 310 can adjust the exposure recipe for subsequent wafers based on the verified results. For example, control unit may decrease exposure dose of scanner 305 for some locations on subsequent wafers based on the verified results.

[035] Reference is now made to **FIG. 4**, which is a flowchart illustrating a conventional method for semiconductor processing. As an example, method 400 can be performed by conventional semiconductor processing system 300.

[036] In step 405, semiconductor processing system 300 can process a wafer coated with photoresist to transfer a pattern onto the wafer. Scanner 305 can expose the wafer to the pattern. Control unit 310 can control an exposure recipe used to expose the wafer. Control unit 310 can adjust various exposure recipe parameters, for example, exposure time, source intensity and exposure dose. HDFM 315 can be recorded corresponding to the exposure. Development tool 320 can develop the pattern on the exposed wafer by removing the photoresist from unwanted regions. Etching tool 325 can transfer the pattern to one or more films under the photoresist by etching the films from portions of the wafer where the photoresist has been removed. Ash tool 330 can remove the remaining photoresist from the etched wafer and the pattern transfer process to the film on the wafer can be completed.

[037] In step 410, point determination tool 345 can receive the exposure recipe

corresponding to the patterning of the wafer in step 405. The exposure recipe can be provided by scanner 305.

[038] In step 415, point determination tool 345 can receive weak point information 340 corresponding to the patterning process. Weak point information 340 can include information regarding locations with a high probability of problems related to the patterning process. Weak point information 340 can be based on the transferred pattern, various process parameters, and properties of the wafer, scanner 305, and etching tool 325.

[039] In step 420, point determination tool 345 can determine regions of the patterned wafer to be monitored. Point determination tool 345 can use one or more pre-determined models to determine the inspection locations based on the exposure recipe received in step 410 and weak point information 340 received in step 415.

[040] In step 425, monitoring tool 335 can inspect the regions of the patterned wafer determined to be monitored by point determination tool 345 in step 420. Monitoring tool 335 can inspect the patterned wafer at one or more locations to generate monitor results. The monitor results can be based on spatial pattern determination, size measurement of different pattern features or a positional shift in different pattern features.

[041] In step 430, verification unit 350 can compare the monitor results from monitoring tool 335 with corresponding design parameters to generate verified results.

[042] In step 435, verification unit 350 can determine if the verified results are correct according to design requirements. If the verified results are determined to be correct, verification unit 350 may take no further action for the corresponding wafer. If the verified results are determined to not be correct, verification unit 350 can provide the verified results to control unit 310 of scanner 305.

[043] In step 445, control unit 310 can adjust the exposure recipe for subsequent wafers based on the verified results. For example, control unit 310 may decrease an exposure dose of scanner 305 for some locations on subsequent wafers based on the verified results.

[044] In conventional method 400, point determination tool 345 uses a static model based on HDFM 315 and weak point information 340 to determine regions to be monitored. The model is not dynamically updated based on the verified results of previous wafers. For example, the verified results for some weak point locations may be correct for multiple monitored wafers. So throughput can be improved by not monitoring these weak point locations. But in conventional method 400, point determination tool 345 cannot use the verified results of previous wafers to determine monitor locations for subsequent wafers. So the throughput is not improved. Further, control unit 310 may adjust the exposure recipe based on the verified results but the model is not dynamically updated in response to the updated exposure recipe. For example, based on the updated exposure recipe, a different weak point location may need to be monitored. Further, an update may be needed in recipe of monitoring tool 335 to detect issues for wafers processed with the updated exposure recipe. But in

conventional method 400, point determination tool 345 cannot make updates to the monitor locations and recipe based on updates in the exposure recipe. The inability to make updates can reduce the detection efficiency of patterning problems in conventional method 400.

[045] Reference is now made to **FIG. 5**, which is a schematic diagram illustrating an exemplary processing system 500, consistent with embodiments of the present disclosure. Semiconductor processing system 500 can include a scanner 505, a control unit 510, a development tool 520, an etching tool 525, an ash tool 530, a monitoring tool 535, a verification unit 550, and a yield improvement system 555. Yield improvement system 555 can comprise a point determination tool 545 and a training tool 560.

[046] Point determination tool 545 and training tool 560 may each include one or more modules. In general, the word "module," as used herein, can be a packaged functional hardware unit designed for use with other components (e.g., portions of an integrated circuit) or a part of a program (stored on a computer readable medium) that performs a particular function of related functions. The module can have entry and exit points and can be written in a programming language, such as, for example, Java, Lua, C or C++. A software module can be compiled and linked into an executable program, installed in a dynamic link library, or written in an interpreted programming language such as, for example, BASIC, Perl, or Python. It will be appreciated that software modules can be callable from other modules or from themselves, and/or can be invoked in response to detected events or interrupts. Software modules configured for execution on computing devices can be provided on a computer readable medium, such as a compact disc, digital video disc, flash drive, magnetic disc, or any other non-transitory medium, or as a digital download (and can be originally stored in a compressed or installable format that requires installation, decompression, or decryption prior to execution). Such software code can be stored, partially or fully, on a memory device of the executing computing device, for execution by the computing device. Software instructions can be embedded in firmware, such as an erasable programmable read-only memory (EPROM). It will be further appreciated that hardware modules can be comprised of connected logic units, such as gates and flip-flops, and/or can be comprised of programmable units, such as programmable gate arrays or processors. The modules or computing device functionality described herein are preferably implemented as software modules, but can be represented in hardware or firmware. Generally, the modules described herein refer to logical modules that can be combined with other modules or divided into sub-modules despite their physical organization or storage.

[047] In some embodiments, point determination tool 545 and training tool 560 can be combined in a single tool. In some embodiments, yield improvement system 555 may be included within monitoring tool 535.

[048] Scanner 505 can expose a wafer coated with photoresist to a circuit pattern to be transferred to the wafer. Control unit 510 can control an exposure recipe used to expose the wafer.

Control unit 510 can adjust various exposure recipe parameters, for example, exposure time, source intensity, and exposure dose. An HDFM 515 can be recorded corresponding to the exposure.

[049] Development tool 520 can develop the pattern on the exposed wafer by removing the photoresist from unwanted regions. For a positive photoresist, the portion of the photoresist that is exposed to light in scanner 505 becomes soluble to the photoresist developer and the unexposed portion of the photoresist remains insoluble to the photoresist developer. For a negative photoresist, the portion of the photoresist that is exposed to light in scanner 505 becomes insoluble to the photoresist developer and the unexposed portion of the photoresist remains soluble to the photoresist developer.

[050] Etching tool 525 can transfer the pattern to one or more films under the photoresist by etching the films from portions of the wafer where the photoresist has been removed. Etching tool 525 can be a dry etch or wet etch tool. Ash tool 530 can remove the remaining photoresist from the etched wafer and the pattern transfer process to the film on the wafer can be completed.

[051] Monitoring tool 535 can inspect the processed wafer at one or more locations on the wafer to generate monitor results. The monitor results can be based on spatial pattern determination, size measurement of different pattern features or a positional shift in different pattern features. The inspection locations can be determined by point determination tool 545 of yield improvement system 555. Point determination tool 545 can comprise one or more models to determine the inspection locations based on HDFM 515, weak point information 540 and training data provided by training tool 560. Point determination tool 545 may include one or more modules.

[052] Weak point information 540 can include information regarding locations with a high probability of problems related to the patterning process. Weak point information 540 can be based on the transferred pattern, various process parameters and properties of the wafer, scanner 505, and etching tool 525.

[053] Verification unit 550 can compare the monitor results from monitoring tool 535 with corresponding design parameters to generate verified results. Verification unit 550 can provide the verified results to control unit 510 of scanner 505. Control unit 510 can adjust the exposure recipe for subsequent wafers based on the verified results. For example, control unit 510 may decrease exposure dose of scanner 305 for some locations on subsequent wafers based on the verified results. Verification unit 550 can further provide the verified results to training tool 560 of yield improvement system 555.

[054] Training tool 560 can generate training data based on the verified results received from verification unit 550. Training tool 560 can comprise a deep neural network to analyze the one or more verified results for generating the training data. In some embodiments, training tool 560 can also receive HDFM 515 and further generate training data based on HDFM 515. Training tool 560 can provide the generated training data to point determination tool 545. Point determination tool 545 can

determine inspection points for other wafers based on the received training data, HDFM 515 and weak point information 540. The monitor points can therefore be dynamically selected instead of a fixed model.

[055] Reference is now made to **FIG. 6A** and **FIG. 6B**, which are schematic diagrams illustrating inspection regions on a first patterned substrate 600A and a second patterned substrate 600B respectively, consistent with embodiments of the present disclosure. Substrate 600A and substrate 600B may be processed by a semiconductor processing system having yield improvement system 555, e.g. semiconductor processing system 500 of **FIG. 5**.

[056] A point determination tool (e.g, point determination tool 545 of semiconductor processing system 500) can determine inspection regions for substrate 600A. Based on an exposure recipe (e.g., HDFM 515) and weak point information (e.g., weak point information 540), the point determination tool can determine eight dies labelled 631, 632, 633, 634, 635, 636, 637, and 638 for inspection. Within each die, the point determination can determine five locations labelled 621, 622, 623, 624, and 625 for inspection.

[057] A monitoring tool (e.g., monitoring tool 535 of semiconductor processing system 500) can perform inspection for the determined locations of substrate 600A. A verification unit (e.g., verification unit 550 of semiconductor processing system 500) can generate verified results by comparing the monitor results with design parameters. The verified results can be used to update the exposure recipe during processing of substrate 600B.

[058] A training tool (e.g., training tool 560 of semiconductor processing system 500) can generate training data based on the verified results and provide it to the point determination tool. The point determination tool can use the training data determine regions for inspection for substrate 600B. For example, the point determination tool can reduce the number of dies to be inspected from eight to seven. As shown in **FIG. 6B**, point determination tool can inspect die 651 for substrate 600B instead of dies 636 and 637 for substrate 600A. In some embodiments, the point determination tool can also reduce the number of inspection points for each die, based on the received training data. Reduction in the number of inspection points can increase the throughput of the processing system. Further, the monitor points or monitor recipe can be updated corresponding to updates in the exposure recipe used during processing of substrate 600B. For example, if a contact is formed by using the updated exposure recipe a different monitoring tool recipe (e.g., different landing energy or different beam current) can be used to capture different open/short defects for substrate 600B. The training data can include information to modify the monitoring tool recipe corresponding to updates in the exposure recipe. If there is no change in the monitoring tool recipe, the changed open/short defects may not be identified. Systems and methods provided by present disclosure can therefore improve detection of defects and thereby improve the semiconductor manufacturing yield.

[059] Reference is now made to **FIG. 7**, which is a flowchart illustrating an exemplary

method for yield improvement, consistent with embodiments of the present disclosure. As an example, method 700 can be performed by semiconductor processing system 500 comprising yield improvement system 555. It will be readily appreciated that the illustrated procedure can be altered to modify the order of steps, delete steps, or further include additional steps.

[060] In step 705, the semiconductor processing system can process a wafer coated with photoresist to transfer a pattern onto the wafer. A scanner (e.g., scanner 505 of semiconductor processing system 500) can expose the wafer to the pattern. A control unit within the scanner (e.g., control unit 510 of semiconductor processing system 500) can control an exposure recipe used to expose the wafer. The control unit can adjust various exposure recipe parameters, for example, exposure time, source intensity, and exposure dose. An HDFM (e.g. HDFM 515 of semiconductor processing system 500) can be recorded corresponding to the exposure. A development tool (e.g., development tool 520 of semiconductor processing system 500) can develop the pattern on the exposed wafer by removing the photoresist from unwanted regions. An etching tool (e.g., etching tool 525 of semiconductor processing system 500) can transfer the pattern to one or more films under the photoresist by etching the films from portions of the wafer where the photoresist has been removed. An ashing tool (e.g., ash tool 530 of semiconductor processing system 500) can remove the remaining photoresist from the etched wafer and the pattern transfer process to the film on the wafer can be completed.

[061] In step 710, a point determination tool (e.g., point determination tool 545 of semiconductor processing system 500) can receive the exposure recipe corresponding to the patterning of the wafer in step 705. The exposure recipe can be provided by the scanner.

[062] In step 715, the point determination tool can receive the weak point information (e.g., weak point information 540 of semiconductor processing system 300) corresponding to the patterning process. The weak point information can include information regarding locations with a high probability of problems related to the patterning process. The weak point information can be based on the transferred pattern, various process parameters and properties of the wafer, the scanner, and the etching tool.

[063] In step 720, the point determination tool can determine regions of the patterned wafer to be monitored. The point determination tool can use one or more pre-determined models to determine the inspection locations based on the exposure recipe received in step 710 and the weak point information received in step 715.

[064] In step 725, a monitoring tool (e.g. monitoring tool 535 of semiconductor processing system 500) can inspect the regions of the patterned wafer determined to be monitored by the point determination tool in step 720. The monitoring tool can inspect the patterned wafer at one or more locations to generate monitor results. The monitor results can be based on spatial pattern determination, size measurement of different pattern features, or a positional shift in different pattern

features.

[065] In step 730, a verification unit (e.g., verification unit 550 of semiconductor processing system 500) can compare the monitor results from the monitoring tool with corresponding design parameters to generate verified results.

[066] In step 735, the verification unit can determine if the verified results are correct according to design requirements. If the verified results are determined to be correct, the verification unit may take no further action for the corresponding wafer. If the verified results are determined to not be correct, the verification unit can provide the verified results to the control unit of the scanner and a training tool of the yield improvement system (e.g., training tool 560 of yield improvement system 555).

[067] In step 740, the control unit can adjust the exposure recipe for subsequent wafers based on the verified results. For example, the control unit may decrease an exposure dose of the scanner for some locations on subsequent wafers based on the verified results.

[068] In step 745, the training tool can receive the verified results from the verification unit and can generate training data based on the verified results. The training tool can comprise a deep neural network to analyze the one or more verified results for generating the training data. The training tool can provide the generated training data to the point determination tool. The point determination tool can determine inspection points for other wafers based on the received training data, the exposure recipe, and the weak point information. The monitor points can therefore be dynamically determined instead of being dependent on a fixed model. This dynamic determination can reduce defects in subsequent processed wafers and therefore improve the semiconductor manufacturing yield. Moreover, the updates to monitoring resulting from the dynamic determination may include monitoring fewer hot spots thereby improving the throughput. The updates to monitoring resulting from the dynamic determination can also include a change in the monitoring to improve detection of defects. The improved defect detection can help in further improving the semiconductor manufacturing yield.

[069] The embodiments may further be described using the following clauses:

1. A yield improvement system comprising:

a training tool configured to generate training data based on receipt of one or more verified results of an inspection of a first substrate; and

a point determination tool configured to determine one or more regions on a second substrate to inspect based on the training data, weak point information for the second substrate, and an exposure recipe for a scanner of the second substrate.

2. The system of clause 1, wherein the training tool is configured to use a deep neural network to analyze the one or more verified results for generating the training data.

3. The system of clauses 1 or 2, wherein the training tool is further configured to generate the training data based on the exposure recipe.

4. The system of any one of claims 1 to 3, wherein the one or more verified results are generated by a verification unit, based on a comparison of one or more monitor results of the first substrate with one or more design parameters.

5. The system of clause 4, wherein the one or more monitor results are generated by a monitoring tool, based on at least one of a spatial pattern determination, a pattern size measurement and a pattern shift measurement.

6. The system of clauses 4 or 5, wherein the exposure recipe is determined based on the one or more monitor results.

7. The system of any one of clauses 1 to 6, wherein the exposure recipe comprises a high density focus map.

8. The system of any one of clauses 1 to 7, wherein the first substrate and the second substrate are processed by a scanner, a development tool, an etching tool and an ash tool.

9. A method comprising:

receiving one or more verified results of an inspection of a first substrate;

generating training data based on the received verified results; and

determining one or more regions on a second substrate to inspect based on the training data, weak point information for the second substrate, and an exposure recipe for a scanner of the second substrate.

10. The method of clause 9, wherein the generating training data comprises using a deep neural network to analyze the one or more verified results.

11. The method of clauses 9 or 10, wherein the generating training data is further based on the exposure recipe.

12. The method of any one of clauses 9 to 11, wherein the verified results are generated by a verification unit, based on a comparison of one or more monitor results of the first substrate with one or more design parameters.

13. The method of clause 12, wherein the one or more monitor results are generated by a monitoring tool, based on at least one of a spatial pattern determination, a pattern size measurement and a pattern shift measurement.

14. The method of clauses 12 or 13, wherein the exposure recipe is determined based on the one or more monitor results.

15. The method of any one of clauses 9 to 14, wherein the exposure recipe comprises a high density focus map.

16. The method of any one of clauses 9 to 15, wherein the first substrate and the second substrate are processed by a scanner, a development tool, an etching tool and an ash tool.

17. A non-transitory computer readable storage medium storing instructions that are executable by a computing device that includes one or more processors to cause the computing device to perform a method comprising:

receiving one or more verified results of an inspection of a first substrate;

generating training data based on the received verified results;

determining one or more regions on a second substrate to inspect based on the training data, weak point information for the second substrate, and an exposure recipe for a scanner of the second substrate.

18. The medium of clause 17, wherein generating training data comprises using a deep neural network to analyze the one or more verified results.

19. The medium of clauses 17 or 18, wherein generating training data is further based on the exposure recipe.

20. The medium of any one of clauses 17 to 19, wherein the verified results are generated by a verification unit, based on a comparison of one or more monitor results of the first substrate with one or more design parameters.

21. The medium of clause 20, wherein the one or more monitor results are generated by a monitoring tool, based on at least one of a spatial pattern determination, a pattern size measurement and a pattern shift measurement.

22. The medium of clauses 20 or 21, wherein the exposure recipe is determined based on the one or more monitor results.

23. The medium of any one of clauses 17 to 22, wherein the exposure recipe comprises a high density focus map.

24. The medium of any one of clauses 17 to 23, wherein the first substrate and the second substrate are processed by a scanner, a development tool, an etching tool, and an ash tool.

[069] It will be appreciated that the present invention is not limited to the exact construction that has been described above and illustrated in the accompanying drawings, and that various modifications and changes can be made without departing from the scope thereof. It is intended that the scope of the invention should only be limited by the appended claims.

WHAT IS CLAIMED IS:

1. A yield improvement system comprising:

a training tool configured to generate training data based on receipt of one or more verified results of an inspection of a first substrate; and

a point determination tool configured to determine one or more regions on a second substrate to inspect based on the training data, weak point information for the second substrate, and an exposure recipe for a scanner of the second substrate.

2. The system of claim 1, wherein the training tool is configured to use a deep neural network to analyze the one or more verified results for generating the training data.

3. The system of claim 1, wherein the training tool is further configured to generate the training data based on the exposure recipe, and/or wherein the exposure recipe comprises a high density focus map.

4. The system of claim 1, wherein the one or more verified results

are generated by a verification unit, based on a comparison of one or more monitor results of the first substrate with one or more design parameters, and/orwherein the one or more monitor results are generated by a monitoring tool, based on at least one of a spatial pattern determination, a pattern size measurement and a pattern shift measurement, and/or wherein the exposure recipe is determined based on the one or more monitor results.

5. The system of claim 1, wherein the first substrate and the second substrate are processed by a scanner, a development tool, an etching tool and an ash tool.

6. A method comprising:

receiving one or more verified results of an inspection of a first substrate;

generating training data based on the received verified results; and

determining one or more regions on a second substrate to inspect based on the training data,

weak point information for the second substrate, and an exposure recipe for a scanner of the second substrate.

7. The method of claim 6, wherein the generating training data comprises using a deep neural network to analyze the one or more verified results.

8. The method of claim 6, wherein the generating training data is further based on the exposure recipe.

9. The method of claim 6, wherein the verified results are generated by a verification unit, based on a comparison of one or more monitor results of the first substrate with one or more design parameters, and/or wherein the one or more monitor results are generated by a monitoring tool, based on at least one of a spatial pattern determination, a pattern size measurement and a pattern shift measurement, and/or wherein the exposure recipe is determined based on the one or more monitor results.

10. The method of claim 6, wherein the exposure recipe comprises a high density focus map.

11. The method of claim 6, wherein the first substrate and the second substrate are processed by a scanner, a development tool, an etching tool and an ash tool.

12. A non-transitory computer readable storage medium storing instructions that are executable by a computing device that includes one or more processors to cause the computing device to perform a method comprising:

receiving one or more verified results of an inspection of a first substrate;

generating training data based on the received verified results;

determining one or more regions on a second substrate to inspect based on the training data, weak point information for the second substrate, and an exposure recipe for a scanner of the second substrate.

13. The medium of claim 12, wherein generating training data comprises using a deep neural network to analyze the one or more verified results, and/or wherein generating training data is further based on the exposure recipe, and/or wherein the exposure recipe is determined based on the one or more monitor results, and/or wherein the exposure recipe comprises a high density focus map.

14. The medium of claim 12, wherein the verified results are generated by a verification unit, based on a comparison of one or more monitor results of the first substrate with one or more design parameters, and/or wherein the one or more monitor results are generated by a monitoring tool, based on at least one of a spatial pattern determination, a pattern size measurement and a pattern shift measurement.

15. The medium of claim 12, wherein the first substrate and the second substrate are processed by a scanner, a development tool, an etching tool, and an ash tool.

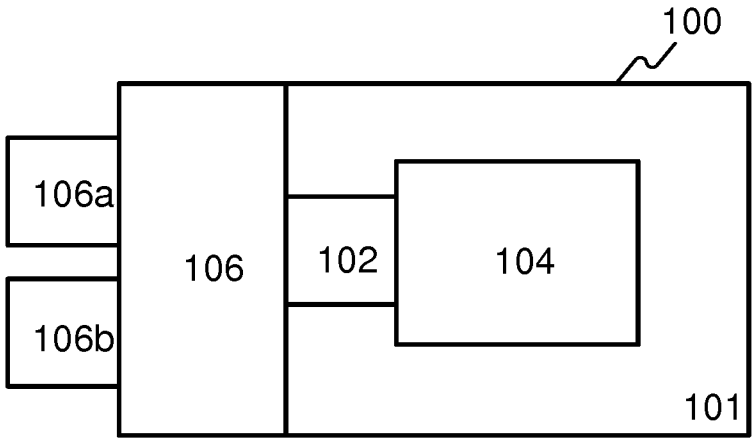
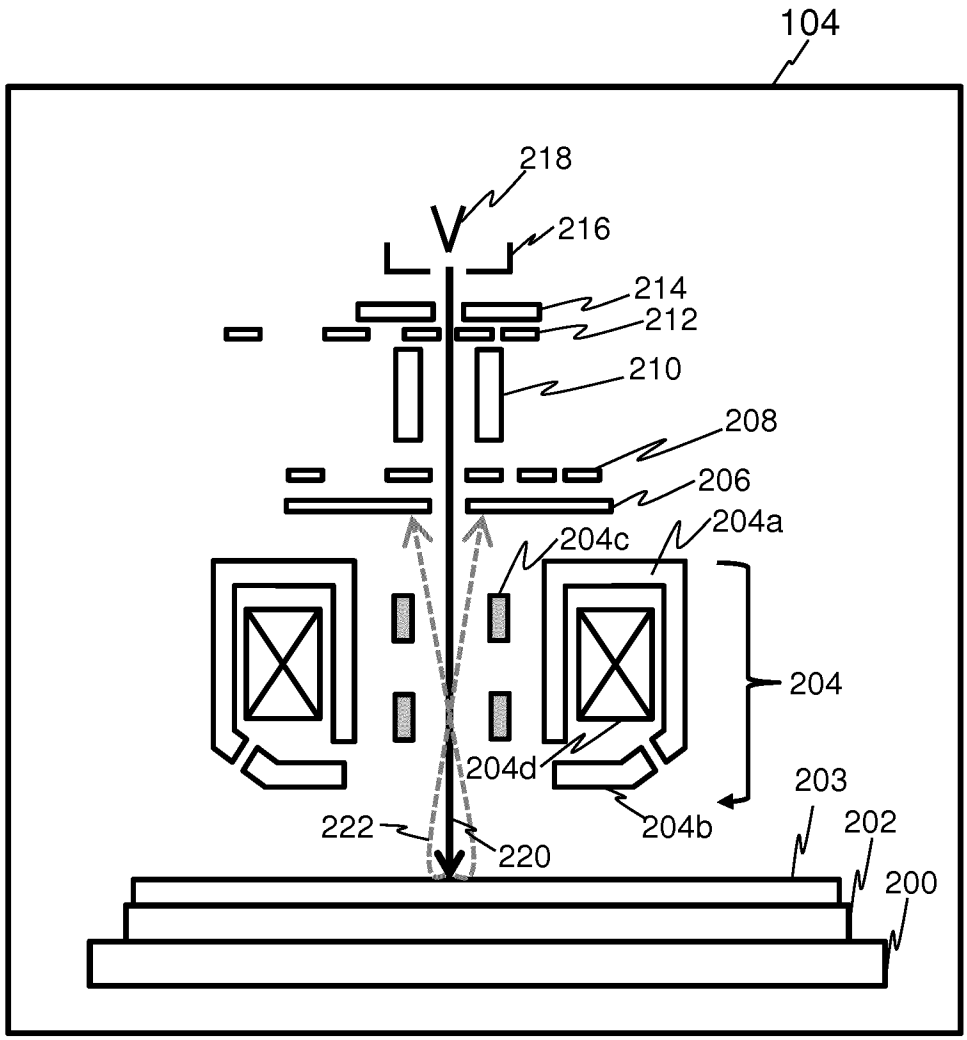


Fig. 1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218
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204c
204a
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204d
204b
203
202
200
222
220

Fig. 2

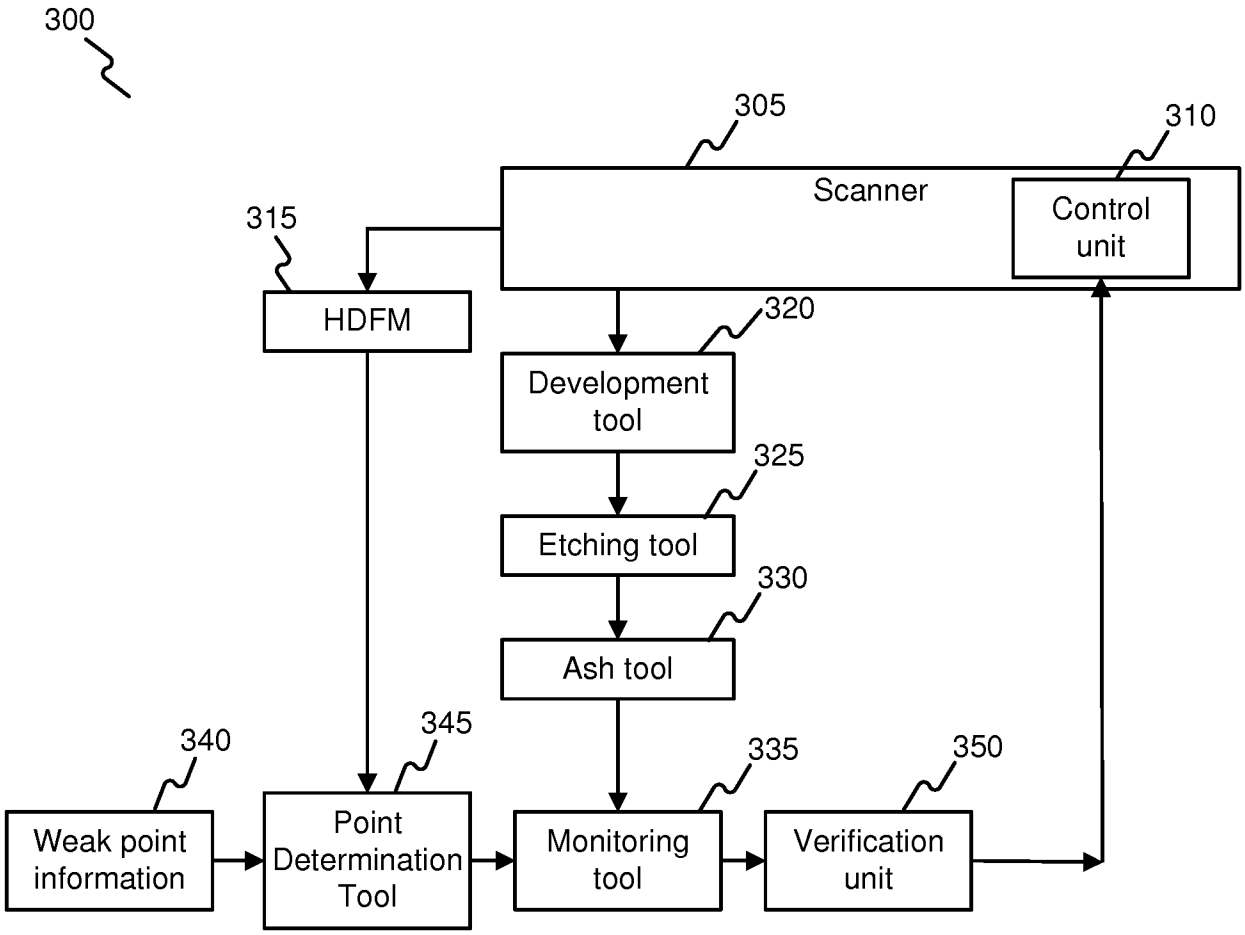
300
305
310
Scanner
Control unit
315
HDFM
320
Development tool
325
Etching tool
330
Ash tool
340
345
335
350
Weak point information
Point Determination Tool
Monitoring tool
Verification unit

Fig. 3

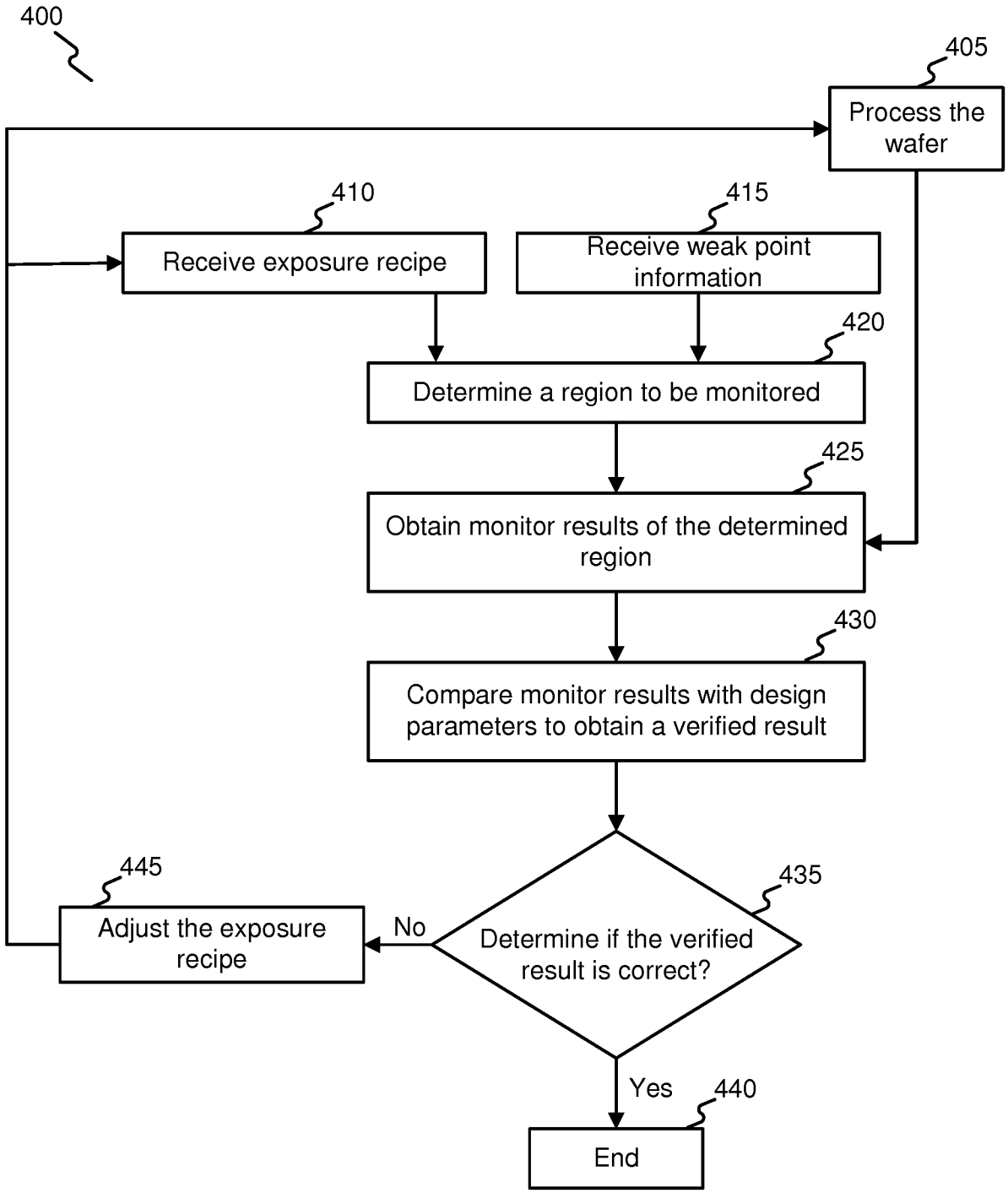
400
405
Process the wafer
410
Receive exposure recipe
415
Receive weak point information
420
Determine a region to be monitored
425
Obtain monitor results of the determined region
430
Compare monitor results with design parameters to obtain a verified result
435
Determine if the verified result is correct?
No
445
Adjust the exposure recipe
Yes
440
End

Fig. 4

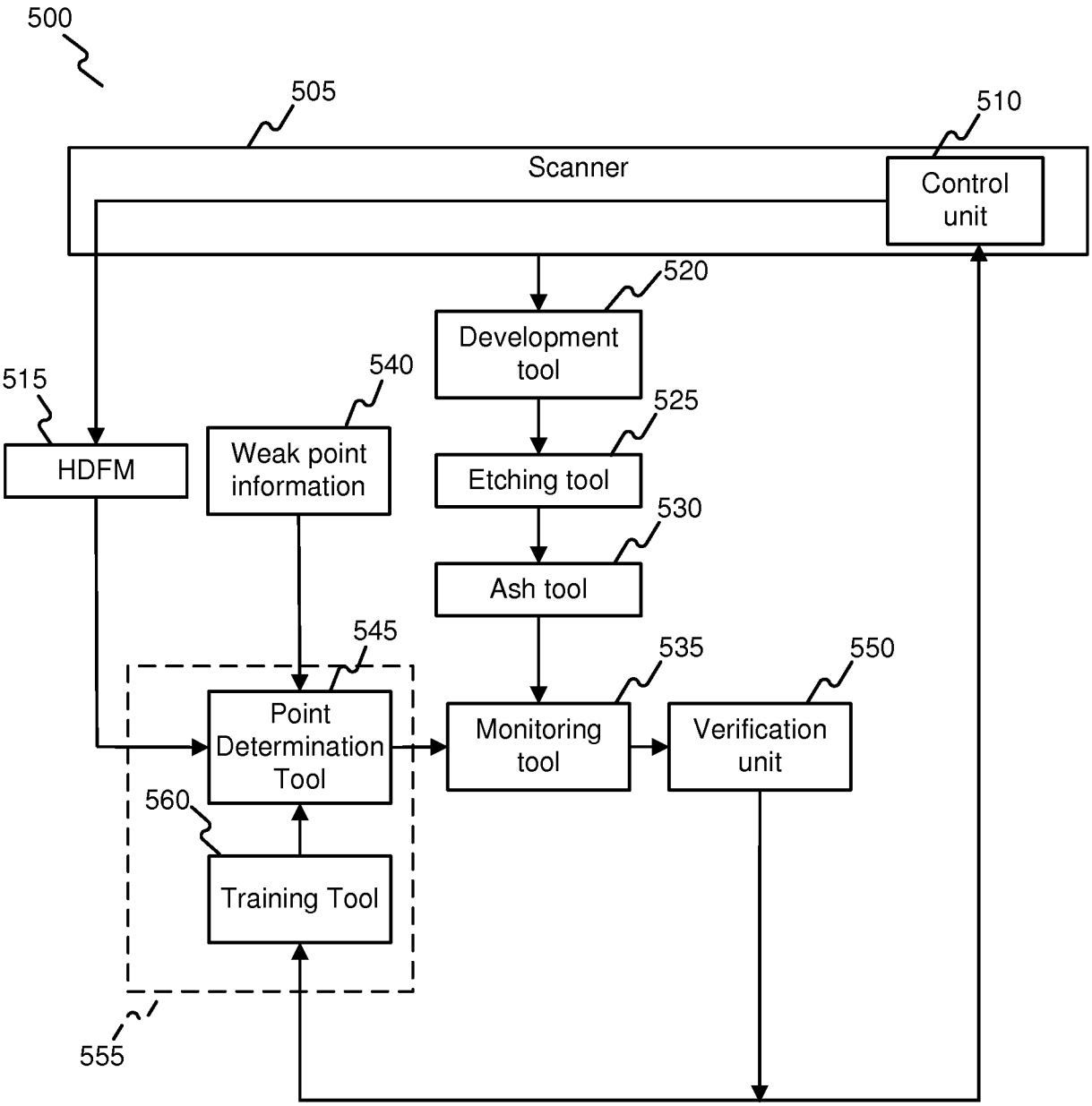
500
505
Scanner
510
Control unit
520
Development tool
515
HDFM
540
Weak point information
525
Etching tool
530
Ash tool
545
Point Determination Tool
535
Monitoring tool
550
Verification unit
560
Training Tool
555

Fig. 5

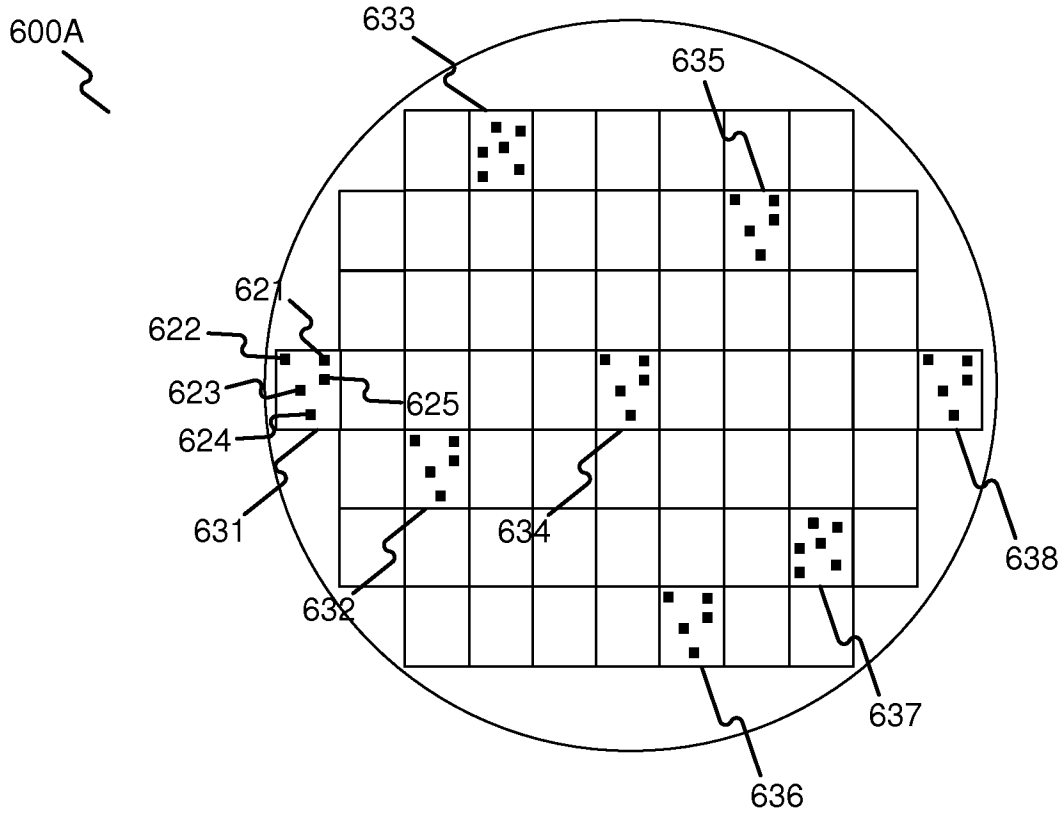

Fig. 6A

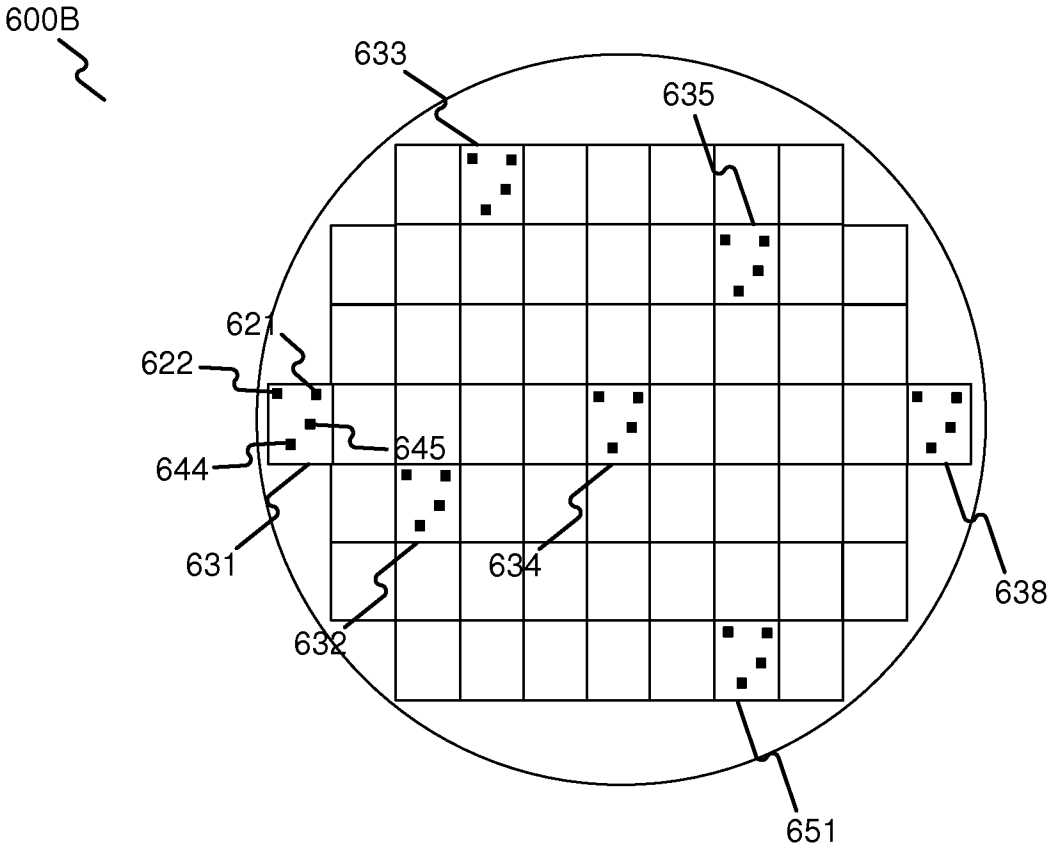

Fig. 6B

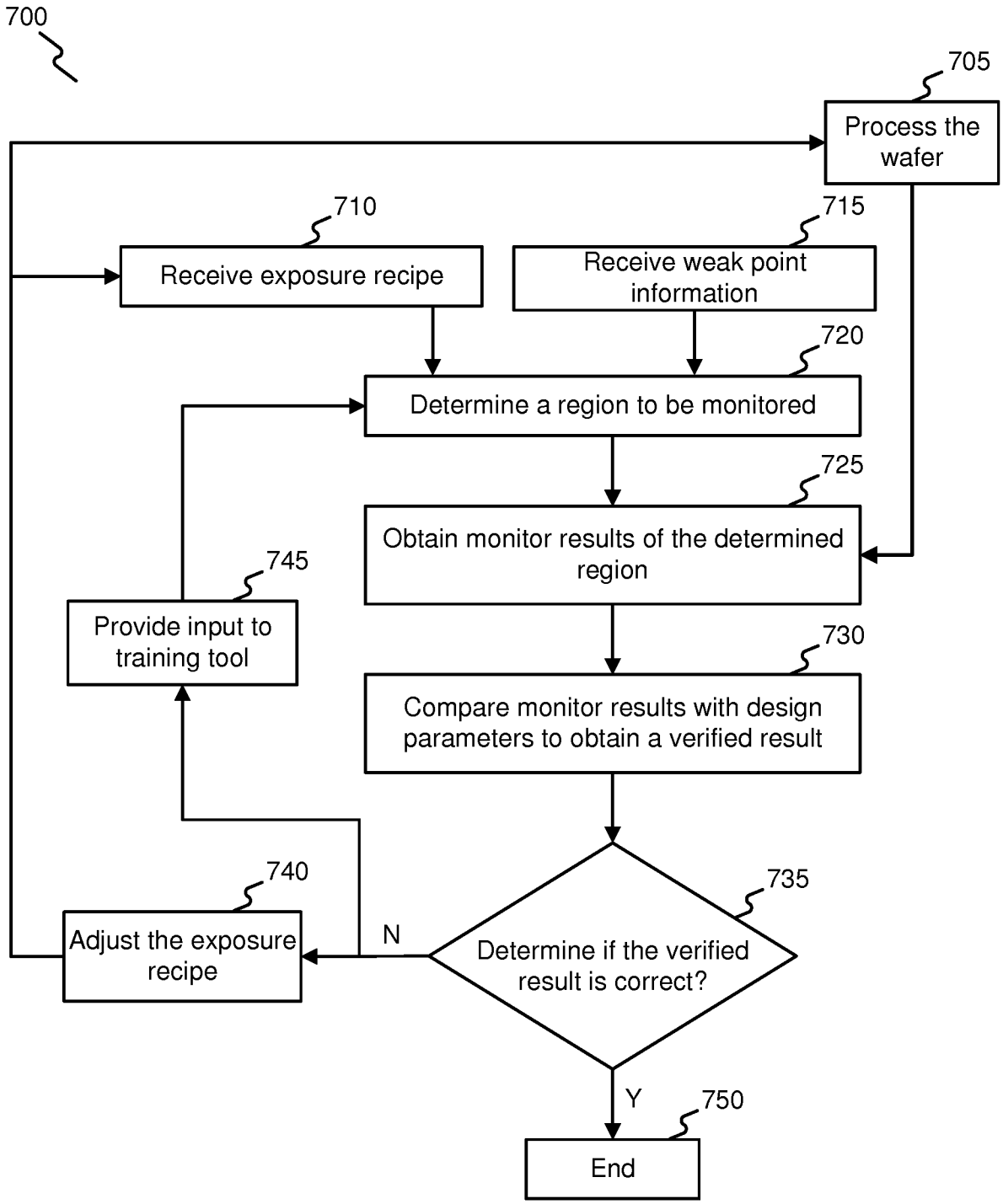
700
705
Process the wafer
710
Receive exposure recipe
715
Receive weak point information
720
Determine a region to be monitored
725
Obtain monitor results of the determined region
730
Compare monitor results with design parameters to obtain a verified result
735
Determine if the verified result is correct?
N
740
Adjust the exposure recipe
745
Provide input to training tool
Y
750
End

Fig. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/070567

A. CLASSIFICATION OF SUBJECT MATTER
INV. G05B19/418
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G05B G03F G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015/356233 A1 (FOUQUET CHRISTOPHE DAVID [BE] ET AL) 10 December 2015 (2015-12-10) paragraphs [0087] - [0102] -----	1-15
A	JP 2006 210931 A (TOSHIBA CORP) 10 August 2006 (2006-08-10) paragraphs [0059] - [0110] -----	1-15
A	WO 2008/077100 A2 (KLA TENCOR CORP [US]; DUFFY BRIAN [US]; KULKARNI ASHOK [US]) 26 June 2008 (2008-06-26) page 4, line 15 - page 8, line 27 page 10, line 20 - page 38, line 23 -----	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 November 2017	27/11/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Prokopiou, Platon

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2017/070567

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